400042 Rev. 1

National
Semiconductor
Corporation

Linear Databook 2

- *Active Filters*
- *Analog Switches/Multiplexers*
- *Analog-to-Digital Converters*
- *Digital-to-Analog Converters*
- *Sample and Hold*
- *Temperature Sensors*
- *Voltage References*
- *Surface Mount*

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Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

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Linear Databook 2

1988 Edition

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  - Operational Amplifiers
  - Buffers
  - Voltage Comparators
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National Semiconductor Corporation first established itself as the Linear Leader in 1967 with the introduction of the FIRST MONOLITHIC VOLTAGE REGULATOR . . . LM100. In the 20 years since, many of our products were firsts in performance and function. Today, this catalog spans the traditional areas of Op Amps, Voltage Regulators, Voltage References and Temperature Sensors, to Data Acquisition, Communication, Automotive, and Power Plus Control. National Semiconductor intends to remain a leader in the traditional product areas while forging ahead into VLSI solutions for analog problems and analog systems.

You can rely on National LINEAR to develop the most comprehensive product offering for use in the commercial, computer, automotive, telecommunication, industrial or military business segments. More than 1,000 basic LINEAR products (5400 options) allow design engineers to find the optimum Linear IC solution from National Semiconductor.

The Linear product line is presented in 3 Databooks. All sections are referenced and cross-indexed to provide quick and easy access. The technical information and basic product specifications are presented in data sheet format, including maximum ratings, electrical characteristics, performance curves and package information.

Additional application information is available as specific application notes or completely compiled in the LINEAR APPLICATIONS HANDBOOK. A product cross reference to the specific application note has been provided. This handbook and the 3-volume set of Linear Data Books represent a complete base of information to the National LINEAR product line.

National Semiconductor Corporation

Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advanced Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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National
Semiconductor
Corporation

CROSS REFERENCE BY PART NUMBER

A complete interchangeability list of Linear IC's offered by most Integrated Circuit Manufacturers are listed in this section and reference the nearest National Semiconductor Corp. direct replacement or recommended replacement with either an improved or functional replacement. The following notations are appended to assist you in finding the best option.

No reference note ......"DIRECT REPLACEMENT"

Note (1) ...."IMPROVED REPLACEMENT" Pin-for-Pin replacement with "SUPERIOR" Electrical Specifications.

Note (2) ...."FUNCTIONAL REPLACEMENT" Similar device. Consult datasheet to determine the suitability for specific application.

Note (3) ...."SIMILAR DEVICE" with superior performance. Consult datasheet to determine suitability of the replacement for specific application.

ANALOG DEVICES	**NATIONAL**	
AD0P07	LM607	(1)
ADDAC-08	DAC0800	
ADDAC-08	DAC0801	
ADDAC-08	DAC0802	
ADDAC80	DAC1280+	(1)
ADDAC85	DAC1280+	(1)
AD101A	LM101A	(1)
AD201A	LM201A	(1)
AD301A	LM301A	(1)
AD506	LH0022	(2)
AD509	LH0003	(2)
AD521	LM363	(2)
AD521	LH0036	(2)
AD524	LH0038	(2)
AD537	LM331	(2)
AD562	DAC1266	(3)
AD563	DAC1265	(3)
AD565A	DAC1265	
AD566A	DAC1266	
AD567	DAC1230	(2)
AD573	ADC1005	(2)
AD573	ADC1025	(2)
AD581	LM581	
AD581	LH0070	(1)
AD582	LF398	(2)
AD583	LF198	(3)
AD588	LM369	(2)
AD589M	LM385	(1)
AD589U	LM185	(1)
AD590	LM135	(2)
AD590	LM34	(3)
AD590	LM134	(2)
AD590	LM35	(3)
AD611K	LF411AC	(1)
AD611J	LF411C	(1)
AD614	LH0086	(2)
AD624	LH0038	(2)
AD650	LM331	(2)
AD651	LM331	(2)
AD654	LM331	(2)
AD673	ADC0841	(2)
AD741	LM741	
ADLH0032	LH0032	(2)
ADLH0033	LH0033	(2)
AD0042	LH0042	(2)
AD3542	LH0042	(2)
AD5035	LH0042	(2)
AD7502	LF13509	(2)
AD7516	CO4066B	(2)
AD7523	DAC0832	(2)
AD7523	DAC0831	(2)
AD7523	DAC0830	(2)
AD7524	DAC0830	(3)
AD7524	DAC0831	(3)
AD7524	DAC0832	(3)
AD7533	DAC1020	
AD7533	DAC1022	
AD7533	DAC1021	
AD7541A	DAC1218	(2)
AD7541A	DAC1219	(2)
AD7541	DAC1219	(1)
AD7541	DAC1218	(1)
AD7542	DAC1210	(2)
AD7542	DAC1209	(2)
AD7542	DAC1208	(2)
AD7545	DAC1209	(2)
AD7545	DAC1210	(2)
AD7545	DAC1208	(2)
AD7548	DAC1230	(2)
AD7548	DAC1232	(2)
AD7548	DAC1231	(2)
AD7552	ADC1225	(2)
AD7552	ADC1205	(2)
AD7571	ADC1005	(2)
AD7571	ADC1025	(2)
AD7575	ADC0820	(2)
AD7576	ADC0820	(2)
AD7578	ADC1225	(2)
AD7578	ADC1205	(2)
AD7820	ADC0820	

APEX	**NATIONAL**	
PA01	LM12	(2)
PA01	LH0101	(2)
PA07	LM12	(2)
PA10	LM12	(2)
PA10	LH0101	(2)
PA11	LM12	(2)
PA51	LM12	(2)
PA73	LM12	(2)

BURR-BROWN	**NATIONAL**	
SHC80	LF398	(2)
SHC85	LF398	(2)
HOS-100	LH0033	(2)
INA102	LH0038	(2)
SHC298A	LF398A	(1)
3507	LM6361	(2)
3533	LH0033	(2)
3542	LH0042	(2)
3550	LM6361	(2)
3551	LM6361	(2)
3553	LH0063	(2)
3554	LH0032	(2)
3571	LM675	(2)
3572	LH0021	(2)
3573	LM675	(2)
3606A6	LH0084	(2)
3606A6	LH0086	(2)
3626	LH0036	(2)
3629	LH0038	(2)

CTS	**NATIONAL**	
CTS0002	LH0002	(1)
CTS0004	LH0004	(1)
CTS0021	LH0021	(1)
CTS0024	LH0024	(1)
CTS0032	LH0032	(1)
CTS0033	LH0033	(1)
CTS0041	LH0041	(1)
CTS0042	LH0042	(1)
CTS2101A	LH2101A	(1)
CTS2111	LH2111	(1)

ELANTEC	**NATIONAL**	
ELH0002	LH0002	(1)
ELH0021	LH0021	(1)
ELH0032	LH0032	(1)
ELH0033	LH0033	(1)
ELH0041	LH0041	(1)
ELH0101	LH0101	(1)
EL2006C	LM6261	(2)
EL2006	LM6161	(2)
EHA2500	LM6161	(2)
EHA2502	LM6161	(2)
EHA2505	LM6361	(2)
EHA2510	LM6161	(2)
EHA2512	LM6161	(2)
EHA2515	LM6361	(2)
EHA2520	LM6164	(2)
EHA2522	LM6164	(2)
EHA2525	LM6364	(2)
EHA2600	LM6161	(2)
EHA2602	LM6161	(2)
EHA2605	LM6361	(2)
EHA2620	LM6164	(2)
EHA2622	LM6164	(2)
EHA2625	LM6364	(2)

EXAR	**NATIONAL**	
XR084M	LF147	(1)
XR084	LF347	(1)
XR146	LM146	(1)
XR246	LM246	(1)
XR346	LM346	(1)
XR-1001	MF4C-100	(1)
XR-1002	MF4C-50	(1)
XR1458	LM1458	(1)

FAIRCHILD	**NATIONAL**	
µA78XXKM	LM140K-XX	(1)
µ78LXXACH	LM78LXXACH	(1)
µ78XXUC	LM340T-XX	(1)
µ78XXUC	LM78XXCT	(1)
µA78LXXACLP	LM78LXXACZ	(1)
µA78LXXAWC	LM78LXXACZ	(1)
µ78MXXCKC	LM78XXCK	(1)
µ78MXXCKC	LM78MXXCT	(1)
µA78MXXUC	LM341P-XX	(1)
µA78MXXCKC	LM78XXCT	(1)
µA78XXKC	LM340K-XX	(1)
µA79XXUC	LM79LXXACZ	(1)
µA79XXUC	LM79MXXCP	(1)
µA79XXCKC	LM79XXCT	(1)
µA79XXCKC	LM79MXXCP	(1)
µA79XXUC	LM79MXXCH	(1)
µA79XXUC	LM320T-XX	(1)
µA79XXCKC	LM79MXXCH	(1)
µA79XXCKC	LM79LXXACZ	(1)
µA79MXXAUC	LM320MP-XX	(1)
µA79XXKM	LM120K-XX	(1)
µA79XXKC	LM320K-XX	(1)
µA79XXUC	LM79XXCT	(1)
µA101A	LM101A	(1)
µA102	LM102	(1)
µA105HM	LM105H	(1)
µA107	LM107	(1)
µA108A	LM108A	(1)
µA108	LM108	(1)
µA109KM	LM109K STEEL	(1)
µA110	LM110	(1)
µA111	LM111	(1)
µA124	LM124	(1)
µA139	LM139	(1)
µA139A	LM139A	(1)
µA201A	LM201A	(1)
µA207	LM207	(1)
µA208	LM208	(1)
µA208A	LM208A	(1)
µA211	LM211	(1)
µA224	LM224	(1)
µA239	LM239	(1)
µA239A	LM239A	(1)
µA248	LM248	(1)
µA249	LM249	(1)
µA301A	LM301A	(1)
µA302	LM302	(1)
µA304HC	LM304H	(1)
µA305HC	LM305H	(1)
µA305AHC	LM305AH	(1)
µA307	LM307	(1)
µA308A	LM308A	(1)
µA308	LM308	(1)
µA309KC	LM309K STEEL	(1)
µA310	LM310	(1)
µA311	LM311	(1)
µA317KC	LM317K STEEL	(1)
µA317UC	LM317T	(1)
µA318	LM318	(1)
µA324	LM324	(1)
µA339	LM339	(1)
µA339A	LM339A	(1)
µA348	LM348	(1)
µA349	LM349	(1)
µA376TC	LM376N	(1)
µA555TC	LM555CN	(1)
µA556PC	LM556CN	(1)
µA709	LM709	(1)
µA709	LM709	(1)
µA710	LM710	(1)
µA710	LM710	(1)
µA711	LM711	(1)
µA714	LM607	(1)
µA723HM	LM723H	(1)
µA723HC	LM723CH	(1)
µA723DC	LM723CJ	(1)
µA723MJ	LM723J	(1)
µA723CJ	LM723CJ	(1)
µA723DM	LM723J	(1)
µA723PC	LM723CN	(1)
µA723CN	LM723CN	(1)
µA725	LM725	(1)
µA725	LM725	(1)
µA733CN	LM733CN	(1)
µA733	LM733	(1)
µA741	LM741	(1)
µA741	LM741	(1)
µA747	LM747	(1)
µA747	LM747	(1)
µA748	LM748	(1)
µA748	LM748	(1)
µA760	LM760	(1)
µA771B	LF411	(1)
µA771	LF351	(1)
µA771A	LF411	(1)
µA772B	LF412A	(1)
µA772	LF353	(1)
µA772A	LF412A	(1)
µA774	LF347	(1)
µA774B	LF347B	(1)
µA776	LM4250	(1)
µA1458	LM1458	(1)
µC1496P	LM1496N	(1)
µC1496G	LM1496H	(1)
µA1558	LM1558	(1)
µC1596G	LM1596H	(1)
TDA2310	LM381	(1)
µA2901	LM2901	(1)
µA2902	LM2902	(1)
TCA3089	LM3089N	(1)
µA3301	LM3301	(1)
µA3302	LM3302	(1)
µC4558CD	LM833CN	(1)
µA7392	LM1014	(1)

HARRIS	**NATIONAL**	
HA-OP07	LM607	(1)
HF-10	MF10	
HI-201	LF13201	
HI-300	AH5020	(2)
LM741	LM741	(1)
HA2400	LM604AM	(2)
HA2404	LM604AM	(2)
HA2405	LM604C	(2)
HA2406	LM604C	(2)
HA2500	LM6161	(2)
HA2502	LM6161	(2)
HA2505	LM6361	(2)
HA2510	LM6161	(2)
HA2512	LM6161	(2)
HA2515	LM6361	(2)
HA2520	LM6164	(2)
HA2520	LH0003	(1)
HA2522	LH0003	(1)
HA2522	LM6164	(2)
HA2525	LH0003	(1)
HA2525	LM6364	(2)
HA2530	LH0024	(2)
HA2535	LH0024	(2)
HA2540	LH0032	(2)
HA2541-5	LM6361	(2)
HA2541-2	LM6161	(2)
HA2542	LH0032	(2)
HA2542-2	LM6164	(2)
HA2542-5	LM6164	(2)
HA2600	LM6161	(2)
HA2602	LM6161	(2)
HA2605	LM6361	(2)
HA2620	LM6164	(2)
HA2622	LM6164	(2)
HA2625	LM6364	(2)
HA2640	LH0004	(1)
HA5033	LH0033	(1)
HA5162	LH0062	(2)
A5180	LH0052	(1)

HEWLETT PACKARD	**NATIONAL**	
HCTL-100	LM628	(3)

HITACHI	NATIONAL	
HA13421A	LM18293	(3)
HA17082	LF353	(1)
HA17082A	LF412	(1)
HA17084	LF347	(1)
HA17084A	LF347B	(1)
HA17094	LM2904	(1)
HA17301	LM3301	(1)
HA17324	LM324	(1)
HA17339	LM339	(1)
HA17358	LM358	(1)
HA17393	LM393	(1)
HA17458	LM1458	(1)
HA17741	LM741	(1)
HA17747	LM747	(1)
HA17901	LM2901	(1)
HA17902	LM2902	(1)
HA17903	LM2903	(1)

LINEAR TECHNOLOGY	NATIONAL	
REF-01	LM168	(1)
REF-01	LM368	(1)
LM129	LM129	
LM134	LM134	
LM185	LM185	
LM199	LM199	
LM234	LM234	
LM329	LM329	
LM334	LM334	
LM385	LM385	
LM399	LM399	
AD581	LM581	
AD581	LH0070	
LT1001	LM607A	(1)
LT1004C	LM385	
LT1004M	LM185	
LT1009M	LM136-2.5	
LT1009C	LM336-2.5	
LT1019C	LM368	(2)
LT1019M	LM168	(2)
LT1020	LP2951	(3)
LT1021M	LM169	(1)
LT1021C	LM369	(1)
LT1029M	LM136-5.0	
LT1029C	LM336-5.0	
LT1031	LH0070	

LSI COMPUTER	NATIONAL	
LS7261	LM621	(3)
LS7263	LM621	(3)

MICRA	NATIONAL	
MC0002	LH0002	(1)
MC0003	LH0003	(1)
MC0004	LH0004	(1)
MC0032	LH0032	(1)
MC0033	LH0033	(1)
MC0041	LH0041	(1)
MC0063	LH0063	(1)

MICRO POWER SYSTEMS	NATIONAL	
MPOP07	LM607	(1)
MP108	LM108	(1)
MP108A	LM108A	(1)
MP155A	LF155A	(1)
MP155	LF155	(1)
MP156	LF156	(1)
MP156A	LF156A	(1)
MP157	LF157	(1)
MP157A	LF157A	(1)
MP208A	LM208A	(1)
MP208	LM208	(1)
MP308	LM308	(1)
MP308A	LM308A	(1)
MP355A	LF355A	(1)
MP356A	LF356A	(1)
MP357A	LF357A	(1)
MP2108A	LH2108A	(1)
MP5010H	LM385	
MP5010L	LM385	
MP5010G	LM185	
MP5010H	LM185	
MP5010L	LM185	
MP5010G	LM385	

MOTOROLA	NATIONAL	
DAC-08	DAC0800	
DAC-08	DAC0802	
DAC-08	DAC0801	
MC78XXACT	LM340AT-XX	(1)
MC78XXCK	LM78XXCK	(1)
MC78LXXACP	LM78LXXACZ	(1)
MC78MXXCT	LM78XXCK	(1)
MC78MXXCT	LM341P-XX	(1)
MC78LXXACG	LM78LXXCH	(1)
LM78XXCT	LM78LXXCH	(1)
MC78MXXCT	LM78MXXCT	(1)
MC78XXCT	LM78XXCT	(1)
MC78LXXCP	LM78LXXACZ	(1)
MX78MXXCT	LM342P-XX	(1)
MC78LXXCG	LM78LXXACH	(1)
MC79XXCK	LM320K-XX	(1)
MC79MXXCKC	LM320MP-XX	(1)
MC79XXCK	LM79XXCK	(1)
MC79XXCKC	LM320T-XX	(1)
LM79XXCP	LM79XXCT	(1)
MC79XXCT	LM79MXXCH	(1)
MC79LXXCP	LM320LZ-XX	(1)
MC79LXXACG	LM320H-XX	(1)
MC79LXXCLP	LM320LZ-XX	(1)
MC79XXCT	LM79MXXCP	(1)
MC79LXXACP	LM79LXXACZ	(1)
MC79LXXCP	LM79LXXCZ	(1)
MC79XXCT	LM320T-XX	(1)
MC79XXCT	LM79XXCT	(1)
MC79XXCT	LM79LXXACZ	(1)
LM79XXCP	LM79LXXACZ	(1)
LM79XXCP	LM79MXXCH	(1)
LM79XXCP	LM79MXXCP	(1)
LM109K	LM109K STEEL	(1)
LM109H	LM109H	(1)
LM117H	LM117K STEEL	(1)
LM123K	LM123K STEEL	(1)
LM137H	LM137H	(1)
LM137K	LM137K STEEL	(1)
LM140K	LM140K-XX	(1)
LM150K	LM150K STEEL	(1)
LM285	LM285	
LM309H	LM309H	(1)
LM309H	LM309K	(1)
LM309K	LM309K STEEL	(1)
LM317H	LM317H	(1)
LM317LZ	LM317LZ	(1)
LM317T	LM317T	(1)
LM317KC	LM317T	(1)
LM317K	LM317K STEEL	(1)
LM323K	LM323K STEEL	(1)
LM330-XKC	LM330T-XX	(1)
LM337H	LM337H	(1)
LM337K	LM337K STEEL	(1)
LM337KC	LM337T	(1)
LM337T	LM337T	(1)
LM340T-XX	LM340T-XX	(1)
LM340T-XX	LM340K-XX	(1)
LM340-XXKC	LM340T-XX	(1)
LM350T	LM350T	(1)
LM350K	LM350K STEEL	(1)
LM350KC	LM350T	(1)
LM350KA	LM350K STEEL	(1)
LM385	LM385	
AD562A	DAC1266	(2)
AD563A	DAC1265	(2)
μPC741	LM741	
MC1408	DAC0806	
MC1408	DAC0808	
MC1408	DAC0807	
MC1414	LM1414	(1)
MC1436	LM343	(1)
MC1458	LM1458	(1)
MC1496	LM1446	
MC1508	DAC0808	
MC1514	LM1514	(1)
MC1536	LM143	(1)
MC1558	LM1558	(1)
MC1596G	LM1596CH	(1)
MC1709	LM709	(1)
MC1709	LM709	
MC1710	LM710	
MC1723CL	LM723CJ	(1)
MC1723CG	LM723CH	(1)
MC1723CP	LM723CN	(1)
MC1723CL	LM723CM	(1)
MC1723L	LM723J	(1)
MC1723G	LM723H	(1)
MC1733CG	LM723CH	(1)
MC1741	LM741	(1)
MC1741	LM741	
MC1747	LM747	(1)
MC1747	LM747	
MC1748	LM748	
LM2930-XKC	LM2930T-XX	(1)
MC3301	LM3301	(1)
MC3302	LM3302	(1)
MC3361	LM3361AN	(1)
MC3401	LM3401	(1)
MC3410	DAC1020	(2)
MC3412	DAC1265	(1)
MC3510	DAC1020	(2)
MC4741	LM348	(1)
MC14442	ADC0829	(2)
MC14444	ADC0830	(2)
MC34001A	LF411C	(1)
MC34001B	LF411C	(1)
MC34001	LF351	(1)
MC34002B	LF412C	(1)
MC34002	LF353	(1)
MC34002A	LF412A	(1)
MC34004B	LF347B	(1)
MC34004	LF347	(1)
MC34004B	LF147	(1)
MC34004	LF147	(1)
MC35001	LF411M	(1)
MC35001A	LF411M	(1)
MC35001B	LF411M	(1)
MC35002B	LF412M	(1)
MC35002	LF412M	(1)
MC35002A	LF412AM	(1)

MC145040	ADC0811	(2)
MC145041	ADC0811	

PRECISION-MONOLITHIC INC.	NATIONAL	
REF-01J	LM368-10	(1)
REF-01	LM369	(1)
AMP-01	LH0038	(2)
DAC-02	DAC1022	(2)
DAC-02	DAC1020	(2)
REF-02	LM368-5.0	(3)
DAC-02	DAC1021	(2)
DAC-03	DAC1020	(2)
DAC-03	DAC1022	(2)
BUF03	LH0033	(1)
DAC-03	DAC1021	(2)
OP05	LM607	(2)
DAC-05	DAC1020	(2)
DAC-05	DAC1021	(2)
DAC-05	DAC1022	(2)
SW06B	LF11333	
SW06G	LF13333	
SW06F	LF13333	
OP07	LM607	(1)
DAC-08	DAC0801	
DAC-08	DAC0800	
MUX-08E	LF13508	
DAC-08	DAC0802	
OP15	LF411	(1)
MUX-24E	LF13509	
REF-43	LM368-2.5	(1)
OP77	LM607	(1)
OP100	LH0052	(2)
DAC100	DAC1021	(2)
DAC100	DAC1020	(2)
DAC100	DAC1022	(2)
OP105/111	LH0052	(2)
PM108A	LM108A	(1)
PM108	LM108	(1)
PM139A	LM139A	(1)
PM139	LM139	(1)
PM155	LF155	(1)
PM155A	LF155A	(1)
PM156	LF156	(1)
PM156A	LF156A	(1)
PM157	LF157	(1)
PM157A	LF157A	(1)
SW201G	LF13201	
SW201B	LF11201	
SW201F	LF13201	
SW202B	LF11202	
SW202F	LF13202	
SW202G	LF13202	
PM208A	LM208A	(1)
PM208	LM208	(1)
OP215	LF412	(1)
PM308A	LM308A	(1)
PM308	LM308	(1)
DAC312	DAC1266	(2)
PM339A	LM339A	(1)
PM355	LF355	(1)
PM355A	LF355A	(1)
PM356A	LF356A	(1)
PM356	LF356	(1)
PM357A	LF357A	(1)
PM357	LF357	(1)
PM420	LF124	(1)
OPA501/3573	LH0101	(2)
PM725	LM725	(1)
PM-725	LM725	
PM741	LM741	(1)
PM-741	LM741	
PM-747	LM747	
PM747	LM747	(1)
DAC888	DAC0831	(2)
DAC888	DAC0832	(2)
DAC888	DAC0830	(2)
ADC910	ADC1005	(2)
ADC910	ADC1025	(2)
DAC0812	DAC1208	(2)
DAC0812	DAC1209	
DAC0812	DAC1210	
DAC1408	DAC0806	(2)
DAC1408	DAC0808	(2)
DAC1408	DAC0807	(2)
PM2108A	LH2108A	(1)
PM7533	DAC1021	
PM7533	DAC1020	
PM7533	DAC1022	
PM7541	DAC1219	
PM7541	DAC1218	

RAYTHEON	NATIONAL	
REF-01	LM369	(1)
REF-01T	LM368	(1)
REF-02	LM368-5.0	(3)
REF-03	LM368-2.5	(1)
LP365	LP365	
RC714	LM607	(1)
RC741	LM741	(1)
RC741	LM741	
RC747	LM747	
RC747	LM747	(1)
RC1458	LM1458	(1)
RC1558	LM1558	(1)

RCA/ INTERSIL/G.E.	NATIONAL	
CA081C	TL081C	(2)
CA081A	LF411C	(2)
CA081	LF411M	(2)
CA081B	LF411C	(2)
CA082C	TL082C	(2)
CA082B	LF412C	(2)
CA082	LF412M	(2)
CA082A	LF412C	(2)
CA084B	LF347B	(2)
CA084	LF147	(2)
CA084C	LF347	(2)
CA124	LM124	(1)
CA139	LM139	(1)
CA139A	LM139A	(1)
CA158	LM158	(1)
CA158A	LM158A	(1)
DG201	LF11201	
DG211	LF13201	
DG212	LF13202	
CA224	LM224	(1)
CA239	LM239	(1)
CA239A	LM239A	(1)
CA258	LM258	(1)
CA258A	LM258A	(1)
CA301A	LM301A	(1)
CA307	LM307	(1)
CA311	LM311	(1)
CA324	LM324	(1)
CA339A	LM339A	(1)
CA339	LM339	(1)
CA358A	LM358A	(1)
CA358	LM358	(1)
CA741	LM741	
CA741	LM741	(1)
CA747	LM747	(1)
CA747	LM747	
CA748	LM748	(1)
μA748	LM748	
CA748	LM748	
ADC0801	ADC0801	
ADC0802	ADC0802	
ADC0803	ADC0803	
ADC0804	ADC0804	
CA1458	LM1458	(1)
CA1558	LM1558	(1)
CA3105	LM675	(2)
CA3290	LF393	(2)
CA3401	LM3401	(1)
IH5009	AH5009	
IH5010	AH5010	
IH5011	AH5011	
IH5012	AH5012	
IH6108	LF13508	
IH6208	LF13509	
ICL7114	ADC1205	(2)
ICL7114	ADC1225	(2)
AD7520	DAC1021	
AD7520	DAC1020	
AD7520	DAC1022	
AD7521	DAC1221	
AD7521	DAC1220	
AD7521	DAC1222	
AD7530	DAC1020	(3)
AD7530	DAC1021	(3)
AD7530	DAC1022	(3)
AD7531	DAC1220	
AD7531	DAC1221	
AD7531	DAC1222	
AD7533	DAC1020	
AD7533	DAC1021	
AD7533	DAC1022	
AD7541	DAC1219	
AD7541	DAC1218	
ICL7650	LMC668	(1)
ICL8069	LM385-1.2	
ICL8069	LM313	
ICH8530	LH0101	(2)

SAMSUNG	NATIONAL	
LM741	LM741	

SGS	NATIONAL	
L78M12CV	LM341P-12	(1)
L78M15CV	LM341P-15	(1)
L78S12CV	LM340T-12	(1)
L78S05CV	LM340T-5.0	(1)
L78S15CV	LM340T-15	(1)
L78M05CV	LM341P-5.0	(1)
LM117K	LM117K	(1)
L123CB	LM723CN	(1)
L272	LM18272	
L293	LM18293	
L298	LM18298	
LM317T	LM317T	(1)
LM317K	LM317K	(1)
LM748	LM748	
TDA2310	LM381	
LM2930A	LM2930T-5.0	(1)
LM2931A	LM2931AT-5.0	(1)
TCA3089	LM3089	
L7805CT	LM7805CK	(1)

L7815CV	LM7815CT	(1)
L7905ACV	LM320T-5.0	(1)
L7905CT	LM7905CK	(1)
L7905CV	LM7905CT	(1)
L7912CT	LM7912CK	(1)
L7912ACV	LM320T-12	(1)
L7915CT	LM7915CK	(1)
L7915ACV	LM320T-15	(1)

SIEMENS	NATIONAL	
TCA365	LH0101	(1)

SIGNETICS	NATIONAL	
DAC-08	DAC0802	
DAC-08	DAC0801	
DAC-08	DAC0800	
78LXXACS	LM78XXACZ	(1)
78LXXADB	LM78XXACH	(1)
78LXXCDB	LM78LXXCH	(1)
78LXXCS	LM78LXXCZ	(1)
78XXCU	LM78XXCT	(1)
78XXDA	LM78XXCK	(1)
79XXDA	LM79XXCK	(1)
79XXCU	LM79XXCT	(1)
LM109DB	LM109H	(1)
TBA120S-4	TBA120SIV	
TBA120S-3	TBA120SIII	
TBA120S-2	TBA120SII	
LF198	LF198	
LF298	LF298	
LM309DA	LM309K	(1)
LM309DB	LM309H	(1)
LM340XXLL	LM340TXX	(1)
LM340XXDA	LM340KXX	(1)
LF398	LF398	
NE529	LM361	(1)
SE529	LM161	(1)
SE532	LM158	(1)
SA532	LM2904	(1)
NE532	LM358	(1)
SA534	LM2902	(1)
NE555N	LM555CN	
SE567	LM567	(2)
μA723CN	LM723CN	(1)
μA723CL	LM723CH	(1)
μA723L	LM723H	(1)
μA723CF	LM723CJ	(1)
μA723F	LM723J	(1)
μA741	LM741	
μA747	LM747	
ADC0801	ADC0801	
ADC0802	ADC0802	
ADC0803	ADC0803	
ADC0804	ADC0804	
ADC0805	ADC0805	
MC1408	DAC0808	
MC1408	DAC0807	
MC1408	DAC0806	
MC1496N	LM1496N	
MC1508	DAC0808	
MC1596K	LM1596H	
NE4558D	LM833CM	(2)
NE4558N	LM833CN	(2)
NE4558	LM833	(2)
NE5034	ADC0841	(2)
SE5118	DAC0830	(2)
NE5118	DAC0830	(2)
NE5410	DAC1020	(2)
SE5410	DAC1020	(2)
NE5532P	LM833CN	(2)
NE5532	LM833	
NE5532N	LM833CN	(2)

SILICON GENERAL	NATIONAL	
SG101	LM101A	(1)
SG101A	LM101A	(1)
SG107	LM107	(1)
SG124	LM124	(1)
SG201	LM201A	(1)
SG201A	LM201A	(1)
SG207	LM207	(1)
SG224	LM224	(1)
SG301A	LM301A	(1)
SG307	LM307	(1)
SG324	LM324	(1)
SG741	LM741	(1)
SG741	LM741	(1)
SG1173	LM675	(2)
SG1436	LM343	(1)
SG1536	LM143	(1)
SG3173	LM675	(2)

SILICONIX	NATIONAL	
DG201	LF13201	
DG202	LF13202	
DG211	LF13201	
DG212	LF13202	
DG508	LF13508	
DG509	LF13509	

SPRAGUE	NATIONAL	
UDN22933	LM18293	

TELEDYNE	NATIONAL	
TP0032	LH0032	(1)
TP0033	LH0033	(1)

TEXAS INSTRUMENTS	NATIONAL	
μA78XXCKC	LM78XXCT	(1)
μA78LXXACL	LM78LXXACZ	(1)
μA78MXXCKD	LM78MXXCP	(1)
μA79MXXCKD	LM79MXXCP	(1)
μA79XXCKC	LM79XXCT	(1)
TL061A	LF441	(1)
TL061B	LF441A	(1)
TL061	LF441	(1)
TL062A	LF442	(1)
TL062B	LF442	(1)
TL062	LF442	(1)
TL064A	LF444	(1)
TL064	LF444	(1)
TL071B	LF411	(1)
TL071A	LF411	(1)
TL071	LF351	(1)
TL072	LF353	(1)
TL072A	LF412	(1)
TL072B	LF412	(1)
TL074	LF347	(1)
TL074A	LF347B	(1)
TL081B	LF411	(1)
TL081	TL081	(1)
TL081A	LF411	(1)
TL082B	LF412	(1)
TL082A	LF412	(1)
TL082	TL082	(1)
TL084A	LF347B	(1)
TL084	LF347	(1)
TL087	LF411A	(1)
TL088	LF411A	(1)
TLC274BI	LMC660AI	(2)
TLC274BM	LMC660AM	(2)
TLC274M	LMC660AM	(2)
TLC274AC	LMC660AI	(2)
TLC274BC	LMC660AI	(2)
TLC274AM	LMC660AM	(2)
TLC274I	LMC660AI	(2)
TLC274C	LMC660C	(2)
TLC274AI	LMC660AI	(2)
TL288	LF412A	(1)
LM317KC	LM317T	(1)
TL487N	LM3915N	(2)
TL489N	LM3914N	(2)
TL490N	LM3914N	(2)
TL491N	LM3914N	(2)
TL520	ADC0848	(2)
TL521	ADC0848	(2)
TL522	ADC0848	(2)
TL530	ADC0830B	
TL531	ADC0830C	
TL532	ADC0829B	
TLC532A	ADC0829B	(2)
TLC533A	ADC0829C	(2)
TL533	ADC0829C	
TLC540	ADC0811	(2)
TLC541	ADC0811	
TLC549	ADC0831	(2)
μA709	LM709	
μA723CN	LM723CN	(1)
μA723CJ	LM723CJ	(1)
μA723MJ	LM723J	(1)
μA733CN	LM733CN	
μA741	LM741	
μA747	LM747	
ADC0801	ADC0801	
ADC0802	ADC0802	
ADC0803	ADC0803	
ADC0804	ADC0804	
ADC0805	ADC0805	
ADC0808	ADC0808	
ADC0809	ADC0809	
ADC0831	ADC0831	
ADC0832	ADC0832	
ADC0834	ADC0834	
ADC0838	ADC0838	
RC4558	LM833	
RV4558D	LM833CM	
RC4558D	LM833CM	

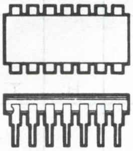
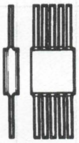
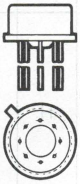
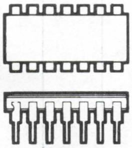
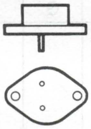
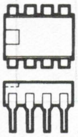
THOMSON	NATIONAL	
LM105H	LM105H	(1)
LM109K	LM109K STEEL	(1)
LM117K	LM117K STEEL	(1)
LM117H	LM117H	(1)
LM123K	LM123K STEEL	(1)
LM134	LM134	
LM135	LM135	
LM137K	LM137K STEEL	(1)
LM137H	LM137H	(1)
LM138K	LM138K STEEL	(1)
LF198	LF198A	(1)
LM234	LM234	
LM235	LM235	
LF298	LF298	
LM305H	LM305H	(1)
LM309H	LM309H	(1)
LM309K	LM309K STEEL	(1)

LM317K	LM317K STEEL	(1)
LM317H	LM317H	(1)
LM323K	LM323K STEEL	(1)
LM334	LM334	
LM335A	LM335A	
LM335	LM335	
LM337H	LM337H	(1)
LM337K	LM337K STEEL	(1)
LM338K	LM338K STEEL	(1)
LF398	LF398A	(1)
µA741	LM741	
µA748	LM748	
TBC0136	LM336	
µA7805CK	LM7805KC	(1)
µA7805MK	LM140K-5.0	(1)
µA7812MK	LM140K-12	(1)
µA7812CK	LM7812KC	(1)
µA7815CK	LM7815KC	(1)
µA7815MK	LM140K-15	(1)
µA7905MK	LM120K-5.0	(1)
µA7905CK	LM7905KC	(1)
µA7912MK	LM120K-12	(1)
µA7912CK	LM7912KC	(1)
µA7915MK	LM120K-15	(1)
µA7915CK	LM7915KC	(1)

TOSHIBA	**NATIONAL**	
TA7504	LM741	
TA75339	LM2901	(1)
TA75358	LM2904	(1)
TA75393	LM2903	(1)
TA75902	LM2902	(1)

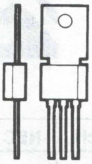
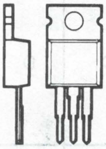
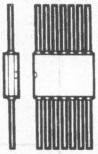
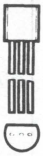
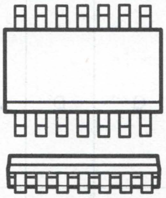
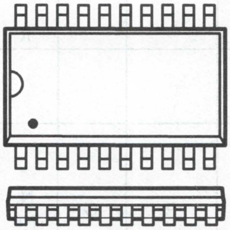
UNITRODE	**NATIONAL**
L293	LM18293
L298	LM18298

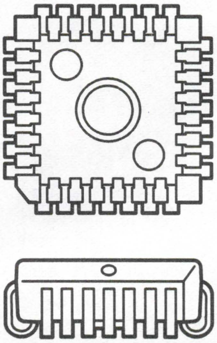
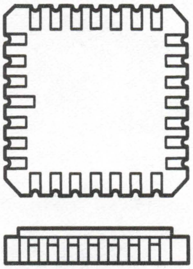
Industry Package Cross-Reference Guide

		NSC	Signetics	Fairchild	Motorola	TI	RCA	Hitachi	NEC	LTC
	4/16 Lead Glass/Metal DIP	D	I	D	L		D	C	D	D
	Glass/Metal Flat Pack	F	Q	F	F	F, S	K	F		Q
	TO-99, TO-100, TO-5	H	T, K, L, DB	H	G	L	S*, V1**		A	H
	8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	F	R, D	U	J		G	D	J, J8
	TO-3 (Steel)	K			KS					K
	TO-3 (Aluminum)	KC	DA	K	K	K				
	8-, 14- and 16-Lead Plastic DIP	N	V, A, B	T, P	P	P, N	E	P	C	N, N8

*With dual-in-line formed leads

**With radically formed leads

		NSC	Signetics	Fairchild	Motorola	TI	RCA	Hitachi	NEC	LTC
	TO-202 (D-40, Durawatt)	P					KD			
	TO-220 3- & 5-Lead	T	U	U		KC		T	H	T
	TO-220 11-, 15- & 23-Lead	T								
	Low Temperature Glass Hermetic Flat Pack	W		F	F	W				
	TO-92 (Plastic)	Z	S	W	P	LP			H	Z
 	SO (Narrow Body)	M	D	S	D	D	M	MP	G	S
	SO (Wide Body)	WM				DW				

		NSC	Signetics	Fairchild	Motorola	TI	RCA	Hitachi	NEC	LTC
	PCC	V	A	Q	FN	FN	Q	CP	L	
	LCC Leadless Ceramic Chip Carrier	E	G	L1	U	FK/ FG/FH	BJ	CG	K	

Linear 1 Databook

Selection Guides

Voltage Regulators

Operational Amplifiers

Buffers

Voltage Comparators

Instrumentation Amplifiers

National
Semiconductor
Corporation

Voltage Regulators
Definition of Terms

Current-Limit Sense Voltage: The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

Feedback Sense Voltage: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

Input Voltage Range: The range of dc input voltages over which the regulator will operate within specifications.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions at 125°C with maximum rated voltages and power dissipation for 1000 hours.

Maximum Power Dissipation: The maximum total device dissipation for which the regulator will operate within specifications.

Output-Input Voltage Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

Output Noise Voltage: The RMS ac voltage at the output with constant load and no inut ripple, measured over a specified frequency range.

Output Voltage Range: The range of regulated output voltages over which the specifications apply.

Output Voltage Scale Factor: The output voltage obtained for a unit value of resistance between the adjustment terminal and ground.

Quiescent Current: That par of input current to the regulator that is not delivered to the load.

Ripply Rejection: The line regulation for ac inupt signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal.

Standby Current Drain: That part of the operating current of the regulator which does not contribute to the load current. (See Quiescent Current)

Temperature Stability: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Thermal Regulation: Percentage change in output voltage for a given change in power dissipation over a specified time period.

National
Semiconductor
Corporation

Voltage Regulators Selection Guide

Adjustable Positive Voltage Regulators

Amps	Device	Output Voltage	Package
10.0	LM196K	1.25V–15V	TO-3
	LM396K	1.25V–15V	TO-3
5.0	LM138K	1.2V–32V	TO-3
	LM338K	1.2V–32V	TO-3
3.0	LM150K	1.2V–33V	TO-3
	LM350K, T	1.2V–33V	TO-3, TO-220
1.5	LM117K	1.2V–37V	TO-3
	LM117HVK	1.2V–57V	TO-3
	LM2941CT	5.0V–24V	TO-220
	LM317K, T	1.2V–37V	TO-3, TO-220
	LM317HVK	1.2V–57V	TO-3
0.5	LM117H	1.2V–37V	TO-39
	LM117HVH	1.2V–57V	TO-39
	LM317H	1.2V–57V	TO-39
	LM317HVH	1.2V–37V	TO-39
	LM317MP	1.2V–37V	TO-202
0.1	LM317LZ, M	1.2V–37V	TO-92, SO-8
	LM2931CT	3.0V–24V	TO-220, 5-LEAD
	LP2951CN, J, H, M	1.24V–29V	DIP, CERDIP, HEADER, SO-8

Adjustable Negative Voltage Regulators

Amps	Device	Output Voltage	Package
3.0	LM133K	−1.2V – −32V	TO-3
	LM333K, T	−1.2V – −32V	TO-3, TO-220
1.5	LM137K	−1.2V – −37V	TO-3
	LM137HVK	−1.2V – −47V	TO-3
	LM337K, T	−1.2V – −37V	TO-3, TO-220
	LM337HVK	−1.2V – −47V	TO-3
0.5	LM137H	−1.2V – −37V	TO-39
	LM137HVH	−1.2V – −47V	TO-39
	LM337H	−1.2V – −37V	TO-39
	LM337HVH	−1.2V – −47V	TO-39
	LM337MP	−1.2V – −37V	TO-202
0.1	LM337LZ, M	−1.2V – −37V	TO-92, SO-8

Fixed Positive Voltage Regulators

Amps	Device	Output Voltage	Package
3.0	LM123K	5V	TO-3
	LM2943CT*	5V	TO-220
	LM323K	5V	TO-3
1.0	LM109K	5V	TO-3
	LM140AK	5V, 12V, 15V	TO-3
	LM140K	5V, 12V, 15V	TO-3
	LM2940CT	5V, 12V, 15V	TO-220
	LM309K	5V	TO-3
	LM340AK, T	5V, 12V, 15V	TO-3, TO-220
	LM340K, T	5V, 12V, 15V	TO-3, TO-220
	LM78xxCK, T	5V, 12V, 15V	TO-3, TO-220
0.5	LM2984CT	5V, 12V, 15V	TO-220, TO-202
	LM341T, P	5V, 12V, 15V	TO-220, TO-202
	LM78MxxCT	5V, 12V, 15V	TO-220
0.2	LM109H	5V	TO-39
	LM309H	5V	TO-39
	LM342P	5V, 12V, 15V	TO-202
0.15	LM2930T	5V, 8V	TO-220
0.1	LM140LAH	5V, 12V, 15V	TO-39
	LM2931Z, T	5V	TO-92, TO-220
	LM340LZ, H	5V, 12V, 15V	TO-92, TO-39
	LM78LxxACZ, H, M	5V, 12V, 15V	TO-92, TO-39, SO-8
	LP2950CZ	5V	TO-92

*Future Product

Fixed Negative Voltage Regulators

Amps	Device	Output Voltage	Package
3.0	LM145K	−5V, −5.2V	TO-3
	LM345K	−5V, −5.2V	TO-3
1.5	LM120K	−5V, −12V, −15V	TO-3
	LM320K, T	−5V, −12V, −15V	TO-3, TO-220
	LM79xxCT, K	−5V, −12V, −15V	TO-3, TO-220
0.5	LM320MP	−5V, −12V, −15V	TO-220
	LM79MxxCP, K	−5V, −12V, −15V	TO-202, TO-3
0.2	LM120H	−5V, −12V, −15V	TO-39
	LM320H	−5V, −12V, −15V	TO-39
0.1	LM320LZ	−5V, −12V, −15V	TO-92
	LM79LxxACZ, M	−5V, −12V, −15V	TO-92, SO-8

*The LM320 has better electrical characteristics than the LM79xx.

LM100 Series	+55°C to +150°C
LM300 Series	0°C to +125°C

Low Dropout Regulators

Amps	Device	Output Voltage	Package
0.100	LM2931T, Z	5V, ADJ	TO-220, TO-92
	LP2950CZ	5V	TO-92
	LP2951N, J, H	ADJ	DIP, CERDIP, HEADER
0.150	LM2930T	5V, 8V	TO-220
0.500	LM2984CT	TRIPLE 5V + WATCHDOG	TO-220, 11-LEAD
0.750	LM2925T	5V WITH DELAYED RESET	TO-220, 5-LEAD
	LM2935T	DUAL 5V	TO-220, 5-LEAD
1.5	LM2940CT	5V, 12V, 15V	TO-220
	LM2941CT*	ADJ	TO-220, 5-LEAD
3.0	LM2943CT*	5V	TO-220

*Future Product

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Operational Amplifiers Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

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General Purpose Operational Amplifier Selection Guide

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Military Temperature Range (−55°C to +125°C) Specs at T_A = 25°C (Note 1)								
LH0044A	0.025	15	0.4	0.06	3	±3	±20	
LM607A	0.025	2	1.8	0.7	1.5	*	±22	
LH0044	0.05	30	0.4	0.06	4	±3	±20	
LM607B	0.05	3	1.8	0.7	1.5	*	±22	
LM11	0.3	0.05	*	0.3	0.6	*	±20	
LF411A	0.5	0.2	4	15	2.8	±6	±22	
LF441A	0.5	0.05	1	1	0.2	±6	±22	
LH0052	0.5	0.003	1	3	3.5	±5	±22	
LM108A	0.5	2	1	0.3	0.4	±2	±20	
LF412A	1	0.2	4	15	5.6	±6	±22	Dual BiFet
LF442A	1	0.05	1	1	0.4	±6	±22	Dual BiFet
LH0004	1	100	*	*	0.15	±5	±45	
LM604A	1	40	7	2	8	4	36	Multiplexed OA
LF155A	2	0.05	2.5	5	4	±5	±22	
LF156A	2	0.05	5	12	7	±5	±22	
LF157A	2	0.05	25	50	7	±5	±22	Minimum Gain of 5
LF411	2	0.2	4	15	3.4	±6	±18	
LMC660A	2	0.02	1.5	1.7	2.2	5	15	Quad CMOS
LM10	2	20	*	*	0.4	(Note 4)		OA + Reference
LM101A	2	75	1	0.5	3	±3	±22	
LM107	2	75	1	0.5	3	±3	±22	
LM108	2	2	1	0.3	0.4	±2	±20	
LM112	2	2	1	0.2	0.6	±2	±20	Compensated LM108
LM124A	2	50	*	*	3	3	32	Quad
LM158A	2	50	*	*	1.2	3	32	Dual
LP124	2	4	0.1	0.05	0.13	3	32	Quad
LH0020	2.5	250	*	*	5	±5	±22	
LF412	3	0.2	4	15	6.8	±6	±22	Dual
LM741A	3	80	1.5	0.7	2.8	±3	±22	
LH0022	4	0.01	1	3	3.5	±5	±22	
LF155	5	0.1	2.5	5	4	±5	±22	

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Military Temperature Range (−55°C to +125°C) Specs at T_A = 25°C (continued)								
LF156	5	0.1	5	12	7	±5	±22	
LF157	5	0.1	20	50	7	±5	±22	Minimum Gain of 5
LF147	5	0.2	4	13	11	±6	±22	Quad BiFet
LF412	5	0.2	4	15	6.8	±6	±18	Dual BiFet
LF442	5	0.1	1	1	0.5	±6	±18	Dual BiFet
LF444A	5	0.1	1	1	0.80	±6	±22	Quad BiFet
LH0086	5	0.5	3	10	15.5	±8	±18	Programmable Gain OA
LM124	5	150	*	*	3	3	32	Quad
LM143	5	20	1	2.5	4	±4	±40	
LM144	5	20	1	2.5	4	±4	±40	Minimum Gain of 10
LM146	5	100	1.2	0.4	2	±1.5	±22	(Note 5)
LM148	5	100	1	0.5	3.6	±5	±22	Quad
LM149	5	100	4	2	3.6	±5	±22	Minimum Gain of 5, Quad
LM158	5	150	*	*	1.2	3	32	Dual
LM192	5	150	*	*	2	3	32	Comparator and Op Amp
LM741	5	500	*	0.5	2.8	±3	±22	
LM1558	5	500	*	*	5	±3	±22	Dual
LM4250	5	50	0.2	0.2	0.1	±1	±18	(Note 5)
LH0042	20	0.025	1	3	3.5	±5	±22	

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Industrial Temperature Range (−25°C to +85°C) (Note 1)								
LMC669B	0.025	0.1	*	*	6	±8	±22	Autozero Block
LH0044B	0.05	30	0.4	0.06	4	±3	±20	
LH0044C	0.05	30	0.4	0.06	4	±3	±20	
LMC669C	0.05	0.1	*	*	6	±8	±22	Autozero Block
LM208A	0.5	2	1	0.3	0.6	±2	±20	
LH0052C	1	0.005	1	3	3.8	±5	±22	
LMC660A	2	0.02	1.5	1.7	2.2	5	15	Quad CMOS
LM10B(L)	2	20	*	*	0.4	(Note 4)		Op Amp and Reference
LM201A	2	75	1	0.5	3	±3	±22	
LM207	2	75	1	0.5	3	±3	±22	
LM208	2	2	1	0.3	0.6	±2	±20	
LM212	2	2	1	0.3	0.6	±2	±20	Compensated LM208
LM224A	3	80	*	*	2	3	32	Quad

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage Min V	Supply Voltage Max V	Special Features
Industrial Temperature Range (−25°C to +85°C) (continued)								
LM258A	3	80	*	*	1.2	3	32	Dual
LF255	5	0.1	2.5	5	4	±5	±22	
LF256	5	0.1	5	12	7	±5	±22	
LF257	5	0.1	20	50	7	±5	±22	Minimum Gain of 5
LM224	5	150	*	*	2	3	32	Quad
LM258	5	150	*	*	1.2	3	32	Dual
LM292	5	250	*	*	2	3	32	Comparator and Op Amp
LH0020C	6	500	*	*	6	±5	±22	
LH0022C	6	0.025	1	3	4	±5	±22	
LM246	6	250	0.5	0.4	2.5	±2	±18	(Note 5)
LM248	6	200	1	0.5	4.5	±5	±18	Quad
LM249	6	200	4	2	4.5	±5	±18	Minimum Gain of 5, Quad
LH0086C	10	0.5	3	10	15.5	±8	±18	Programmable Gain 1 to 200
LH0042C	20	0.05	1	3	4	±5	±22	

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage Min V	Supply Voltage Max V	Special Features
Commercial Temperature Range (0°C to +70°C) (Notes 1 and 2)								
LMC668A	0.005	0.06	1	2.5	3.5	*	18	Commutating Autozero
LMC668	0.01	0.06	1	2.5	3.5	*	18	Commutating Autozero
LMC669B	0.025	0.1	*	*	6	±8	±22	Autozero Block
LM607A	0.025	2	1.8	0.7	1.5	*	±22	
LMC669C	0.05	0.1	*	*	6	±8	±22	Autozero Block
LM607B	0.05	3	1.8	0.7	1.5	*	±22	
LM607	0.15	10	1.8	0.7	1.8	*	±22	
LF411A	0.5	0.2	4	15	2.8	±6	±22	
LF441A	0.5	0.05	1	1	0.2	±6	±22	
LM308A	0.5	7	1	0.3	0.8	±2	±20	
LM11C	0.6	0.1	*	0.3	0.8	*	±20	
LF412A	1	0.2	4	15	5.6	±6	±22	Dual
LF442A	1	0.05	1	1	0.4	±6	±22	Dual
LM604A	1	40	5	3	9	4	36	Multiplexed Op Amp
LF355A	2	0.05	2.5	5	4	±5	±22	
LF356A	2	0.05	5	12	10	±5	±22	
LF357A	2	0.05	20	50	10	±5	±22	Minimum Gain of 5

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage Min V	Supply Voltage Max V	Special Features
Commercial Temperature Range (0°C to +70°C) (continued)								
LF411	2	0.2	4	15	3.4	±6	±22	
LF412	3	0.2	4	15	6.8	±6	±22	Dual
LM324A	3	100	*	*	3	3	32	Quad
LM358A	3	100	*	*	2	3	32	Dual
LM604	3	60	5	7	9	4	36	Multiplexed Op Amp
LM741E	3	80	1.5	0.7	2.8	±3	±22	
LM10C(L)	4	30	*	*	0.5	(Note 4)		OA and Reference
LP324	4	10	0.1	0.05	0.15	3	32	
LF347B	5	0.2	4	13	11	±6	±22	Quad
LF355B	5	0.1	2.5	5	4	±5	±22	
LF356B	5	0.1	5	12	4	±5	±22	
LF357B	5	0.1	20	50	7	±5	±22	
LF441	5	0.1	1	1	0.25	±6	±22	
LF442	5	0.1	1	1	0.5	±6	±22	Dual
LM11CL	5	0.2	*	0.3	0.8	*	±20	
LM392	5	250	*	*	2	3	32	
LM833	5	1000	10	5	8	*	±18	Dual Low Noise
LMC660	6	0.02	1.5	1.7	2.7	5	15	Quad CMOS
LM346	6	250	0.5	0.4	2.5	±1.5	±22	(Note 5)
LM348	6	200	1	0.5	4.5	±5	±18	
LM349	6	200	4	2	4.5	±5	±18	
LM741C	6	500	1.5	0.5	2.8	±3	±18	
LM1458	6	500	*	*	5.6	±3	±18	
LM4250C	6	75	0.2	0.2	0.1	±1	±18	(Note 5)
LM324	7	250	*	*	3	3	32	
LM358	7	250	*	*	2	3	32	
LM301A	7.5	250	1	0.5	3	±3	±18	
LM307	7.5	250	1	0.5	3	±3	±18	
LM308	7.5	7	1	0.3	0.8	±2	±18	
LM312	7.5	7	1	0.2	0.8	±2	±18	Compensated LM308
LM343	8	40	1	2.5	5	±4	±34	
LM344	8	40	1	2.5	5	±4	±34	Minimum Gain of 10
LF347	10	0.2	4	13	11	±6	±18	Quad BiFet
LF351	10	0.2	4	13	3.4	±6	±18	
LF353	10	0.2	4	13	6.8	±6	±18	Dual BiFet
LF355	10	0.2	2.5	5	4	±5	±18	
LF356	10	0.2	5	12	10	±5	±18	
LF357	10	0.2	20	50	10	±5	±18	Minimum Gain of 5

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Commercial Temperature Range (0°C to +70°C) (continued)								
LF444	10	0.1	1	1	1	±6	±18	Quad BiFet
LF13741	15	0.2	1	0.5	4	*	±18	
TL081C	15	0.2	4	13	2.8	±6	±18	
TL082C	15	0.2	4	13	5.6	±6	±18	Dual BiFet

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/µs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Automotive Temperature Range (−40°C to +85°C)								
LM604	3	60	7	3	9	4	36	Multiplexed Op Amp
LP2902	4	20	0.1	0.05	0.15	3	26	Quad
LM2902	7	250	*	*	3	3	26	Quad
LM2904	7	250	*	*	2	3	26	Quad
LM2924	7	250	*	*	2	3	26	Comparator Plus Op Amp

*Not Specified.

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: Those looking for a commercial part should also look at the Industrial Temp Range guide as many Hybrids are listed there.

Note 3: Supply current is for all amplifiers in a package.

Note 4: The LM10 has 2 versions: one a high voltage part, good to 45V and a low voltage part, good to 7V. Refer to the datasheet for more information.

Note 5: The LM146 and LM4250 are programmable amplifiers. The data shown is for $V_S = \pm 15V$ and $I_{SET} = 10\ \mu A$. Refer to the datasheets for more information.

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Low I_{BIAS} Selection Guide

≤5 pA	≤20 pA	≤50 pA	≤100 pA	≤200 pA	≤500 pA	≤1 nA
T_A = 25°C						
LH0022	LMC668	LH0032A	LH0032	LF401A	LH4101	LH4104
LH0022C	LMC660	LF155A/156A	LF155/156	LF401	LH0032C	
LH0042		LF157A	LF157	LF400A	LH0086	
LH0042C		LF355A/356A	LF255/256	LF400	LH0086C	
LH0052		LF357A	LF257	TL081		
LH0052C		LF441A	LF355B/356B	LH0032AC		
LH0062		LF442A	LF357B	LF351		
		LF444A	LF441	LF411A/411		
		LM11	LF442	LF355/356		
			LF444	LF357		
			LM11C	LF147/347B/347		
			LH0062C	LF353		
				LF412A/412		
				LF13741		
				LM11CL		

Note: Datasheet should be referred to for conditions and more detailed information.

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High Speed Operational Amplifier Selection Guide

Part #	Slew Rate V/µs (Typ)	GBW MHz (Typ)	V_{OS} mV (Max)	I_S mA (Max) (Note 2)	Notes
GBW ≥ 4 MHz, T_A = 25°C					
LH0024	500	70	8	15	
LH0032	500	70	15	22	FET Input
LM6361	300	50	20	6.8	
LM6364	300	175	9	6.8	Min Gain of 5
LM6365	300	725	7	6.8	Min Gain of 25
LH4101	250	40	15	40	Medium Power JFET
LF400	70	16	2.5	12	Fast Settling JFET
LF401	70	16	0.5	12	Precision Fast Settling JFET
LH0003	70	30	3	3	
LH0062	70	15	15	12	FET Input
LM318	70	15	10	10	
LF357	50	20	10	10	Min Gain of 5, JFET
LH4104	40	16	10	25	Medium Power Fast Settling JFET
LM359	30	30	*	22	Dual Current Mode (Norton) Amp
LF411	15	4	2	3.4	JFET
LF412	15	4	3	6.8	Dual JFET
LF347	13	4	10	11	Quad JFET
LF351	13	4	10	3.4	JFET
LF353	13	4	10	6.8	Dual JFET
LF356	12	4.5	10	10	JFET
LM833	7	15	5	8	Dual Low Noise

*Not specified.

Note 1: Datasheet should be referred to for conditions and more detailed information. Many versions with better DC specs are available in addition to those listed above.

Note 2: Supply current is for all amplifiers in a package.

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Medium and High Power Operational Amplifier Selection Guide ($\geq$ 0.1A Output)

Part #	I_{OUT} A (Typ)	V_{OS} mV (Max)	I_S mA (Max)	Slew Rate V/μS (Typ)	PBW kHz (Typ)
LH4104	0.1	10	25	40	*
LH4101	0.1	15	40	250	*
LH0041	0.2	6	4	1	20
LH0061	0.5	15	15	25	1000
LH0021	1.0	6	4	1	20
LH0101A	2	3	35	10	300
LH0101	2	10	35	10	300
LM675	3	10	50	8	*
LM12(L)	(Note 2)	7	80	9	60
LM12C(L)	(Note 2)	15	120	9	60

*Not Specified

Note 1: Refer to Datasheet for conditions and more detailed information.

Note 2: I_{OUT} for the LM12 is dependent on the amount of power dissipated in the output transistor. The datasheet should be referred to, to determine amount of current available.

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Special Amplifier Selection Guide

LH0045	Two Wire Transmitter
LH0082	20 MHz Transimpedance Amplifier
LH0086	Programmable Gain Operational Amplifier
LM359	Dual Current Mode (Norton) Amplifier
LM2900, 3900, 3301, 3401	Quad Current Mode (Norton) Amplifier
LM3080	Operational Transconductance Amplifier
LM13600	Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers
13700	Improved Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers
LM604	4 In, 1 Out Multiplexed Op Amp

Note: Refer to the datasheet for specifications.

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Buffers
Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental.

$$\begin{array}{c}\text{\% harmonic}\\ \text{distortion}\end{array} = \frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

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Buffers Selection Guide (Notes 1 and 2)

Device Type	−3 dB MHz (Typ)	V_{OS} mV (Max)	I_S mA (Max)	Voltage Gain (Typ)	V_{OUT} V (Min)	S. R. V/µs (Typ)	I_{OUT} mA (Typ)
LM110, 210, 310	20	7.5	5.5	0.9999	±10	3.0	10
LH4001	25	500	10	0.97	±10	125	200
LH0002	30	±30	10	0.97	±10	100	200
LH0033	100	20	24	0.98	±9	1400	100
LH4002	200	50	35	0.85	±3	1250	40
LH0063	200	±50	65	0.93	±10	2400	250

*Not specified

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: 200°C Temp Range Parts are available. Consult local sales office for information.

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Voltage Comparators Definition of Terms

Input Bias Current: The average of the two input currents.

Input Offset Current: The absolute value of the difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

Input Offset Voltage: The absolute value of the voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

Input Voltage Range: The range of voltage on the input terminals (common-mode) over which the offset specifications apply.

Logic Threshold Voltage: The voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

Negative Output Level: The negative DC output voltage with the comparator saturated by a differential input equal to or greater than a specified voltage.

Output Leakage Current: The current into the output terminal with the output voltage within a given range and the input drive equal to or greater than a given value.

Output Resistance: The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

Output Sink Current: The maximum negative current that can be delivered by the comparator.

Positive Output Level: The high output voltage level with a given load and the input drive equal to or greater than a specified value.

Power Consumption: The power required to operate the comparator with no output load. The power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

Response Time: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Saturation Voltage: The low-output voltage level with the input drive equal to or greater than a specified value.

Strobe Current: The current out of the strobe terminal when it is at the zero logic level.

Strobe Output Level: The DC output voltage, independent of input conditions, with the voltage on the strobe terminal equal to or less than the specified low state.

Strobe "ON" Voltage: The maximum voltage on either strobe terminal required to force the output to the specified high state independent of the input voltage.

Strobe "OFF" Voltage: The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator.

Strobe Release Time: The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to the one logic level.

Supply Current: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

Voltage Gain: The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

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Voltage Comparators Selection Guide

	Response Time (Typ) ns	V_{OS} mV(Max)	I_S mA(Max)	I_B nA(Max)	Comments
$T_A = 25°C$ (Notes 1 and 2)					
LM361	12	5	25	30,000	High Speed w/Strobes
LM360	16	5	32	20,000	High Speed, Complementary Outputs
LM306	40	5	10	25,000	High Speed, High Drive
LM319	80	8	12.5	1000	High Speed Dual
LF311	200	10	7.5	0.15	FET Input
LM311	200	10	7.5	300	General Purpose Single
LM339	1300	5	2	400	General Purpose Quad
LM392	1300	10	1	400	One Comparator Plus One Op Amp
LM393	1300	5	2.5	250	General Purpose Dual
LM2903	1300	5	2.5	250	Automotive Dual
LM2901	1300	7	2	400	Automotive Quad
LP365	4000	9	0.30	200	Programmable Quad
LP311	4000	10	0.3	150	Low Power Single
LP339	5000	9	0.1	40	Low Power Quad

*Not Specified

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: This selection guide should be used to select for Response Time required. Industrial and Military Temperature Range types are available. The DC specs are for the lowest Commercial Grade available.

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Instrumentation Amplifiers
Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

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Instrumentation Amplifiers Selection Guide

Part Number	Gain Error (Max)	Gain Linearity (Typ)	CMRR dB (Min)	I_B nA (Max)
$T_A = 25°C$				
LH0036 μ Power	3%	0.03%	46	125
LH0038	3%	0.0001%	86	100
LH0084	0.3%	0.005%	80	0.500
LM363	2.5%	0.01%	90	10

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Linear 3 Databook

Selection Guides

Audio Circuits

Radio Circuits

Video Circuits

Motion Control

Special Functions

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Audio Circuits
Definition of Terms

Amplifier

Class A

A class A transistor audio amplifier refers to an amplifier with a single output device that has a collector flowing for the full 360° of the input cycle.

Class B

The most common type of audio amplifier that basically consists of two output devices each of which conducts for 180° of the input cycle.

Class C

In a class C amplifier the collector current flows for less than 180°. Although highly efficient, high distortion results and the load is frequently tuned to minimize this distortion (primarily used in R.F. power amplifiers).

Class D

A switching or sampling amplifier with extremely high efficiency (approaching 100%). The output devices are used as switches, voltage appearing across them only while they are off, and current flowing only when they are saturated.

Crossover Distortion

Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current allowing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for I/Cs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion for negative going transition through zero at the higher audio frequencies.

Dolby B

Dolby B is a simplified version of the Dolby A professional quality noise reduction system. The amplitude of low level signals over a selected frequency range is increased prior to recording to enhance them above tape noise. On playback the original levels are restored causing a corresponding reduction in the audible tape noise. The major difference with Dolby A which used four frequency bands, is the use of a single variable frequency band with a cut-off frequency that increases in the presence of high level high frequency signals.

Dolby Level

Because of the complementary nature of the Dolby B noise reduction system, the audio channel between the encoder and the decoder must have a fixed gain such that the decoding signal level is within 2 dB of the encoding signal level. Also if recordings are interchangeable the signals in the noise reduction system must be related to the levels in the audio channel. Dolby level provides this reference and corresponds to a specified tape flux density when recorded with a 400 Hz tone. For reel to reel and eight track cartridge tapes this is 185 nWb/m, and for cassettes Dolby level is 200 nWb/m.

Large-Signal Voltage Gain

The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Resistance

The ratio of the change in output voltage to the change in output current with the output around zero.

Output Voltage Swing

The peak output voltage swing, referred to zero, that can be obtained without clipping.

Power Bandwidth

The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 6 dB below the rated output. For example, an amplifier rated at 60 watts with $\leq$0.25% THD, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30 watts.

Power Supply Rejection

The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Slew Rate

The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Supply Current

The current required from the power supply to operate the amplifier with no load and the output at zero.

Thermal Resistance (R_{TH})

An analogy for heat transfer where the ability of a heat conductive system to transfer heat is described in similar terms to those used in an electrical system for power dissipated in a resistor with a given applied voltage. The thermal resistance is given by the temperature differential established when a given amount of power is being dissipated ($\theta = T1 - T2/P_D$) with units of °C/watt.

National Semiconductor Corporation

Audio Selection Guide

PREAMPLIFIERS

	Application			Package	Voltage Range	Equivalent Input Noise	THD	PSR	Input Coupling	Notes
	Portable	Home	Auto							
LM381	•	•		14 Pin DIP	9V–40V	0.5 μV	0.1%	120 dB	AC	Stereo
LM382	•	•	•	14 Pin DIP	9V–40V	0.8 μV	0.1%	120 dB	AC	Stereo
LM387	•	•	•	8 Pin DIP	9V–30V	0.65 μV	0.1%	110 dB	AC	Stereo
LM1818	•	•	•	20 Pin DIP	3.5V–18V	0.85 μV	0.05%	85 dB	AC	Tape System
LM1837	•	•	•	18 Pin DIP	4V–18V	0.6 μV†	0.03%	105 dB	DC	Autoreverse
LM1897	•	•	•	16 Pin DIP	4V–18V	0.6 μV†	0.03%	105 dB	DC	Few Externals
LM833 (Note 1)		•	•	8 Pin DIP 8 Pin SO	±5V–±15V	0.5 μV	0.002%	100 dB	DC	Low Noise Dual Op Amp
LM837 (Note 1)		•	•	14 Pin DIP 14 Pin SO	±5V–±15V	0.5 μV	0.002%	100 dB	DC	Low Noise Quad Op Amp Drives 600Ω Load

†CCIR/ARM in DIN circuit referred to unity gain at 2 kHz.

Note 1: Data sheet in Linear 1.

AUDIO POWER AMPLIFIERS

	Application			Package	Power*			@ Voltage	Bridgeable	THD*	Input Noise*	Single/ Dual	Notes
	Portable	Home	Auto		8Ω	4Ω	2Ω						
LM380		•		8 Pin DIP 14 Pin DIP	2.5W			18V		0.2%		Single	See AN-69
LM383	•		•	5 Pin TO-220		5.5W	8.6W	14.4V	Yes	0.2%	2 μV	Single	Protected
LM384		•		14 Pin DIP	5.5W			22V		0.25%		Single	Fixed Gain
LM386	•	•		8 Pin DIP 8 Pin SO		0.33W		6V		0.2%		Single	4V Operation
LM388	•			14 Pin DIP	2.2W			12V	Yes	0.1%		Single	Minimum Externals
LM389	•			18 Pin DIP		0.33W		6V		0.2%		Single	Includes Transistor Array
LM390	•			14 Pin DIP		1W		6V	Yes	0.2%		Single	Battery Operation
LM391				16 Pin DIP				60V–100V		0.01%	3 μV	Single	Power Driver
LM1877	•	•	•	14 Pin DIP	3W			20V		0.05%	2.5 μV	Dual	6V–24V
LM2877	•	•	•	11 Pin SIP	4.5W			20V		0.07%	2.5 μV	Dual	Single-In-Line Package
LM1895	•	•	•	8 Pin DIP		1.1W		6V		0.2%	1.4 μV	Single	Low AM Radiation
LM2895	•	•	•	11 Pin SIP		4.3W		12V		0.15%	1.4 μV	Single	3V–15V

AUDIO POWER AMPLIFIERS (Continued)

	Application			Package	Power*			@ Voltage	Bridgeable	THD*	Input Noise*	Single/ Dual	Notes
	Portable	Home	Auto		8Ω	4Ω	2Ω						
LM1896	•	•	•	14 Pin DIP		1.1W		6V	Yes	0.1%	1.4 μV	Dual	Low AM Radiation
LM2896	•	•	•	11 Pin SIP		2.5W		9V	Yes	0.1%	1.4 μV	Dual	No Pops
LM2002	•		•	5 Pin TO-220		5.2W	8W	14.4V	Yes	0.1%	2 μV	Single	Protected
LM2878		•		11 Pin SIP	5.5W			22V	Yes	0.15%	2.5 μV	Dual	6V–32V
LM831	•			16 Pin DIP 20 Pin SO	0.44W			3V	Yes	0.2%	1.3 μV	Dual	1.8V–6V
LM12 (Note 1)		•		TO-3	50W	85W		±30V		0.01%		Single	Power Op Amp
LM675 (Note 1)		•		5 Pin TO-220	20W			±25V			3 μV	Single	Power Op Amp
LM1875		•		5 Pin TO-220	20W			±25V		0.015%	3 μV	Single	Low Crossover Distortion
LM2005			•	11 Pin TO-220		20W		14.4V	Yes	0.3%	1.5 μV	Dual	Protected
LM2879		•		11 Pin TO-220	8W			28V	Yes	0.05%	2.5 μV	Dual	6V–32V

*Note that all values shown are typical. Please refer to data sheets for test conditions.

Note 1: Data sheet in Linear 1.

AUDIO CONTROLS

	Application			Package	Voltage Range	Volume Control Range	Signal to Noise	THD	Separation	Notes
	Portable	Home	Auto							
LM1035/ LM1036	•	•	•	20 Pin DIP	8V–18V	80 dB	80 dB	0.05%	75 dB	Dual DC Controlled Tone/Volume/Balance
LM1037	•	•	•	18 Pin DIP	5V–30V		100 dB	0.04%	100 dB	DC Audio Switch
LM1038	•	•	•	18 Pin DIP	5V–30V		100 dB	0.04%	100 dB	BCD Logic Control
LM13600 (Note 1)	•	•	•	16 Pin DIP	±2V–±18V			0.5%	100 dB	Transconductance Amplifiers
LM13700 (Note 1)	•	•	•	16 Pin SO						
LM3080 (Note 1)	•	•	•	8 Pin DIP	±2V–±18V					Transconductance Amplifier
LM1040	•	•	•	24 Pin DIP	9V–16V	75 dB	80 dB	0.06%	75 dB	Dual DC Controlled Tone/Volume/Balance Stereo Enhancement
LMC835		•	•	28 Pin DIP	±2.5V–±8V		114 dB	*		7 Band Graphic Equalizer MICROWIRE™ Controlled
LMC1992/ LMC1993 (Note 2)		•	•	28 Pin DIP	7V–15V	80 dB	105 dB	0.03%	95 dB	Stereo Volume/ Tone/Fade/Select MICROWIRE™ Controlled

*Distortion determined by external op amps.

Note 1: Data sheet in Linear 1.

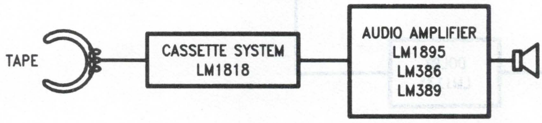
Note 2: LMC1992 selects 4 inputs.
LMC1993 selects 3 inputs and has a loudness control.

NOISE REDUCTION

	Application			Package	Voltage Range	NR Type	NR Effect*	Encoding Required	Single/ Dual/	Decode S/N*	Notes
	Portable	Home	Auto								
LM1131	•	•	•	18 Pin DIP	7V–20V	Dolby	10 dB	Yes	Dual	90 dB	DC Switched
LM1894	•	•	•	14 Pin DIP, SO	4.5V–18V	DNR	12 dB	No	Dual	76 dB	NSC System
LM1112	•	•	•	16 Pin DIP	6V–20V	Dolby	10 dB	Yes	Single	83 dB	
LM1141	•	•	•	28 Pin DIP, Quad	5V–16V	Dolby		Yes	Single		Dolby B/C
LM832	•			14 Pin DIP, SO	1.5V–9V	DNR	12 dB	No	Dual	76 dB	NSC System

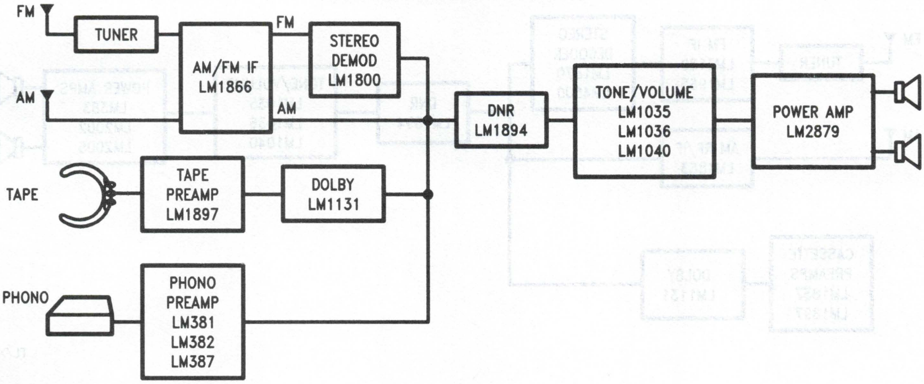
*Note that all values shown are typical. Please refer to data sheets for test conditions.

Monaural Cassette Player


TAPE
CASSETTE SYSTEM
LM1818
AUDIO AMPLIFIER
LM1895
LM386
LM389

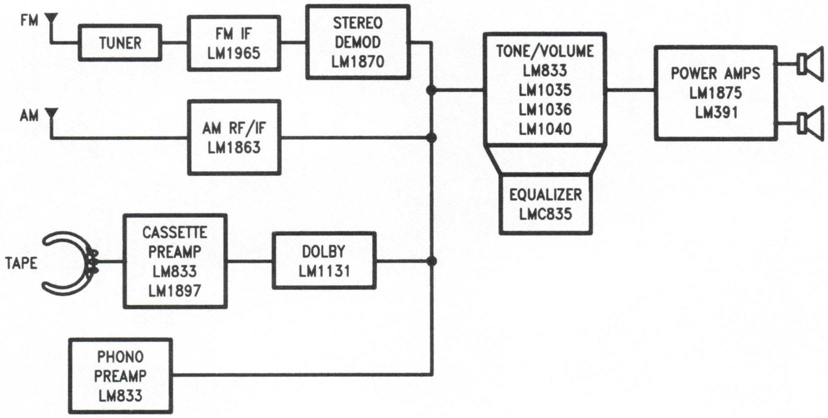
TL/XX/0013–1

Home Stereo System (Audio Power < 10W)


FM
TUNER
AM/FM IF
LM1866
FM
STEREO
DEMOD
LM1800
AM
AM
DNR
LM1894
TONE/VOLUME
LM1035
LM1036
LM1040
POWER AMP
LM2879
TAPE
TAPE
PREAMP
LM1897
DOLBY
LM1131
PHONO
PHONO
PREAMP
LM381
LM382
LM387

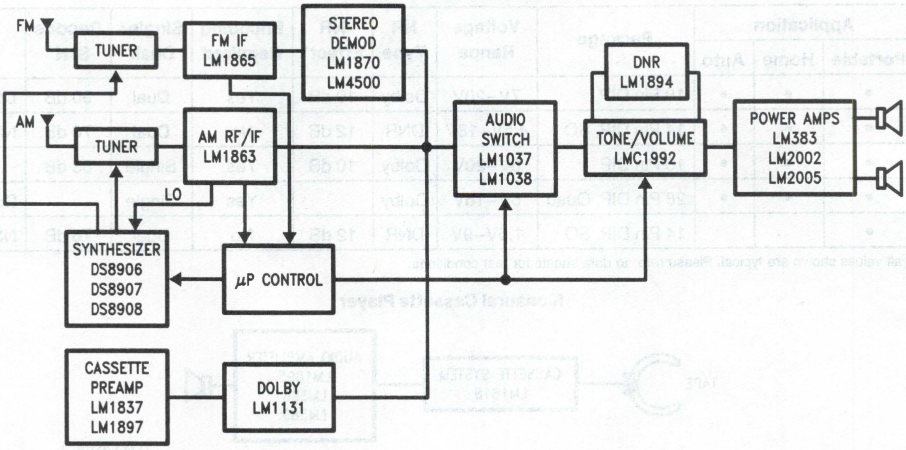
TL/XX/0013–2

Home Component Stereo (Audio Power > 10W)


FM
TUNER
FM IF
LM1965
STEREO
DEMOD
LM1870
AM
AM RF/IF
LM1863
TONE/VOLUME
LM833
LM1035
LM1036
LM1040
EQUALIZER
LMC835
POWER AMPS
LM1875
LM391
TAPE
CASSETTE
PREAMP
LM833
LM1897
DOLBY
LM1131
PHONO
PREAMP
LM833

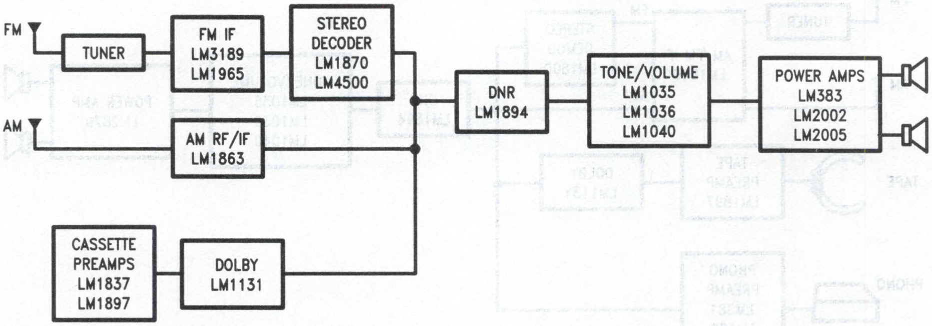
TL/XX/0013–3

Automotive Radio (Electronically Tuned)


FM
TUNER
FM IF
LM1865
STEREO
DEMOD
LM1870
LM4500
DNR
LM1894
AM
TUNER
AM RF/IF
LM1863
AUDIO
SWITCH
LM1037
LM1038
TONE/VOLUME
LMC1992
POWER AMPS
LM383
LM2002
LM2005
LO
SYNTHESIZER
DS8906
DS8907
DS8908
μP CONTROL
CASSETTE
PREAMP
LM1837
LM1897
DOLBY
LM1131

TL/XX/0013-4

Auto Radio (Manually Tuned)


FM
TUNER
FM IF
LM3189
LM1965
STEREO
DECODER
LM1870
LM4500
AM
AM RF/IF
LM1863
DNR
LM1894
TONE/VOLUME
LM1035
LM1036
LM1040
POWER AMPS
LM383
LM2002
LM2005
CASSETTE
PREAMPS
LM1837
LM1897
DOLBY
LM1131

TL/XX/0013-5

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Radio Circuits Definition of Terms

AGC dc Output Shift: The shift of the quiescent IC output voltage of the AGC section for a given change in AGC central voltage.

AGC Figure of Merit: The widest possible range of input signal level required to make the output signal drop by a specified amount from the specified maximum output level. Typical F.O.M. numbers are from 40 dB to 50 dB, for domestic radios and about 60 dB for automotive radios (for −10 dB output level change).

AGC Input Current: The current required to bias the central voltage input of the AGC section.

AM Rejection Ratio: The ratio of the recovered audio output produced by a desired FM signal of specified level and deviation to the recovered audio output produced by an unwanted AM signal of specified amplitude and modulating index.

Channel Separation: The level of output signal of an undriven amplifier with respect to the output level of an adjacent driven amplifier.

Detection Bandwidth: That frequency range about the free running frequency of the tone decoder/phase locked loop where a signal above a specified level will cause a detected signal condition at the output.

Detection Bandwidth Skew: The measure of how well the detection bandwidth is centered about the free running frequency. It is equal to the maximum detection bandwidth frequency plus the minimum detection bandwidth frequency minus twice the free running frequency.

Hold In Range: That range of frequencies about the free running frequency for which the phase locked loop will stay in lock if initially starting out in lock.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Sensitivity: The minimum level of input signal at a specified frequency required to produce a specified signal-to-noise ratio at the recovered audio output.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

−3 dB Limiting Sensitivity: In FM the input signal level which causes the recovered audio output level to drop 3 dB from the output level with a specified large signal input.

Lock In Range: That range of frequencies about the free running frequency for which the phase locked loop will come into lock if initially starting out of lock.

Maximum Sweep Rate: The maximum rate that the VCO may be made to vary its oscillating frequency over its Sweep Range.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Phase Detector Sensitivity: The change in the output voltage of the phase detector for a given change in phase between the two input signals to the phase detector.

Power Bandwidth: The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 6 dB below the rated output. For example, an amplifier rated a 60W with ≤0.25% THD, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Sweep Range: That ratio of maximum oscillating frequency to minimum operating frequency produced by varying the central voltage of the VCO from its maximum value to its minimum value with fixed values of timing resistance and capacitance.

VCO Sensitivity: The change in operating frequency for a given change in VCO central voltage.

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Radio Circuits Selection Guide

AM RF/IF Detector

	Portable	Home	Auto	Synthesized	Pin Count (Dip Package)	Supply Voltage	Supply Current	Input Sensitivity for 20 dB S/N Ratio	AM and FM IF	Audio Power Amplifier	Internal Detector	Meter Output
LM1863	•	•	•	•	20*	7-16	8.3 mA	30 µV			•	•
LM1866	•	•			20	3-15	15 mA	25 µV	•		•	•
LM1868	•	•			20	4.5-15	22 mA	12 µV	•	•	•	
LM3820	•	•	•		14	4.5-16	18 mA	35 µV				

*SO Surface Mount Package Only

Stereo Decoder

	Portable	Home	Auto	Pin Count Dip Package	Supply Voltage	Supply Current	THD	Separation	Blend	High Cut	Lamp Driver	Output Buffer	ARI Interference Rejection
LM1800		•		16	10-18	21 mA	0.4%	45 dB			•	•	
LM1870	•	•	•	20	7-15	26 mA	0.05%	45 dB	•	•	•	•	
LM1884*		•		16	8-16	35 mA	0.1%	—			•	•	
LM4500A	•	•	•	16	8-16	35 mA	0.1%	40 dB			•	•	•

*TV Stereo Decoder

Radio Remote Control

	Function	Pin Count (Dip Package)	Supply Voltage	Supply Current	Channels		Frequency Range
					Analog	Digital	
LM1871	Encoder/Transmitter	18	4.5-15V	14 mA	up to 6	2	up to 72 MHz
LM1872	Decoder/Receiver	18	2.5-7V	13 mA	2	2	up to 72 MHz

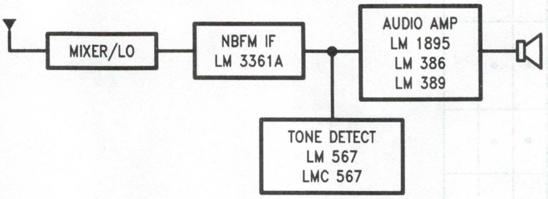
FM IF/Detector

	Portable	Home	Auto	Synthesized	Pin Count Dip	Pin Count S.O.	Supply Voltage	Supply Current	−3 dB Limiting Sensitivity	THD	Mute	AGC Outputs	AFC	Meter Output	AM/ FM IF
LM1865		●	●	●	20		7.3-16	43 mA	60 μV*	0.1%	●	Reverse	●	●	
LM1965		●	●		20		7.3-16	43 mA	60 μV*	0.1%	●	Reverse	●	●	
LM2065		●	●	●	20		7.3-16	43 mA	60 μV*	0.1%	●	Forward	●	●	
LM1866	●	●			20		3-15	17 mA	12 μV	0.5%	●	●	●	●	●
LM1868	●	●			20		4.5-15	19 mA	15 μV	1.1%					●
LM3089		●	●		16		8-16	23 mA	12 μV	0.5%	●	●	●	●	
LM3189		●	●		16		8-16	31 mA	12 μV	0.5%	●	●	●	●	
LM3361A†	●		●		16	16	2-9	2.8 mA	2 μV	-	●				

*Exclusive of 26 dB Buffer

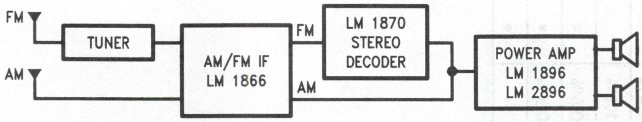
†Narrow-Band FM-IF

Cordless Telephone Receiver


MIXER/LO
NBFM IF
LM 3361A
AUDIO AMP
LM 1895
LM 386
LM 389
TONE DETECT
LM 567
LMC 567

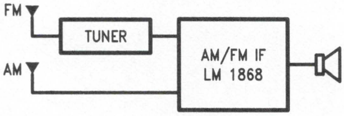
TL/XX/0011-1

Portable Radio (Stereo)


FM
AM
TUNER
AM/FM IF
LM 1866
FM
AM
LM 1870
STEREO
DECODER
POWER AMP
LM 1896
LM 2896

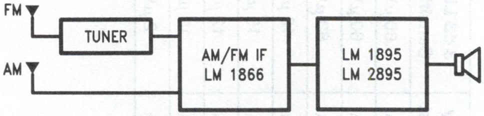
TL/XX/0011-2

Portable Radio (Monaural)


FM
AM
TUNER
AM/FM IF
LM 1868

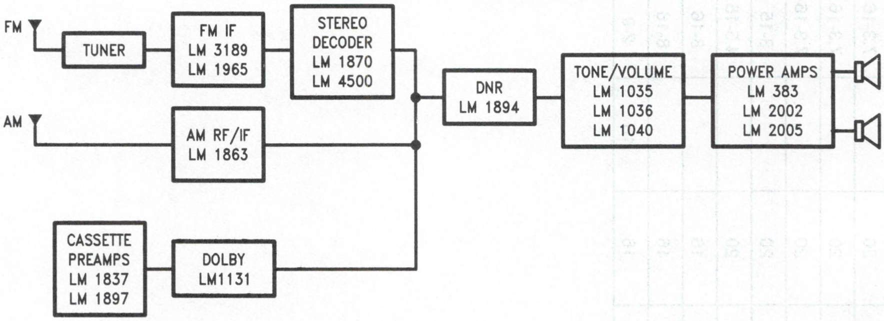
TL/XX/0011-3

Table/Clock Radio


FM
AM
TUNER
AM/FM IF
LM 1866
LM 1895
LM 2895

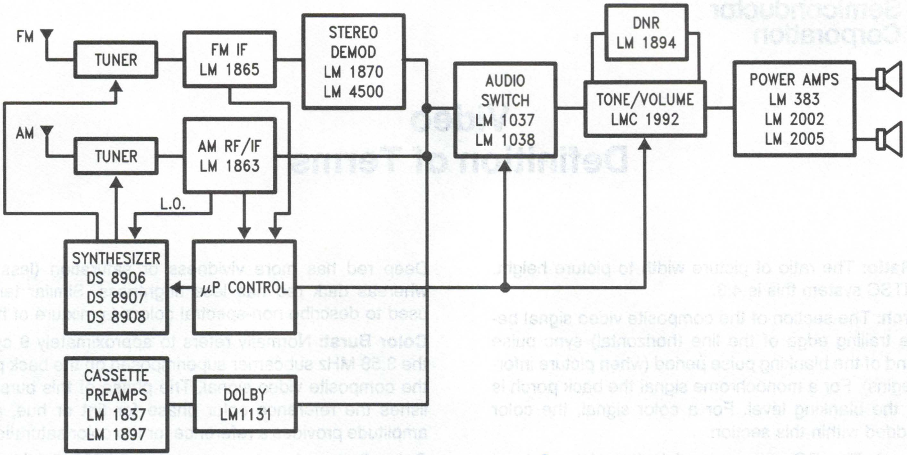
TL/XX/0011-4

Auto Radio (Manually Tuned)


FM
AM
TUNER
FM IF
LM 3189
LM 1965
STEREO
DECODER
LM 1870
LM 4500
AM RF/IF
LM 1863
CASSETTE
PREAMPS
LM 1837
LM 1897
DOLBY
LM1131
DNR
LM 1894
TONE/VOLUME
LM 1035
LM 1036
LM 1040
POWER AMPS
LM 383
LM 2002
LM 2005

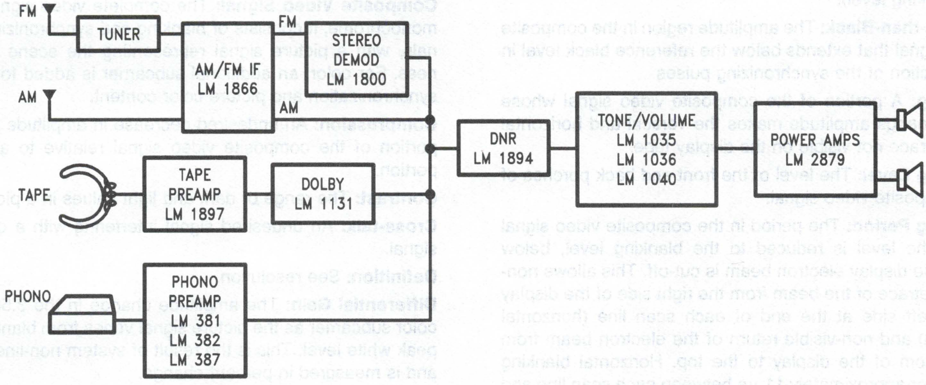
TL/XX/0011-5

Automotive Radio (Electronically Tuned)


FM
TUNER
FM IF LM 1865
STEREO DEMOD LM 1870 LM 4500
AUDIO SWITCH LM 1037 LM 1038
DNR LM 1894
TONE/VOLUME LMC 1992
POWER AMPS LM 383 LM 2002 LM 2005
AM
TUNER
AM RF/IF LM 1863
L.O.
SYNTHESIZER DS 8906 DS 8907 DS 8908
μP CONTROL
CASSETTE PREAMPS LM 1837 LM 1897
DOLBY LM1131

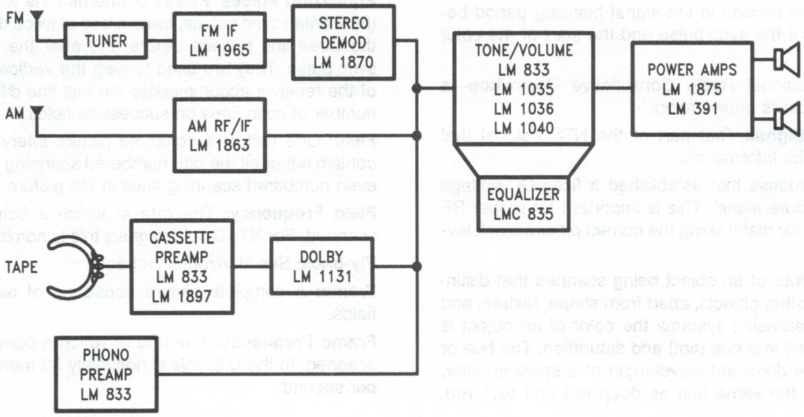
TL/XX/0011–6

Home Stereo System (Audio Power < 10W)


FM
TUNER
AM
AM/FM IF LM 1866
FM
STEREO DEMOD LM 1800
AM
DNR LM 1894
TONE/VOLUME LM 1035 LM 1036 LM 1040
POWER AMPS LM 2879
TAPE
TAPE PREAMP LM 1897
DOLBY LM 1131
PHONO
PHONO PREAMP LM 381 LM 382 LM 387

TL/XX/0011–7

Home Component Stereo (Audio Power > 10W)


FM
TUNER
FM IF LM 1965
STEREO DEMOD LM 1870
AM
AM RF/IF LM 1863
TONE/VOLUME LM 833 LM 1035 LM 1036 LM 1040
EQUALIZER LMC 835
POWER AMPS LM 1875 LM 391
TAPE
CASSETTE PREAMP LM 833 LM 1897
DOLBY LM 1131
PHONO PREAMP LM 833

TL/XX/0011–8

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Video
Definition of Terms

Aspect Ratio: The ratio of picture width to picture height. For the NTSC system this is 4:3.

Back Porch: The section of the composite video signal between the trailing edge of the line (horizontal) sync pulse and the end of the blanking pulse period (when picture information begins). For a monochrome signal the back porch is simply at the blanking level. For a color signal, the color burst is added within this section.

Black Level: The DC voltage level in the picture signal which corresponds to beam cut-off on the display tube. It can be at the blanking level (given by the back porch) or slightly higher (7.5% to 10% of the peak white signal above the blanking level).

Blacker-than-Black: The amplitude region in the composite video signal that extends below the reference black level in the direction of the synchronizing pulses.

Blanking: A portion of the composite video signal whose instantaneous amplitude makes the vertical and horizontal scan retrace not visible on the display tube.

Blanking Level: The level of the front and back porches of the composite video signal.

Blanking Period: The period in the composite video signal where the level is reduced to the blanking level, below which the display electron beam is cut-off. This allows non-visible retrace of the beam from the right side of the display to the left side at the end of each scan line (horizontal blanking) and non-visible return of the electron beam from the bottom of the display to the top. Horizontal blanking occurs for approximately 11 μs between each scan line and vertical blanking for 1.2 ms between each field.

Blooming: Defocussing of the picture in regions where the brightness is too high.

Breezeway: The section in the signal blanking period between the end of the sync pulse and the start of the color burst.

C.C.I.R.: International Radio Consultative Committee—a worldwide standards organization.

Chrominance Signal: That part of the NTSC signal that contains the color information.

Clamping: A process that established a fixed DC voltage level for the picture signal. This is important for proper RF modulation and for maintaining the correct picture black level.

Color: An attribute of an object being scanned that distinguishes it from other objects, apart from shape, texture, and brightness. In television systems the color of an object is further subdivided into hue (tint) and saturation. The hue or tint refers to the dominant wavelength of a spectral color, i.e., light red is the same hue as deep red and dark red. Deep red has more vividness or saturation (less white), whereas dark red has less brightness. Similar terms are used to describe non-spectral colors (a mixture of hues).

Color Burst: Normally refers to approximately 9 cycles of the 3.58 MHz subcarrier superimposed on the back porch of the composite video signal. The phase of this burst establishes the reference color phase for tint or hue, and the amplitude provides a reference for the color saturation level.

Color Subcarrier: A subcarrier at 3.579545 MHz (NTSC) whose modulation sidebands are added to a monochrome video signal to convey the color information. Similar subcarriers are used for SECAM and PAL.

Composite Video Signal: The complete video signal. For monochrome, it consists of blanking and synchronizing signals, with a picture signal representing the scene brightness. For color, an additional subcarrier is added for color synchronization and picture color content.

Compression: An undesired decrease in amplitude of one portion of the composite video signal relative to another portion.

Contrast: The range of dark and light values in a picture.

Cross-talk: An undesired signal interfering with a desired signal.

Definition: See resolution.

Differential Gain: The amplitude change in the 3.58 MHz color subcarrier as the picture signal varies from blanking to peak white level. This is the result of system non-linearities and is measured in percent change.

Differential Phase: The phase change, measured in degrees, of the 3.58 MHz color subcarrier as the picture signal varies from blanking to peak white level.

Equalizing Pulses: Pulses of one half the width of the line (horizontal) sync pulses, transmitted at twice the line rate for the three line periods before and after the field (vertical) sync pulse. They are used to help the vertical sync system of the receiver accommodate the half line difference in the number of scan lines on successive fields.

Field: One half of a complete picture interval. A field will contain either all the odd numbered scanning lines or all the even numbered scanning lines in the picture.

Field Frequency: The rate at which a complete field is scanned. For NTSC color signals this is nominally 59.94 Hz.

Fly-back: See Horizontal Retrace.

Frame: A complete picture consisting of two interlocking fields.

Frame Frequency: The rate at which a complete frame is scanned. In the U.S. this is nominally 30 frames or pictures per second.

Front Porch: The section of the composite video signal between the end of the picture information on a scan line (start of blanking) and the start of the line synchronization pulse.

Horizontal Blanking: The blanking signal at the end of each scan line that prevents the retrace of the display tube electron beam from being visible.

Horizontal Retrace: The rapid return of the scanning electron beam from the right side of the raster to the left side.

Horizontal Hum Bars: Relatively broad horizontal bars drifting slowly up the screen as a result of interference from the 60 Hz main frequency.

Hue (Tint): Describes the color that is being represented on the screen, i.e., red, blue, magenta, green, orange, etc.

Interlace: A scanning process in which each adjacent line belongs to the alternate field.

I.R.E.: Institute of Radio Engineers. Now combined with the AIEE to form the IEEE.

I.R.E. Scale: An oscilloscope scale calibrated for composite video and divided vertically into 140 units. The picture signal occupies the range from 0 to 100 with syncs in the range 0 to −40.

Luminance: The monochrome or brightness part of the color signal, composed of specific proportions of the three primary colors, red, blue, and green.

N.T.S.C.: National Television System Committee, used in reference to the system adopted for color television broadcasting in the U.S. at the end of 1953.

Noise: In a television picture, 'noise' refers to random interference producing a salt and pepper pattern over the picture. Heavy noise totally obscuring the picture is called "snow".

Overshoot: An (excessive) response to a unidirectional signal change. Overshoot is often used deliberately to enhance the luminance portion of a signal.

Pairing: A partial or complete failure of interlace in which scan lines of alternate fields fall in pairs, one on top of the other.

Pedestal Level: See Blanking Level.

Percentage Sync:

Video: The ratio in percent of the amplitude of the synchronizing pulse to the peak amplitude of the picture signal between blanking and reference white level. For a properly constituted composite video signal this is 40%.

RF: The ratio is a percent of the amplitude of the synchronizing pulse to the peak amplitude of the modulated RF signal. For correct modulation this is 25%.

P.A.L.: Phase Alternation Line. A variation of the NTSC system involving phase reversal of one of the color difference signals on a line by line basis, introduced into the U.K. and Germany in 1967.

Picture Signal: That portion of the composite video signal which is above the blanking level and contains the picture information.

Pre-emphasis: An increase in the level of a band of frequency components with respect to the remainder of the signal. For U.S. television, the audio signal is increased at a 6 db/octave rate above 2.1 kHz.

Raster: The area on the face of the display tube that is scanned by the electron beam. This is not always entirely visible since commercial receivers employ overscan so that the edges of the raster are hidden by the faceplate.

Reference Signals: See V.I.T.S. and V.I.R.S.

Resolution (Horizontal): The amount of resolvable detail in the horizontal direction of the picture. This depends on the high frequency and phase response of the transmission system and the receiver.

Resolution (Vertical): The amount of resolvable detail in the vertical direction of the picture. This depends primarily on the number of scan lines that are used and secondarily on the size (shape) of the electron scanning beam.

Saturation (Color): The amplitude of the chrominance signal. Increased saturation means increased chrominance signal level. Visibly, this refers to a color increasing from pale or pastel to deep.

S.E.C.A.M.: Sequential Couleur Avec Memoire. The color broadcasting system used predominantly in France which utilizes sequential transmission of the color difference signals, which are FM modulated on two separate subcarriers (1967).

Setup: The difference in level between the blanking level and the reference black level expressed as a percent of the reference white level.

Smear: Smear describes a picture condition where objects appear extended in the horizontal direction producing an ill-defined, blurry picture. This often occurs when the receiver is tuned slightly above the proper pix carrier frequency.

Sync: Abbreviation for synchronizing or synchronization.

Sync Level: The level of the synchronizing pulse tips.

Vertical Blanking: The blanking signal at the end of each field starting three lines before the vertical sync pulse.

Vertical Retrace: The return of the electron beam from the bottom of the display to the top after a complete field has been scanned.

V.I.R.S.: Vertical Interval Reference Signal. A quality control signal added to a horizontal scan line during the vertical blanking period. It is used to provide a chrominance, luminance and black level reference.

V.I.T.S.: Vertical Interval Test Signals. A series of test signals that are added to horizontal lines during the vertical blanking for in-service testing of the transmission equipment. They can be deleted or added at various points in the transmission link, unlike the VIRS, which is added at program origination and stays with the program material.

Vestigal Sideband Transmission: A broadcast transmission technique wherein only one side band of an amplitude modulated carrier is fully transmitted with the other sideband (usually lower) truncated.

Video: The visible portion of the transmitted signal representing the picture.

National Semiconductor Corporation

Video Selection Guide

VIDEO AMPLIFIERS

	Bandwidth	Gain	Package	Supply Voltage	Comments
LM592	120 MHz	100, 400	14 Pin DIP 14 PIN SO	±3V–±6V	Differential IN, Differential OUT
LM733	120 MHz	10, 100, 400	14 Pin DIP	±3V–±6V	Differential IN, Differential OUT
LM1201 (Advanced Information)	100 MHz	4–10	16 Pin DIP	+12V	Single Amplifier with Black Level and Contrast Control
LM1203	50 MHz	4–10	28 Pin DIP	+12V	Triple Amplifier System with Black Level and Contrast Control
LM359 (Note 1)	400 MHz GBW 30 MHz @ $A_V = 1$		14 Pin DIP	5V–22V	Dual Norton Amplifiers

VIDEO TIMING

	Function	Package	Supply Voltage	Comments
LM1391	PLL	8 Pin DIP	Internal Shunt Zener	—
LM1880	No-Holds Vert/Horiz	14 Pin DIP	Internal Shunt Zener	—
LM1881	Sync Separator	8 Pin DIP 8 Pin SO	5V–15V	Outputs Provided: Composite Sync Vertical Burst Gate Odd/Even Field

VIDEO MODULATORS/DEMODULATORS

	Function	Package	Comments
LM1496 (Note 2)	Balanced Modulator-Demodulator (Modulator—Suppressed Carrier, AM Demodulator—Synchronous, FM Phase Detection)	14 Pin DIP 10 Pin TO-5 14 Pin SO	Operating Frequency to 100 MHz Balanced Inputs and Outputs
LM1889	Modulates Color Difference, Luminance, Audio onto Low-VHF Channels	18 Pin DIP	DC Channel Switching Chroma Reference
LM2889	Modulates Composite Video, Audio onto Low-VHF Channels	14 Pin DIP	DC Channel Switching, Low Distortion FM Sound Modulator, Video Clamp

Note 1: Data sheet in Linear 1.

Note 2: Data sheet in Linear 3—Special Functions Chapter 5.

VIDEO IFs

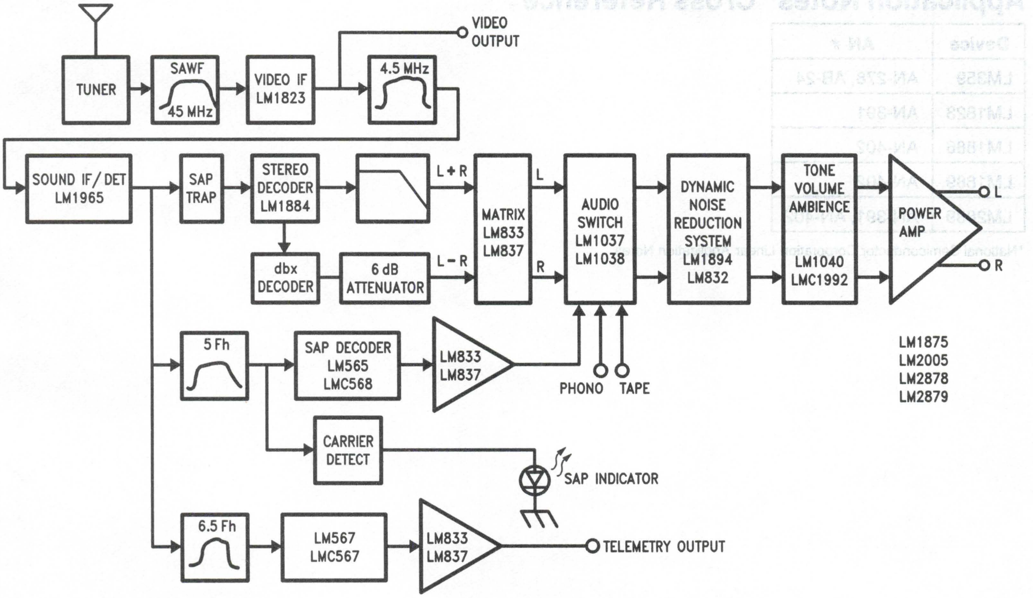
	Application	Package	Comments
LM1211 (Note 3)	Broadband Demodulator	20 Pin DIP	Operating Range 20 MHz–80 MHz Quasi-Synchronous Detector 25 MHz Output Amplifier
LM1823	Video IF	28 Pin DIP	Operating Range 20 MHz–70 MHz Synchronous Detector using PLL 9 MHz Output Amplifier

OTHER VIDEO PRODUCTS

	Function	Package	Supply Voltage	Comments
LM1044	Video Switch	24 Pin DIP	8V–16V	• DC Switch between 3 Composite Video Channels or 2 RGB Channels • 60 dB Channel Separation
LM1884 (Note 4)	TV Stereo Decoder	16 Pin DIP	9V–15V	Provides L − R, L + R Outputs from Composite Input
LM1886	TV Video Matrix D to A	20 Pin DIP	+5V, +12V	Encodes Luminance and Color Difference Signals from 3-Bit RGB Inputs

Note 3: Data Sheet in Linear 3.

Note 4: Data Sheet in Linear 3.


TUNER
SAWF
45 MHz
VIDEO IF
LM1823
VIDEO OUTPUT
4.5 MHz
SOUND IF/DET
LM1965
SAP TRAP
STEREO DECODER
LM1884
L + R
L − R
dbx DECODER
6 dB ATTENUATOR
MATRIX
LM833
LM837
L
R
AUDIO SWITCH
LM1037
LM1038
DYNAMIC NOISE REDUCTION SYSTEM
LM1894
LM832
TONE VOLUME AMBIENCE
LM1040
LMC1992
POWER AMP
L
R
LM1875
LM2005
LM2878
LM2879
PHONO
TAPE
5 Fh
SAP DECODER
LM565
LMC568
LM833
LM837
CARRIER DETECT
SAP INDICATOR
6.5 Fh
LM567
LMC567
LM833
LM837
TELEMETRY OUTPUT

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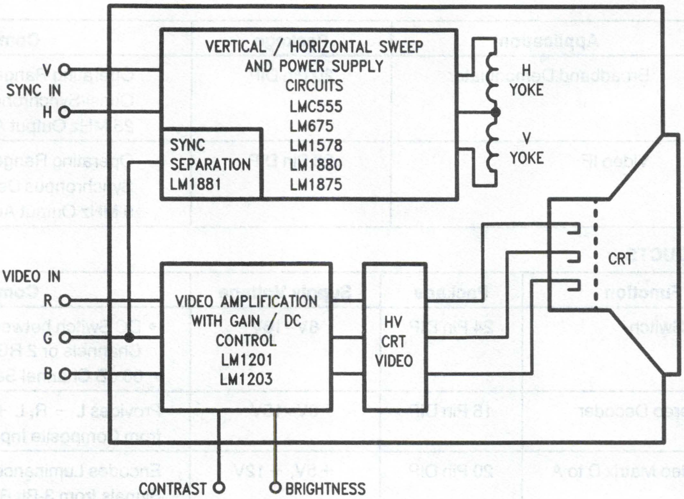
VERTICAL / HORIZONTAL SWEEP AND POWER SUPPLY CIRCUITS
LMC555
LM675
LM1578
LM1880
LM1875
SYNC SEPARATION LM1881
V
SYNC IN
H
H YOKE
V YOKE
VIDEO IN
R
G
B
VIDEO AMPLIFICATION WITH GAIN / DC CONTROL
LM1201
LM1203
HV CRT VIDEO
CRT
CONTRAST
BRIGHTNESS

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FIGURE 1. Typical RGB Color Monitor Block Diagram

Application Notes* Cross Reference

Device	AN #
LM359	AN-278, AB-24
LM1823	AN-391
LM1886	AN-402
LM1889	AN-402
LM2889	AN-391, AN-402

*National Semiconductor Corporation Linear Application Notes

National Semiconductor Corporation

Motion Control Selection Guide

Dedicated Motor Control Functions

Part Number	Function	Features
LM621	Brushless D.C. Motor	Deadband Timer for Direction Reversal 40V Max. Operation 35 mA Outputs for Direct Drive of Bipolar Power Transistors
LM628	High Performance Position Control for D.C. and Brushless D.C. Motors	On Board 32-Bit Incremental Shaft Encoder Interface 256 μs Loop Time Automatic Trajectory Generator Velocity Programmable "On-the-Fly" Internal Programmable PID Filter Convenient 8-Bit Host Interface 8-Bit or 12-Bit Port to DAC (LM628) 8-Bit PWM Output (LM629)
LM622	P.W.M. Controller for Brushless and Brush D.C. Motors	Flexible Output Structure Drives H-Switches or Commutators Precision On-Board Reference Flexible Error Amp/Feedback Structure

H-Switches

Output Current (Amps)		Device	Supply Voltage (Max)	Full Current Saturation Voltage		Operating Temp. Range	Package	Description
Peak (Typical)	Continuous (Max)			Source (Max)	Sink (Max)			
4	2	LM18298	50	2.8	2.6	−40°C to +150°C	15-Pin TO-220	Quad ½ H Switch
1.5	1	LM18293	36	1.8	1.8	−40°C to +125°C	16-Pin DIP	Dual Full H Switch

Power Op-Amps*

Output Current Amps		Device	Supply Voltage (Max)	Input Offset Voltage (Max)	Quiescent Current	Slew Rate (Typical)	Operating Temp. Range	Package	Features
Peak (Typical)	Continous (Max)								
3	1.5	LM675	60	10 mV	50 mA	8 V/μs	0°C to +70°C	5-Pin TO-220	Thermal Parole
15	10	LM12L	60	15 mV	80 mA	9 V/μs	−55°C to +125°C	4-Pin TO-3	Fully Protected
15	10	LM12CL	60	20 mV	120 mA	9 V/μs	0°C to +70°C	4-Pin TO-3	Fully Protected
15	10	LM12	80	15 mV	80 mA	9 V/μs	−55°C to +125°C	4-Pin TO-3	Fully Protected
15	10	LM12C	80	20 mV	120 mA	9 V/μs	0°C to +70°C	4-Pin TO-3	Fully Protected
1	0.5	LM18272	28	100 mV	15 mA (Typ)	0.5 V/μs	0°C to +85°C	8-Pin DIP	Dual (Bridge)

*For more information on Power Amps, see the Amplifier section of the Linear Databook. For more High Power Amplifiers, refer to the Audio Amplifier section.

National Semiconductor Corporation

Building Blocks

Communications-Related Building Blocks

Modulators & Demodulators Selection Guide

	LM1211	LM1496	LM1889	LM2889
Typical Application	Broadband Demodulator	Balanced Modulator-Demodulator	TV Video Modulator	TV Video Modulator
Key Features	• Configurable for AM or FM Based Signals • 0 MHz–70 MHz Operating Frequency Range • 25 MHz Detector Output Bandwidth • Linear Output Phase Response	• Wide Frequency Response to 100 MHz • Fully Balanced Inputs and Outputs • Adjustable Gain and Signal Handling	• Input Signals —Audio Modulation —Color Difference —Luminance • Channel 3 (61.25 MHz) or Channel 4 (67.25 MHz) Output • Companion Circuit to LM1886 TV Video Matrix D to A	• Input Signals —Audio —Composite Video • Channel 3 (61.25 MHz) or Channel 4 (67.25 MHz) Output • Video DC Restoration

PLL's AND TONE DECODERS

General purpose PLL's and tone decoders are available for applications that include FSK demodulation, tone decoding, SAP and SCA demodulation, and telemetry reception. Both bipolar and CMOS devices are offered. Special purpose PLL's for TV synchronization and FM stereo demodulation are also available for use in other low frequency signal processing applications.

PLL and Tone Decoder Selection Guide

	LM565	LM567	LMC567* (CMOS LM567)	LMC568	LM1391	LM1800, LM1870, LM4500A
Typical Application	PLL	Tone Decoder	Tone Decoder	PLL	TV—Horizontal PLL	FM Stereo Demodulator PLL
Center Frequency Range	15 Hz–500 kHz	0.01 Hz–500 kHz	0.01 Hz–500 kHz	0.01 Hz–500 kHz		
VCO Control Range	±30%	±7%	±7%	±30%	±300 Hz	
Supply Voltage	±5V to ±12V	4.75V–9V	2V–9V	2V–9V	8V–9.2V	Lowest: 7V Highest: 16V (See Datasheets)
Supply Current (Typ)	8 mA	12 mA	0.8 mA	1.2 mA	20 mA	Lowest: 21 mA Highest: 45 mA (See Datasheet)

*The CMOS LMC567 oscillator runs at twice the frequency of the bipolar LM567 oscillator. Refer to the datasheets for additional information.

POWER LINE CARRIER

The LM2893/LM1893 Carrier-Current Transceiver performs as a power line interface for half-duplex (bi-directional) communication of serial bit streams of virtually any coding. Applications include energy management systems, inter-office control, fire alarm systems, security systems, telemetry, and remote meter reading.

TIMERS

General purpose timers are available for generating accurate time delays or oscillation. Both bipolar and CMOS devices are offered.

Timer Selection Guide

	LM322	LM2905	LM555	LMC555* (CMOS LM555)	LM556 (Dual LM555)
Trigger Pulse Relative to Output Pulse	Can Be Longer	Can Be Longer	Must Be Shorter	Must Be Shorter	Must Be Shorter
Typical Application	Monostable	Monostable	Astable	Astable	Astable
Supply Voltage	4.5V–40V	4.5V–40V	4.5V–15V	1.2V–12V	4.5V–15V
Supply Current (Typical)	2.5 mA	2.5 mA	10 mA	0.15 mA	10 mA (Each Timer Section)

*The CMOS LMC555 can handle −10 mA to +50 mA of output current and the bipolar LM555 can handle up to ±200 mA of output current.

VCO AND FUNCTION GENERATOR

The LM566 is a general purpose voltage controlled oscillator which may be used to generate square and triangle waves. Typical applications include FM modulation, signal generation, function generation, frequency shift keying, and tone generation. The LM566 has very linear modulation characteristics.

Drive-Related Building Blocks

DISPLAY DRIVERS

LED flasher/oscillator and dot/bar display drivers are offered.

Display Driver Selection Guide

	LM3909	LM3914	LM3915	LM3916
Typical Application	Flasher/ Oscillator	Dot/Bar Display Driver	Dot/Bar Display Driver	Dot/Bar Display Driver
Display Scale	N/A	Linear	Log	VU Meter
Display Type	LED, Incandescent	LED, LCD, Vacuum Fluorescent	LED, LCD, Vacuum Fluorescent	LED, LCD, Vacuum Fluorescent

METER DRIVERS

The LM1819 Air-Core Meter Driver is a function generator/driver for air-core (moving-magnet) meter movements in tachometers and ruggedized instruments. Driver outputs are self-centering and better than 2% linearity is guaranteed over a full 305° deflection range. Signal conditioning circuitry is included on chip.

TEMPERATURE CONTROLLER

The LM3911 (Note 1) is a temperature controller containing a precision temperature sensor, op amp, and reference. It is designed for temperature sensing and closed loop temperature control applications over the −25°C to +85°C range.

Note 1: See Linear 2 for datasheet.

Precision-Related Building Blocks

CHOPPER BLOCK

The LMC669 Auto Zero Block (Note 1) is a universal commutating auto-zero block that can be used with any operational amplifier to correct offset voltage.

Note 1: See Linear 2 for datasheet.

TRANSISTOR ARRAYS

A variety of matched and power transistors are offered.

Transistor Array Selection Guide

	LM394	LM395	LM3046	LM3146
Description	NPN Transistor Pair	Power Transistor	5 NPN Transistors	5 NPN Transistors
Key Features	• Emitter-Base Voltage Matched to 50 μV • Current Gain Matched to 2%	• Collector Current: 1A • Quiescent Current: 10 mA • Switching Time: 2 μs • Current Limit • Thermal Limit • Safe Area Protection	• Emitter-Base Voltage Matched to ±5 mV • Breakdown Voltages —$V_{(BR)(CBO)}$: 20V —$V_{(BR)(CEO)}$: 15V —$V_{(BR)(CIO)}$: 20V —$V_{(BR)(EBO)}$: 5V • DC—120 MHz	• Emitter-Base Voltage Matched to ±5 mV • Breakdown Voltages —$V_{(BR)(CBO)}$: 40V —$V_{(BR)(CEO)}$: 30V —$V_{(BR)(CIO)}$: 40V —$V_{(BR)(EBO)}$: 5V • DC—120 MHz

Sensing-Related Building Blocks

LIQUID LEVEL SENSORS

A variety of liquid level sensing circuits are offered.

Liquid Level Sensor Selection Guide

	LM903	LM1042	LM1812	LM1830
Output Type	Digital HI/LO	Analog	Pulse-Echo Timing	Digital HI/LO
Operation Method	Thermoresistive Probe	Thermoresistive Probe	Acoustic Transducer	Conductive Liquid

SPECIAL AMPLIFIERS

A variety of special sensor amplifiers are offered.

Special Amplifiers Selection Guide

	LM1815	LM1964
Typical Application	Adaptive Sense Amplifier	Sensor Interface Amplifier
Sensor	Inductive Pickup	Lambda Sensor
Key Features	• Operates from 2.5V to 12V Supply • Adaptive Hysteresis • True Zero Crossing Timing Reference	• Normal Operation Guaranteed with Inputs up to 3V Below Ground on a Single Supply • Fully Protected Inputs • Input Open Circuit Detection

SPECIAL COMPARATOR

The LM1801 Battery Operated Power Comparator is an extremely low power comparator with a high current, open collector output stage. Typical applications include intrusion alarms, water leak detectors, gas leak detectors, overvoltage crowbars and battery operated monitors. The LM1801 is designed to operate in a standby mode for 1 year, powered by a 9V alkaline battery.

SPECIAL CONVERTERS

A variety of special converters for signal transformation applications are offered.

Special Converters Selection Guide

	LH0091 (Note 1)	LH0094 (Note 1)	LM331 (Note 1)	LM2907, LM2917
Converter Type	True RMS-to-DC	Multifunction	Voltage-to-Frequency	Frequency-to-Voltage
Key Features	• 0.1% Accuracy with External Trim • Uncommitted Amplifier for Filtering, Gain or High Crest Factor Configuration • True RMS Conversion	• $OUT = IN_Y \left(\frac{IN_Z}{IN_X} \right)^m$, $0.1 \leq m \leq 10$, m Continuously Adjustable • Applications —Precision Divider, Multiplier —Square Root —Square —Trigonometric Function Generator —Companding —Linearization —Control Systems —Log Amp	• 1 Hz to 100 kHz Frequency Range • Split or Single Supply Operation	• Operates Relay, Lamp or Other Load when Input Exceeds a Selected Rate • Ground Referenced Tachometer Fully Protected from Damage Due to Swings Above Supply or Below Ground

Note 1: See Linear 2 for datasheets.

ULTRASONIC TRANSCEIVER

The LM1812 Ultrasonic Transceiver is a general purpose ultrasonic transceiver designed for use in a variety of ranging, sensing, and communications applications. Typical uses include liquid level measurement, sonar, surface profiling, data links, hydro-acoustic communications, non-contact sensing and industrial process control. Depending on the acoustic transducer, typical performance capabilities include 5 feet to 100 feet in water and 4 inches to 35 feet in air.

Section 1
Active Filters

Section 1 Contents

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***Devices Not Covered In Last Publication**

Active Filters
Definition of Terms

f_{CLK}: the switched capacitor filter external clock frequency.

f_o: center of frequency of the second order function complex pole pair. f_o is measured at the bandpass output of each ½ MF10, and it is the frequency of the bandpass peak occurrence.

Q: quality factor of the 2nd order function complex pole pair. Q is also measured at the bandpass output of each ½ MF10 and it is the ratio of f_o over the −3 dB bandwidth of the 2nd order bandpass filter. The value of Q is not measured at the lowpass or highpass outputs of the filter, but its value relates to the possible amplitude peaking at the above outputs.

H_{OBP}: the gain in (V/V) of the bandpass output at $f = f_o$.

H_{OLP}: the gain in (V/V) of the lowpass output of each ½ MF10 at $f \rightarrow 0$ Hz.

H_{OHP}: the gain in (V/V) of the highpass output of each ½ MF10 as $f \rightarrow f_{CLK}/2$.

Q_Z: the quality factor of the 2nd order function complex zero pair, if any. (Q_Z is a parameter used when an allpass output is sought and unlike Q it cannot be directly measured).

f_Z: the center frequency of the 2nd order function complex zero pair, if any. If f_Z is different from f_o, and if the Q_Z is quite high it can be observed as a notch frequency at the allpass output.

f_{notch}: the notch frequency observed at the notch output(s) of the MF10.

H_{ON_1}: the notch output gain as $f \rightarrow 0$ Hz.

H_{ON_2}: the notch output gain as $f \rightarrow f_{CLK}/2$.

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Active Filter Selection Guide

Device #	Type	Function	Max Order	Max Freq Accuracy	Freq Range	Typ. Q Accuracy	Max F x Q
MF10 (S, T)	Universal	Universal	4th	±0.6%	0.1–30 kHz	±2%	200 kHz
MF8 (T)	Bandpass	Chebyshev Butterworth	4th	±1.0%	0.1–20 kHz	±2%	5 MHz
MF6 (S, T)	Lowpass	Butterworth	6th	±1.0	0.1–20 kHz	N/A	N/A
MF5 (S)	Universal	Universal	2nd	±1.0%	0.1–30 kHz	±6%	200 kHz
MF4 (S)	Lowpass	Butterworth	4th	±0.6%	0.1–20 kHz	N/A	N/A
*LMF100	Universal	Universal	4th	±0.6%	40 kHz	±2%	1.8 MHz
*LMF60	Lowpass	Butterworth	6th	±0.6%	40 kHz	N/A	N/A

S Surface Mount Available

T Extended Temperature Available

* Advance Information

National Semiconductor

AF100 Universal Active Filter

General Description

The AF100 state variable active filter is a general second order lumped RC network. Only four external resistors are required to program the AF100 for specific second order functions. Lowpass, highpass, and bandpass functions are available simultaneously at separate outputs. Notch and allpass functions are available by summing the outputs using the uncommitted output summing amplifier. Higher order systems are realized by cascading AF100 active filters.

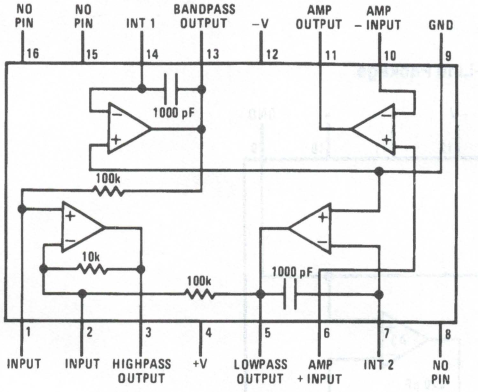
Any of the classical filter configurations, such as Butterworth, Bessel, Cauer, and Chebyshev can be implemented.

Features

- Military or commercial specifications
- Independent Q, cutoff frequency
- Low sensitivity to external component variation
- Separate lowpass, highpass, bandpass outputs
- Inputs may be differential, inverting, or non-inverting
- Allpass and notch outputs may be formed using the uncommitted amplifier
- Operates to 10 kHz
- Q range to 500
- Power supply range ±5V to ±18V
- Frequency accuracy ±1% unadjusted
- Q frequency product ≤ 50,000

Connection Diagrams

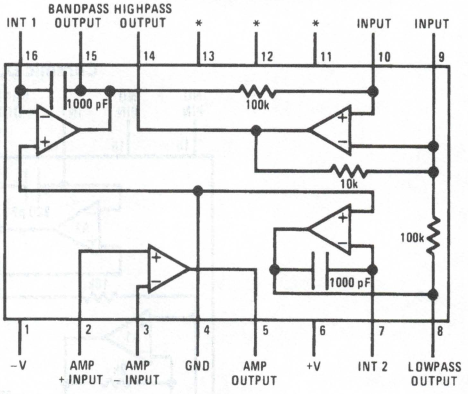
Ceramic Dual-In-Line Package


NO PIN
16
NO PIN
15
INT 1
14
BANDPASS OUTPUT
13
−V
12
AMP OUTPUT
11
AMP − INPUT
10
GND
9
1000 pF
100k
10k
100k
1000 pF
1
INPUT
2
INPUT
3
HIGHPASS OUTPUT
4
+V
5
LOWPASS OUTPUT
6
AMP + INPUT
7
INT 2
8
NO PIN
TOP VIEW

TL/H/5642-1

AF100-1CJ, AF100-2CJ
See NS Package Number HY13A

Plastic Dual-In-Line Package


INT 1
16
BANDPASS OUTPUT
15
HIGHPASS OUTPUT
14
*
13
*
12
*
11
INPUT
10
INPUT
9
1000 pF
100k
10k
100k
1000 pF
1
−V
2
AMP + INPUT
3
AMP − INPUT
4
GND
5
AMP OUTPUT
6
+V
7
INT 2
8
LOWPASS OUTPUT
TOP VIEW

*Note: Internally connected. Do not use. TL/H/5642-2

AF100-1CN, AF100-2CN
See NS Package Number N16A

National Semiconductor

AF150 Universal Wideband Active Filter

General Description

The AF150 wide band active filter is a general second order lumped RC network. Only four external resistors are required to program the AF150 for specific second order functions. Low pass, high pass and band pass functions are available simultaneously at separate outputs. Notch and all pass functions can be formed by summing the outputs using an external amplifier. Higher order filters are realized by cascading AF150 active filters.

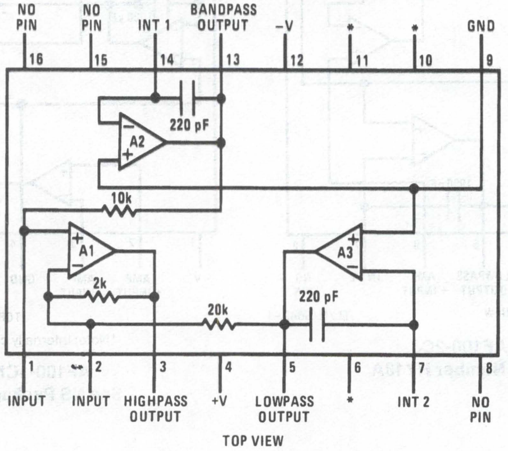
Any of the classical filter configurations, such as Butterworth, Bessel, Cauer and Chebyshev can be implemented.

Features

- Independent Q cutoff frequency
- Low sensitivity to external component variation
- Separate low pass, high pass, band pass outputs
- Inputs may be differential, inverting or non-inverting
- All pass and notch outputs may be formed
- Operates to 100 kHz
- Q range to 500
- Power supply range ±5V to ±18V
- High accuracy ±1% unadjusted
- Q frequency product 2×10^5

Connection Diagram

Ceramic Dual-In-Line Package


NO PIN
NO PIN
INT 1
BANDPASS OUTPUT
−V
*
*
GND
16
15
14
13
12
11
10
9
220 pF
A2
10k
A1
A3
2k
20k
220 pF
1
2
3
4
5
6
7
8
INPUT
INPUT
HIGHPASS OUTPUT
+V
LOWPASS OUTPUT
*
INT 2
NO PIN
TOP VIEW

TL/H/5643-1

Order Number AF150-1CJ or AF150-2CJ
See NS Package HY13A

***Note:** Internally connected. DO NOT USE.

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AF151 Dual Universal Active Filter

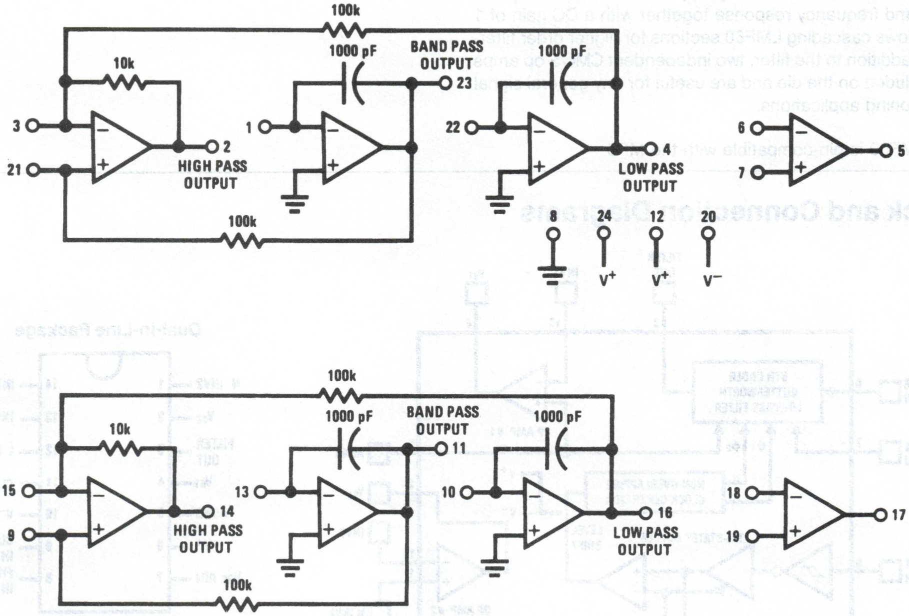
General Description

The AF151 consists of 2 general purpose state variable active filters in a single package. By using only 4 external resistors for each section, various second order functions may be formed. Low pass, high pass and band pass functions are available simultaneously at separate outputs. In addition, there are 2 uncommitted operational amplifiers which are available for buffering or for forming all pass and notch functions. Any of the classical filter configurations, such as Butterworth, Bessel, Cauer and Chebyshev can be easily formed.

Features

- Independent Q, frequency and gain adjustment
- Very low sensitivity to external component variation
- Separate low pass, high pass and band pass outputs
- Operation to 10 kHz
- Q range to 500
- Wide power supply range—±5V to ±18V
- Accuracy—±1%
- Fourth order function in one package

Circuit Diagrams (Unlisted pins are not connected.)


100k
10k
1000 pF
BAND PASS OUTPUT
23
1000 pF
3
21
2
HIGH PASS OUTPUT
1
22
4
LOW PASS OUTPUT
6
7
5
100k
8
24
12
20
V+
V+
V−
100k
10k
1000 pF
BAND PASS OUTPUT
11
1000 pF
15
9
14
HIGH PASS OUTPUT
13
10
16
LOW PASS OUTPUT
18
19
17
100k

TL/H/5644-1

Ceramic Dual-In-Line Package
Order Number AF151-1CJ or AF151-2CJ
See NS Package Number HY24A

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ADVANCED INFORMATION

LMF60 6th Order LMCMOS™ Switched Capacitor Butterworth Lowpass Filter

General Description

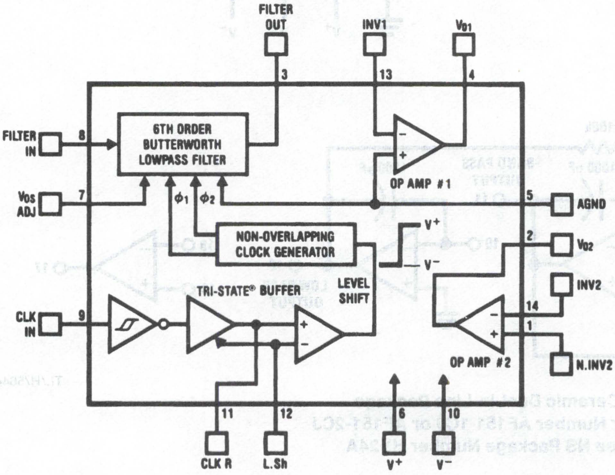
The LMF60 is a high-performance precision 6th Order Butterworth lowpass active filter. It is fabricated using National's LMCMOS process, which is an improved silicon-gate CMOS process specifically designed for analog products. Switched capacitor techniques eliminate external component requirements and allow a clock tunable cutoff frequency. The ratio of the clock frequency to the lowpass cutoff frequency is internally set to 50 to 1 (LMF60-50) or 100 to 1 (LMF60-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control, a TTL or CMOS logic compatible clock can be directly applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading LMF60 sections for higher order filtering. In addition to the filter, two independent CMOS op amps are included on the die and are useful for any general signal conditioning applications.

The LMF60 is pin-compatible with the MF6.

Features

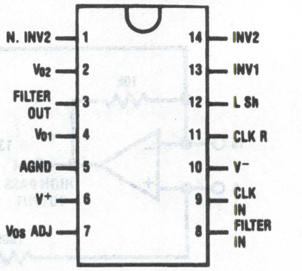
- Low DC offsets (less than 20 mV typical)
- Low clock feedthrough (5 mV typical)
- Cutoff frequency accuracy of ±0.3%
- Cutoff frequency range of 0.1 Hz to 25 kHz
- Two uncommitted op amps available
- 5V to 14V operation
- Cutoff frequency set by external or internal clock
- No external components

Block and Connection Diagrams


FILTER OUT
INV1
V01
3
13
4
6TH ORDER BUTTERWORTH LOWPASS FILTER
OP AMP #1
FILTER IN
8
VOS ADJ
7
φ1
φ2
NON-OVERLAPPING CLOCK GENERATOR
V+
V−
5
AGND
2
V02
INV2
14
1
N.INV2
OP AMP #2
CLK IN
9
TRI-STATE® BUFFER
LEVEL SHIFT
11
12
6
10
CLK R
L.Sh
V+
V−

TL/H/9294-1

Dual-In-Line Package


N. INV2
1
V02
2
FILTER OUT
3
V01
4
AGND
5
V+
6
VOS ADJ
7
FILTER IN
8
CLK IN
9
V−
10
CLK R
11
L Sh
12
INV1
13
INV2
14

TL/H/9294-2

Top View

National Semiconductor Corporation

ADVANCED INFORMATION

LMF90 4th-Order LMCMOS™ Programmable Elliptic Notch Filter

General Description

The LMF90 is a fourth-order elliptic notch (band-reject) filter based on switched-capacitor techniques. No external components are needed to define the response function. The depth and width of the notch are set using two separate three-level logic inputs. Three different notch depths and three different ratios of notch width to center frequency may be programmed by connecting these pins to V^+, ground, or V^-. Another three-level logic pin sets the ratio of clock frequency to notch frequency.

An internal crystal oscillator is provided. Used in conjunction with a low-cost color TV crystal and the internal logic divider, a notch filter can be built with center frequency at 50 Hz, 60 Hz, 100 Hz, 120 Hz, 150 Hz, or 180 Hz. Several LMF90s can be operated from a single crystal. An additional input is provided for an externally-generated clock signal.

Features

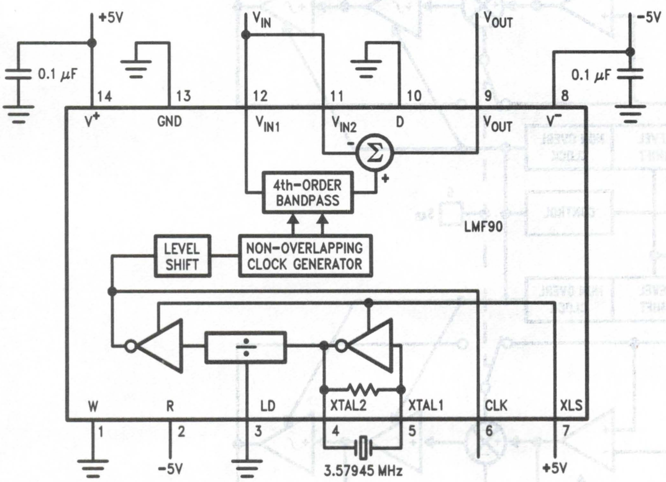
- Center frequency set by external clock or on-board oscillator
- No external components needed to set response characteristic
- Notch bandwidth, attenuation, and clock-to-center frequency ratio independently programmable
- Reduced aliasing compared to other switched-capacitor filter topologies

Key Specifications

■ f_0 range:	0.1 Hz to 30 kHz
■ Supply range:	4V to 14V
■ Passband ripple:	0.25 dB
■ Attenuation at f_0:	30 dB, 40 dB or 50 dB
■ f_{CLK}: f_0 ratio:	100:1, 50:1, or 33.33:1
■ Notch bandwidth:	0.1 f_0, 0.2 f_0, or 0.4 f_0
■ f_0 accuracy over full temperature range:	±1%

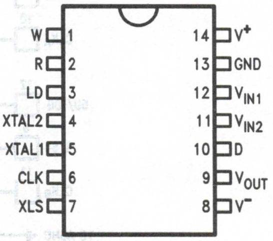
Typical Application and Connection Diagrams

60 Hz Notch Filter



+5V
V_IN
V_OUT
-5V
0.1 µF
0.1 µF
14
13
12
11
10
9
8
V+
GND
V_IN1
V_IN2
D
V_OUT
V-
Σ
+
4th-ORDER BANDPASS
LMF90
LEVEL SHIFT
NON-OVERLAPPING CLOCK GENERATOR
÷
W
R
LD
XTAL2
XTAL1
CLK
XLS
1
2
3
4
5
6
7
-5V
3.57945 MHz
+5V

TL/H/9268-1



W 1
R 2
LD 3
XTAL2 4
XTAL1 5
CLK 6
XLS 7
14 V+
13 GND
12 V_IN1
11 V_IN2
10 D
9 V_OUT
8 V-

TL/H/9268-14

National Semiconductor Corporation

ADVANCED INFORMATION

LMF100 Universal Monolithic Dual LMCMOS™ Switched Capacitor Filter

General Description

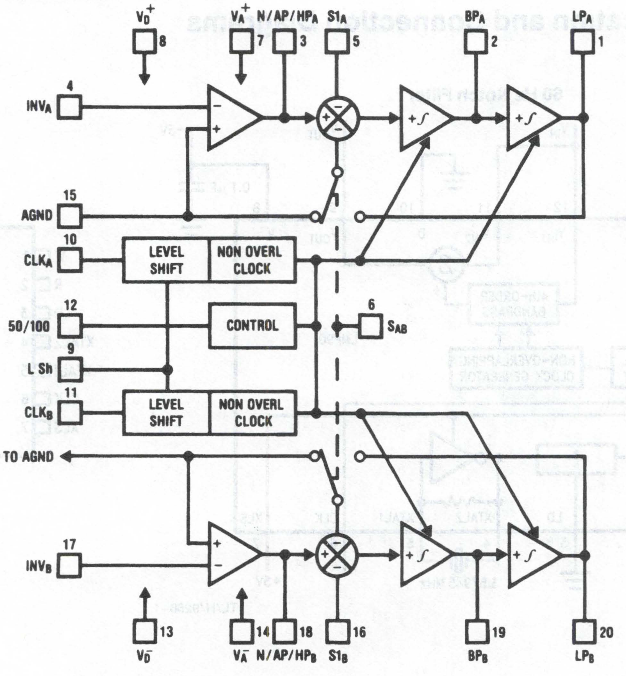
The LMF100 consists of two independent general purpose high performance switched capacitor filters. With an external clock and 2 to 4 resistors, various second order filtering functions can be realized by each filter block. Each block has three outputs. One output can be configured to perform either an allpass, highpass or a notch function. The other two outputs perform bandpass and lowpass functions. The center frequency of each filter can be tuned by an external clock or by both an external clock and an external resistor ratio. Up to a 4th order biquadratic function can be realized with a single LMF100. Higher order filters are implemented by simply cascading additional packages and all the classical filters (such as Butterworth, Bessel, Cauer and Chebyshev) can be realized.

The LMF100 is fabricated on National Semiconductor's high performance analog silicon gate CMOS process, LMCMOS. This allows for the production of a very low offset, high frequency filter building block.

Features

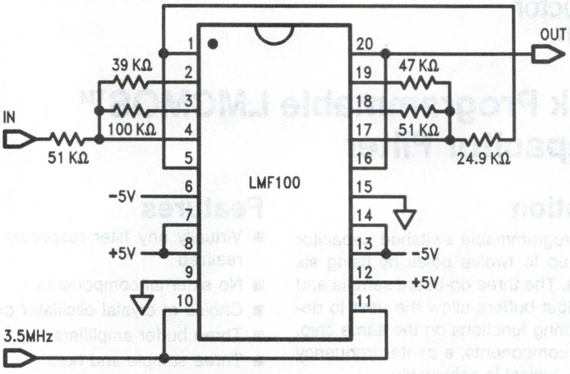
- Wider power supply range: 4V to 14V
- Operation up to 100 kHz
- Low offset voltages (50:1 or 100:1 mode)
  typically $V_{OS1} = \pm 5$ mV
  $V_{OS2} = \pm 10$ mV
  $V_{OS3} = \pm 15$ mV
- Low crosstalk
- Clock to center frequency ratio accuracy ±0.3%
- $f_o \times Q$ up to 1.8 MHz
- Pin-compatible with the MF10

System Block Diagram

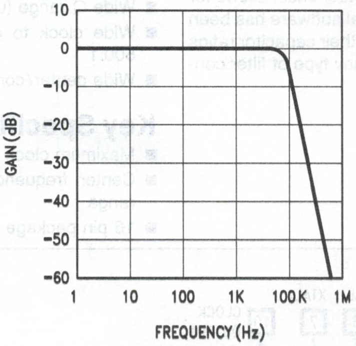

V_D^+ 8
V_A^+ 7
N/AP/HP$_A$ 3
S1$_A$ 5
BP$_A$ 2
LP$_A$ 1
INV$_A$ 4
AGND 15
CLK$_A$ 10
50/100 12
L Sh 9
CLK$_B$ 11
TO AGND
INV$_B$ 17
6 S$_{AB}$
LEVEL SHIFT
NON OVERL CLOCK
CONTROL
LEVEL SHIFT
NON OVERL CLOCK
13 V_D^-
14 V_A^-
18 N/AP/HP$_B$
16 S1$_B$
19 BP$_B$
20 LP$_B$

TL/H/9266–1

4th Order Butterworth Lowpass Filter


IN
51 KΩ
39 KΩ
100 KΩ
1
2
3
4
5
6
7
8
9
10
-5V
+5V
3.5MHz
LMF100
20
19
18
17
16
15
14
13
12
11
OUT
47 KΩ
51 KΩ
24.9 KΩ
-5V
+5V

TL/H/9266-2



TL/H/9266-3

National Semiconductor Corporation

ADVANCED INFORMATION

LMF120 Mask Programmable LMCMOS™ Switched Capacitor Filter

General Description

The LMF120 is a mask programmable switched capacitor filter capable of realizing up to twelve poles by using six independent biquad blocks. The three on-board sample and hold circuits and three output buffers allow the user to define three independent filtering functions on the same chip. Due to close matching of components, a center frequency tolerance as low as 0.25% typical is achievable.

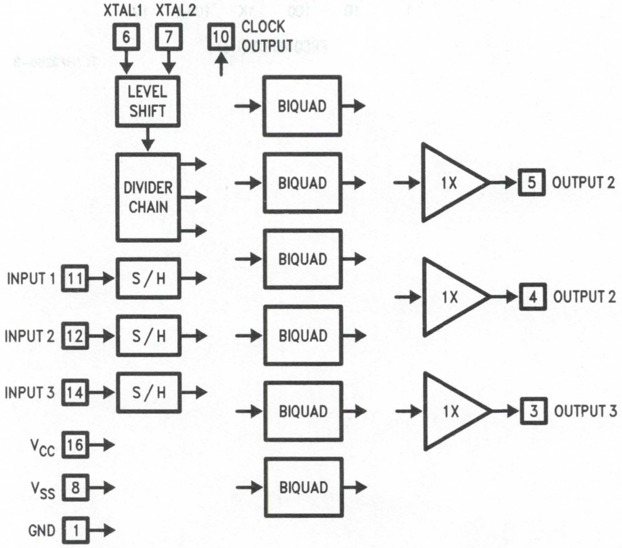
The clock can be supplied externally or by a simple internal crystal oscillator. The programmable divider chain allows for different input clock frequencies. Special software has been developed to aid designers in choosing their capacitor ratios and realization of metal mask. Almost any type of filter configuration can be formed.

Features

- Virtually any filter response (up to 12th order) can be realized
- No external components
- Choice of crystal oscillator or external clock
- Three buffer amplifiers
- Three sample and hold
- Programmable divider chain
- Wide range of supply voltage ±2V to ±7V
- Wide Q range (up to 100)
- Wide clock to center/corner frequency range 10:1 to 500:1
- Wide center/corner frequency range: 0.1 Hz to 100 kHz

Key Specifications

- Maximum clock frequency: 1.5 MHz
- Center frequency accuracy 1% over full temperature range
- 16 pin package


XTAL1
XTAL2
6
7
10
CLOCK OUTPUT
LEVEL SHIFT
DIVIDER CHAIN
BIQUAD
BIQUAD
BIQUAD
BIQUAD
BIQUAD
BIQUAD
1X
5
OUTPUT 2
1X
4
OUTPUT 2
1X
3
OUTPUT 3
INPUT 1
11
S/H
INPUT 2
12
S/H
INPUT 3
14
S/H
V_{CC}
16
V_{SS}
8
GND
1

TL/H/9267–1

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MF4 4th Order Switched Capacitor Butterworth Lowpass Filter

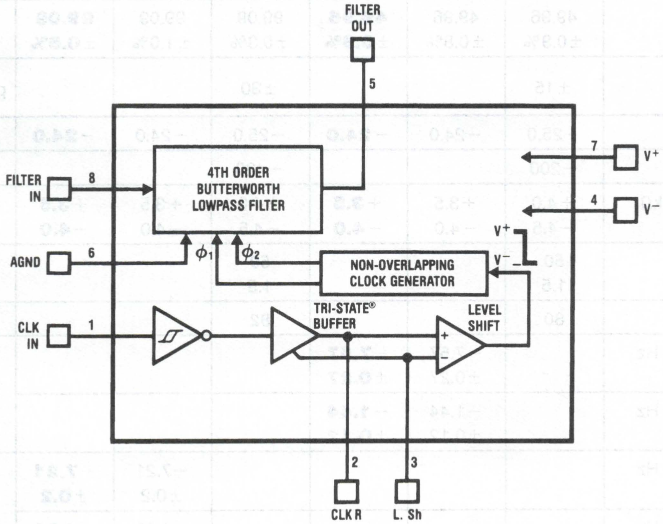
General Description

The MF4 is a versatile, easy to use, precision 4th order Butterworth low-pass filter. Switched-capacitor techniques eliminate external component requirements and allow a clock-tunable cutoff frequency. The ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50 to 1 (MF4-50) or 100 to 1 (MF4-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control an external TTL or CMOS logic compatible clock can be applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF4 sections together for higher order filtering.

Features

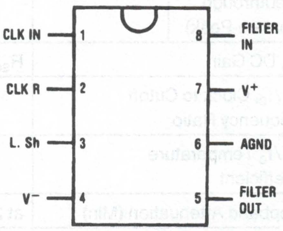
- Low Cost
- Easy to use
- 8-pin mini-DIP or 14-pin wide-body S.O.
- No external components
- 5V to 14V supply voltage
- Cutoff frequency range of 0.1 Hz to 20 kHz
- Cutoff frequency accuracy of ± 0.3% typical
- Cutoff frequency set by external clock
- Separate TTL and CMOS/Schmitt-trigger clock inputs

Block and Connection Diagrams


FILTER OUT
5
7
V+
4
V−
FILTER IN
8
4TH ORDER BUTTERWORTH LOWPASS FILTER
AGND
6
ϕ_1
ϕ_2
V+
V−
NON-OVERLAPPING CLOCK GENERATOR
CLK IN
1
TRI-STATE® BUFFER
LEVEL SHIFT
+
−
2
3
CLK R
L. Sh

TL/H/5064–1

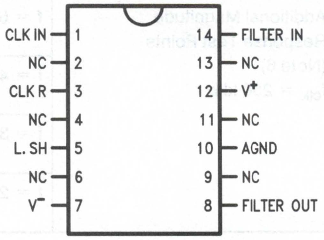
Dual-In-Line Package


CLK IN
1
CLK R
2
L. Sh
3
V−
4
FILTER IN
8
V+
7
AGND
6
FILTER OUT
5

TL/H/5064–2

Order Number MF4CN-50
or MF4CN-100
See NS Package Number N08E

Small-Outline
Wide-Body Package


CLK IN
1
NC
2
CLK R
3
NC
4
L. SH
5
NC
6
V−
7
FILTER IN
14
NC
13
V+
12
NC
11
AGND
10
NC
9
FILTER OUT
8

TL/H/5064–25

Top View
Order Number MF4CWM-50
or MF4CWM-100
See NS Package Number M14B

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	14V
Voltage At Any Pin	$V^+ + 0.2V$ $V^- - 0.2V$
Input Current at Any Pin (Note 14)	5 mA
Package Input Current (Note 14)	20 mA
Power Dissipation (Note 15)	500 mW
Storage Temperature	150°C
ESD Susceptibility (Note 13)	800 V

Soldering Information:

• N Package: 10 sec.		260°C
• SO Package:	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Note 2)

Temperature Range	$T_{min} \le T_A \le T_{max}$
MF4CN-50, MF4CN-100	$0°C \le T_A \le 70°C$
MF4CWM-50, MF4CWM-100	$0°C \le T_A \le 70°C$
Supply Voltage ($V^+ - V^-$)	5V to 14V

Filter Electrical Characteristics

The following specifications apply for $f_{CLK} \le 250$ kHz (see Note 5) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	MF4-50 Typical (Note 10)	MF4-50 Tested Limit (Note 11)	MF4-50 Design Limit (Note 12)	MF4-100 Typical (Note 10)	MF4-100 Tested Limit (Note 11)	MF4-100 Design Limit (Note 12)	Unit
$V^+ = +5V, V^- = -5V$								
f_c, Cutoff Frequency Range (Note 3) Min Max				0.1 20k			0.1 10k	Hz
Supply Current	$f_{clk} = 250$ kHz	2.5	3.5	**3.5**	2.5	3.5	**3.5**	mA
Maximum Clock Feedthrough (Peak-to-Peak) Filter Output	$V_{in} = 0V$	25			25			mV
H_o, DC Gain	$R_{source} \le 2\,k\Omega$	0.0	±0.15	**±0.15**	0.0	±0.15	**±0.15**	dB
f_{clk}/f_c, Clock to Cutoff Frequency Ratio		49.96 ±0.3%	49.96 ±0.8%	**49.96** **±0.6%**	99.09 ±0.3%	99.09 ±1.0%	**99.09** **±0.6%**	
f_{clk}/f_c Temperature Coefficient		±15			±30			ppm/°C
Stopband Attenuation (Min)	at $2\,f_c$	−25.0	−24.0	**−24.0**	−25.0	−24.0	**−24.0**	dB
DC Offset Voltage		−200			−400			mV
Minimum Output Swing	$R_L = 10\,k\Omega$	+4.0 −4.5	+3.5 −4.0	**+3.5** **−4.0**	+4.0 −4.5	+3.5 −4.0	**+3.5** **−4.0**	V V
Output Short Circuit Current (Note 8) Source Sink		50 1.5			50 1.5			mA mA
Dynamic Range (Note 4)		80			82			dB
Additional Magnitude Response Test Points (Note 6) $f_{clk} = 250$ kHz	f = 6000 Hz		−7.57 ±0.27	**−7.57** **±0.27**				dB
	f = 4500 Hz		−1.44 ±0.12	**−1.44** **±0.12**				
	f = 3000 Hz					−7.21 ±0.2	**−7.21** **±0.2**	dB
	f = 2250 Hz					−1.39 ±0.1	**−1.39** **±0.1**	

Filter Electrical Characteristics

The following specifications apply for $f_{CLK} \leq 250$ kHz (see Note 5) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Continued)

Parameter		Conditions	MF4-50 Typical (Note 10)	MF4-50 Tested Limit (Note 11)	MF4-50 Design Limit (Note 12)	MF4-100 Typical (Note 10)	MF4-100 Tested Limit (Note 11)	MF4-100 Design Limit (Note 12)	Unit
$V^+ = +2.5V$, $V^- = -2.5V$									
f_c Cutoff Frequency Range (Note 3)	min max				0.1 10k			0.1 5k	Hz
Supply Current		$f_{clk} = 250$ kHz	1.5	2.25	**2.25**	1.5	2.25	**2.25**	mA
Maximum Clock Feedthrough (Peak-to-Peak)	Filter Output	$V_{in} = 0V$	15			15			mV
H_o, DC Gain		$R_{source} \leq 2$ kΩ	0.0	±0.15	**±0.15**	0.0	±0.15	**±0.15**	dB
f_{clk}/f_c, Clock to Cutoff Frequency Ratio			50.07 ±0.3%	50.07 ±1.0%	**50.07** **±0.6%**	99.16 ±0.3%	99.16 ±1.0%	**99.16** **±0.6%**	
f_{CLK}/f_C Temperature Coefficient			±25			±60			ppm/°C
Stopband Attenuation (Min)		at 2 f_c	−25.0	−24.0	**−24.0**	−25.0	−24.0	**−24.0**	dB
DC Offset Voltage			−150			−300			mV
Minimum Output Swing		$R_L = 10$ kΩ	+1.5 −2.2	+1.0 −1.7	**+1.0** **−1.7**	+1.5 −2.2	+1.0 −1.7	**+1.0** **−1.7**	V V
Output Short Circuit Current (Note 8)	Source Sink		28 0.5			28 0.5			mA mA
Dynamic Range (Note 4)			78			78			dB
Additional Magnitude Response Test Points (Note 6) ($f_c = 5$ kHz) Magnitude at		$f_{clk} = 250$ kHz f = 6000 Hz		−7.57 ±0.27	**−7.57** **±0.27**				dB
		f = 4500 Hz		−1.46 ±0.12	**−1.46** **±0.12**				dB
($f_c = 2.5$ kHz) Magnitude		f = 3000 Hz					−7.21 ±0.2	**−7.21** **±0.2**	dB
		f = 2250 Hz					−1.39 ±0.1	**−1.39** **±0.1**	

Logic Input-Output Characteristics

The following specifications apply for $V^- = 0V$ (see Note 7) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter		Conditions	Typical (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Unit
SCHMITT TRIGGER						
V_{T+}, Positive Going Threshold Voltage	Min Max	$V^+ = 10V$	7.0	6.1	**6.1** **8.9**	V
	Min Max	$V^+ = 5V$	3.5	3.1 4.4	**3.1** **4.4**	V

Logic Input-Output Characteristics

The following specifications apply for $V^- = 0V$ (see Note 7) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = t_J = 25°C$. (Continued)

Parameter		Conditions		Typical (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Unit
SCHMITT TRIGGER (Continued)							
V_{T-}, Negative Going Threshold Voltage	Min	$V^+ = 10V$		3.0	1.3	**1.3**	V
	Max				3.8	**3.8**	
	Min	$V^+ = 5V$		1.5	0.6	**0.6**	V
	Max				1.9	**1.9**	
Hysteresis ($V_{T+} - V_{T-}$)	Min	$V^+ = 10V$		4.0	2.3	**2.3**	V
	Max				7.6	**7.6**	
	Min	$V^+ = 5V$		2.0	1.2	**1.2**	V
	Max				3.8	**3.8**	
Minimum Logical "1" Output Voltage (pin 2)		$I_0 = -10\ \mu A$	$V^+ = 10V$		9.0	**9.0**	V
			$V^+ = 5V$		4.5	**4.5**	V
Maximum Logical "0" Output Voltage (pin 2)		$I_0 = 10\ \mu A$	$V^+ = 10V$		1.0	**1.0**	V
			$V^+ = 5V$		0.5	**0.5**	V
Minimum Output Source Current (pin 2)		CLK R Shorted to Ground	$V^+ = 10V$	6.0	3.0	**3.0**	mA
			$V^+ = 5V$	1.5	0.75	**0.75**	mA
Maximum Output Sink Current (pin 2)		CLK R Shorted to V^+	$V^+ = 10V$	5.0	2.5	**2.5**	mA
			$V^+ = 5V$	1.3	0.65	**0.65**	mA
TTL CLOCK INPUT, CLK R PIN (Note 9)							
Maximum V_{IL}, Logical "0" Input Voltage				0.8			V
Minimum V_{IH}, Logical "1" Input Voltage				2.0			V
Maximum Leakage Current at CLK R Pin		L. Sh Pin at Mid-Supply		2.0			μA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. AC and DC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are with respect to GND.

Note 3: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 4: For ±5V supplies the dynamic range is referenced to 2.82 Vrms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 280 μVrms for the MF4-50 and 230 μVrms for the MF4-100. For ±2.5V supplies the dynamic range is referenced to 1.06 Vrms (1.5V peak) where the wideband noise over a 20 kHz bandwidth is typically 130 μVrms for both the MF4-50 and the MF4-100.

Note 5: The specifications for the MF4 have been given for a clock frequency (f_{CLK}) of 250 kHz or less. Above ths clock frequency the cutoff frequency begins to deviate from the specified error band of ±0.6% but the filter still maintains its magnitude characteristics. See Application Hints.

Note 6: Besides checking the cutoff frequency (f_c) and the stopband attenuation at 2 f_c, two additional frequencies are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB.

Note 7: For simplicity all the logic levels have been referenced to $V^- = 0V$ (except for the TTL input logic levels). The logic levels will scale accordingly for ±5V and ±2.5V supplies.

Note 8: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage and then shorting that output to the positive supply. These are worst case conditions.

Note 9: The MF4 is operating with symmetrical split supplies and L. Sh is tied to ground.

Note 10: Typicals are at 25°C and represent most likely parametric norm.

Note 11: Guaranteed to National's Average Outgoing Quality Level (AOQL).

Note 12: Guaranteed, but not 100% production tested. These limits are not used to determine outgoing quality levels.

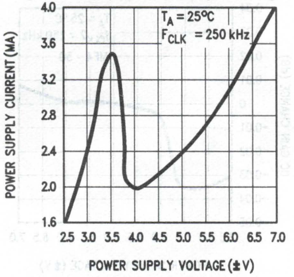
Note 13: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

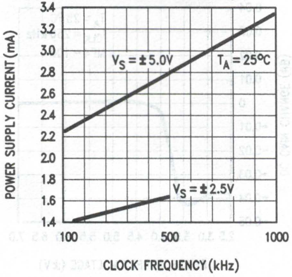
Note 14: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

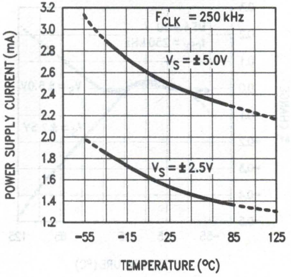
Note 15: Thermal Resistance

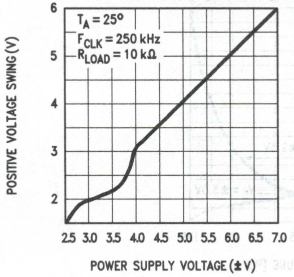
θ_{JA} (Junction to Ambient) N Package . . . . 105°C/W.
θ_{JA} M Package . . . . 95°C/W.

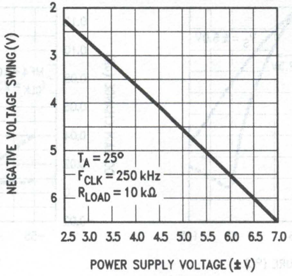
Typical Performance Characteristics

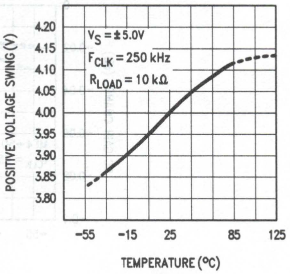

Power Supply Current vs Power Supply Voltage

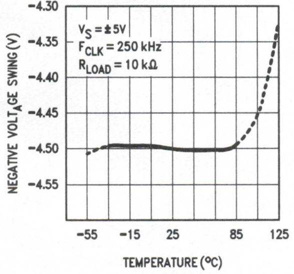

Power Supply Current vs Clock Frequency

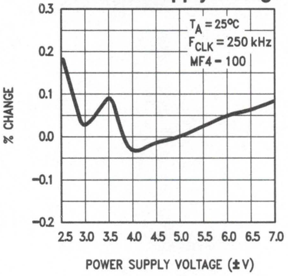

Power Supply Current vs Temperature

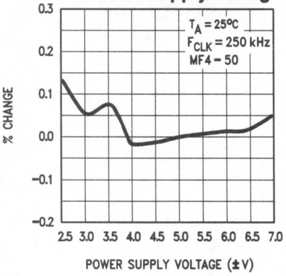

Positive Voltage Swing vs Power Supply Voltage

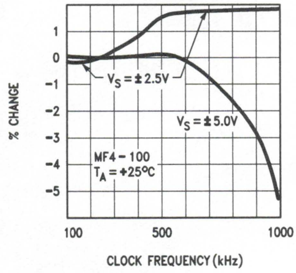

Negative Voltage Swing vs Power Supply Voltage

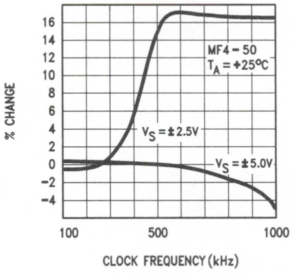

Positive Voltage Swing vs Temperature

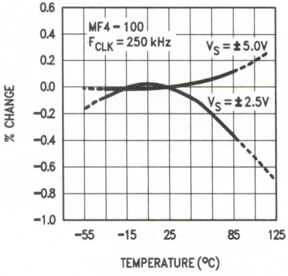

Negative Voltage Swing vs Temperature


f_{CLK}/f_c Deviation vs Power Supply Voltage


f_{CLK}/f_c Deviation vs Power Supply Voltage


f_{CLK}/f_c Deviation vs Clock Frequency

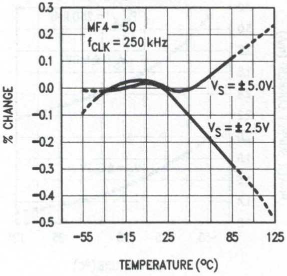

f_{CLK}/f_c Deviation vs Clock Frequency


f_{CLK}/f_c Deviation vs Temperature

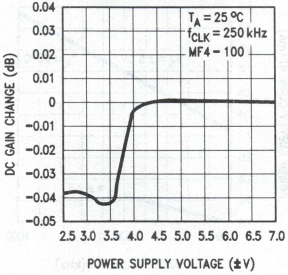
TL/H/5064–9

Typical Performance Characteristics (Continued)

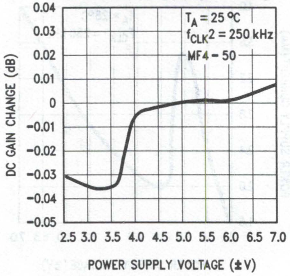
f_{CLK}/f_c Deviation vs Temperature



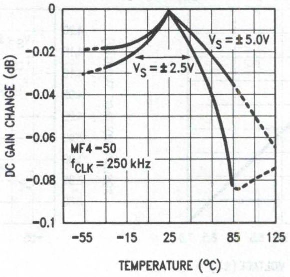
DC Gain Deviation vs Power Supply Voltage



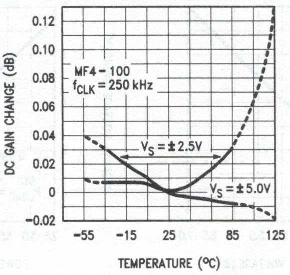
DC Gain Deviation vs Power Supply Voltage



DC Gain Deviation vs Temperature



DC Gain Deviation vs Temperature



TL/H/5064–10

Pin Descriptions

(Numbers in ( ) are for 14-pin package.)

Pin #	Pin Name	Function
1 (1)	CLK IN	A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self clocking Schmitt-trigger oscillator (see section 1.1).
2 (3)	CLK R	A TTL logic level clock input when in split supply operation (±2.5V to ±7V) with L. Sh tied to system ground. This pin becomes a low impedance output when L. Sh is tied to V^-. Also used in conjunction with the CLK IN pin for a self clocking Schmitt-trigger oscillator (see section 1.1). The TTL input signal must not exceed the supply voltages by more than 0.2V.
3 (5)	L. Sh	Level shift pin; selects the logic threshold levels for the clock. When tied to V^- it enables an internal tri-state buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output. When the voltage level at this input exceeds 25% $(V^+ - V^-) + V^-$ the internal tri-state buffer is disabled allowing the CLK R pin to become the clock input for the internal clock level-shift stage. The CLK R threshold level is now 2V above the voltage on the L. Sh pin. The CLK R pin will be compatible with TTL logic levels when the MF4 is operated on split supplies with the L. Sh pin connected to system ground.
5 (8)	FILTER OUT	The output of the low-pass filter. It will typically sink 0.9 mA and source 3 mA and swing to within 1V of each supply rail.
6 (10)	AGND	The analog ground pin. This pin sets the DC bias level for the filter section and must be tied to the system ground for split supply operation or to mid-supply for single supply operation (see section 1.2). When tied to mid-supply this pin should be well bypassed.
7, 4 (7, 12)	V^+, V^-	The positive and negative supply pins. The total power supply range is 5V to 14V. Decoupling these pins with 0.1 µF capacitors is highly recommended.
8 (14)	FILTER IN	The input to the low-pass filter. To minimize gain errors the source impedance that drives this input should be less than 2K (see section 3). For single supply operation the input signal must be biased to mid-supply or AC coupled through a capacitor.

1.0 MF4 Application Hints

The MF4 is a non-inverting unity gain low-pass fourth-order Butterworth switched-capacitor filter. The switched-capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio (100:1 or 50:1) of the clock frequency supplied to the filter. Internal integrator time constants set the filter's cutoff frequency. The resistive element of these integrators is actually a capacitor which is "switched" at the clock frequency (for a detailed discussion see Input Impedance Section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock-to-cutoff-frequency ratio ($f_{CLK}f_c$) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock-to-cutoff-frequency ratio the closer this approximation is to the theoretical Butterworth response. The MF4 is available in f_{CLK}/f_c ratios of 50:1 (MF4-50) or 100:1 (MF4-100).

1.1 CLOCK INPUTS

The MF4 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. Pin 3 is connected to V^- which makes Pin 2 a low impedance output. The oscillator's frequency is nominally

$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_{t-}}{V_{CC} - V_{t+}}\right)\left(\frac{V_{t+}}{V_{t-}}\right)\right]} \quad (1)$$

which, is typically

$$f_{CLK} \cong \frac{1}{1.69\ RC} \quad (1a)$$

for $V_{CC} = 10V$.

Note that f_{CLK} is dependent on the buffer's threshold levels as well as the resistor/capacitor tolerance (see *Figure 1*). Schmitt-trigger threshold voltage levels can change significantly causing the R/C oscillator's frequency to vary greatly from part to part.

Where accurate cutoff frequency is required, an external clock can be used to drive the CLK R input of the MF4. This input is TTL logic level compatible and also presents a very light load to the external clock source (~2 µA). With split supplies and the level shift (L. Sh) tied to system ground, the logic level is about 2V. (See the Pin Description for L. Sh).

1.2 POWER SUPPLY

The MF4 can be powered from a single supply or split supplies. The split supply mode shown in *Figure 2* is the most flexible and easiest to implement. Supply voltages of ±5V to ±7V enable the use of TTL or CMOS clock logic levels. *Figure 3* shows AGND resistor-biased to $V^+/2$ for single supply operation. In this mode only CMOS clock logic levels can be used, and input signals should be capacitor-coupled or biased near mid-supply.

1.3 INPUT IMPEDANCE

The MF4 low-pass filter input (FILTER IN) is not a high impedance buffer input. This input is a switched-capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the filter's input can be seen in *Figure 4*. The input capacitor charges to V_{in} during the first half of the clock period; during the second half the charge is transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore $Q = C_{in}V_{in}$, and since current is defined as the flow of charge per unit time, the average input current becomes

$$I_{in} = Q/T$$

1.0 MF4 Application Hints (Continued)

(where T equals one clock period) or

$$I_{in} = \frac{C_{in}V_{in}}{T} = C_{in}V_{in}f_{CLK}$$

The equivalent input resistor (R_{in}) then can be expressed as

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{C_{in}f_{CLK}}$$

The input capacitor is 2 pF for the MF4-50 and 1 pF for the MF4-100, so for the MF4-100

$$R_{in} = \frac{1 \times 10^{12}}{f_{CLK}} = \frac{1 \times 10^{12}}{f_c \times 100} = \frac{1 \times 10^{10}}{f_c}$$

and

$$R_{in} = \frac{5 \times 10^{11}}{f_{CLK}} = \frac{5 \times 10^{11}}{f_c \times 50} = \frac{1 \times 10^{10}}{f_c}$$

for the MF4-50. The above equation shows that for a given cutoff frequency (f_c), the input resistance of the MF4-50 is the same as that of the MF4-100. The higher the clock-to-cutoff-frequency ratio, the greater equivalent input resistance for a given clock frequency.

This input resistance will form a voltage divider with the source impedance (R_{source}). Since R_{in} is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to load the input signal which would appear as an overall decrease in gain to the output of the filter. Since the filter's ideal gain is unity, the overall gain is given by:

$$A_v = \frac{R_{in}}{R_{in} + R_{source}}$$

If the MF4-50 or the MF-100 were set up for a cutoff frequency of 10 kHz the input impedance would be:

$$R_{in} = \frac{1 \times 10^{10}}{10\ \text{kHz}} = 1\ \text{M}\Omega$$

In this example with a source impedance of 10K the overall gain, if the MF4 had an ideal gain of 1 or 0 dB, would be:

$$A_v = \frac{1\ \text{M}\Omega}{10\ \text{k}\Omega + 1\ \text{M}\Omega} = 0.99009 \text{ or } -0.086\ \text{dB}$$

Since the maximum overall gain error for the MF4 is ±0.15 dB with $R_s \leq 2\ \text{k}\Omega$ the actual gain error for this case would be +0.06 dB to −0.24 dB.

1.4 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency (f_c) has a lower limit due to leakage currents through the internal switches draining the charge stored on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error, for example:

$$f_{CLK} = 100\ \text{Hz},\ I_{leakage} = 1\ \text{pA},\ C = 1\ \text{pF}$$

$$V = \frac{1\ \text{pA}}{1\ \text{pF}\ (100\ \text{Hz})} = 10\ \text{mV}$$

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors limit the filter's accuracy at high clock frequencies. The amplitude characteristic on ±5V supplies will typically stay flat until f_{CLK} exceeds 750 kHz and then peak at about 0.5 dB at the corner frequency with a 1 MHz clock. As supply voltage drops to ± 2.5V, a shift in the f_{CLK}/f_c ratio occurs which will become noticeable when the clock frequency exceeds 250 kHz. The response of the MF4 is still a good approximation of the ideal Butterworth low-pass characteristic shown in *Figure 5*.

2.0 Designing With The MF4

Given any low-pass filter specification, two equations will come in handy in trying to determine whether the MF4 will do the job. The first equation determines the order of the low-pass filter required to meet a given response specification:

$$n = \frac{\log\left[(10^{0.1A_{min}} - 1)/(10^{0.1A_{max}} - 1)\right]}{2 \log (f_s/f_b)} \tag{2}$$

where n is the order of the filter, A_{min} is the minimum stopband attenuation (in dB) desired at frequency f_s, and A_{max} is the passband ripple or attenuation (in dB) at cutoff frequency f_b. If the result of this equation is greater than 4, more than a single MF4 is required.

The attenuation at any frequency can be found by the following equation:

$$\text{Attn}\ (f) = 10 \log \left[1 + (10^{0.1A_{max}} - 1)\ (f/f_b)^{2n}\right]\ \text{dB} \tag{3}$$

where n = 4 for the MF4.

2.1 A LOW-PASS DESIGN EXAMPLE

Suppose the amplitude response specification in *Figure 6* is given. Can the MF4 be used? The order of the Butterworth approximation will have to be determined using (1):

$$A_{min} = 18\ \text{dB},\ A_{max} = 1.0\ \text{dB},\ f_s = 2\ \text{kHz, and}\ f_b = 1\ \text{kHz}$$

$$n = \frac{\log\left[(10^{1.8} - 1)/(10^{0.1} - 1)\right]}{2\log(2)} = 3.95$$

Since n can only take on integer values, n = 4. Therefore the MF4 can be used. In general, if n is 4 or less a single MF4 stage can be utilized.

Likewise, the attenuation at f_s can be found using (3) with the above values and n = 4:

$$\text{Attn}\ (2\ \text{kHz}) = 10 \log \left[1 + 10^{0.1} - 1)\ (2\ \text{kHz}/1\ \text{kHz})^8\right] = 18.28\ \text{dB}$$

This result also meets the design specification given in *Figure 6* again verifying that a single MF4 section will be adequate.

Since the MF4's cutoff frequency (f_c), which corresponds to a gain attenuation of −3.01 dB, was not specified in this example, it needs to be calculated. Solving equation 3 where $f = f_c$ as follows:

$$\begin{aligned} f_c &= f_b \left[\frac{(10^{0.1(3.01\ \text{dB})} - 1}{(10^{0.1A_{max}} - 1)}\right]^{1/(2n)} \\ &= 1\ \text{kHz} \left[\frac{10^{0.301} - 1}{10^{0.1} - 1}\right]^{1/8} \\ &= 1.184\ \text{kHz} \end{aligned}$$

where $f_c = f_{CLK}/50$ or $f_{CLK}/100$. To implement this example for the MF4-50 the clock frequency will have to be set to $f_{CLK} = 50(1.184\ \text{kHz}) = 59.2\ \text{kHz}$, or for the MF4-100, $f_{CLK} = 100\ (1.184\ \text{kHz}) = 118.4\ \text{kHz}$.

2.2 CASCADING MF4s

When a steeper stopband attenuation rate is required, two MF4s can be cascaded (*Figure 7*) yielding an 8th order

2.0 Designing With The MF4 (Continued)

slope of 48 dB per octave. Because the MF4 is a Butterworth filter and therefore has no ripple in its passband when MF4s are cascaded, the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1V/V. The resulting response is shown in *Figure 9*.

In determining whether the cascaded MF4s will yield a filter that will meet a particular amplitude response specification, as above, equations 3 and 4 can be used, shown below.

$$n = \frac{\log[(10^{0.05A_{\text{min}}} - 1)/(10.^{0.05A_{\text{max}}} - 1)]}{2 \log (f_s/f_c)} \qquad (2)$$

$$\text{Attn}(f) = 10 \log [1 + (10^{0.05A_{\text{max}}} - 1)(f/f_c)^2] \text{ dB} \qquad (3)$$

where $n = 4$ (the order of each filter).

Equation 2 will determine whether the order of the filter is adequate ($n \leq 4$) while equation 3 can determine the actual stopband attenuation and cutoff frequency (f_c) necessary to obtain the desired frequency response. The design procedure would be identical to the one shown in section 2.0.

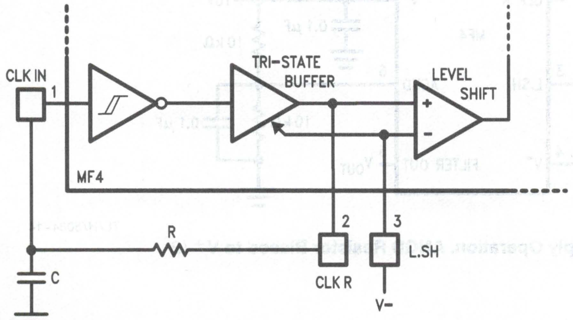
2.3 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The MF4 will respond favorably to an instantaneous change in clock frequency. If the control signal in *Figure 9* is low the MF4-50 has a 100 kHz clock making $f_c = 2$ kHz; when this signal goes high the clock frequency changes to 50 kHz yielding $f_c = 1$ kHz. As the Figure illustrates, the output signal changes quickly and smoothly in response to a sudden change in clock frequency.

The step response of the MF4 in *Figure 10* is dependent on f_c. The MF4 responds as a classical fourth-order Butterworth low-pass filter.

2.4 ALIASING CONSIDERATIONS

Aliasing effects have to be considered when input signal frequencies exceed half the sampling rate. For the MF4 this equals half the clock frequency (f_{CLK}). When the input signal contains a component at a frequency higher than half the clock frequency $f_{CLK}/2$, as in *Figure 11a*, that component will be "reflected" about $f_{CLK}/2$ into the frequency range below $f_{CLK}/2$, as in *Figure 11b.* If this component is within the passband of the filter and of large enough amplitude it can cause problems. Therefore, if frequency components in the input signal exceed $f_{CLK}2$ they must be attenuated before being applied to the MF4 input. The necessary amount of attenuation will vary depending on system requirements. In critical applications the signal components above $f_{CLK}/2$ will have to be attenuated at least to the filter's residual noise level.



$$f = \frac{1}{\mathrm{FC} \ln \left[\left(\frac{V_{CC} - V_{t-}}{V_{CC} - V_{t+}} \right) \left(\frac{V_{t+}}{V_{t-}} \right) \right]}$$

$$f \cong \frac{1}{1.69\ RC}$$

$$(V_{CC} = 10V)$$

TL/H/5064-11

FIGURE 1. Schmitt Trigger R/C Oscillator

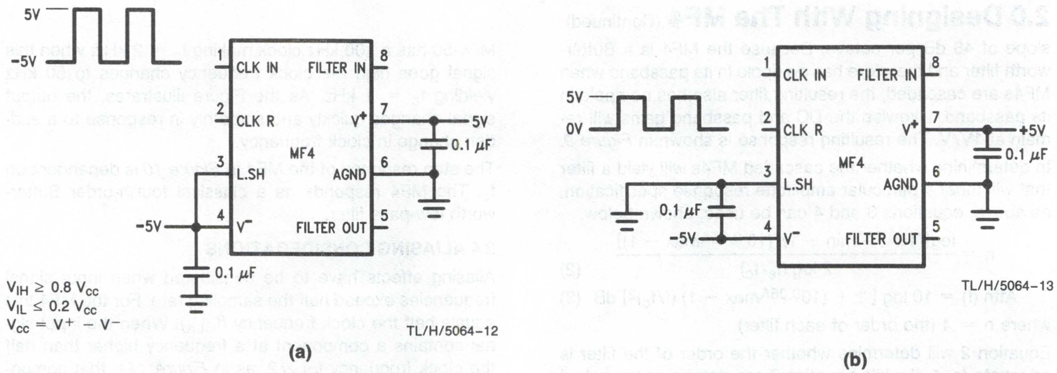

5V
-5V
1 CLK IN
FILTER IN 8
2 CLK R
V+ 7
5V
0.1 μF
MF4
3 L.SH
AGND 6
-5V
4 V−
FILTER OUT 5
0.1 μF
$V_{IH} \geq 0.8\ V_{cc}$
$V_{IL} \leq 0.2\ V_{cc}$
$V_{cc} = V^+ - V^-$
TL/H/5064–12
(a)
5V
0V
+5V
0.1 μF
-5V
TL/H/5064–13
(b)

FIGURE 2. Split Supply Operation with CMOS Level Clock (a) and TTL Level Clock (b)

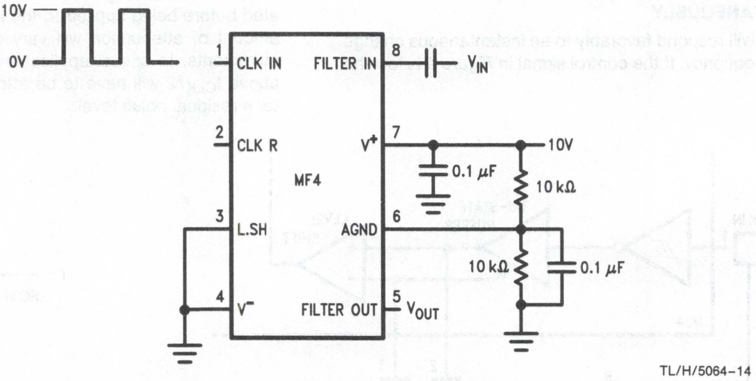
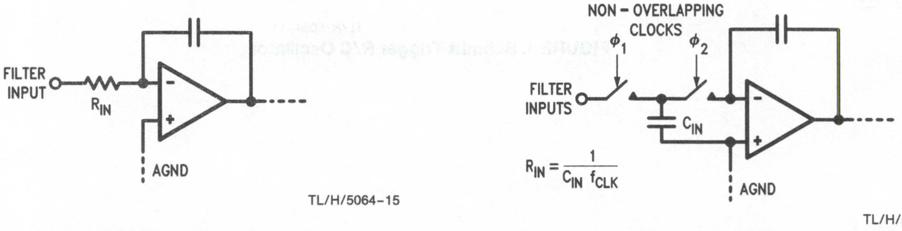

10V
0V
1 CLK IN
FILTER IN 8
V_{IN}
2 CLK R
V+ 7
10V
0.1 μF
10 kΩ
MF4
3 L.SH
AGND 6
10 kΩ
0.1 μF
4 V−
FILTER OUT 5
V_{OUT}
TL/H/5064–14

FIGURE 3. Single Supply Operation. ANGD Resistor Biased to V+/2


FILTER INPUT
R_{IN}
AGND
TL/H/5064–15
NON-OVERLAPPING CLOCKS
ϕ_1
ϕ_2
FILTER INPUTS
C_{IN}
$R_{IN} = \frac{1}{C_{IN}\ f_{CLK}}$
AGND
TL/H/5064–20

a) Equivalent Circuit for MF4 Filter Input

b) Actual Circuit for MF4 Filter Input

FIGURE 4. MF4 Filter Input

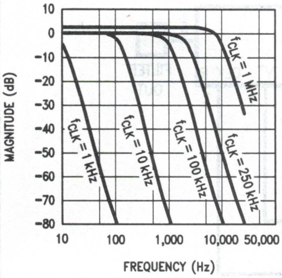


FIGURE 5a. MF4-100 Amplitude Response with ±5V Supplies

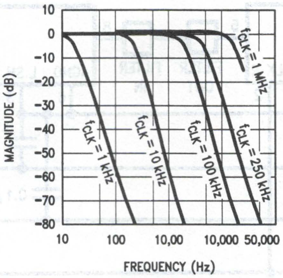


FIGURE 5b. MF4-50 Amplitude Response with ±5V Supplies

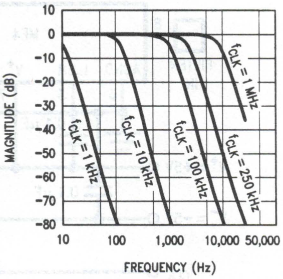
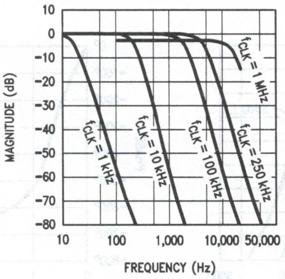
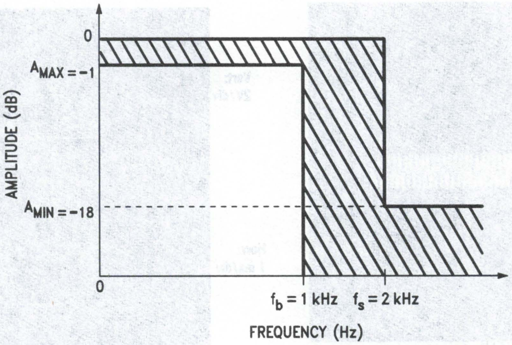


FIGURE 5c. MF4-100 Amplitude Response with ±2.5V Supplies



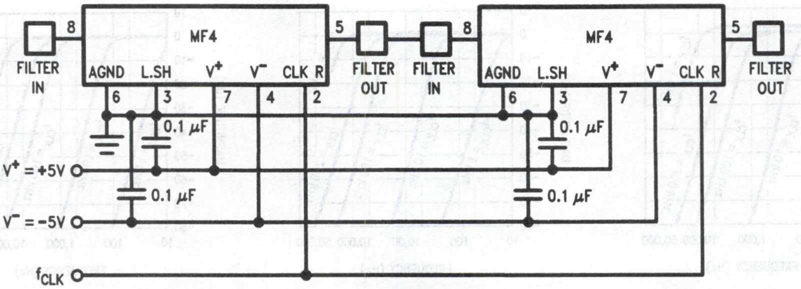
TL/H/5064–21

FIGURE 5d. MF4-50 Amplitude Response with ±2.5V Supplies


AMPLITUDE (dB)
0
AMAX = −1
AMIN = −18
0
fb = 1 kHz
fs = 2 kHz
FREQUENCY (Hz)

TL/H/5064–22

FIGURE 6. Design Example Magnitude Response Specification where the Response of the Filter Design must fall within the shaded area of the specification


FILTER IN
8
MF4
AGND
L.SH
V+
V−
CLK R
6
3
7
4
2
5
FILTER OUT
0.1 µF
0.1 µF
V+ = +5V
V− = −5V
fCLK

TL/H/5064-23

FIGURE 7. Cascading Two MF4s

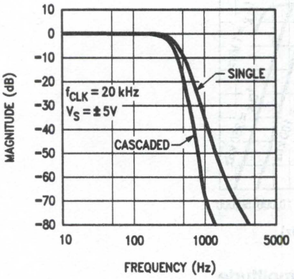
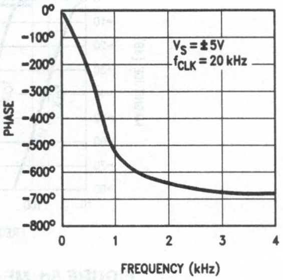
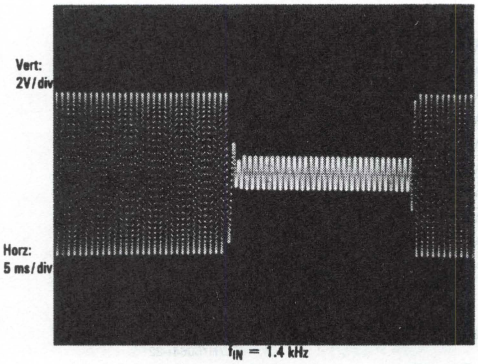


FIGURE 8a. One MF4-50 vs Two MF4-50s Cascaded



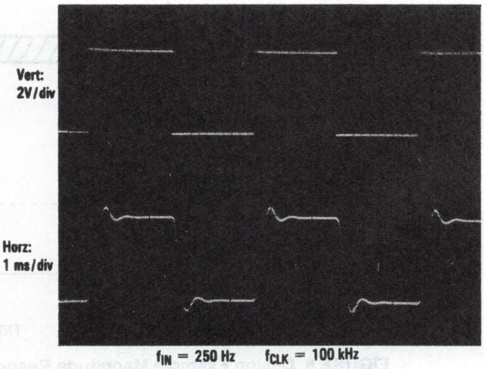
TL/H/5064-18

FIGURE 8b. Phase Response of Two Cascaded MF4-50s



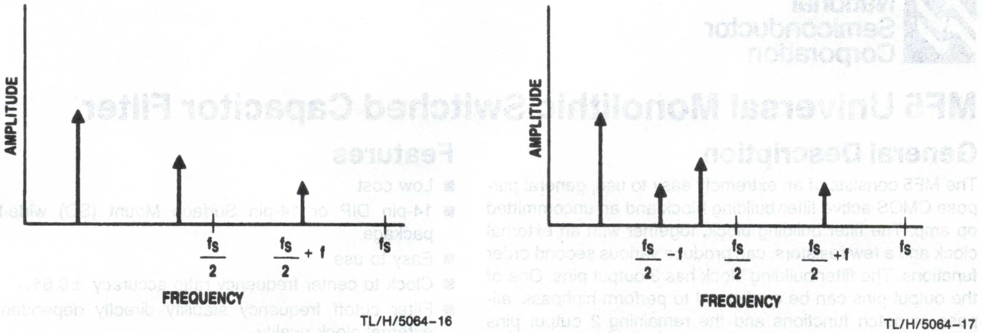
TL/H/5064-24

FIGURE 9. MF4-50 Abrupt Clock Frequency Change



TL/H/5064-19

FIGURE 10. MF4-50 Input Step Response



(a) Input signal spectrum

(b) Output signal spectrum. Note that the input signal at $f_c/2 + f$ causes an output signal to appear at $f_c/2 - f$.

FIGURE 11. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the MF4, $f_s = f_{CLK}$.

National Semiconductor Corporation

MF5 Universal Monolithic Switched Capacitor Filter

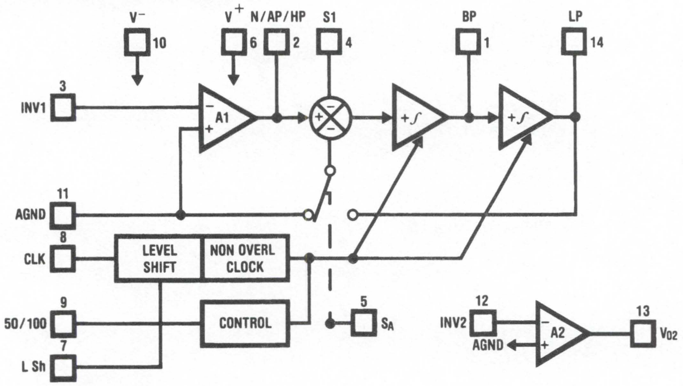
General Description

The MF5 consists of an extremely easy to use, general purpose CMOS active filter building block and an uncommitted op amp. The filter building block, together with an external clock and a few resistors, can produce various second order functions. The filter building block has 3 output pins. One of the output pins can be configured to perform highpass, allpass or notch functions and the remaining 2 output pins perform bandpass and lowpass functions. The center frequency of the filter can be directly dependent on the clock frequency or it can depend on both clock frequency and external resistor ratios. The uncommitted op amp can be used for cascading purposes, for obtaining additional allpass and notch functions, or for various other applications. Higher order filter functions can be obtained by cascading several MF5s or by using the MF5 in conjuction with the MF10 (dual switched capacitor filter building block). The MF5 is functionally compatible with the MF10. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

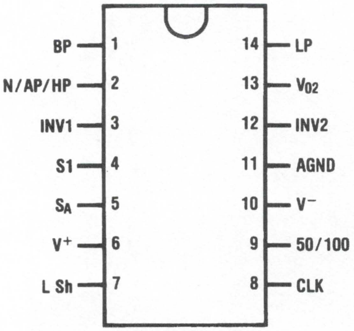
- Low cost
- 14-pin DIP or 14-pin Surface Mount (SO) wide-body package
- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variations
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_O \times Q$ range up to 200 kHz
- Operation up to 30 kHz (typical)
- Additional uncommitted op-amp

Block and Connection Diagrams



TL/H/5066-1

All Packages



Top View

Order Number MF5CN
See NS Package Number N14A

Order Number MF5CWM
See NS Package Number M14B

TL/H/5066-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)		14V
Power Dissipation $T_A = 25°C$ (note 1)		500 mW
Storage Temp.		150°C
Soldering Information:		
N Package:	10 sec.	260°C
SO Package:	Vapor phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Input Voltage (any pin)	$V^- \leq V_{in} \leq V^+$
Operating Temp. Range	$T_{MIN} \leq T_A \leq T_{MAX}$
MF5CN, MF5CWM	$0°C \leq T_A \leq 70°C$

Electrical Characteristics

$V^+ = 5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Supply Voltage ($V^+ - V^-$)	Min				**8**	V
	Max				**14**	V
Maximum Supply Current		Clock applied to Pin 8 No Input Signal	4.5	6.0		mA
Clock Feedthrough	Filter Output		10			mV
	Op-amp Output		10			mV

Filter Electrical Characteristics

$V^+ = 5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Center Frequency Range (f_o)	Max			30		**20**	kHz
	Min			0.1		**0.2**	Hz
Clock Frequency Range (f_{CLK})	Max			1.5		**1.0**	MHz
	Min			5.0		**10**	Hz
Clock to Center Frequency Ratio (f_{CLK}/f_o)		Ideal Q=10 Mode 1	$V_{pin9} = +5V$ $F_{CLK} = 250$ kHz	50.11 ± 0.2%	50.11 ± 1.5%		
			$V_{pin9} = -5V$ $F_{CLK} = 500$ kHz	100.04 ± 0.2%	100.04 ± 1.5%		
f_{CLK}/f_o Temp. Coefficient		$V_{pin9} = +5V$ (50:1 CLK ratio)		±10			ppm/°C
		$V_{pin9} = -5V$ (100:1 CLK ratio)		±20			ppm/°C
Q Accuracy (Max) (Note 2)		Ideal Q=10 Mode 1	$V_{pin9} = +5V$ $F_{CLK} = 250$ kHz		±6		%
			$V_{pin9} = -5V$ $F_{CLK} = 500$ kHz		±6		%
Q Temperature Coefficient		$V_{pin9} = +5V$ (50:1 CLK ratio)		−200			ppm/°C
		$V_{pin9} = -5V$ (100:1 CLK ratio)		−70			ppm/°C
DC Lowpass Gain Accuracy (Max)		Mode 1 R1 = R2 = 10 kΩ			±0.2		dB
DC Offset Voltage (Max)	V_{os1}			±5.0			mV
	V_{os2}	$V_{pin9} = +5V$ (50:1 CLK ratio)		−185			mV
	V_{os3}			+115			mV
(Note 3)	V_{os2}	$V_{pin9} = -5V$ (100:1 CLK ratio)		−310			mV
	V_{os3}			+240			mV

Filter Electrical Characteristics

$V^+ = 5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$. (Continued)

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Output Swing (Min)	BP, LP pins	RL = 5 kΩ	±4.0	±3.8		V
	N/AP/HP pin	RL = 3.5 kΩ	±4.2	±3.8		V
Dynamic Range (Note 4)		$V_{pin9} = +5V$ (50:1 CLK ratio)	83			dB
		$V_{pin9} = -5V$ (100:1 CLK ratio)	80			dB
Maximum Output Short Circuit Current (Note 5)	Source		20			mA
	Sink		3.0			mA

OP-AMP Electrical Characteristics

$V^+ = +5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless other noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Gain Bandwidth Product			2.5			MHz
Output Voltage Swing (Min)		RL = 3.5 kΩ	±4.2	±3.8		V
Slew Rate			7.0			V/µs
DC Open-Loop Gain			80			db
Input Offset Voltage (Max)			±5.0	±20		mV
Input Bias Current			10			pA
Maximum Output Short Circuit Current (Note 5)	Source		20			mA
	Sink		3.0			mA

Logic Input Characteristics

Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$. All other limits $T_A = 25°C$.

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CMOS Clock Input	Min Logical "1" Input Voltage	$V^+ = +5V$, $V^- = -5V$, $V_{L.Sh.} = 0V$		3.0		V
	Max Logical "0" Input Voltage			−3.0		V
	Min Logical "1" Input Voltage	$V^+ = +10V$, $V^- = 0V$, $V_{L.Sh.} = +5V$		8.0		V
	Max Logical "0" Input Voltage			2.0		V
TTL Clock Input	Min Logical "1" Input Voltage	$V^+ = +5V$, $V^- = -5V$, $V_{L.Sh.} = 0V$		2.0		V
	Max Logical "0" Input Voltage			0.8		V

Note 1: The typical junction-to-ambient thermal resistance (θ_{JA}) of the 14 pin N package is 160°C/W, and 82°C/W for the M package.

Note 2: The accuracy of the Q value is a function of the center frequency (f_o). This is illustrated in the curves under the heading "Typical Performance Characteristics".

Note 3: V_{os1}, V_{os2}, and V_{os3} refer to the internal offsets as discussed in the Application Information section 3.4.

Note 4: For ±5V supplies the dynamic range is referenced to 2.82V rms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 µV rms for the MF5 with a 50:1 CLK ratio and 280 µV rms for the MF5 with a 100:1 CLK ratio.

Note 5: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Guaranteed and 100% tested.

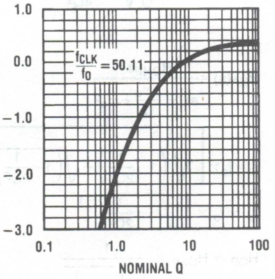
Note 8: Guaranteed, but not 100% tested. These limits are not used to calculate outgoing quality levels.

Pin Description

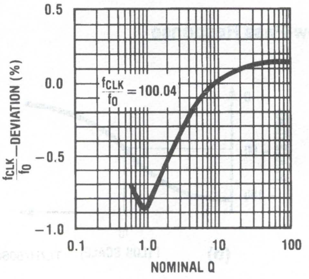
LP(14), BP(1), N/AP/HP(2):	The second order lowpass, bandpass, and notch/allpass/highpass outputs. The LP and BP outputs can typically sink 1 mA and source 3 mA. The N/AP/HP output can typically sink 1.5 mA and source 3 mA. Each output typically swings to within 1V of each supply.
INV1(3):	The inverting input of the summing op amp of the filter. This is a high impedance input, but the non-inverting input is internally tied to AGND, making INV1 behave like a summing junction (low impedance current input).
S1(4):	S1 is a signal input pin used in the allpass filter configurations (see modes 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).
SA(5):	This pin activates a switch that connects one of the inputs of the filter's second summer to either AGND (SA tied to V−) or to the lowpass (LP) output (SA tied to V+). This offers the flexibility needed for configuring the filter in its various modes of operation.
50/100(9):	This pin is used to set the internal clock to center frequency ratio (f_{CLK}/f_o) of the filter. By tying the pin to V+ an f_{CLK}/f_o ratio of about 50:1 (typically 50.11 ± 0.2%) is obtained. Tying the 50/100 pin to either AGND or V− will set the f_{CLK}/f_o ratio to about 100:1 (typically 100.04 ± 0.2%).
AGND(11):	This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.
V+(6), V−(10):	These are the positive and negative supply pins. The MF5 will operate over a total supply range of 8V to 14V. Decoupling the supply pins with 0.1 μF capacitors is highly recommended.
CLK(8):	This is the clock input for the filter. CMOS or TTL logic level clocks can be accomodated by setting the L. Sh pin to the levels described in the L. Sh pin description. For optimum filter performance a 50% duty cycle clock is recommended for clock frequencies greater than 200 kHz. This gives each op amp the maximum amount of time to settle to a new sampled input.
L. Sh(7):	This pin allows the MF5 to accommodate either CMOS or TTL logic level clocks. For dual supply operation (i.e., ±5V), a CMOS or TTL logic level clock can be accepted if the L. Sh pin is tied to mid-supply (AGND), which should be the system ground. For single supply operation the L. Sh pin should be tied to mid-supply (AGND) for a CMOS logic level clock. The mid-supply bias should be a very low impedance node. See Applications Information for biasing techniques. For a TTL logic level clock the L. Sh pin should be tied to V− which should be the system ground.
INV2(12):	This is the inverting input of the uncommitted op amp. This is a very high impedance input, but the non-inverting input is internally tied to AGND, making INV2 behave like a summing junction (low-impedance current input).
Vo2(13):	This is the output of the uncommitted op amp. It will typically sink 1.5 mA and source 3.0 mA. It will typically swing to within 1V of each supply.

Typical Performance Characteristics

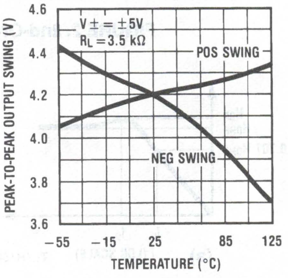
Deviation of $\frac{F_{CLK}}{F_o}$ vs Nominal Q



Deviation of $\frac{F_{CLK}}{F_o}$ vs Nominal Q

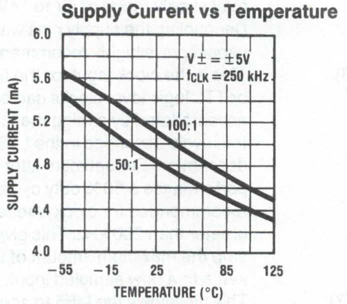


OPAMP Output Voltage Swing vs Temperature



TL/H/5066-3

Typical Performance Characteristics (Continued)



TL/H/5066-4

1.0 Definitions of Terms

f_{CLK}: the frequency of the external clock signal applied to pin 8.

f_o: center frequency of the second order function complex pole pair. f_o is measured at the bandpass output of the MF5, and is the frequency of maximum bandpass gain. (*Figure 1*).

f_{notch}: the frequency of minimum (ideally zero) gain at the notch output.

f_z: the center frequency of the second order complex zero pair, if any. If f_z is different from f_o and if Q_z is high, it can be observed as the frequency of a notch at the allpass output. (*Figure 10*).

Q: "quality factor" of the 2nd order filter. Q is measured at the bandpass output of the MF5 and is equal to f_o divided by the −3dB bandwidth of the 2nd order bandpass filter (*Figure 1*). The value of Q determines the shape of the 2nd order filter responses as shown in *Figure 6*.

Q_z: the quality factor of the second order complex zero pair, if any. Q_z is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \dfrac{s\omega_o}{Q_z} + \omega_o{}^2\right)}{s^2 + \dfrac{s\omega_o}{Q} + \omega_o{}^2}$$

where $Q_z = Q$ for an all-pass response.

H_{OBP}: the gain (in V/V) of the bandpass output at $f = f_o$.

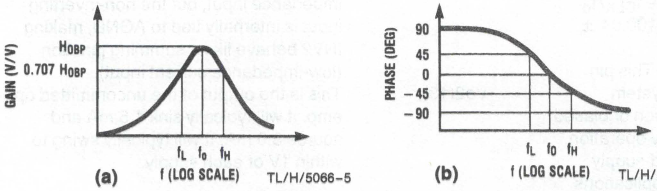
H_{OLP}: the gain (in V/V) of the lowpass output as f → 0 Hz (*Figure 2*).

H_{OHP}: the gain (in V/V) of the highpass output as $f \rightarrow f_{clk}/2$ (*Figure 3*).

H_{ON}: the gain (in V/V) of the notch output as f → 0 Hz and as $f \rightarrow f_{clk}/2$, when the notch filter has equal gain above and below the center frequency (*Figure 4*). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (*Figures 11 and 8*), the two quantities below are used in place of H_{ON}.

H_{ON1}: the gain (in V/V) of the notch output as f → 0 Hz.

H_{ON2}: the gain (in V/V) of the notch output as $f \rightarrow f_{clk}/2$.



TL/H/5066-5 TL/H/5066-6

FIGURE 1. 2nd-Order Bandpass Response

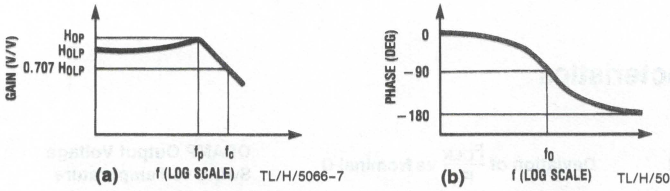
$$H_{BP}(s) = \frac{H_{OBP}s}{s^2 + \dfrac{s\omega_o}{Q} + \omega_o{}^2}$$

$$Q = \frac{f_o}{f_H - f_L};\quad f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$\omega_o = 2\pi f_o$$



TL/H/5066-7 TL/H/5066-8

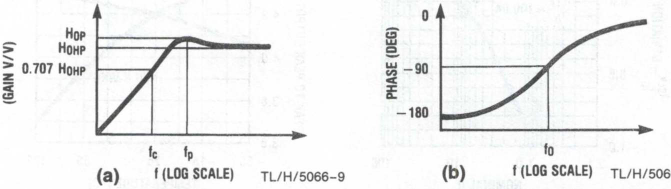
FIGURE 2. 2nd-Order Low-Pass Response

$$H_{LP}(s) = \frac{H_{OLP}\omega_o{}^2}{s^2 + \dfrac{s\omega_o}{Q} + \omega_o{}^2}$$

$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_o\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\dfrac{1}{Q}\sqrt{1 - \dfrac{1}{4Q^2}}}$$



TL/H/5066-9 TL/H/5066-10

FIGURE 3. 2nd-Order High-Pass Response

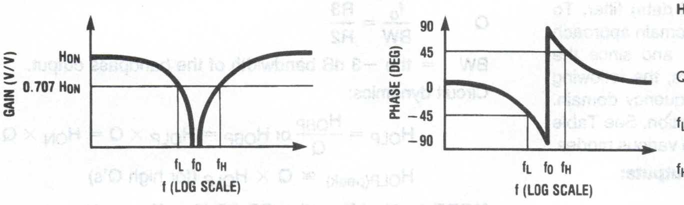
$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \dfrac{s\omega_o}{Q} + \omega_o{}^2}$$

$$f_c = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_p = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\dfrac{1}{Q}\sqrt{1 - \dfrac{1}{4Q^2}}}$$

1.0 Definition of Terms (Continued)



TL/H/5066–11

(a)

TL/H/5066–12

(b)

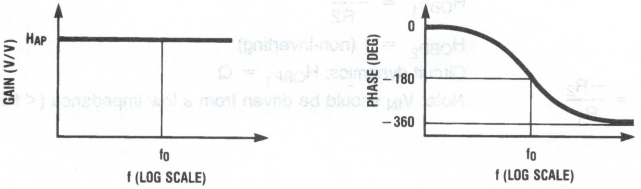
$$H_N(s) = \frac{H_{ON}(s^2 + \omega_o^2)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$Q = \frac{f_o}{f_H - f_L};\ f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

FIGURE 4. 2nd-Order Notch Response



$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q} + \omega_o^2\right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

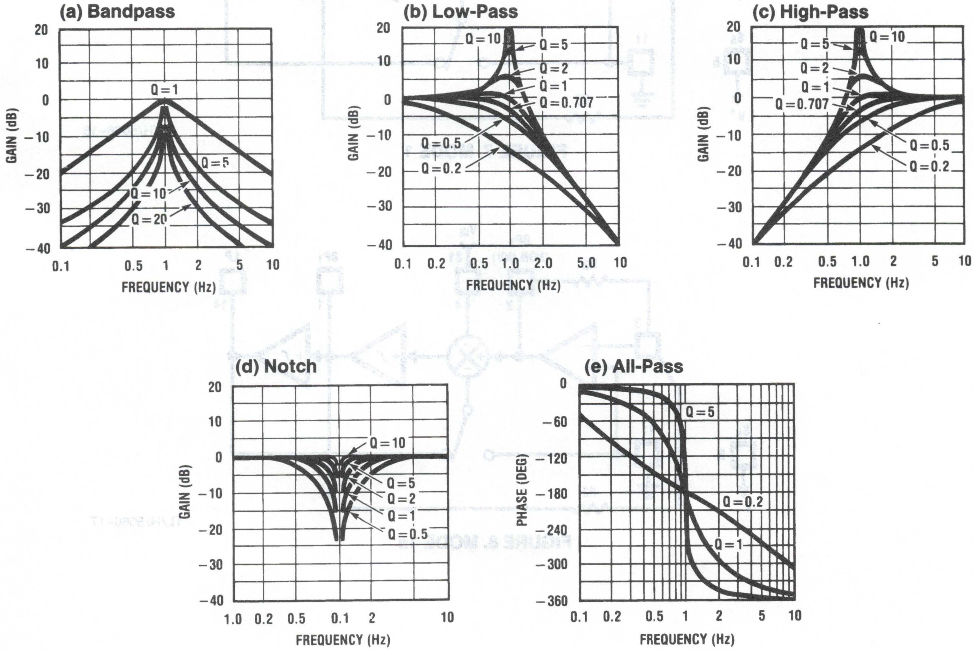
TL/H/5066–13

(a)

TL/H/5066–14

(b)

FIGURE 5. 2nd-Order All-Pass Response



TL/H/5066–15

FIGURE 6. Responses of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.

2.0 Modes of Operation

The MF5 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach is appropriate. Since this is cumbersome, and since the MF5 closely approximates continuous filters, the following discussion is based on the well known frequency domain. Each MF5 can produce a full 2nd order function. See Table 1 for a summary of the characteristics of the various modes.

MODE 1: Notch 1, Bandpass, Lowpass Outputs:

$f_{notch} = f_o$ (See *Figure 7*)

f_o = center frequency of the complex pole pair

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_{notch} = center frequency of the imaginary zero pair = f_o.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\dfrac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_o$) $= -\dfrac{R3}{R1}$

$$H_{ON} = \text{Notch output gain as } \left.\begin{matrix} f \rightarrow 0 \\ \\ f \rightarrow f_{CLK}/2 \end{matrix}\right\} = \frac{-R_2}{R_1}$$

$$Q = \frac{f_o}{BW} = \frac{R3}{R2}$$

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$$H_{OLP} = \frac{H_{OBP}}{Q} \text{ or } H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q.$$

$$H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)}$$

MODE 1a: Non-Inverting BP, LP (See *Figure 8*)

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{R3}{R2}$$

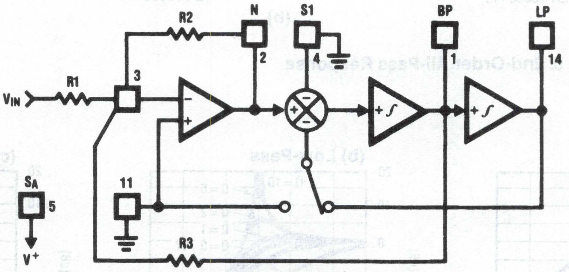
H_{OLP} = −1; $H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$$H_{OBP_1} = -\frac{R3}{R2}$$

H_{OBP_2} = 1 (non-inverting)

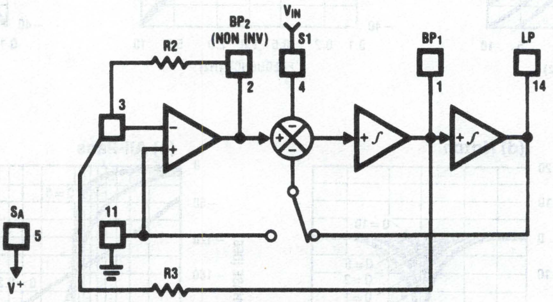
Circuit dynamics: $H_{OBP_1} = Q$

Note: V_{IN} should be driven from a low impedance (<1 kΩ)



TL/H/5066-16

FIGURE 7. MODE 1



TL/H/5066-17

FIGURE 8. MODE 1a

2.0 Modes of Operation (Continued)

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_o$ (See *Figure 9*)

f_o = center frequency

$$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

Q = quality factor of the complex pole pair

$$= \frac{\sqrt{R2/R4+1}}{R2/R3}$$

H_{OLP} = Lowpass output gain (as f → 0)

$$= -\frac{R2/R1}{R2/R4+1}$$

H_{OBP} = Bandpass output gain (at $f = f_o$) = $-R3/R1$

H_{ON_1} = Notch output gain (as f → 0)

$$= -\frac{R2/R1}{R2/R4+1}$$

$$H_{ON_2} = \text{Notch output gain } \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}H_{ON_2}} = Q\sqrt{H_{ON_1}H_{ON_2}}$

MODE 3: Highpass, Bandpass, Lowpass Outputs (See *Figure 10*)

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = \text{Highpass gain } \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

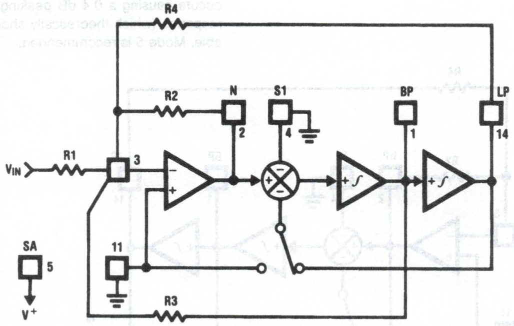
$$H_{OBP} = \text{Bandpass gain (at } f = f_o) = -\frac{R3}{R1}$$

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\frac{R4}{R1}$$

Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$; $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q$

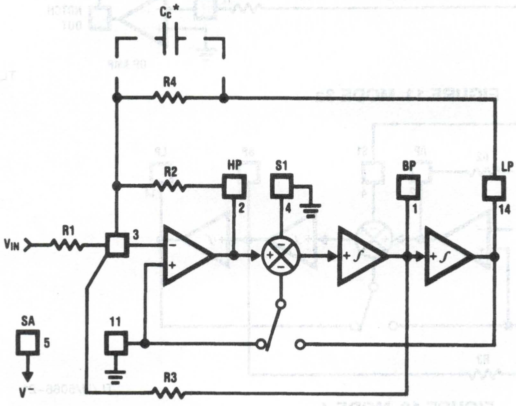
$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP(peak)} \cong Q \times H_{OHP}$ (for high Q's)



TL/H/5066-18

FIGURE 9. MODE 2



*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF–100 pF) across R4 to provide some phase lead.

TL/H/5066-19

FIGURE 10. MODE 3

2.0 Modes of Operation (Continued)

MODE 3a: HP, BP, LP and Notch with External Op amp (See *Figure 11*)

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

$$f_n = \text{notch frequency} = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$$

$$H_{on} = \text{gain of notch at } f = f_o = \left\| Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)\right\|$$

$$H_{n1} = \text{gain of notch (as } f \longrightarrow 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{n2} = \text{gain of notch} \left(\text{as } f \longrightarrow \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP}$$

MODE 4: Allpass, Bandpass, Lowpass Outputs (See *Figure 12*)

$$f_o = \text{center frequency}$$

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50};$$

$$f_z^* = \text{center frequency of the complex zero pair} \cong f_o$$

$$Q = \frac{f_o}{BW} = \frac{R3}{R2};$$

$$Q_z = \text{quality factor of complex zero pair} = \frac{R3}{R1}$$

For AP output make R1 = R2

$$H^*_{OAP} = \text{Allpass gain}\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$$

$$H_{OLP} = \text{Lowpass gain (as } f \longrightarrow 0)$$

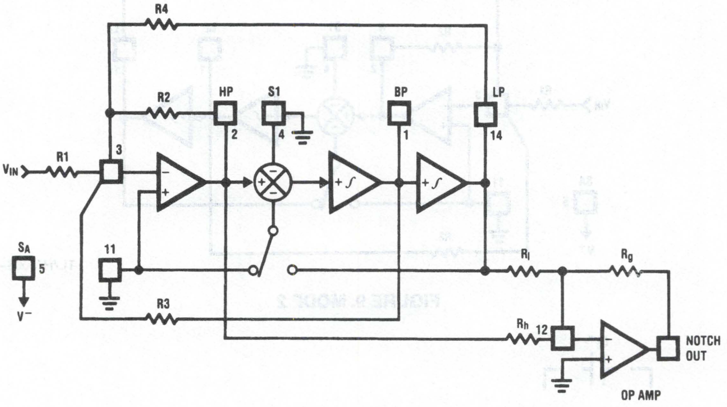
$$= -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_o)$$

$$= -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$$

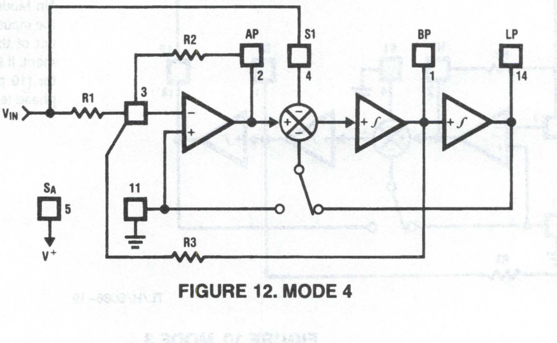
Circuit dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)\,Q$

*Due to the sampled data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4 dB peaking around f_o of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.



TL/H/5066-20

FIGURE 11. MODE 3a



TL/H/5066-21

FIGURE 12. MODE 4

2.0 Modes of Operation (Continued)

MODE 5: Numerator Complex Zeros, BP, LP (See *Figure 13*)

$$f_O = \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1+R2/R4} \times \frac{R3}{R2}$$

$$Q_z = \sqrt{1-R1/R4} \times \frac{R3}{R1}$$

$$H_{0_{z1}} = \text{gain at C.Z. output (as } f \rightarrow 0 \text{ Hz)} = \frac{-R2\,(R4-R1)}{R1\,(R4+R2)}$$

$$H_{0_{z2}} = \text{gain at C.Z. output} \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{-R2}{R1}$$

$$H_{OBP} = -\left(\frac{R2}{R1}+1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = -\left(\frac{R2+R1}{R2+R4}\right) \times \frac{R4}{R1}$$

MODE 6a: Single Pole, HP, LP Filter (See *Figure 14*)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

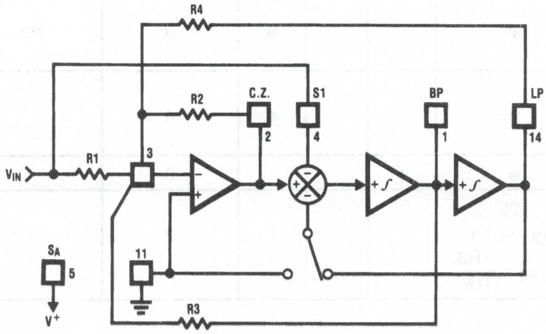
MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See *Figure 15*)

f_c = cutoff frequency of LP outputs

$$\cong \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

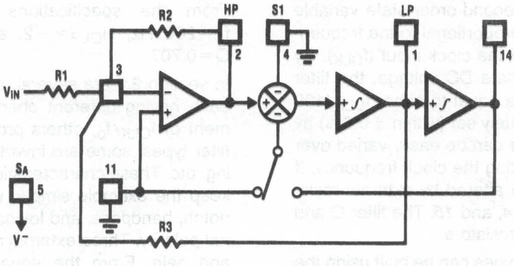
$$H_{OLP_1} = 1 \text{ (non-inverting)}$$

$$H_{OLP_2} = -\frac{R3}{R2}$$


R4
R2
C.Z.
S1
BP
LP
2
4
1
14
3
R1
V_{IN}
S_A
5
V^+
11
R3

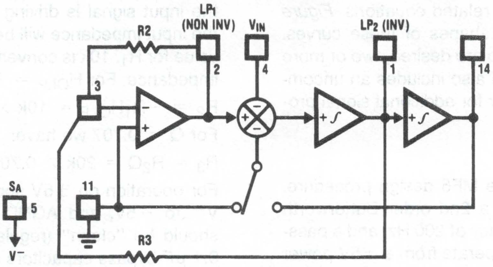
TL/H/5066–22

FIGURE 13. MODE 5


R2
HP
S1
LP
2
4
1
14
R1
3
V_{IN}
S_A
5
V^-
11
R3

TL/H/5066–23

FIGURE 14. MODE 6a


LP_1 (NON INV)
V_{IN}
LP_2 (INV)
R2
2
4
1
14
3
S_A
5
V^-
11
R3

TL/H/5066–24

FIGURE 15. MODE 6b

2.0 Modes of Operation (Continued)

TABLE I. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks. Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

Mode	BP	LP	HP	N	AP	Number of resistors	Adjustable f_{CLK}/f_o	Notes
1	*	*		*		3	No	
1a	(2) $H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} = +1$				2	No	May need input buffer. Poor dynamics for high Q.
2	*	*		*		3	Yes (above $f_{CLK}/50$ or $f_{CLK}/100$)	
3	*	*	*			4	Yes	Universal State-Variable Filter. Best general-purpose mode.
3a	*	*	*	*		7	Yes	As above, but also includes resistor-tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$.
5	*	*			*	4		Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$.
6a		*	*			3		Single pole.
6b		(2) $H_{OLP} = +1$ $H_{OLP2} = \frac{-R3}{R2}$				2		Single pole

3.0 Applications Information

The MF5 is a general-purpose second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input (f_{CLK}). By connecting pin 9 to the appropriate DC voltage, the filter center frequency f_o can be made equal to either $f_{CLK}/100$ or $f_{CLK}/50$. f_o can be very accurately set (within ±0.6%) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the f_{CLK}/f_o ratio can be altered by external resistors as in *Figures 9, 10, 11, 13, 14,* and *15.* The filter Q and gain are determined by external resistors.

All of the five second-order filter types can be built using the MF5. These are illustrated in *Figures 1* through *5* along with their transfer functions and some related equations. *Figure 6* shows the effect of Q on the shapes of these curves. When filter orders greater than two are desired, two or more MF5s can be cascaded. The MF5 also includes an uncommitted CMOS operational amplifier for additional signal processing applications.

3.1 DESIGN EXAMPLE

An example will help illustrate the MF5 design procedure. For the example, we will design a 2nd order Butterworth low-pass filter with a cutoff frequency of 200 Hz, and a passband gain of −2. The circuit will operate from a ±5V power supply, and the clock amplitude will be ±5v (CMOS) levels).

From the specifications, the filter parameters are: $f_o = 200$ Hz, $H_{OLP} = -2$, and, for Butterworth response, $Q = 0.707$.

In section 2.0 are several modes of operation for the MF5, each having different characteristics. Some allow adjustment of f_{CLK}/f_o, others produce different combinations of filter types, some are inverting while others are non-inverting, etc. These characteristics are summarized in Table I. To keep the example simple, we will use mode 1, which has notch, bandpass, and lowpass outputs, and inverts the signal polarity. Three external resistors determine the filter's Q and gain. From the equations accompanying *Figure 7*, $Q = R_3/R_2$ and the passband gain $H_{OLP} = -R_2/R_1$. Since the input signal is driving a summing junction through R_1, the input impedance will be equal to R_1. Start by choosing a value for R_1. 10k is convenient and gives a reasonable input impedance. For $H_{OLP} = -2$, we have:

$R_2 = -R_1 H_{OLP} = 10k \times 2 = 20k.$

For $Q = 0.707$ we have:

$R_3 = R_2 Q = 20k \times 0.707 = 14.14k.$ Use 15k.

For operation on ±5V supplies, V^+ is connected to +5V, V^- to −5V, and AGND to ground. The power supplies should be "clean" (regulated supplies are preferred) and 0.1 μF bypass capacitors are recommended.

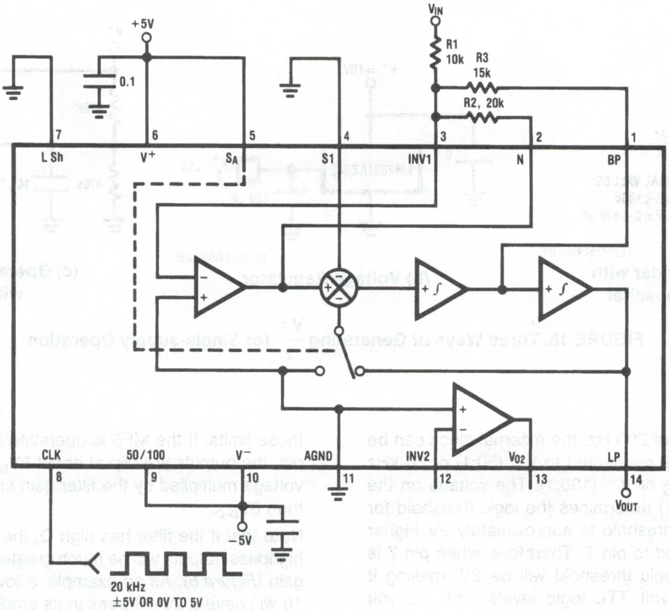

+5V
0.1
VIN
R1
10k
R3
15k
R2, 20k
7
6
5
4
3
2
1
L Sh
V+
SA
S1
INV1
N
BP
CLK
50/100
V−
AGND
INV2
VO2
LP
8
9
10
11
12
13
14
VOUT
−5V
20 kHz
±5V OR 0V TO 5V

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FIGURE 16. 2nd-Order Butterworth Low-Pass Filter of Design Example. For $\frac{f_{CLK}}{f_0} = 50$, Connect Pin 9 to +5V, and Change Clock Frequency to 10 kHz.

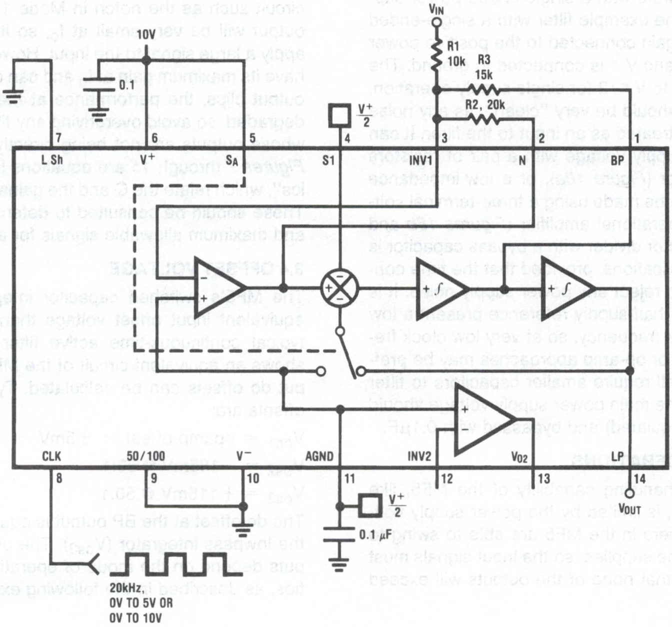
10V
0.1
VIN
R1
10k
R3
15k
R2, 20k
$\frac{V^+}{2}$
7
6
5
4
3
2
1
L Sh
V+
SA
S1
INV1
N
BP
CLK
50/100
V−
AGND
INV2
VO2
LP
8
9
10
11
12
13
14
VOUT
$\frac{V^+}{2}$
0.1 μF
20kHz,
0V TO 5V OR
0V TO 10V

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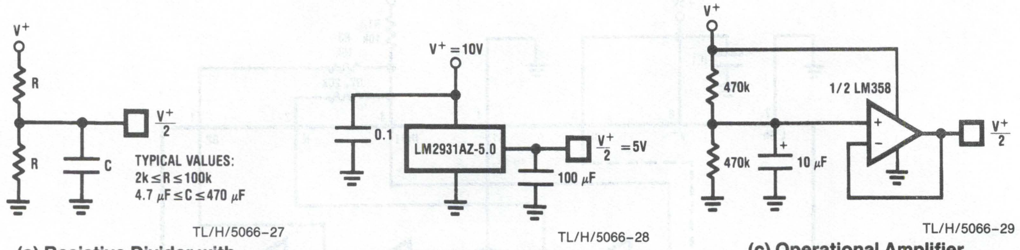
FIGURE 17. Butterworth Low-Pass Circuit of Example, but Designed for Single-Supply Operation

3.0 Applications Information (Continued)



(a) Resistive Divider with Decoupling Capaciter

(b) Voltage Regulator

(c) Operational Amplifier with Divider

FIGURE 18. Three Ways of Generating $\frac{V^+}{2}$ for Single-supply Operation

For a cutoff frequency of 200 Hz, the external clock can be either 10 kHz with pin 9 connected to V^+ (50:1) or 20 kHz with pin 9 tied to A_{GND} or V^- (100:1). The voltage on the Logic Level Shift pin (7) determines the logic threshold for the clock input. The threshold is approximately 2V higher than the voltage applied to pin 7. Therefore, when pin 7 is grounded, the clock logic threshold will be 2V, making it compatible with 0–5 volt TTL logic levels and ±5 volt CMOS levels. Pin 7 should be connected to a clean, low-impedance (less than 1000Ω) voltage source.

The complete circuit of the design example is shown for a 100:1 clock ratio in *Figure 16*.

3.2 SINGLE SUPPLY OPERATION

The MF5 can also operate with a single-ended power supply. *Figure 17* shows the example filter with a single-ended power supply. V^+ is again connected to the positive power supply (8 to 14 volts), and V^- is connected to ground. The A_{GND} pin must be tied to $V^+/2$ for single supply operation. This half-supply point should be very "clean", as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor (*Figure 18a*), or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier (*Figures 18b* and *18c*). The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1μF.

3.3 DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the MF5, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the MF5 are able to swing to within about 1 volt of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the MF5 is operating on ±5 volts, for example, the outputs will clip at about $8V_{p\text{-}p}$. The maximum input voltage multiplied by the filter gain should therefore be less than $8V_{p\text{-}p}$.

Note that if the filter has high Q, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain (*Figure 6*). As an example, a lowpass filter with a Q of 10 will have a 20 dB peak in its amplitude response at f_o. If the nominal gain of the filter H_{OLP} is equal to 1, the gain at f_o will be 10. The maximum input signal at f_o must therefore be less than 800 $mV_{p\text{-}p}$ when the circuit is operated on ±5 volt supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 (*Figure 7*). The notch output will be very small at f_o, so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at f_o and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying *Figures 7* through *15* are equations labeled "circuit dynamics", which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

3.4 OFFSET VOLTAGE

The MF5's switched capacitor integrators have a higher equivalent input offset voltage than would be found in a typical continuous-time active filter integrator. *Figure 19* shows an equivalent circuit of the MF5 from which the output dc offsets can be calculated. Typical values for these offsets are:

V_{os1} = opamp offset = ±5mV

V_{os2} = −185mV @ 50:1 −310mV @ 100:1

V_{os3} = +115mV @ 50:1 +240mV @ 100:1

The dc offset at the BP output is equal to the input offset of the lowpass integrator (V_{os3}). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

3.0 Applications Information (Continued)

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + \left\|H_{OLP}\right\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 1a

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right) V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{R_p} + 1\right) V_{OS1} \times \frac{1}{1 + R2/R4} + V_{OS2}\frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}};$$

$$R_p = R1//R2//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = -\frac{R4}{R2}\left(\frac{R2}{R3}V_{OS3} + V_{OS2}\right) + -\frac{R4}{R2}\left(1 + \frac{R2}{R_p}\right)V_{OS1};\ R_p = R1//R3//R4$$

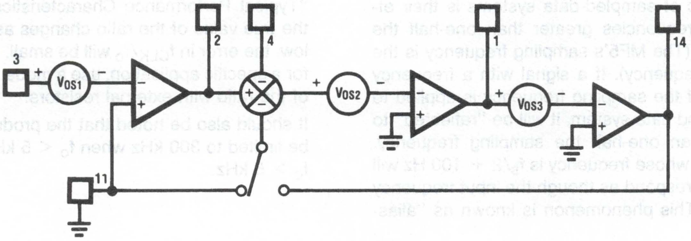


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FIGURE 19. Block Diagram Showing MF5 Offset Voltage Sources

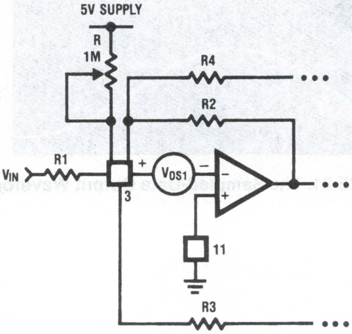

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FIGURE 20. Method for Trimming V_{OS}, See Text, Section 3.4

3.0 Applications Information (Continued)

For most applications, the outputs are AC coupled and DC offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower ac signal levels, and clipping at any of the outputs will cause gain nonlinearities and will change f_o and Q. When operating in Mode 3, offsets can become excessively large if R_2 and R_4 are used to make f_{CLK}/f_o significantly higher than the nominal value, especially if Q is also high. An extreme example is a bandpass filter having unity gain, a Q of 20, and $f_{CLK}/f_o = 250$ with pin 9 tied to V^- (100:1 nominal). R_4/R_2 will therefore be equal to 6.25 and the offset voltage at the lowpass output will be about +1.9V. Where necessary, the offset voltage can be adjusted by using the circuit of *Figure 20*. This allows adjustment of V_{os1}, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ($V_{os(BP)}$ in modes 1a and 3, for example).

3.5 SAMPLED DATA SYSTEM CONSIDERATIONS

The MF5 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF5's sampling frequency is the same as its clock frequency). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2 + 100$ Hz will cause the system to respond as though the input frequency was $f_s/2 - 100$ Hz. This phenomenon is known as "aliasing", and can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter ahead of the MF5 to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in "steps" in the output voltage which occur at the clock rate. (*Figure 21*) If necessary, these can be "smoothed" with a simple R-C low-pass filter at the MF5 output.

The ratio of f_{CLK} to f_c (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise sensitive applications, however, a ratio of 50:1 may be better as it will result in 3 dB lower output noise. The 50:1 ratio also results in lower DC offset voltages, as discussed in 3.4.

The accuracy of the f_{CLK}/f_o ratio is dependent on the value of Q. This is illustrated in the curves under the heading "Typical Performance Characteristics". As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in f_{CLK}/f_o will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

It should also be noted that the product of Q and f_o should be limited to 300 kHz when $f_o < 5$ kHz, and to 200 kHz for $f_o > 5$ kHz.

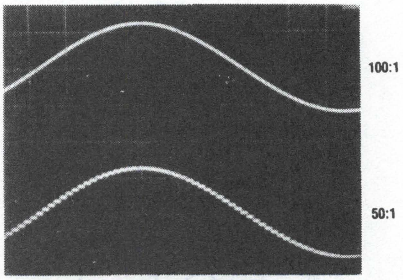

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FIGURE 21. The Sampled-Data Output Waveform

National Semiconductor Corporation

MF6 6th Order Switched Capacitor Butterworth Lowpass Filter

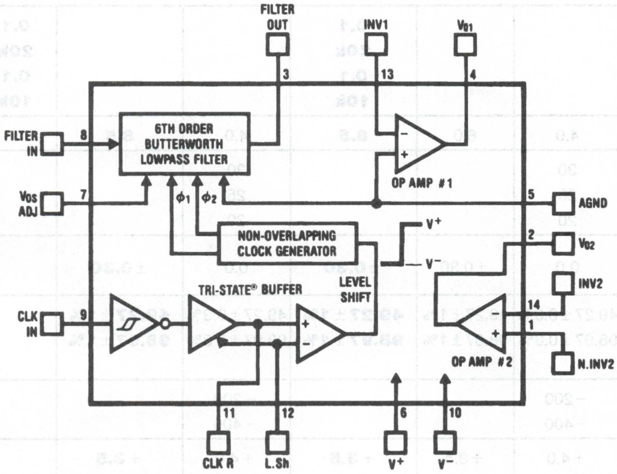
General Description

The MF6 is a versatile easy to use, precision 6th order Butterworth lowpass active filter. Switched capacitor techniques eliminate external component requirements and allow a clock tunable cutoff frequency. The ratio of the clock frequency to the lowpass cutoff frequency is internally set to 50 to 1 (MF6-50) or 100 to 1 (MF6-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or an external TTL or CMOS logic compatible clock can be used for tighter cutoff frequency control. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF6 sections for higher order filtering. In addition to the filter, two independent CMOS op amps are included on the die and are useful for any general signal conditioning applications.

Features

- No external components
- 14-pin DIP or 14-pin wide-body S.O. package
- Cutoff frequency accuracy of ±0.3% typical
- Cutoff frequency range of 0.1 Hz to 20 kHz
- Two uncommitted op amps available
- 5V to 14V total supply voltage
- Cutoff frequency set by external or internal clock

Block and Connection Diagrams


FILTER OUT
INV1
V_{01}
3
13
4
FILTER IN
8
6TH ORDER BUTTERWORTH LOWPASS FILTER
OP AMP #1
V_{OS} ADJ
7
ϕ_1
ϕ_2
5
AGND
NON-OVERLAPPING CLOCK GENERATOR
V+
V−
2
V_{02}
TRI-STATE® BUFFER
LEVEL SHIFT
INV2
CLK IN
9
14
1
OP AMP #2
N.INV2
11
12
6
10
CLK R
L.Sh
V+
V−

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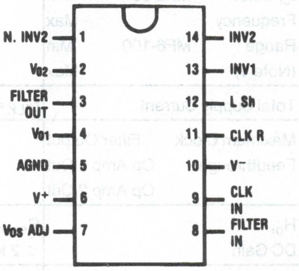
All Packages


N. INV2
1
V_{02}
2
FILTER OUT
3
V_{01}
4
AGND
5
V+
6
V_{OS} ADJ
7
14
INV2
13
INV1
12
L Sh
11
CLK R
10
V−
9
CLK IN
8
FILTER IN

TL/H/5065–2

Top View

Order Number MF6CWM-50
or MF6CWM-100
See NS Package Number M14B

Order Number MF6CN-50
or MF6CN-100
See NS Package Number N14A

Order Number MF6CJ-50
or MF6CJ-100
See NS Package Number J14A

Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	14V
Voltage at Any Pin	V− − 0.2V, V+ + 0.2V
Input Current at Any Pin (Note 13)	5 mA
Package Input Current (Note 13)	20 mA
Power Dissipation (Note 14)	500 mW
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 12)	800V
Soldering Information	
N Package (10 sec.)	260°C
J Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Operating Ratings (Note 11)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
MF6CN-50, MF6CN-100	$0°C \leq T_A \leq +70°C$
MF6CWM-50, MF6CWM-100	$0°C \leq T_A \leq +70°C$
MF6CJ-50, MF6CJ-100	$-40°C \leq T_A \leq +85°C$
Supply Voltage ($V_S = V+ - V-$)	5V to 14V

Filter Electrical Characteristics

The following specifications apply for $f_{CLK} \leq 250$ kHz (see Note 3) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	MF6CWM-50, MF6CWM-100, MF6CN-50, MF6CN-100			MF6CJ-50, MF6CJ-100			Units
		Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ = +5V, V^- = -5V$								
f_c, Cutoff Frequency Range (Note 1) MF6-50 Min Max MF6-100 Min Max				**0.1** **20k** **0.1** **10k**			**0.1** **20k** **0.1** **10k**	Hz
Total Supply Current	$f_{CLK} = 250$ kHz	4.0	6.0	**8.5**	4.0	**8.5**		mA
Maximum Clock Feedthrough Filter Output Op Amp 1 Out Op Amp 2 Out		30 25 20			30 25 20			mV (peak-to-peak)
H_o, DC Gain	$R_{source} \leq 2$ kΩ	0.0	±0.30	**±0.30**	0.0	**±0.30**		dB
f_{CLK}/f_c, Clock to Cutoff Frequency Ratio MF6-50 MF6-100		49.27±0.3% 98.97±0.3%	49.27±1% 98.97±1%	**49.27±1%** **98.97±1%**	49.27±0.3% 98.97±0.3%	**49.27±1%** **98.97±1%**		
DC Offset Voltage MF6-50 MF6-100		−200 −400			−200 −400			mV
Minimum Output Voltage Swing	$R_L = 10$ kΩ	+4.0 −4.1	+3.5 −3.8	**+3.5** **−3.5**	+4.0 −4.1	**+3.5** **−3.5**		V
Maximum Output Short Circuit Current (Note 6) Source Sink		50 1.5	60 2.0	**80** **3.0**	50 1.5	**80** **3.0**		mA
Dynamic Range (Note 2) MF6-50 MF6-100		83 81			83 81			dB
Additional Magnitude Response Test Points (Note 4) MF6-50	$f_{CLK} = 250$ kHz f = 6000 Hz f = 4500 Hz	 −9.47 −0.92	 −9.47±0.5 −0.92±0.2	 **−9.47±0.65** **−0.92±0.3**	 −9.47 −0.92	 **−9.47±0.65** **−0.92±0.3**		dB
MF6-100	$f_{CLK} = 250$ kHz f = 3000 Hz f = 2250 Hz	 −9.48 −0.97	 −9.48±0.5 −0.97±0.2	 **−9.48±0.65** **−0.97±0.3**	 −9.48 −0.97	 **−9.48±0.65** **−0.97±0.3**		dB

Filter Electrical Characteristics

(Continued) The following specifications apply for $f_{CLK} \le 250$ kHz (see Note 3) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter		Conditions	MF6CWM-50, MF6CWM-100 MF6CN-50, MF6CN-100			MF6CJ-50, MF6CJ-100			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ = +5V, V^- = -5V$ (Continued)									
Attenuation Rate	MF6-50	$f_{CLK} = 250$ kHz $f_1 = 6000$ Hz $f_2 = 8000$ Hz		−36	**−36**		**−36**		dB/ octave
	MF6-100	$f_{CLK} = 250$ kHz $f_1 = 3000$ Hz $f_2 = 4000$ Hz		−36	**−36**		**−36**		dB/ octave
$V^+ = +2.5V, V^- = -2.5V$									
f_c, Cutoff Frequency Range (Note 1)	MF6-50 Min				**0.1**			**0.1**	Hz
	Max				**10k**			**10k**	
	MF6-100 Min				**0.1**			**0.1**	
	Max				**5k**			**5k**	
Total Supply Current		$f_{CLK} = 250$ kHz	2.5	4.0	**4.0**	2.5	**4.0**		mA
Maximum Clock Feedthrough	Filter Output		20			20			mV (peak-to-peak)
	Op Amp 1 Out		15			15			
	Op Amp 2 Out		10			10			
H_o, DC Gain		$R_{source} \le 2$ kΩ	0.0	±0.30	**±0.30**	0.0	**±0.30**		dB
f_{CLK}/f_c, Clock to Cutoff Frequency Ratio	MF6-50		49.45±0.3%	49.45±1%	**49.45±2.5%**	49.45±0.3%	**49.45±2.5%**		
	MF6-100		99.35±0.3%	99.35±1%	**99.35±1.25%**	99.35±0.3%	**99.35±1.25%**		
DC Offset Voltage	MF6-50		−200			−200			mV
	MF6-100		−400			−400			
Minimum Output Voltage Swing		$R_L = 10$ kΩ	+1.5 −2.2	+1.0 −1.7	**+1.0** **−1.5**	+1.5 −2.2	**+1.0** **−1.5**		V
Maximum Output Short Circuit Current (Note 6)	Source		28	40	**50**	28	**50**		mA
	Sink		0.5	1.0	**1.5**	0.5	**1.5**		
Dynamic Range (Note 2)			77			77			dB
Additional Magnitude Response Test Points (Note 4)	MF6-50	$f_{CLK} = 250$ kHz f = 6000 Hz f = 4500 Hz	−9.54 −0.96	−9.54±0.5 −0.96±0.2	**−9.54±0.65** **−0.96±0.3**	−9.54 −0.96	**−9.54±0.65** **−0.96±0.3**		dB
	MF6-100	$f_{CLK} = 250$ kHz f = 3000 Hz f = 2250 Hz	−9.67 −1.01	−9.67±0.5 −1.01±0.2	**−9.67±0.65** **−1.01±0.3**	−9.67 −1.01	**−9.67±0.65** **−1.01±0.3**		dB
Attenuation Rate	MF6-50	$f_{CLK} = 250$ kHz $f_1 = 6000$ Hz $f_2 = 8000$ Hz		−36	**−36**		**−36**		dB/ octave
	MF6-100	$f_{CLK} = 250$ kHz $f_1 = 3000$ Hz $f_2 = 4000$ Hz		−36	**−36**		**−36**		dB/ octave

Op Amp Electrical Characteristics

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	MF6CN-50, MF6CN-100, MF6CWM-50, MF6CWM-100			MF6CJ-50, MF6CJ-100			Units
		Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ = +5V$, $V^- = -5V$								
Input Offset Voltage		±8.0	±20	**±20**	±8.0	**±20**		mV
Input Bias Current		10			10			pA
CMRR (Op Amp #2 Only)	$V_{CM1} = 1.8V$, $V_{CM2} = -2.2V$	60	55		60	55		dB
Output Voltage Swing	$R_L = 10\ k\Omega$	+4.0 −4.5	+3.8 −4.0	**+3.6** **−4.0**	+4.0 −4.5	**+3.6** **−4.0**		V
Maximum Output Short Circuit Current (Note 6) Source Sink		54 2.0	65 4.0	**80** **6.0**	54 2.0	**80** **6.0**		mA
Slew Rate		7.0			7.0			V/µs
DC Open Loop Gain		72		**65**	72		**65**	dB
Gain Bandwidth Product		1.2			1.2			MHz
$V^+ = +2.5V$, $V^- = -2.5V$								
Input Offset Voltage		±8.0	±20	**±20**	±8.0	**±20**		mV
Input Bias Current		10			10			pA
CMRR (Op-Amp #2 Only)	$V_{CM1} = +0.5V$, $V_{CM2} = -0.9V$	60	55		60	55		dB
Output Voltage Swing	$R_L = 10\ k\Omega$	+1.5 −2.2	+1.3 −1.7	**+1.1** **−1.7**	+1.5 −2.2	**+1.1** **−1.7**		V
Maximum Output Short Circuit Current (Note 6) Source Sink		24 1.0	35 2.0	**50** **4.0**	24 1.0	**50** **4.0**		mA
Slew Rate		6.0			6.0			V/µs
DC Open Loop Gain		67		**60**	67		**60**	dB
Gain Bandwidth Product		1.2			1.2			MHz

Logic Input-Output Electrical Characteristics

The following specifications apply for $V^- = 0V$ (see Note 5) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter		Conditions		MF6CN-50, MF6CN-100 MF6CWM-50, MF6CWM-100			MF6CJ-50, MF6CJ-100			Units
				Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
TTL CLOCK INPUT, CLK R PIN (Note 7)										
Maximum V_{IL}, Logical "0" Input Voltage					0.8	**0.8**		**0.8**		V
Minimum V_{IH}, Logical "1" Input Voltage					2.0	**2.0**		**2.0**		V
Maximum Leakage Current at CLK R Pin		L Sh Pin at Mid- Supply			2.0	**2.0**		**2.0**		μA
SCHMITT TRIGGER										
V_{T+}, Positive Going Threshold Voltage	Min	$V^+ = 10V$		7.0	6.1	**6.1**	7.0	**6.1**		V
	Max				8.9	**8.9**		**8.9**		
	Min	$V^+ = 5V$		3.5	3.1	**3.1**	3.5	**3.1**		V
	Max				4.4	**4.4**		**4.4**		
V_{T-}, Negative Going Threshold Voltage	Min	$V^+ = 10V$		3.0	1.3	**1.3**	3.0	**1.3**		V
	Max				3.8	**3.8**		**3.8**		
	Min	$V^+ = 5V$		1.5	0.6	**0.6**	1.5	**0.6**		V
	Max				1.9	**1.9**		**1.9**		
Hysteresis ($V_{T+} - V_{T-}$)	Min	$V^+ = 10V$		4.0	2.3	**2.3**	4.0	**2.3**		V
	Max				7.6	**7.6**		**7.6**		
	Min	$V^+ = 5V$		2.0	1.2	**1.2**	2.0	**1.2**		V
	Max				3.8	**3.8**		**3.8**		
Minimum Logical "1" Output Voltage (Pin 11)		$I_o = -10\mu A$	$V^+ = 10V$		9.0	**9.0**		**9.0**		V
			$V^+ = 5V$		4.5	**4.5**		**4.5**		
Maximum Logical "0" Output Voltage (Pin 11)		$I_o = 10\mu A$	$V^+ = 10V$		1.0	**1.0**		**1.0**		V
			$V^+ = 5V$		0.5	**0.5**		**0.5**		
Minimum Output Source Current (Pin 11)		CLK R Tied to Ground	$V^+ = 10V$	6.0	3.0	**3.0**	6.0	**3.0**		mA
			$V^+ = 5V$	1.5	0.75	**0.75**	1.5	**0.75**		
Maximum Output Sink Current (Pin 11)		CLK R Tied to V^+	$V^+ = 10V$	5.0	2.5	**2.5**	5.0	**2.5**		mA
			$V^+ = 5V$	1.3	0.65	**0.65**	1.3	**0.65**		

Note 1: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 2: For ±5V supplies the dynamic range is referenced to 2.82 Vrms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μVrms for the MF6-50 and 250 μVrms for the MF6-100. For ±2.5V supplies the dynamic range is referenced to 1.06 Vrms (1.5V peak) where the wideband noise over a 20 kHz bandwidth is typically 140 μVrms for both the MF6-50 and the MF6-100.

Note 3: The specifications for the MF6 have been given for a clock frequency (f_{CLK}) of 250 kHz and less. Above this clock frequency the cutoff frequency begins to deviate from the specified error band of ±1.0% but the filter still maintains its magnitude characteristics. See Application Hints, Section 1.5.

Note 4: Besides checking the cutoff frequency (f_c) and the stopband attenuation at 2 f_c, two additional frequencies are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB.

Note 5: For simplicity all the logic levels have been referenced to $V^- = 0V$ and will scale accordingly for ±5V and ±2.5V supplies (except for the TTL input logic levels).

Note 6: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst-case conditions.

Note 7: The MF6 is operating with symmetrical split supplies and L.Sh is tied to ground.

Note 8: Typicals are at 25°C and represent most likely parametric norm.

Note 9: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level.

Note 10: Design limits are guaranteed, but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 11: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified conditions.

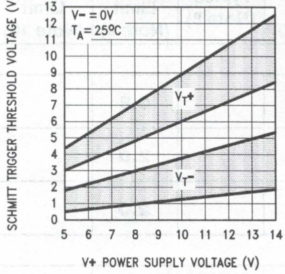
Note 12: Human body model, 100 pF discharged through a 1.5k Ω resistor.

Note 13: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

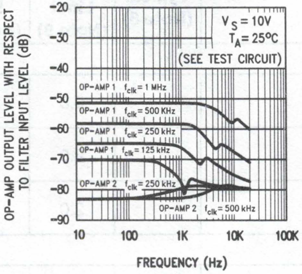
Note 14: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF6CN when board mounted is 67°C/W. For the MF6CJ this number decreases to 62°C/W. For MF6CWM, $\theta_{JA} = 78°C/W$.

Typical Performance Characteristics

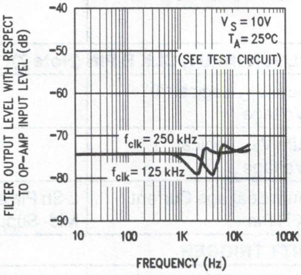
Schmitt Trigger Threshold Voltage vs Power Supply Voltage



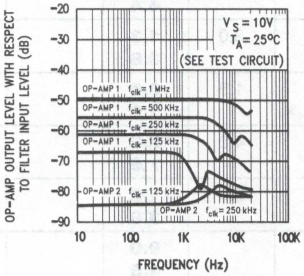
Crosstalk from Filter to Op-Amps (MF6-100)



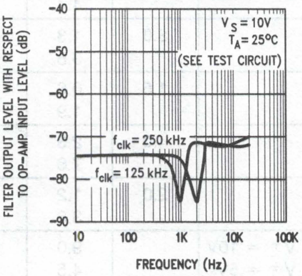
Crosstalk from Either Op-Amp to Filter Output (MF6-50)



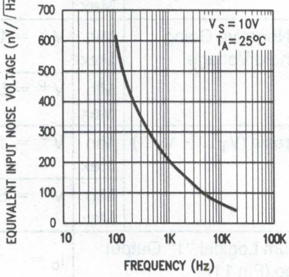
Crosstalk from Filter to Op-Amps (MF6-50)



Crosstalk from Either Op-Amp to Filter Output (MF6-100)



Equivalent Input Noise Voltage of Op-Amps



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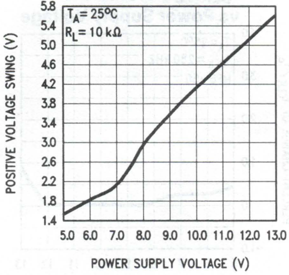
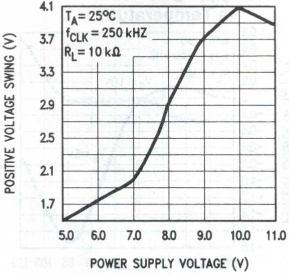
Typical Performance Characteristics (Continued)

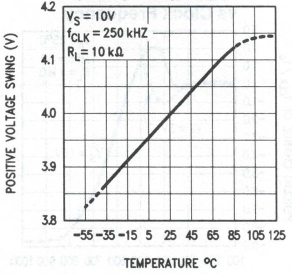
Positive Voltage Swing vs Power Supply Voltage (Op Amp Output)



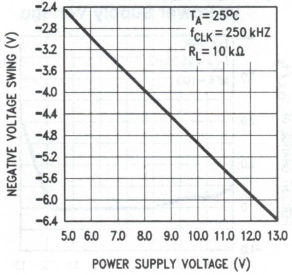
Positive Voltage Swing vs Power Supply Voltage (Filter Output)



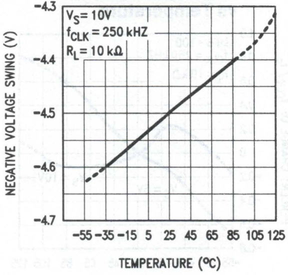
Positive Voltage Swing vs Temperature (Filter and Op Amp Outputs)



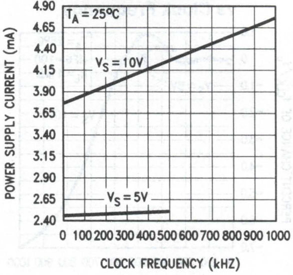
Negative Voltage Swing vs Power Supply Voltage (Filter and Op Amp Outputs)



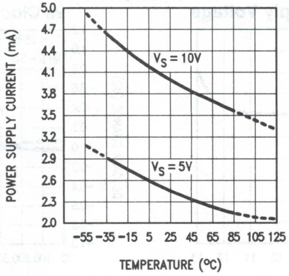
Negative Voltage Swing vs Temperature (Filter and Op Amp Outputs)



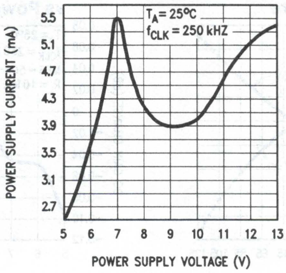
Power Supply Current vs Clock Frequency



Power Supply Current vs Temperature



Power Supply Current vs Power Supply Voltage



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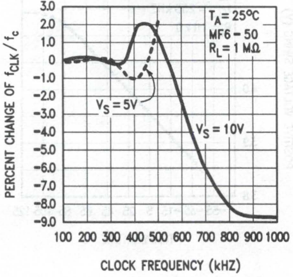
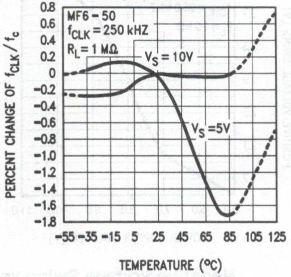
Typical Performance Characteristics (Continued)

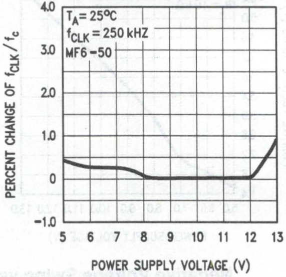
f_{CLK}/f_c Deviation vs Clock Frequency



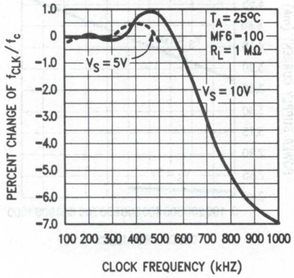
f_{CLK}/f_c Deviation vs Temperature



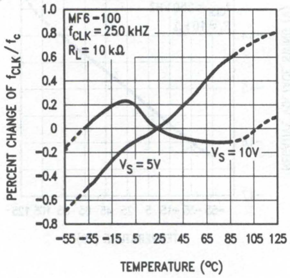
f_{CLK}/f_c Deviation vs Power Supply Voltage



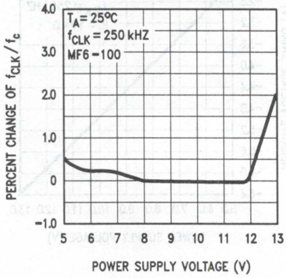
f_{CLK}/f_c Deviation vs Clock Frequency



f_{CLK}/f_c Deviation vs Temperature

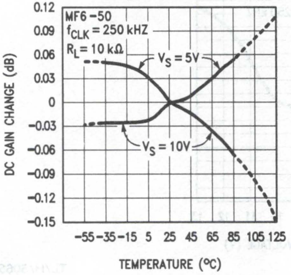


f_{CLK}/f_c Deviation vs Power Supply Voltage

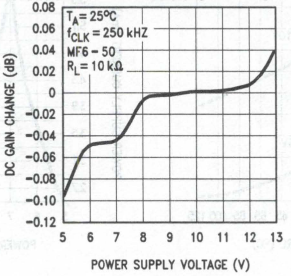


TL/H/5065–36

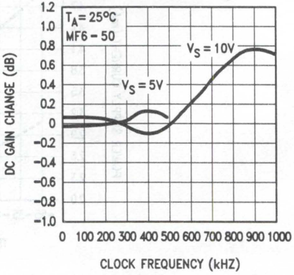
DC Gain Deviation vs Temperature



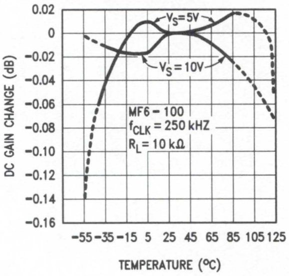
DC Gain Deviation vs Power Supply Voltage



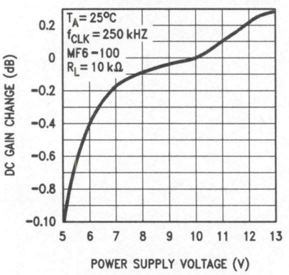
DC Gain Deviation vs Clock Frequency



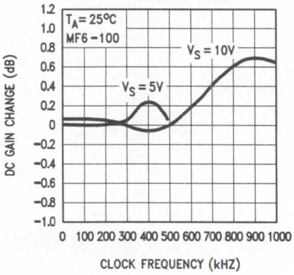
DC Gain Deviation vs Temperature



DC Gain Deviation vs Power Supply Voltage



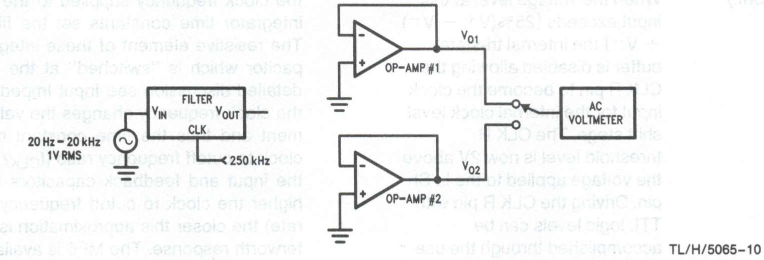
DC Gain Deviation vs Clock Frequency



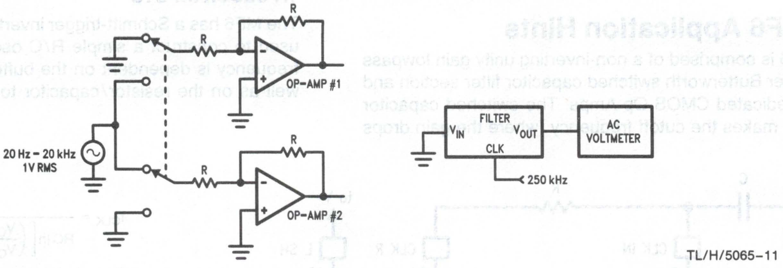
TL/H/5065–39

Crosstalk Test Circuits

From Filter to Opamps



From Either Opamp to Filter Output



Pin Descriptions (Pin Numbers)

Pin	Description
FILTER OUT (3)	The output of the lowpass filter. It will typically sink 0.9 mA and source 3 mA and swing to within 1V of each supply rail.
FILTER IN (8)	The input to the lowpass filter. To minimize gain errors the source impedance that drives this input should be less than 2k (see section 1.4). For single supply operation the input signal must be biased to mid-supply or AC coupled.
V_{OS}ADJ (7)	This pin is used to adjust the DC offset of the filter output; if not used it must be tied to the AGND potential. (See section 1.3)
AGND (5)	The analog ground pin. This pin sets the DC bias level for the filter section and the non-inverting input of Op-Amp #1 and must be tied to the system ground for split supply operation or to mid-supply for single supply operation (see section 1.2). When tied to mid-supply this pin should be well bypassed.
V_{O1} (4), INV1 (13)	V_{O1} is the output and INV1 is the inverting input of Op-Amp #1. The non-inverting input of this Op-Amp is internally connected to the AGND pin.
V_{O2} (2), INV2 (14), NINV2 (1)	V_{O2} is the output, INV2 is the inverting input, and NINV2 is the non-inverting input of Op-Amp #2.
V+ (6), V− (10)	The positive and negative supply pins. The total power supply range is 5V to 14V. Decoupling these pins with 0.1 μF capacitors is highly recommended.
CLK IN (9)	A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self-clocking Schmitt-trigger oscillator (see section 1.1).
CLK R (11)	A TTL logic level clock input when in split supply operation (±2.5V to ±7V) and L. Sh tied to system ground. This pin becomes a low impedance output when L. Sh is tied to V−. Also used in conjunction with the CLK IN pin for a self clocking Schmitt-trigger oscillator (see section 1.1).
L. Sh (12)	Level shift pin, selects the logic threshold levels for the desired clock. When tied to V− it enables an internal tri-state buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output.

Pin Descriptions (Pin Numbers) (Continued)

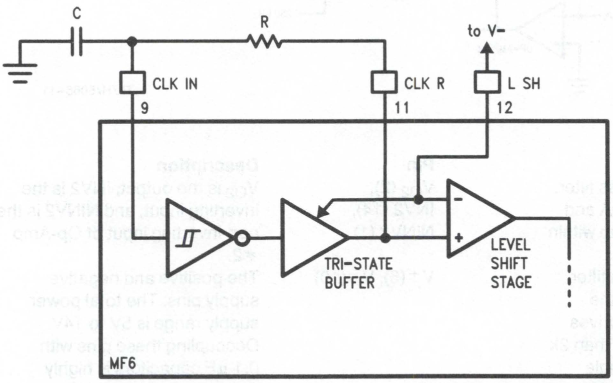
Pin	Description
L. Sh (cont.)	When the voltage level at this input exceeds [25%($V^+ - V^-$) + V^-] the internal tri-state buffer is disabled allowing the CLK R pin to become the clock input for the internal clock level shift stage. The CLK R threshold level is now 2V above the voltage applied to the L. Sh pin. Driving the CLK R pin with TTL logic levels can be accomplished through the use of split supplies and by tying the L. Sh pin to system ground.

1.0 MF6 Application Hints

The MF6 is comprised of a non-inverting unity gain lowpass sixth order Butterworth switched capacitor filter section and two undedicated CMOS Op-Amps. The switched capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio (100:1 or 50:1) of the clock frequency supplied to the lowpass filter. Internal integrator time constants set the filter's cutoff frequency. The resistive element of these integrators is actually a capacitor which is "switched" at the clock frequency (for a detailed discussion see Input Impedance Section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock to cutoff frequency ratio (f_{CLK}/f_c) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock to cutoff frequency ratio (or the sampling rate) the closer this approximation is to the theoretical Butterworth response. The MF6 is available in f_{CLK}/f_c ratios of 50:1 (MF6-50) or 100:1 (MF6-100).

1.1 CLOCK INPUTS

The MF6 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. The oscillator's frequency is dependent on the buffer's threshold levels as well as on the resistor/capacitor tolerance (see *Figure 1*).


C
R
to V−
CLK IN
9
CLK R
11
L SH
12
TRI-STATE BUFFER
LEVEL SHIFT STAGE
MF6

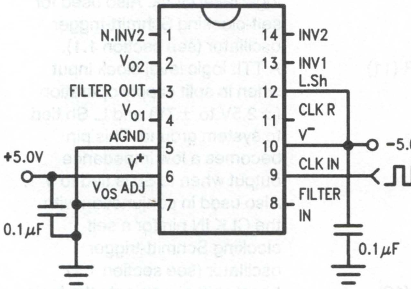
$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}\right)\frac{V_{T+}}{V_{T-}}\right]}$$

Typically for $V_{CC} = V^+ - V^- = 10V$:

$$f_{CLK} = \frac{1}{1.69\ RC}$$

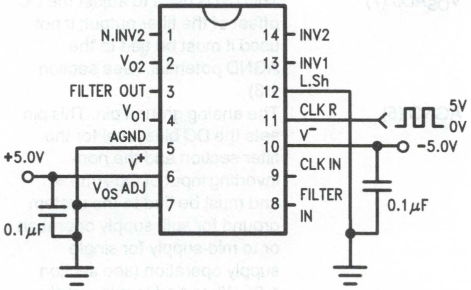
TL/H/5065-12

FIGURE 1. Schmitt Trigger R/C Oscillator


N.INV2
1
V_{O2}
2
FILTER OUT
3
V_{O1}
4
AGND
5
V+
6
V_{OS} ADJ
7
14
INV2
13
INV1
L.Sh
12
CLK R
11
V−
10
CLK IN
9
FILTER IN
8
+5.0V
0.1 µF
−5.0V
+5V
−5V
0.1 µF

TL/H/5065-3

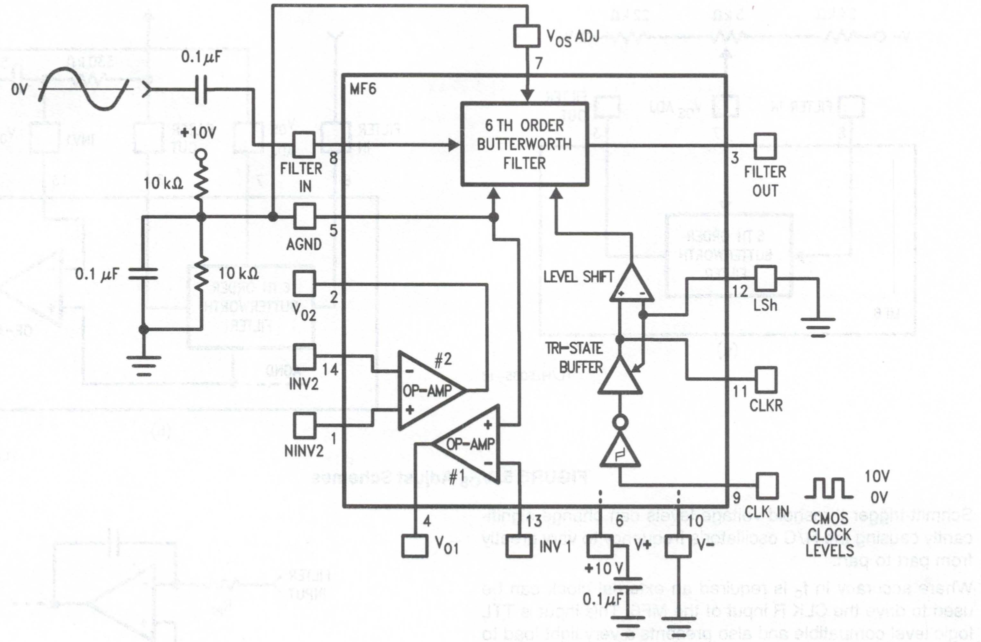
FIGURE 2. Dual Supply Operation MF6 Driven with CMOS Logic Level Clock ($V_{IH} \geq 0.8\ V_{CC}$ and $V_{IL} \leq 0.2\ V_{CC}$ where $V_{CC} = V^+ - V^-$)


N.INV2
1
V_{O2}
2
FILTER OUT
3
V_{O1}
4
AGND
5
V+
6
V_{OS} ADJ
7
14
INV2
13
INV1
L.Sh
12
CLK R
11
V−
10
CLK IN
9
FILTER IN
8
+5.0V
0.1 µF
5V
0V
−5.0V
0.1 µF

TL/H/5065-4

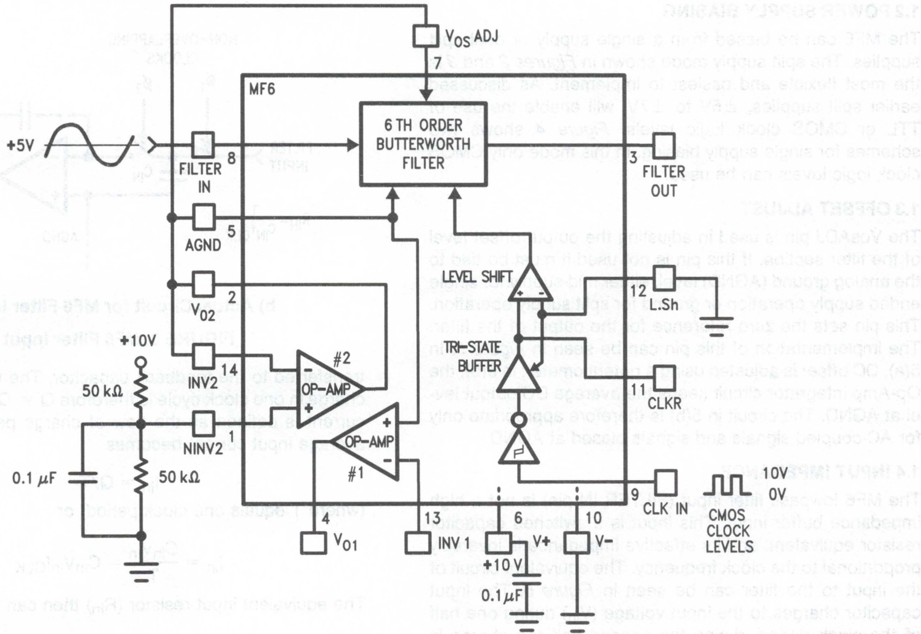
FIGURE 3. Dual Supply Operation MF6 Driven with TTL Logic Level Clock

Application Hints (Continued)


V_OS ADJ
7
0.1 μF
0V
MF6
6 TH ORDER BUTTERWORTH FILTER
+10V
FILTER IN
8
3
FILTER OUT
10 kΩ
AGND
5
0.1 μF
10 kΩ
LEVEL SHIFT
12
LSh
V02
2
TRI-STATE BUFFER
INV2
14
#2
OP-AMP
11
CLKR
NINV2
1
OP-AMP
#1
9
CLK IN
10V
0V
CMOS CLOCK LEVELS
4
V01
13
INV 1
6
V+
10
V−
+10 V
0.1 μF

TL/H/5065–14

a) Resistor Biasing of AGND

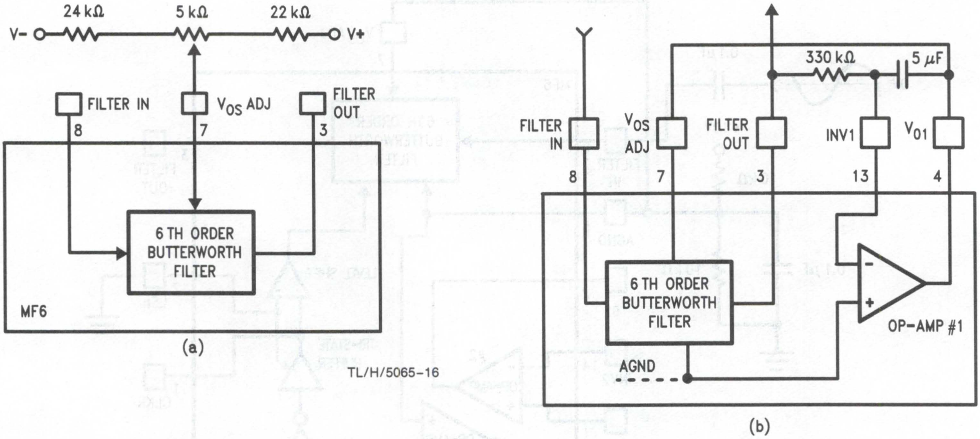

V_OS ADJ
7
MF6
6 TH ORDER BUTTERWORTH FILTER
+5V
FILTER IN
8
3
FILTER OUT
AGND
5
LEVEL SHIFT
V02
2
12
L.Sh
+10V
TRI-STATE BUFFER
INV2
14
#2
OP-AMP
50 kΩ
11
CLKR
NINV2
1
OP-AMP
#1
0.1 μF
50 kΩ
9
CLK IN
10V
0V
CMOS CLOCK LEVELS
4
V01
13
INV 1
6
V+
10
V−
+10 V
0.1 μF

TL/H/5065–15

b) Using Op-Amp 2 to Buffer AGND

FIGURE 4. Single Supply Operation

Application Hints (Continued)



TL/H/5065–16

TL/H/5065–17

FIGURE 5. V_{OS} Adjust Schemes

Schmitt-trigger threshold voltage levels can change significantly causing the R/C oscillator's frequency to vary greatly from part to part.

Where accuracy in f_c is required an external clock can be used to drive the CLK R input of the MF6. This input is TTL logic level compatible and also presents a very light load to the external clock source (~2 μA) with split supplies and L. Sh tied to system ground. The logic level is programmed by the voltage applied to level shift (L. Sh) pin (See the Pin description for L. Sh pin).

1.2 POWER SUPPLY BIASING

The MF6 can be biased from a single supply or dual split supplies. The split supply mode shown in *Figures 2* and *3* is the most flexible and easiest to implement. As discussed earlier split supplies, ±5V to ±7V, will enable the use of TTL or CMOS clock logic levels. *Figure 4* shows two schemes for single supply biasing. In this mode only CMOS clock logic levels can be used.

1.3 OFFSET ADJUST

The VosADJ pin is used in adjusting the output offset level of the filter section. If this pin is not used it must be tied to the analog ground (AGND) level, either mid-supply for single ended supply operation or ground for split supply operation. This pin sets the zero reference for the output of the filter. The implementation of this pin can be seen in *Figure 5*. In 5(a), DC offset is adjusted using a potentiometer; in 5(b), the Op-Amp integrator circuit keeps the average DC output level at AGND. The circuit in 5(b) is therefore appropriate only for AC-coupled signals and signals biased at AGND.

1.4 INPUT IMPEDANCE

The MF6 lowpass filter input (FILTER IN pin) is not a high impedance buffer input. This input is a switched capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the input to the filter can be seen in *Figure 6*. The input capacitor charges to the input voltage (V_{in}) during one half of the clock period, during the second half the charge is transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore $Q = C_{in}V_{in}$, and since current is defined as the flow of charge per unit time the average input current becomes

$$I_{in} = Q/T$$

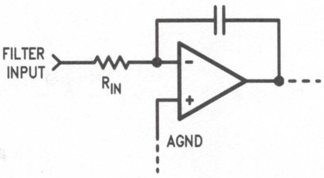
(where T equals one clock period) or

$$I_{in} = \frac{C_{in}V_{in}}{T} = C_{in}V_{in}f_{CLK}$$

The equivalent input resistor (R_{in}) then can be defined as

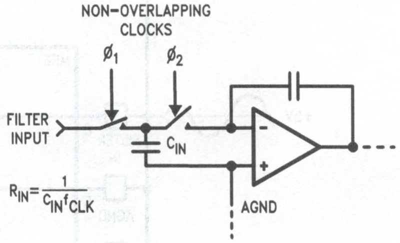
$$R_{in} = V_{in}/I_{in} = \frac{1}{C_{in}f_{CLK}}$$

The input capacitor is 2 pF for the MF6-50 and 1 pF for the



TL/H/5065–18

a) Equivalent Circuit for MF6 Filter Input



TL/H/5065–19

b) Actual Circuit for MF6 Filter Input

FIGURE 6. MF6 Filter Input

Application Hints (Continued)

MF6-100, so for the MF6-100

$$R_{in} = \frac{1 \times 10^{12}}{f_{CLK}} = \frac{1 \times 10^{12}}{f_c \times 100} = \frac{1 \times 10^{10}}{f_c}$$

and

$$R_{in} = \frac{5 \times 10^{11}}{f_{CLK}} = \frac{5 \times 10^{11}}{f_c \times 50} = \frac{1 \times 10^{10}}{f_c}$$

for the MF6-50. As shown in the above equations for a given cutoff frequency (f_c) the input impedance remains the same for the MF6-50 and the MF6-100. The higher the clock to center frequency ratio, the greater equivalent input resistance for a given clock frequency. As the cutoff frequency increases the equivalent input impedance decreases. This input resistance will form a voltage divider with the source impedance (R_{source}). Since R_{in} is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to load the input signal which would appear as an overall decrease in gain to the output of the filter. Since the filter's ideal gain is unity its overall gain is given by:

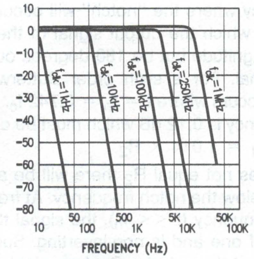
$$A_v = \frac{R_{in}}{R_{in} + R_{source}}$$

If the MF6-50 or the MF6-100 were set up for a cutoff frequency of 10 kHz the input impedance would be:

$$R_{in} = \frac{1 \times 10^{10}}{10\ \text{kHz}} = 1\ \text{M}\Omega$$

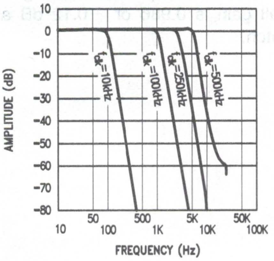
In this example with a source impedance of 10k the overall gain, if the MF6 had an ideal gain of 1 or 0 dB, would be:

$$A_v = \frac{1\ \text{M}\Omega}{10\ \text{k}\Omega + 1\ \text{M}\Omega} = 0.99009 \text{ or } -86.4\ \text{mdB}$$



TL/H/5065-20

FIGURE 7a. MF6-100 ±5V Supplies Amplitude Response



TL/H/5065-22

FIGURE 7c. MF6-100 ±2.5V Supplies Amplitude Response

Since the maximum overall gain error for the MF6 is ±0.3 dB with a $R_s \leq 2\ \text{k}\Omega$ the actual gain error for this case would be +0.21 dB to −0.39 dB.

1.5 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency (f_c) has a lower limit caused by leakage currents through the internal switches discharging the stored charge on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error, for example:

$$f_{CLK} = 100\ \text{Hz},\ I_{leakage} = 1\ \text{pA},\ C = 1\ \text{pF}$$

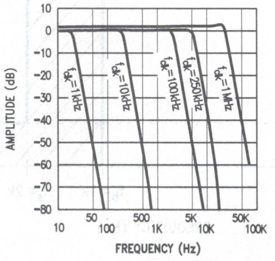
$$V = \frac{1\ \text{pA}}{1\ \text{pF}\ (100\ \text{Hz})} = 10\ \text{mV}$$

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors increases as the MF6 power supply voltage decreases. This causes a shift in the f_{CLK}/f_c ratio which will become noticeable when the clock frequency exceeds 250 kHz. The amplitude characteristic will stay within tolerance until f_{CLK} exceeds 500 kHz and will peak at about 0.5 dB at the corner frequency with a 1 MHz clock. The response of the MF6 is still a reasonable approximation of the ideal Butterworth lowpass characteristic as can be seen in *Figure 7*.

2.0 Designing with the MF6

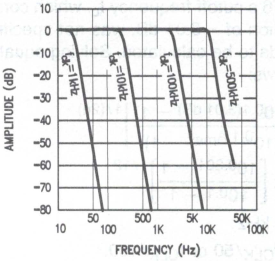
Given any lowpass filter specification two equations will come in handy in trying to determine whether the MF6 will do the job. The first equation determines the order of the lowpass filter required:

$$n = \frac{\log\left(10^{0.1\,A_{min}} - 1\right) - \log\left(10^{0.1\,A_{max}} - 1\right)}{2 \log\left(f_s/f_b\right)} \qquad (1)$$



TL/H/5065-21

FIGURE 7b. MF6-50 ±5V Supplies Amplitude Response



TL/H/5065-23

FIGURE 7d. MF6-50 ±2.5V Supplies Amplitude Response

Designing with the MF6 (Continued)

where n is the order of the filter, A_{min} is the minimum stopband attenuation (in dB) desired at frequency f_s, and A_{max} is the passband ripple or attenuation (in dB) at frequency f_b. If the result of this equation is greater than 6, then more than a single MF6 is required.

The attenuation at any frequency can be found by the following equation:

$$\text{Attn}(f) = 10 \log \left[1 + (10^{0.1 A_{max}} - 1)(f/f_b)^{2n}\right] \text{dB} \quad (2)$$

where n = 6 (the order of the filter).

2.1 A LOWPASS DESIGN EXAMPLE

Suppose the amplitude response specification in *Figure 8* is given. Can the MF6 be used? The order of the Butterworth approximation will have to be determined using eq. 1:

$$A_{min} = 30 \text{ dB},\ A_{max} = 1.0 \text{ dB},\ f_s = 2 \text{ kHz, and } f_b = 1 \text{ kHz}$$

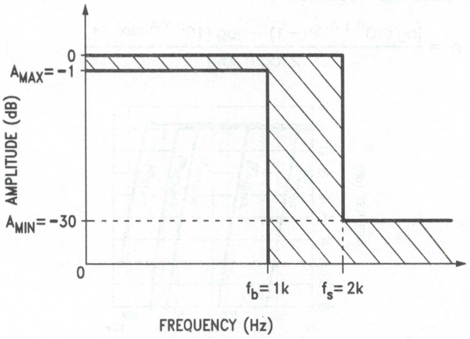
$$n = \frac{\log(10^3 - 1) - \log(10^{0.1} - 1)}{2 \log(2)} = 5.96$$

Since n can only take on integer values, n = 6. Therefore the MF6 can be used. In general, if n is 6 or less a single MF6 stage can be utilized.

Likewise, the attenuation at f_s can be found using equation 2 with the above values and n = 6 giving:

$$\text{Atten}(2 \text{ kHz}) = 10 \log \left[1 + (10^{0.1} - 1)(2 \text{ kHz}/1 \text{ kHz})^{12}\right] = 30.26 \text{ dB}$$

This result also meets the design specification given in *Figure 8* again verifying that a single MF6 section will be adequate.



TL/H/5065-24

FIGURE 8. Design Example Magnitude Response Specification Where the Response of the Filter Design Must Fall Within the Shaded Area of the Specification

Since the MF6's cutoff frequency f_c, which corresponds to a gain attenuation of −3.01 dB, was not specified in this example it needs to be calculated. Solving equation 2 where $f = f_c$ as follows:

$$f_c = f_b \left[\frac{(10^{0.1(3.01 \text{ dB})} - 1)}{(10^{0.1 A_{max}} - 1)}\right]^{1/(2n)}$$

$$= 1 \text{ kHz} \left[\frac{10^{0.301} - 1}{10^{0.1} - 1}\right]^{1/12}$$

$$= 1.119 \text{ kHz}$$

where $f_c = f_{CLK}/50$ or $f_{CLK}/100$.

To implement this example for the MF6-50 the clock frequency will have to be set to $f_{CLK} = 50(1.116 \text{ kHz}) = 55.8$ kHz or for the MF6-100 $f_{CLK} = 100(1.116 \text{ kHz}) = 111.6$ kHz.

2.2 CASCADING MF6s

In the case where a steeper stopband attenuation rate is required two MF6's can be cascaded (*Figure 9*) yielding a 12th order slope of 72 dB per octave. Because the MF6 is a Butterworth filter and therefore has no ripple in its passband, when MF6s are cascaded the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1V/V. The resulting response is shown in *Figure 10*.

In determining whether the cascaded MF6s will yield a filter that will meet a particular amplitude response specification, as above, equations 3 and 4 can be used, shown below.

$$n = \frac{\log(10^{0.05 A_{min}} - 1) - \log(10^{0.05 A_{max}} - 1)}{2 \log(f_s/f_b)} \quad (3)$$

$$\text{Attn}(f) = 10 \log \left[1 + (10^{0.05 A_{max}} - 1)(f/f_b)^{2n}\right] \text{dB} \quad (4)$$

where n = 6 (the order of each filter).

Equation 3 will determine whether the order of the filter is adequate ($n \leq 6$) while equation 4 can determine if the required stopband attenuation is met and what actual cutoff frequency (f_c) is required to obtain the particular frequency response desired. The design procedure would be identical to the one shown in section 2.1.

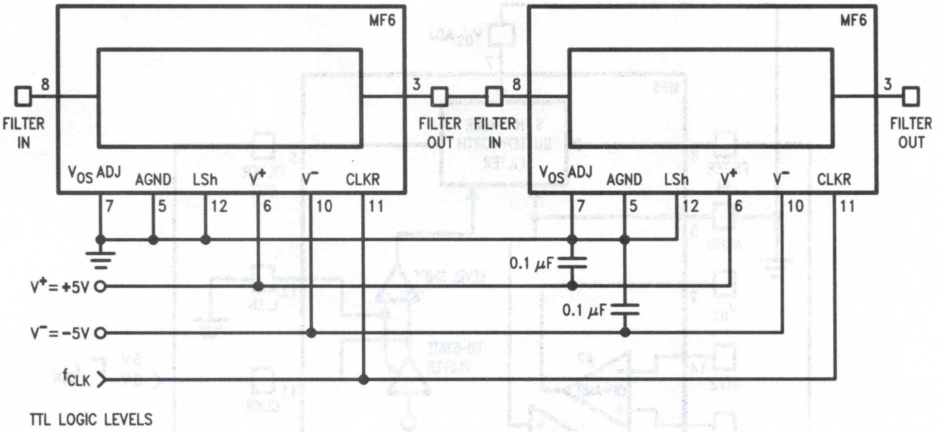
2.3 IMPLEMENTING A "NOTCH" FILTER WITH THE MF6

A "notch" filter with 60 dB of attenuation can be obtained by using one of the Op-Amps, available in the MF6, and three external resistors. The circuit and amplitude response are shown in *Figure 11*.

The frequency where the "notch" will occur is equal to the frequency at which the output signal of the MF6 will have the same magnitude but be 180 degrees out of phase with its input signal. For a sixth order Butterworth filter 180° phase shift occurs where $f = f_n = 0.742 f_c$. The attenuation at this frequency is 0.12 dB which must be compensated for by making $R_1 = 1.014 \times R_2$.

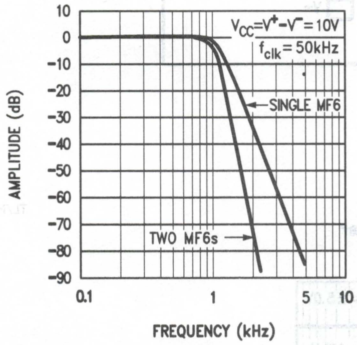
Since R_1 does not equal R_2 there will be a gain inequality above and below the notch frequency. At frequencies below the notch frequency ($f << f_n$), the signal through the filter has a gain of one and is non-inverting. Summing this with the input signal through the Op-Amp yields an overall gain of two or +6 dB. For $f >> f_n$, the signal at the output of the filter is greatly attenuated thus only the input signal will appear at the output of the Op-Amp. With $R_3 = R_1 = 1.014\ R_2$ the overall gain is 0.986 or −0.12 dB at frequencies above the notch.

Designing with the MF6 (Continued)


MF6
FILTER IN
8
3
FILTER OUT
FILTER IN
FILTER OUT
VOS ADJ
AGND
LSh
V+
V−
CLKR
7
5
12
6
10
11
0.1 µF
0.1 µF
V+ = +5V
V− = −5V
fCLK
TTL LOGIC LEVELS

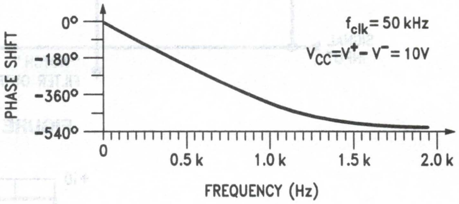
TL/H/5065-25

FIGURE 9. Cascading Two MF6s



TL/H/5065-26

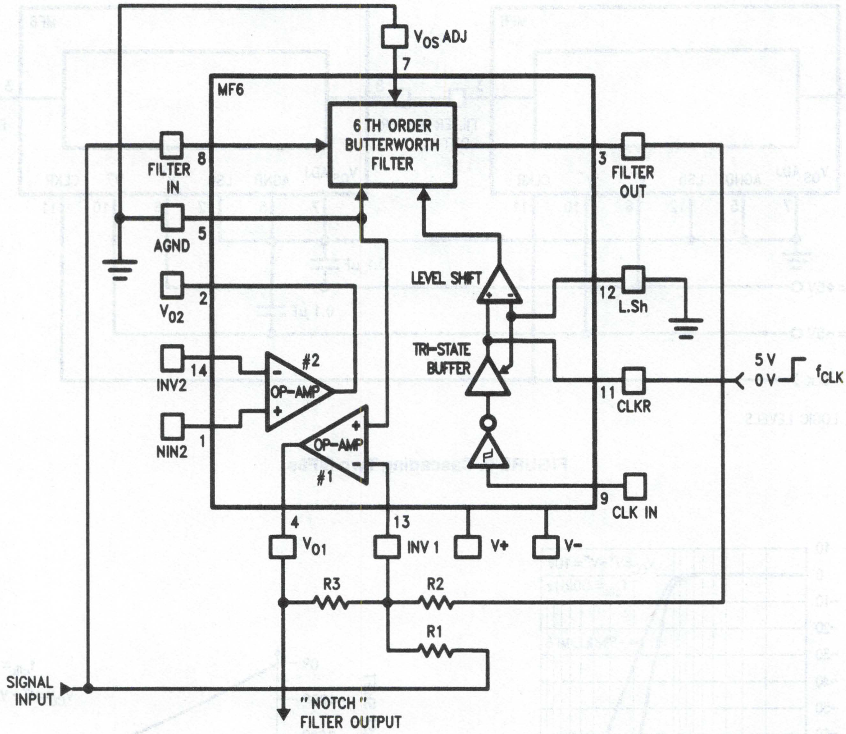
FIGURE 10a. One MF6-50 vs. Two MF6-50s Cascaded



TL/H/5065-27

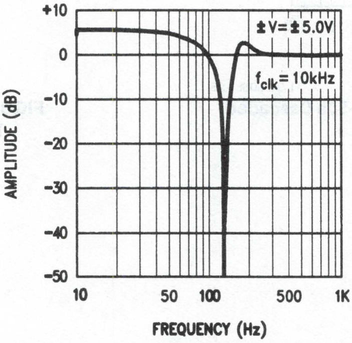
FIGURE 10b. Phase Response of Two Cascaded MF6-50s

Designing with the MF6 (Continued)


MF6
V_OS ADJ
7
6 TH ORDER BUTTERWORTH FILTER
8
FILTER IN
5
AGND
2
V02
14
INV2
1
NIN2
#2
OP-AMP
OP-AMP
#1
3
FILTER OUT
LEVEL SHIFT
TRI-STATE BUFFER
12
L.Sh
11
CLKR
5 V
0 V
fCLK
9
CLK IN
4
V01
13
INV 1
V+
V−
R3
R2
R1
SIGNAL INPUT
"NOTCH" FILTER OUTPUT

TL/H/5065-28

FIGURE 11a. "Notch" Filter



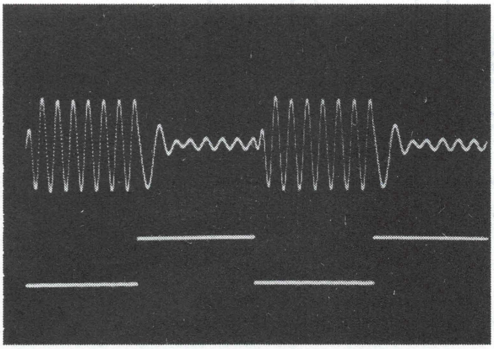
TL/H/5065-29

FIGURE 11b. MF6-50 "Notch" Filter Amplitude Response

2.4 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The MF6 will respond favorably to a sudden change in clock frequency. Distortion in the output signal occurs at the transition of the clock frequency and lasts approximately three cutoff frequency (f_c) cycles. As shown in *Figure 12,* if the control signal is low the MF6-50 has a 100 kHz clock making $f_c = 2$ kHz; when this signal goes high the clock frequency changes to 50 kHz yielding 1 kHz f_c.

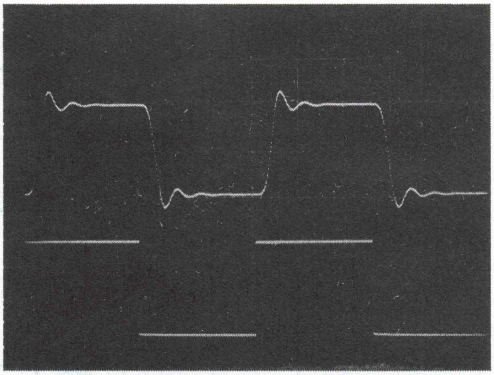
The transient response of the MF6 seen in *Figure 13* is also dependent on the f_c and thus the f_{CLK} applied to the filter. The MF6 responds as a classical sixth order Butterworth lowpass filter.



TL/H/5065-30

$f_{IN} = 1.5$ kHz (scope time base = 2 ms/div)

FIGURE 12. MF6-50 Abrupt Clock Frequency Change

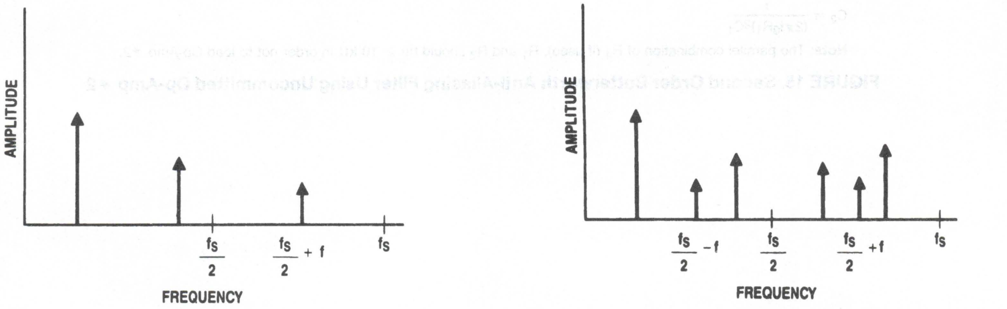


TL/H/5065-31

FIGURE 13. MF6-50 Step Input Response, Vertical = 2V/div., Horizontal = 1 ms/div., f_{CLK} = 100 kHz

2.5 ALIASING CONSIDERATIONS

Aliasing effects have to be taken into consideration when input signal frequencies exceed half the sampling rate. For the MF6 this equals half the clock frequency (f_{CLK}). When the input signal contains a component at a frequency higher than half the clock frequency, as in *Figure 14a,* that component will be "reflected" about $f_{CLK}/2$ into the frequency range *below* $f_{CLK}/2$ as in *Figure 14b.* If this component is within the passband of the filter and of large enough amplitude it can cause problems. Therefore if frequency components in the input signal exceed $f_{CLK}/2$ they must be attenuated before being applied to the MF6 input. The necessary amount of attenuation will vary depending on system requirements. In critical applications the signal components above $f_{CLK}/2$ will have to be attenuated at least to the filter's residual noise level. An example circuit is shown in *Figure 15* using one of the uncommitted Op-Amps available in the MF6.



TL/H/5065-37

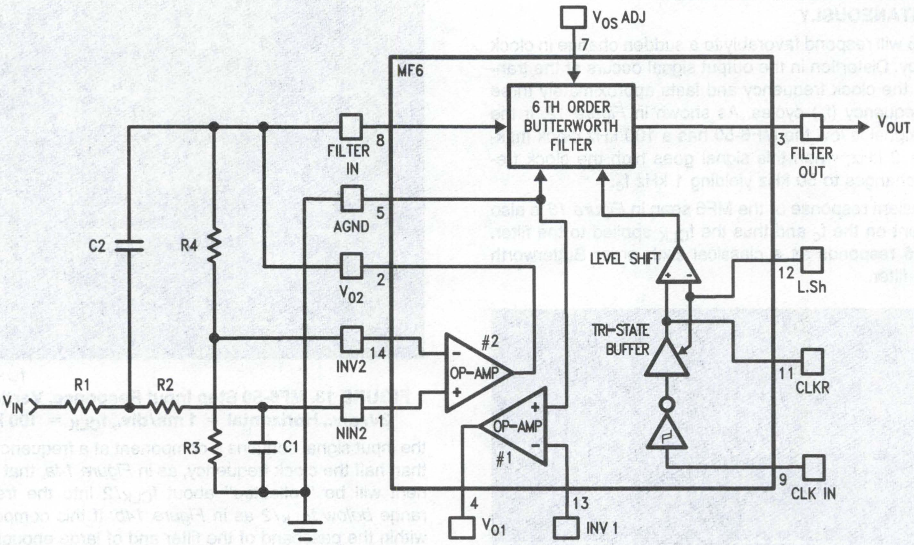
(a) Input Signal Spectrum

TL/H/5065-38

(b) Output Signal Spectrum. Note that the input signal at $f_s/2 + f$ causes an output signal to appear at $f_s/2 - f$.

Figure 14. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the MF6, $f_s = f_{CLK}$.

Designing with the MF6 (Continued)


V_OS ADJ
7
MF6
6 TH ORDER
BUTTERWORTH
FILTER
V_OUT
3
FILTER
OUT
8
FILTER
IN
5
AGND
C2
R4
LEVEL SHIFT
12
L.Sh
2
V_O2
TRI-STATE
BUFFER
14
INV2
#2
OP-AMP
11
CLKR
R1
R2
V_IN
1
NIN2
OP-AMP
R3
C1
#1
9
CLK IN
4
V_O1
13
INV 1

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$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

$H_0 = R_4/R_3$ ($H_0 = 1$ when R_3 and R_4 are omitted and V_{O2} is directly tied to INV2).

Design Procedure:

pick C_1

$$R_2 = \frac{1}{2QC_1\omega_0}$$

for a 2nd Order Butterworth Q = 0.707

$$R_2 = \frac{0.113}{C_1 f_0}$$

make $R_1 = R_2$

and

$$C_2 = \frac{1}{(2\pi f_0 R_1)^2 C_1}$$

Note: The parallel combination of R_4 (if used), R_1 and R_2 should be $\geq$ 10 kΩ in order not to load Op-Amp #2.

FIGURE 15. Second Order Butterworth Anti-Aliasing Filter Using Uncommitted Op-Amp #2

National Semiconductor Corporation

MF8 4th-Order Switched Capacitor Bandpass Filter

General Description

The MF8 consists of two second-order bandpass filter stages and an inverting operational amplifier. The two filter stages are identical and may be used as two tracking second-order bandpass filters, or cascaded to form a single fourth-order bandpass filter. The center frequency is controlled by an external clock for optimal accuracy, and may be set anywhere between 0.1 Hz and 20 kHz. The ratio of clock frequency to center frequency is programmable to 100:1 or 50:1. Two inputs are available for TTL or CMOS clock signals. The TTL input will accept logic levels referenced to either the negative power supply pin or the ground pin, allowing operation on single or split power supplies. The CMOS input is a Schmitt inverter which can be made to self-oscillate using an external resistor and capacitor.

By using the uncommitted amplifier and resistors for negative feedback, any all-pole (Butterworth, Chebyshev, etc.) filter can be formed. This requires only three resistors for a fourth-order bandpass filter. Q of the second-order stages may be programmed to any of 31 different values by the five "Q logic" pins. The available Q values span a range from 0.5 through 90. Overall filter bandwidth is programmed by connecting the appropriate Q logic pins to either V^+ or V^-. Filters with order higher than four can be built by cascading MF8s.

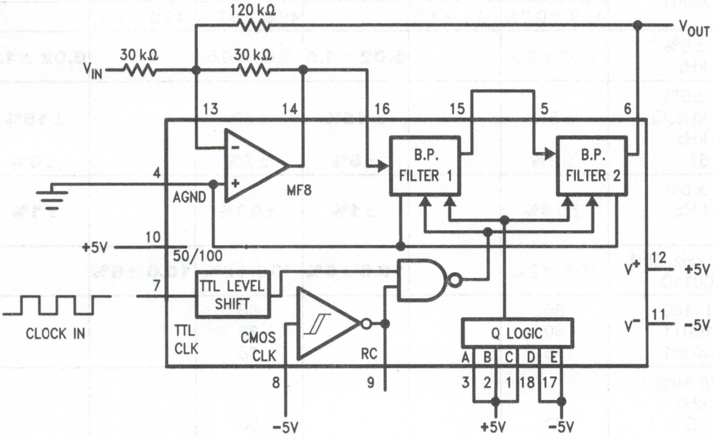
Features

- Center frequency set by external clock
- Q set by five-bit digital word
- Uncommitted inverting op amp
- 4th-order all-pole filters using only three external resistors
- Cascadable for higher-order filters
- Bandwidth, response characteristic, and center frequency independently programmable
- Separate TTL and CMOS clock inputs
- 18 pin 0.3″ wide package

Key Specifications

- Center frequency range 0.1 Hz to 20 kHz
- Q range 0.5 to 90
- Supply voltage range 9V to 14V (±4.5V to ±7V)
- Center frequency accuracy 1% over full temperature range

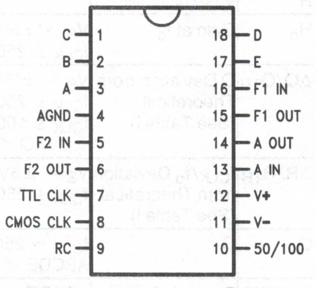
Typical Application & Connection Diagrams


120 kΩ
30 kΩ
30 kΩ
V_{IN}
V_{OUT}
13
14
16
15
5
6
4
AGND
MF8
B.P. FILTER 1
B.P. FILTER 2
+5V
10
50/100
7
TTL LEVEL SHIFT
CLOCK IN
TTL CLK
CMOS CLK
RC
8
9
-5V
Q LOGIC
A B C D E
3 2 1 18 17
+5V
-5V
V^+
12
+5V
V^-
11
-5V

TL/H/8694-1

Fourth-Order Butterworth Bandpass Filter

Dual-In-Line Package


C 1
B 2
A 3
AGND 4
F2 IN 5
F2 OUT 6
TTL CLK 7
CMOS CLK 8
RC 9
18 D
17 E
16 F1 IN
15 F1 OUT
14 A OUT
13 A IN
12 V+
11 V−
10 50/100

TL/H/8694-2

Top View

Order Number MF8CCJ or MF8CCN
See NS Package Number J18A or N18A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V_S = V^+ - V^-$)	−0.3V to +15V
Voltage at any Input (Note 2)	$V^- - 0.3V$ to $V^+ + 0.3V$
Input Current at any Input Pin (Note 2)	±1 mA
Output Short-Circuit Current (Note 7)	±1 mA
Power Dissipation (Note 3)	500 mW
Storage Temperature	−65°C to +150°C

Soldering Information:

J Package:	10 sec.	260°C
N Package:	10 sec.	300°C
SO Package:	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C

ESD rating is to be determined.

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
MF8CCN	$0°C \le T_A \le +70°C$
MF8CCJ	$-40°C \le T_A \le +85°C$
Supply Voltage ($V_S = V^+ - V^-$)	+9V to +14V
$f_{CLK} \times Q$ Range	
for $10\text{ Hz} \le f_{CLK} \le 250\text{ kHz}$	any Q
for $250\text{ kHz} \le f_{CLK} \le 1\text{ MHz}$	$f_{CLK} \times Q \le 5\text{ MHz}$

Filter Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V^- = -5V$, $C_{LOAD} = 50\text{ pF}$ and $R_{LOAD} = 50\text{ k}\Omega$ on filter output unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter (Notes 4, 5)	Conditions	MF8CCN			MF8CCJ			Units
			Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	
H_o	Gain at f_o	$f_{CLK} = 250\text{ kHz}$ 100:1 ABCDE = 11100	6.02 ±.05	6.02 ±0.2		6.02 ±0.05	6.02 ±0.2		dB
Q	Q		3.92 ±2%	3.92 ±6%		3.92 ±2%	3.92 ±6%		
R	f_{CLK}/f_o		99.2 ±0.3%	99.2 ±1%		99.2 ±0.3%	99.2 ±1%		
H_o	Gain at f_o	$f_{CLK} = 250\text{ kHz}$ 100:1 ABCDE = 10011	6.02 ±0.2	6.02 ±0.5		6.02 ±0.2	6.02 ±0.5		dB
Q	Q		15.5 ±3%	15.5 ±8%		15.5 ±3%	15.5 ±8%		
R	f_{CLK}/f_o		99.7 ±0.3%	99.7 ±1%		99.7 ±0.3%	99.7 ±1%		
H_o	Gain at f_o	$f_{CLK} = 250\text{ kHz}$ 50:1 ABCDE = 00001	5.85 ±0.4	5.85 ±1		5.85 ±0.4	5.85 ±1		dB
Q	Q		55 ±5%	55 ±10%		55 ±5%	55 ±10%		
R	f_{CLK}/f_o		49.9 ±0.2%	49.9 ±1%		49.9 ±0.2%	49.9 ±1%		
H_o	Gain at f_o	$V_S = \pm 5V \pm 5\%$ $f_{CLK} \le 250\text{ kHz}$	6.02 ±0.5		**6.02 ±1.5**	6.02 ±0.5		**6.02 ±1.5**	dB
$\Delta Q/Q_{TH}$	Q Deviation from Theoretical (See Table I)	$V_S = \pm 5V \pm 5\%$ $f_{CLK} \le 250\text{ kHz}, Q > 1$ $f_{CLK} \le 100\text{ kHz}, 1 < Q < 57$	±5% ±2%		**±15%** **±6%**	±5% ±2%		**±15%** **±6%**	
$\Delta R/R_{TH}$	f_{CLK}/f_o Deviation from Theoretical (See Table I)	$V_S = \pm 5V \pm 5\%$ $f_{CLK} \le 250\text{ kHz}$	±0.3%		**±1%**	±0.3%		**±1%**	
Q	Q	$f_{CLK} = 250\text{ kHz}$, 50:1 ABCDE = 00110	10.6 ±2%		**10.6 ±6%**	10.6 ±2%	**10.6 ±8%**		
	Dynamic Range (Note 6)	ABCDE = 11100 ABCDE = 10011 ABCDE = 00001	86 80 75			86 80 75			dB dB dB
	Clock Feedthrough	Filter and Op Amp $f_{CLK} \le 250\text{ kHz}$ $Q \le 1$ $Q > 1$	80 40			80 40			mV mV
I_S	Maximum Supply Current	$f_{CLK} = 250\text{ kHz}$, no loads on outputs	9	12	**12**	9	**13**		mA
V_{OS}	Maximum Filter Output Offset Voltage	$f_{CLK} = 250\text{ kHz}, Q = 4$ 50:1 100:1	±40 ±80	±120 ±240		±40 ±80	±120 ±240		mV mV
V_{OUT}	Minimum Filter Output Swing	$R_{LOAD} = 5\text{ k}\Omega$ (Note 6)	±4.1	±3.8	**±3.8**	±4.1	**±3.6**		V

Op Amp Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V^- = -5V$ and no load on the Op Amp output unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	MF8CCN Typical (Note 9)	MF8CCN Tested Limit (Note 10)	MF8CCN Design Limit (Note 11)	MF8CCJ Typical (Note 9)	MF8CCJ Tested Limit (Note 10)	MF8CCJ Design Limit (Note 11)	Units
V_{OS}	Maximum Input Offset Voltage		±8	±20		±8	±20		mV
I_B	Maximum Input Bias Current		10			10			pA
V_{OUT}	Minimum Output Voltage Swing	$R_{LOAD} = 5\ k\Omega$	±3.8	±3.5	±**3.4**	±3.8	±**3.1**		V
A_{VOL}	Open Loop Gain		80			80			dB
GBW	Gain Bandwidth Product		1.8			1.8			MHz
SR	Slew Rate		10			10			V/μs

Logic Input and Output Characteristics

The following specifications apply for $V^+ = +10V$ and $V^- = 0V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions	MF8CCN Typical (Note 9)	MF8CCN Tested Limit (Note 10	MF8CCN Design Limit (Note 11)	MF8CCJ Typical (Note 9)	MF8CCJ Tested Limit (Note 10)	MF8CCJ Design Limit (Note 11)	Units
V_T^+	Positive Threshold Voltage on pin 8	Min	$V_S = V^+ - V^-$ referred to $V^- = 0V$ (Note 8)	$0.7V_S$	$0.58V_S$		$0.7V_S$	$0.58V_S$		V
		Max		$0.7V_S$	$0.89V_S$		$0.7V_S$	$0.89V_S$		V
V_T^-	Negative Threshold Voltage on pin 8	Min	$V_S = V^+ - V^-$ referred to $V^- = 0V$ (Note 8)	$0.35V_S$	$0.11V_S$		$0.35V_S$	$0.11V_S$		V
		Max		$0.35V_S$	$0.47V_S$		$0.35V_S$	$0.47V_S$		V
V_{OH}	Output Voltage on pin 9 (Note 12)	Min High	$I_O = -10\ \mu A$		9.0	**9.0**		**9.0**		V
V_{OL}		Max Low	$I_O = +10\ \mu A$		1.0	**1.0**		**1.0**		V
I_{OH}	Output Current on pin 9	Min Source	Pin 9 tied to V^-	6.0	3.0		6.0	3.0		mA
I_{OL}		Min Sink	Pin 9 tied to V^+	5.0	2.5		5.0	2.5		mA
V_{IH}	Input Voltage on pins: 1, 2, 3, 10, 17, & 18 (Note 12)	Min High		7.0		**9.0**	7.0	**9.0**		V
V_{IL}		Max Low		3.0		**1.0**	3.0	**1.0**		V
I_{IN}	Input Current on pins: 1, 2, 3, 7, 8, 10, 17, & 18				10	**10**		**10**		μA
V_{IH}	Input Voltage on pin 7	Min High	$V^+ = +10V$, $V^- = 0V$ or $V^+ = +5V$, $V^- = -5V$		2.0	**2.0**		**2.0**		V
V_{IL}		Max Low			0.8	**0.8**		**0.8**		V

Note 1: Absolute Maximum Raings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: When the applied voltage at any pin falls outside the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$), the absolute value of current at that pin should be limited to 1 mA or less.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, Θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF8CCN when board mounted is 50°C/W. For the MF8CCJ, this number increases to 65°C/W.

Note 4: The center frequency of each 2nd-order filter section is defined as the frequency where the phase shift through the filter is zero.

Note 5: Q is defined as the measured center frequency divided by the measured bandwidth, where the bandwidth is the difference between the two frequencies where the gain is 3 dB less than the gain measured at the center frequency.

Note 6: Dynamic range is defined as the ratio of the tested minimum output swing of 2.75 Vrms (±3.8V peak-to-peak) to the wideband noise over a 20 kHz bandwidth. For Qs of 1 or less the dynamic range and output swing will degrade because the gain at an internal node is 2/Q. Keeping the input signal level below 1.23xQ Vrms will avoid distortion in this case.

Note 7: If it is possible for a signal output (pin 6, 14, or 15) to be shorted to V+, V− or ground, add a series resistor to limit output current.

Note 8: If V− is anything other than 0V then the value of V− should be added to the values given in the table. For example for $V^+ = +5V$ and $V^- = -5V$ the typical $V_T^+ = 0.7\ (10V) + (-5V) = +2V$.

Note 9: Typicals are at 25°C and represent the most likely parametric norm.

Note 10: Tested Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Design Limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 12: These logic levels have been referenced to V−. The logic levels will shift accordingly for split supplies.

Pin Descriptions

Q Logic Inputs A, B, C, D, E (3, 2, 1, 18, 17):	These inputs program the Qs of the two 2nd-order bandpass filter stages. Logic "1" is V+ and logic "0" is V−.
AGND (4):	This is the analog and digital ground pin and should be connected to the system ground for split supply operation or biased to mid-supply for single supply operation. For best filter performance, the ground line should be "clean".
V+ (12), V− (11):	These are the positive and negative power supply inputs. Decoupling the power supply pins with 0.1 μF or larger capacitors is highly recommended.
F1 IN (16), F2 IN (5):	These are the inputs to the bandpass filter stages. To minimize gain error the source impedance should be less than 2 kΩ. Input signals should be referenced to AGND.
F1 OUT (15), F2 OUT (6):	These are the outputs of the bandpass filter stages.
A IN (13):	This is the inverting input to the uncommitted operational amplifier. The non-inverting input is internally connected to AGND.
A OUT (14):	This is the output of the uncommitted operational amplifier.
50/100 (10):	This pin sets the ratio of the clock frequency to the bandpass center frequency. Connecting this pin to V+ sets the ratio to 100:1. Connecting it to V− sets the ratio to 50:1.
TTL CLK (7):	This is the TTL-level clock input pin. There are two logic threshold levels, so the MF8 can be operated on either single-ended or split supplies with the logic input referred to either V− or AGND. When this pin is not used (or when CMOS logic levels are used), it should be connected to either V+ or V−.
CMOS CLK (8):	This pin is the input to a CMOS Schmitt inverter. Clock signals with CMOS logic levels may be applied to this input. If the TTL input is used this pin should be connected to V−.
RC (9):	This pin allows the MF8 to generate its own clock signal. To do this, connect an external resistor between the RC pin and the CMOS Clock input, and an external capacitor from the CMOS Clock input to AGND. The TTL Clock input should be connected to V− or V+. When the MF8 is driven from an external clock, the RC pin should be left open.

1.0 Application Information

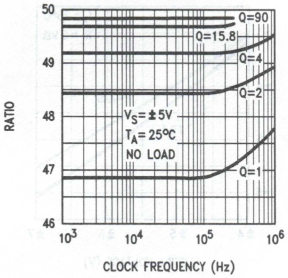
1.1 INTRODUCTION

A simplified block diagram for the MF8 is shown in *Figure 1*. The analog signal path components are two identical 2nd-order bandpass filters and an operational amplifier. Each filter has a fixed voltage gain of 2. The filters' cutoff frequency is proportional to the clock frequency, which may be applied to the chip from an external source or generated internally with the aid of an external resistor and capacitor. The proportionality constant f_{CLK}/f_0 can be set to either 50 or 100 depending on the logic level on pin 10. The "Q" of the two filters can have any of 31 values ranging from 0.5 to 90 and is set by the logic levels on pins 1, 2, 3, 17, and 18. Table I shows the available values of Q and the logic levels required to obtain them. The operational amplifier's non-inverting input is internally grounded, so it may be used only for inverting applications.

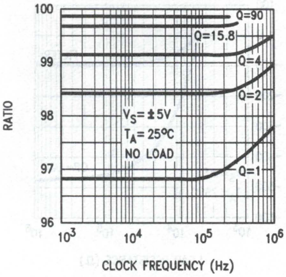
The components in the analog signal path can be interconnected in several ways, three of which are illustrated in *Figures 2a, 2b* and *2c*. The two second-order filter sections can be used as separate filters whose center frequencies track very closely as in *Figure 2a*. Each filter section has a high input impedance and low output impedance. The op amp may be used for gain scaling or other inverting functions. If sharper cutoff slopes are desired, the two filter sections may be cascaded as in *Figure 2b*. Again, the op amp is uncommitted. The circuit in *Figure 2c* uses both filter sections with the op amp and three resistors to build a "multiple feedback loop" filter. This configuration offers the greatest flexibility for fourth-order bandpass designs. Virtually any fourth-order all pole response shape (Butterworth, Chebyshev) can be obtained with a wide range of bandwidths, simply by proper choice of resistor values and Q. The three connection schemes in *Figure 2* will be discussed in more detail in Sections 1.4 and 1.5.

Typical Performance Characteristics

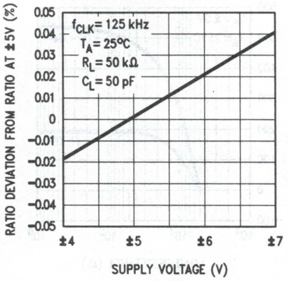
f_{CLK}/f_o Ratio vs Clock Frequency—50:1 Mode



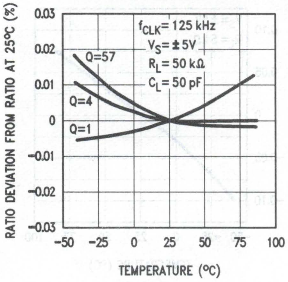
f_{CLK}/f_o Ratio vs Clock Frequency—100:1 Mode



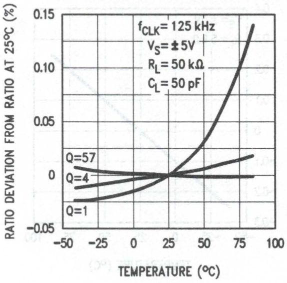
f_{CLK}/f_o Ratio vs Supply Voltage—50:1 and 100:1 Mode



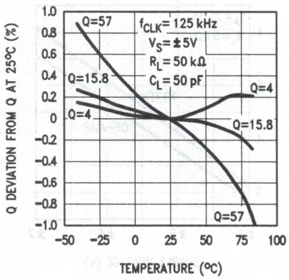
f_{CLK}/f_o Ratio vs Temperature—100:1 Mode



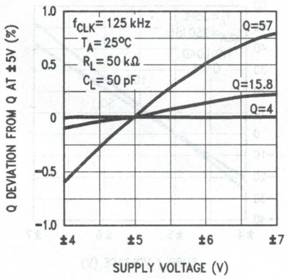
f_{CLK}/f_o Ratio vs Temperature—50:1 Mode



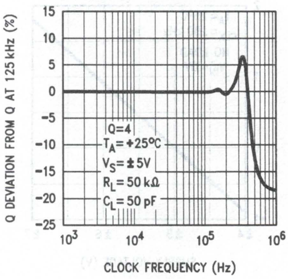
Q vs Temperature—50:1 and 100:1



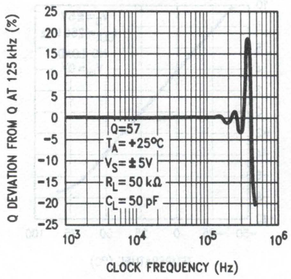
Q vs Supply Voltage—50:1 and 100:1



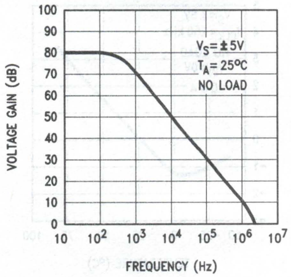
Q vs Clock Frequency—50:1 and 100:1



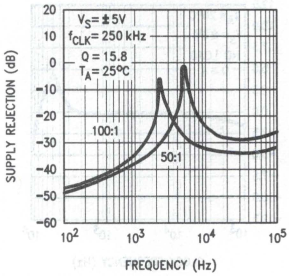
Q vs Clock Frequency—50:1 and 100:1



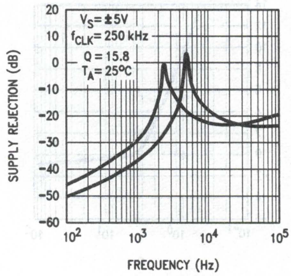
Op Amp—Open Loop Frequency Response



Positive Power Supply Rejection



Negative Power Supply Rejection



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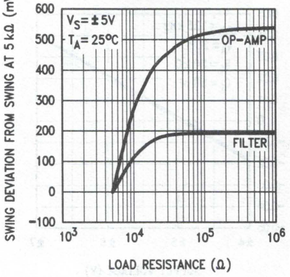
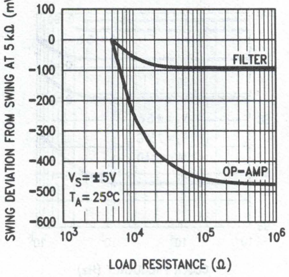
Typical Performance Characteristics (Continued)

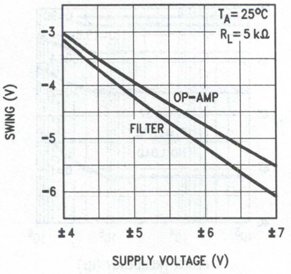
Positive Swing vs Load Resistance



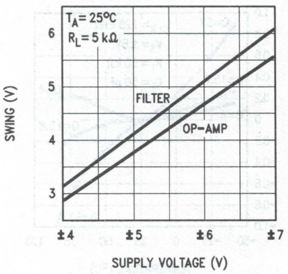
Negative Swing vs Load Resistance



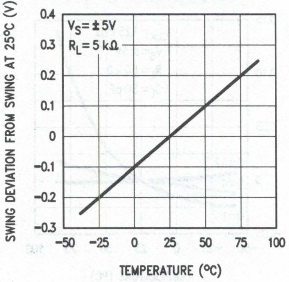
Negative Swing vs Supply Voltage



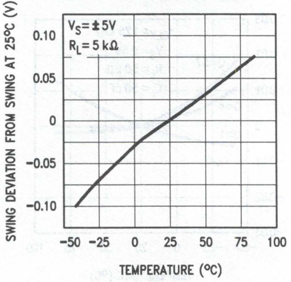
Positive Swing vs Supply Voltage



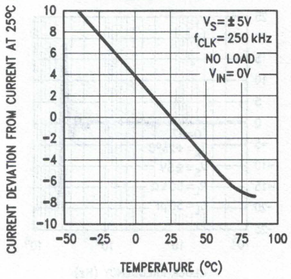
Negative Swing vs Temperature (Filter and Op Amp)



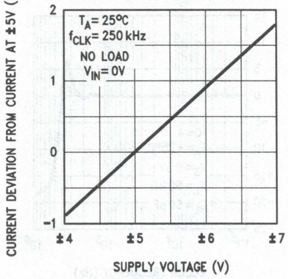
Positive Swing vs Temperature (Filter and Op Amp)



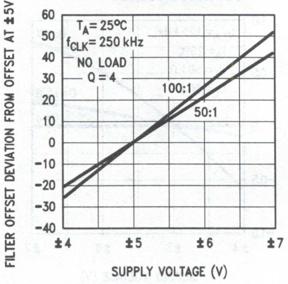
Supply Current vs Temperature



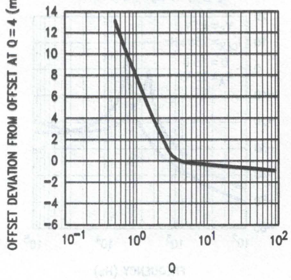
Supply Current vs Supply Voltage



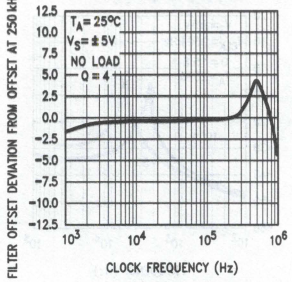
Filter Offset Voltage vs Supply Voltage



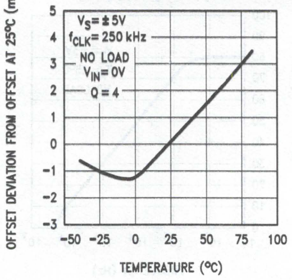
Filter Offset Voltage vs Q—50:1 and 100:1



Filter Offset Voltage vs Clock Frequency—50:1 and 100:1



Filter Offset Voltage vs Temperature—50:1 and 100:1



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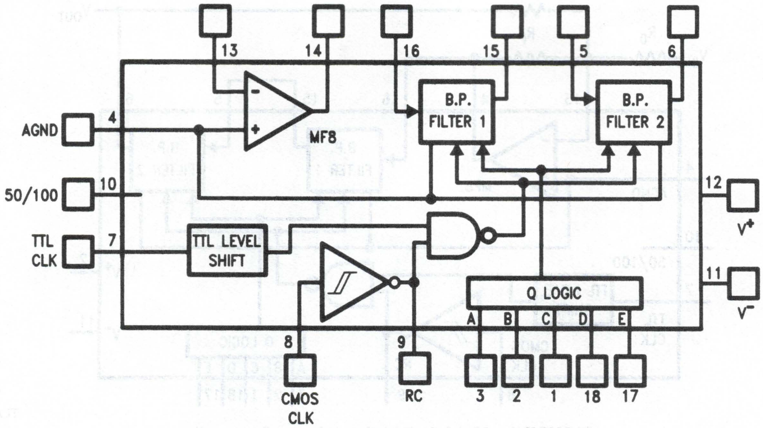
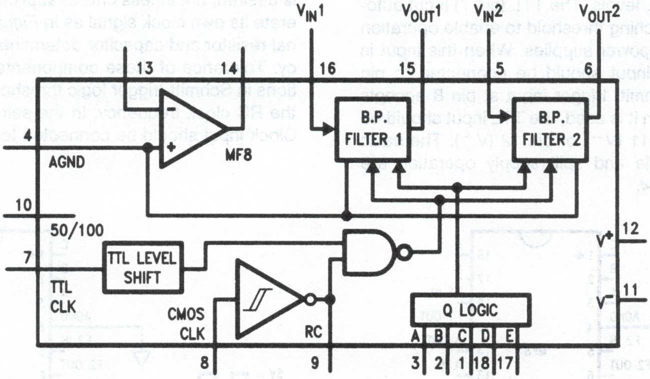
1.0 Application Information (Continued)


13
14
16
15
5
6
AGND
4
50/100
10
TTL
CLK
7
B.P.
FILTER 1
B.P.
FILTER 2
MF8
TTL LEVEL
SHIFT
Q LOGIC
A
B
C
D
E
12
V+
11
V−
8
9
CMOS
CLK
RC
3
2
1
18
17

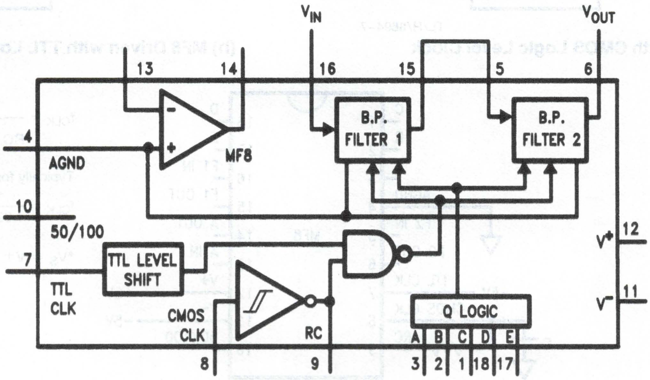
TL/H/8694-3

FIGURE 1. Simplified Block Diagram of the MF8


$V_{IN}1$
$V_{OUT}1$
$V_{IN}2$
$V_{OUT}2$
13
14
16
15
5
6
4
AGND
B.P.
FILTER 1
B.P.
FILTER 2
MF8
10
50/100
7
TTL LEVEL
SHIFT
TTL
CLK
CMOS
CLK
RC
Q LOGIC
A
B
C
D
E
3
2
1
18
17
12
V+
11
V−
8
9

TL/H/8694-4

FIGURE 2a. Separate Second-Order "Tracking" Filters


V_{IN}
V_{OUT}
13
14
16
15
5
6
4
AGND
B.P.
FILTER 1
B.P.
FILTER 2
MF8
10
50/100
7
TTL LEVEL
SHIFT
TTL
CLK
CMOS
CLK
RC
Q LOGIC
A
B
C
D
E
3
2
1
18
17
12
V+
11
V−
8
9

TL/H/8694-5

FIGURE 2b. Fourth-Order Bandpass Made by Cascading Two Second-Order Stages

1.0 Application Information (Continued)

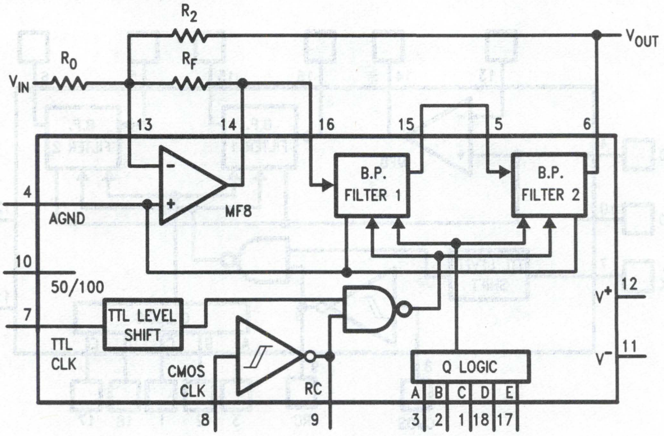

R2
VOUT
R0
RF
VIN
13
14
16
15
5
6
B.P. FILTER 1
B.P. FILTER 2
4
AGND
MF8
10
50/100
7
TTL LEVEL SHIFT
TTL CLK
CMOS CLK
RC
8
9
Q LOGIC
A B C D E
3 2 1 18 17
12
V+
11
V−

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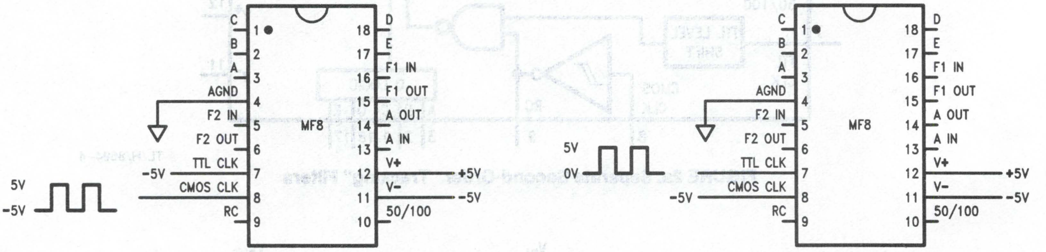
FIGURE 2c. Multiple Feedback Loop Connection

1.2 CLOCKS

The MF8 has two clock input pins, one for CMOS logic levels and the other for TTL levels. The TTL (pin 7) input automatically adjusts its switching threshold to enable operation on either single or split power supplies. When this input is used, the CMOS logic input should be connected to pin 11(V−). The CMOS Schmitt trigger input at pin 8 accepts CMOS logic levels. When it is used, the TTL input should be connected to either pin 11 (V−) or pin 12 (V+). The basic clock hookups for single and split supply operation are shown in *Figures 3* and *4*.

Clock signals derived from a crystal-controlled oscillator are recommended when maximum center frequency accuracy is desired, but in less critical applications the MF8 can generate its own clock signal as in *Figures 3c* and *4c*. An external resistor and capacitor determine the oscillation frequency. Tolerance of these components and part-to-part variations in Schmitt-trigger logic thresholds limit the accuracy of the RC clock frequency. In the self-clocked mode the TTL Clock input should be connected to either pin 11 or pin 12.

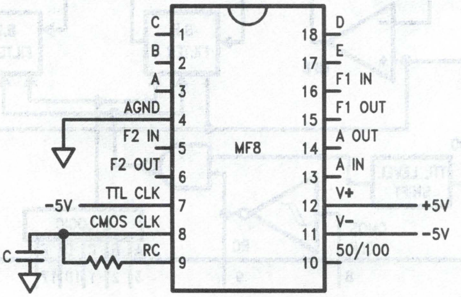

C
B
A
AGND
F2 IN
F2 OUT
TTL CLK
CMOS CLK
RC
1
2
3
4
5
6
7
8
9
MF8
18
17
16
15
14
13
12
11
10
D
E
F1 IN
F1 OUT
A OUT
A IN
V+
V−
50/100
+5V
−5V
5V
−5V
0V

TL/H/8694-7

(a) MF8 Driven with CMOS Logic Level Clock

TL/H/8694-8

(b) MF8 Driven with TTL Logic Level Clock


C
B
A
AGND
F2 IN
F2 OUT
TTL CLK
CMOS CLK
RC
1
2
3
4
5
6
7
8
9
MF8
18
17
16
15
14
13
12
11
10
D
E
F1 IN
F1 OUT
A OUT
A IN
V+
V−
50/100
−5V
+5V
−5V

$$f_{CLK} = \frac{1}{RC \ln \left| \left(\frac{V_S - V_{T-}}{V_S - V_{T+}} \right) \left(\frac{V_{T+}}{V_{T-}} \right) \right|}$$

Typically for $V_S{}^* = 10V$

$$f_{CLK} \cong \frac{1}{1.69\,RC}$$

$^*V_S = V^+ - V^-$

TL/H/8694-9

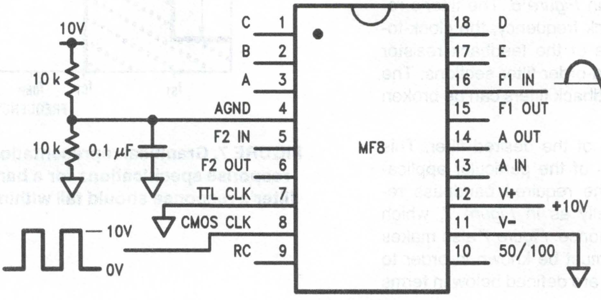
(c) MF8 Driven with Schmitt Trigger Oscillator

FIGURE 3. Dual Supply Operation

1.0 Application Information (Continued)

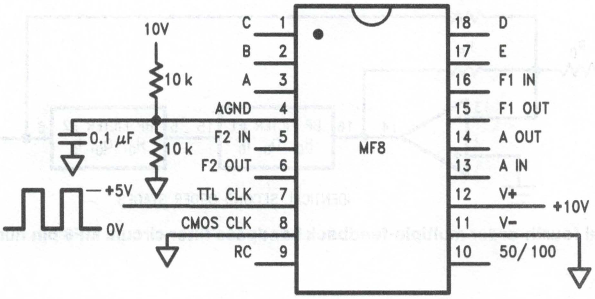
1.3 POWER SUPPLIES AND ANALOG GROUND

The MF8 can be operated from single or dual-polarity power supplies. For dual-supply operation, the analog ground (pin 4) should be connected to system ground. When single supplies are used, pin 4 should be biased to V+/2 as in *Figures 3* and *4*. The input signal should either be capacitively coupled to the filter input or biased to V+/2. It is strongly recommended that each power supply pin be bypassed to ground with at least a 0.1 μF ceramic capacitor. In single supply applications, with V− connected to ground, V+ and AGND should be bypassed to system ground.


10V
10 k
10 k
0.1 μF
10V
0V
C 1
B 2
A 3
AGND 4
F2 IN 5
F2 OUT 6
TTL CLK 7
CMOS CLK 8
RC 9
MF8
18 D
17 E
16 F1 IN
15 F1 OUT
14 A OUT
13 A IN
12 V+
11 V−
10 50/100
5V DC
+10V

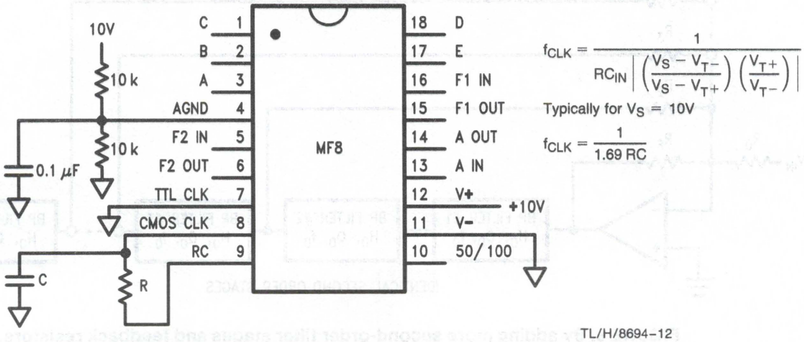
TL/H/8694-10

(a) MF8 Driven with CMOS Logic Level Clock


10V
10 k
0.1 μF
10 k
+5V
0V
C 1
B 2
A 3
AGND 4
F2 IN 5
F2 OUT 6
TTL CLK 7
CMOS CLK 8
RC 9
MF8
18 D
17 E
16 F1 IN
15 F1 OUT
14 A OUT
13 A IN
12 V+
11 V−
10 50/100
+10V

TL/H/8694-11

(b) MF8 Driven with TTL Logic Clock


10V
10 k
10 k
0.1 μF
C
R
C 1
B 2
A 3
AGND 4
F2 IN 5
F2 OUT 6
TTL CLK 7
CMOS CLK 8
RC 9
MF8
18 D
17 E
16 F1 IN
15 F1 OUT
14 A OUT
13 A IN
12 V+
11 V−
10 50/100
+10V

$$f_{CLK} = \frac{1}{RC_{IN}\left|\left(\frac{V_S - V_{T-}}{V_S - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right|}$$

Typically for $V_S = 10V$

$$f_{CLK} = \frac{1}{1.69\ RC}$$

TL/H/8694-12

(c) MF8 Driven with the Schmitt Trigger Oscillator

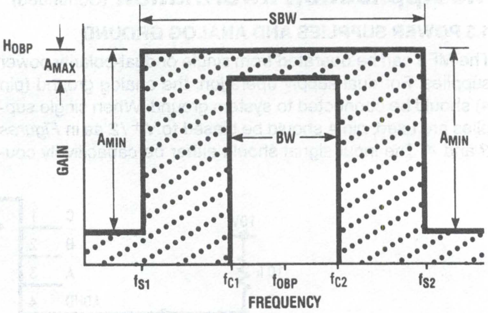
FIGURE 4. Single supply operation. The AGND pin must be biased to mid-supply. The input signal should be dc biased to mid-supply or capacitor-coupled to the input pin.

1.0 Application Information (Continued)

1.4 MULTIPLE FEEDBACK LOOP CONFIGURATION

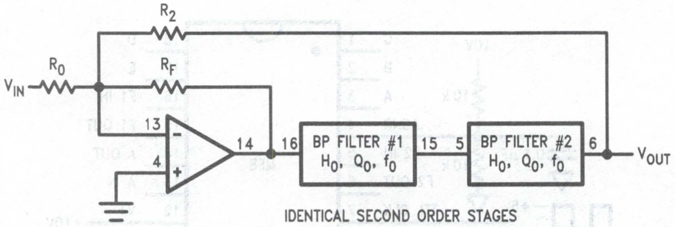
The multi-loop approach to building bandpass filters is highly flexible and stable, yet uses few external components. *Figure 5* shows the MF8's internal operational amplifier and two second-order filter stages with three external resistors in a fourth-order multiple feedback configuration. Higher-order filters may be built by adding more second-order sections and feedback resistors as in *Figure 6*. The filter's response is determined by the clock frequency, the clock-to-center-frequency ratio, the ratios of the feedback resistor values, and the Qs of the second-order filter sections. The design procedure for multiple feedback filters can be broken down into a few simple steps:

1) Determine the characteristics of the desired filter. This will depend on the requirements of the particular application. For a given application, the required bandpass response can be shown graphically as in *Figure 7*, which shows the limits for the filter response. *Figure 7* also makes use of several parameters that must be known in order to design a filter. These parameters are defined below in terms of *Figure 7*.



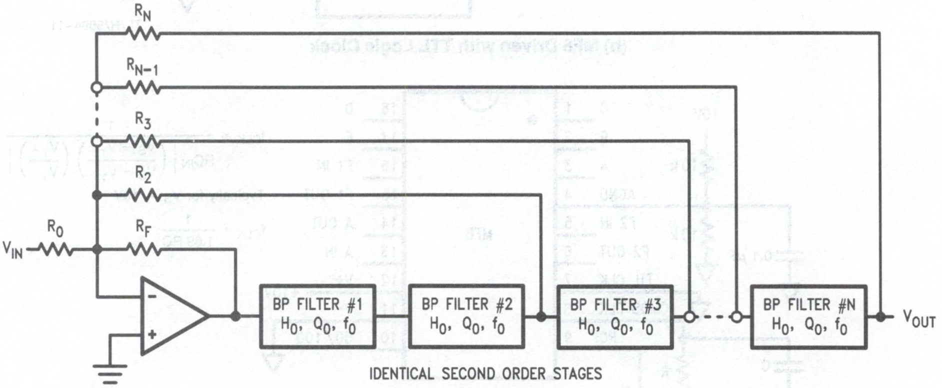
TL/H/8694-15

FIGURE 7. Graphical representation of the amplitude response specifications for a bandpass filter. The filter's response should fall within the shaded area.


R_2
R_0
R_F
V_{IN}
13
4
14
16
BP FILTER #1
H_0, Q_0, f_0
15
5
BP FILTER #2
H_0, Q_0, f_0
6
V_{OUT}
IDENTICAL SECOND ORDER STAGES

TL/H/8694-13

FIGURE 5. General fourth-order multiple-feedback bandpass filter circuit. MF8 pin numbers are shown.


R_N
R_{N-1}
R_3
R_2
R_0
R_F
V_{IN}
BP FILTER #1
H_0, Q_0, f_0
BP FILTER #2
H_0, Q_0, f_0
BP FILTER #3
H_0, Q_0, f_0
BP FILTER #N
H_0, Q_0, f_0
V_{OUT}
IDENTICAL SECOND ORDER STAGES

TL/H/8694-14

FIGURE 6. By adding more second-order filter stages and feedback resistors, higher order multiple-feedback filters may be built.

1.0 Application Information (Continued)

f_{C1} and f_{C2}: The filter's lower and upper cutoff frequencies. These define the filter's passband.

f_{S1} and f_{S2}: The boundaries of the filter's stopband.

BW: The filter's bandwidth. $BW = f_{C2} - f_{C1}$.

SBW: The width of the filter's stopband. $SBW = f_{S2} - f_{S1}$.

f_0: The center frequency of the filter. f_0 is equal to the geometric mean of f_{C1} and f_{C2}: $f_0 = \sqrt{f_{C1}f_{C2}}$. f_0 is also equal to the geometric mean of f_{S1} and f_{S2}.

H_{OBP}: The nominal passband gain of the bandpass filter. This is normally taken to be the gain at f_0.

f_0/BW: The ratio of the center frequency to the bandwidth. For second-order filters, this quantity is also known as "Q".

SBW/BW: The ratio of stopband width to bandwidth. This quantity is also called "Omega" and may be represented by the symbol "Ω".

A_{max}: The maximum allowable gain variation within the filter passband. This will depend on the system requirements, but typically ranges from a fraction of a dB to 3 dB.

A_{min}: The minimum allowable attenuation in the stopband. Again, the required value will depend on system constraints.

2). Choose a Butterworth or Chebyshev response characteristic. Butterworth bandpass filters are monotonic on either side of the center frequency, while Chebyshev filters will have "ripple" in the passband, but generally faster attenuation outside the passband. Chebyshev filters are specified according to the amount of ripple (in dB) within the passband.

3) Determine the filter order necessary to meet the response requirements defined above. This may be done with the aid of the nomographs in *Figures 8* and *9* for Butterworth and Chebyshev filters. To use the nomographs, draw a line through the desired values on the A_{MAX}/A_{MIN} scales to the left side of the graph. Draw a horizontal line to the right of this point and mark its intersection with the vertical line corresponding to the required ratio SBW/BW. The required filter order will be equal to the number of the curve falling on or just above the intersection of the two lines. This is illustrated in *Figure 10* for a Chebyshev filter with 1 dB ripple, 30 dB minimum attenuation in the stopband, and SBW/BW = 3. From the *Figure,* the required filter order is 6.

4) The design tables in section 2.0 can now be used to find the component values that will yield the desired response for filters of order 4 through 12. The "K_n" give the ratios of resistors "R_n" to R_F, and K_Q is Q divided by f_0/BW.

As an example of the Tables' use, consider a fourth-order Chebyshev filter with 0.5 dB ripple and $f_0/BW = 6$. Begin by choosing a convenient value for R_F, such as 100 kΩ. From the "0.5 dB Chebyshev" filter table, $K_0 = R_0/R_F = 1.3405$. This gives $R_0 = R_F \times 1.345 = 134.05k$. In a similar manner, R_2 is found to equal 201.61k. Q is found using the column labeled K_Q. This gives $Q = K_Q \times f_0/BW = 8.4174$. Table I shows the available Q values; the nearest value is 8.5, which is programmed by tying pins 1, 2, 3, and 18 to V^+ and pin 17 to V^-.

Note that the resistor values obtained from the tables are normalized for center frequency gain $H_{OBP} = 1$. For different gains, simply divide R_0 by the desired gain.

5) Choose the clock-to-center-frequency ratio. This will nominally be 100:1 when pin 10 is connected to pin 12(V^+) and 50:1 when pin 10 is connected to pin 11(V^-). 100:1 generally gives a response curve nearer the ideal and fewer (if any) problems with aliasing, while 50:1 allows operation over the highest octave of center frequencies (10 kHz to 20 kHz). Supply the MF8 with a clock signal of the appropriate frequency to either the TTL or CMOS input, depending on the available clock logic levels.

TABLE I. Q and Clock-to-Center-Frequency Ratio Versus Logic Levels on "Q-set" Pins

	50:1 mode		100:1 mode	
ABCDE	**F_{CLK}/F_o**	**Q**	**F_{CLK}/F_o**	**Q**
10000	43.7	0.45	94.0	0.47
11000	45.8	0.71	95.8	0.73
01000	46.8	0.96	96.8	0.98
10100	48.4	2.0	98.4	2.0
00100	48.7	2.5	98.7	2.5
01100	48.9	3.0	98.9	3.0
11100	49.2	4.0	99.2	4.0
01010	49.3	5.0	99.3	5.0
10010	49.4	5.7	99.4	5.7
10110	49.4	6.4	99.4	6.4
00010	49.5	7.6	99.5	7.6
11110	49.6	8.5	99.6	8.5
00110	49.6	10.6	99.6	10.6
11001	49.6	11.7	99.6	11.7
11010	49.7	12.5	99.7	12.5
11101	49.7	13.6	99.7	13.6
01001	49.7	14.7	99.7	14.7
10011	49.7	15.8	99.7	15.8
10101	49.7	16.5	99.7	16.5
01110	49.7	17	99.7	17
10001	49.8	19	99.8	19
10111	49.8	22	99.8	22
11011	49.8	27	99.8	27
11111	49.8	30	99.8	30
00101	49.8	33	99.8	33
01011	49.8	40	99.8	40
00111	49.8	44	99.8	44
00001	49.9	57	99.9	57
01101	49.9	68	99.9	68
00011	49.9	79	99.9	79
01111	49.9	90	99.9	90

1.0 Application Information (Continued)

Higher-order filters are designed in a similar manner. An eighth-order Chebyshev with 0.1 dB ripple, center frequency equal to 1 kHz, and 100 Hz bandwidth, for example, could be built as in *Figure 11* with the following component values:

R_0 = 79.86k
R_F = 100k
R_2 = 57.82k
R_3 = 188.08k
R_4 = 203.42k

Pins 1, 3, 17 and 18 high, pin 2 low. For 100:1 clock-to-center-frequency ratio, pin 10 is tied to V^+ and the clock frequency is 100 kHz. For 50:1 clock-to-center-frequency ratio, pin 10 is tied to V^- and the clock frequency is 50 kHz.

When building filters of order 4 or higher, best performance will always be realized when the filter blocks are cascaded in numerical order: Filter 1 (pins 16 and 15) should always precede Filter 2 (pins 5 and 6). If a second MF8 is used, Filter 2 of the first MF8 should precede Filter 1 of the second MF8, and so on.

Dynamic Considerations

Some filter response characteristics will result in high gain at certain internal nodes, particularly at the op amp output. This can cause clipping in intermediate stages even when no clipping is evident at the filter output. The consequences are significant distortion and degradation of the overall transfer function. The likelihood of clipping at the op amp output becomes greater as R_F/R_0 increases. As the design tables show, R_F/R_0 increases with increasing filter order and increasing ripple. It is good practice to keep out-of-band input signal levels small enough that the first stage can't overload.

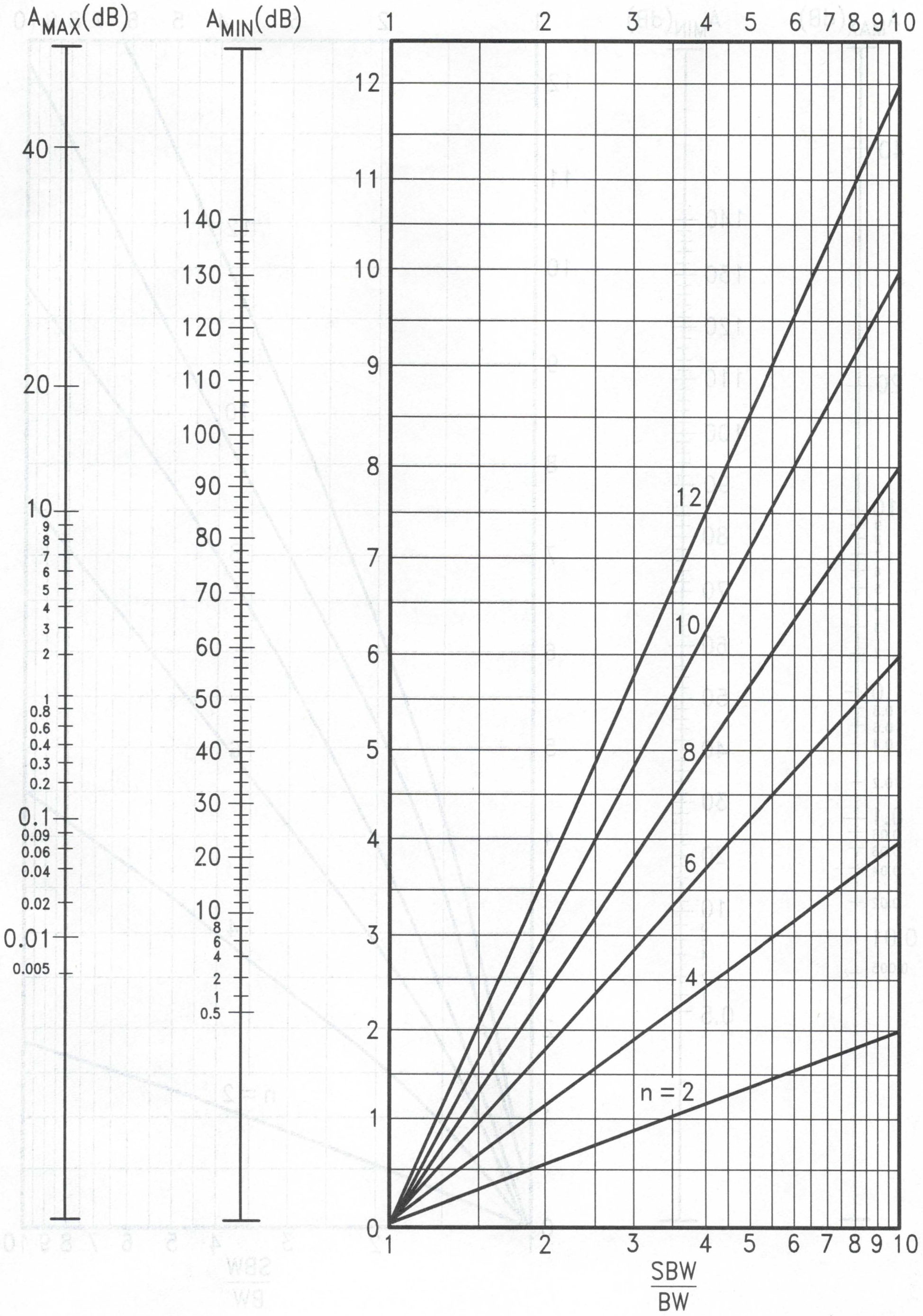


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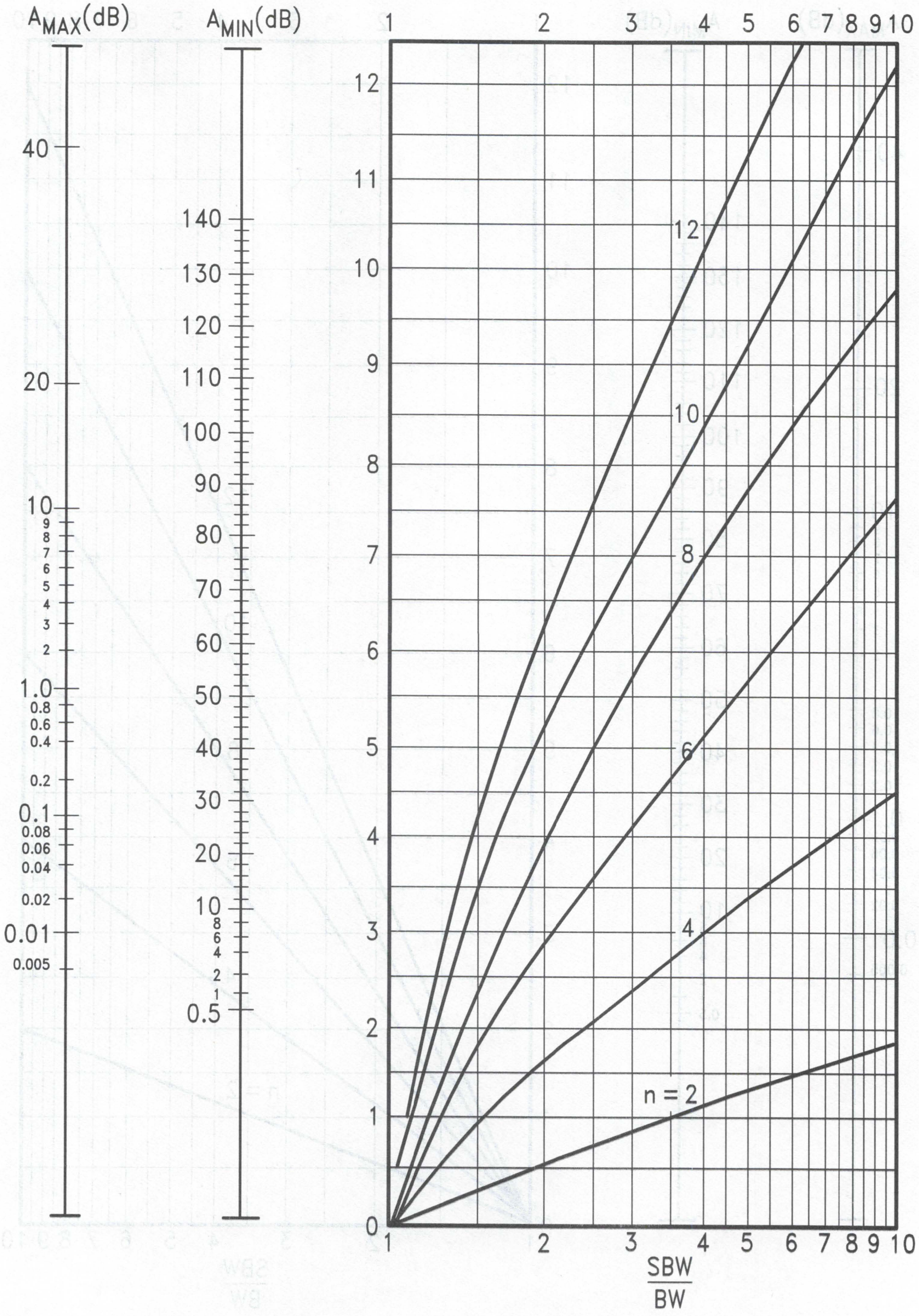
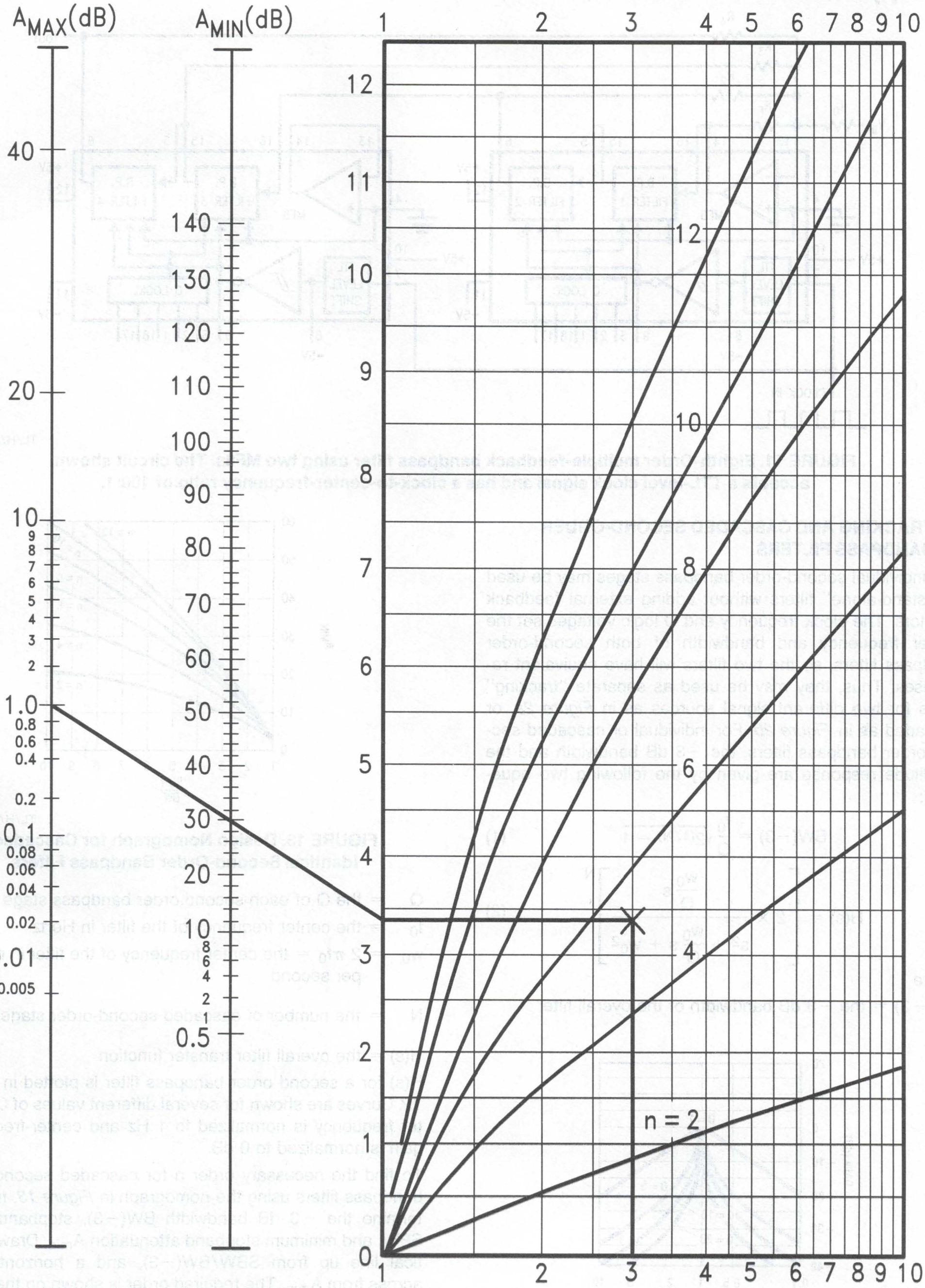
FIGURE 8. Butterworth Bandpass Filter Design Nomograph



TL/H/8694-17

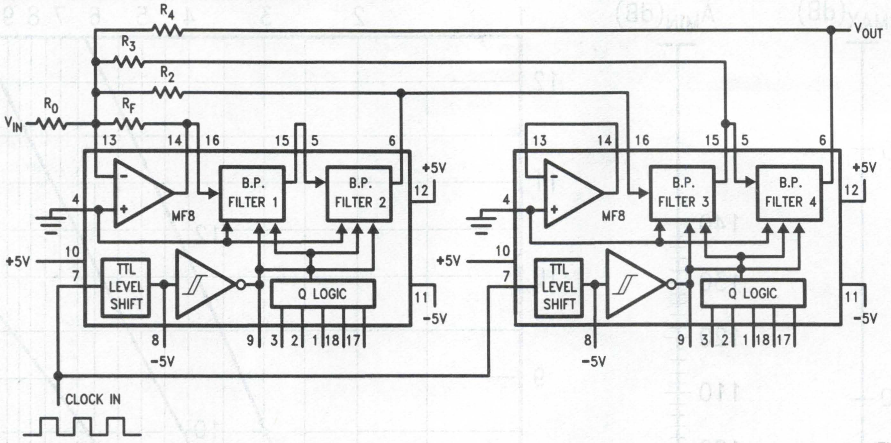
FIGURE 9. Chebyshev Bandpass Filter Design Nomograph



TL/H/8694-18

FIGURE 10. Example of Chebyshev Bandpass Nomograph Use.
A_{max} = 1 dB, A_{min} = 30 dB, and $\frac{SBW}{BW}$ = 3, resulting in n = 6.

1.0 Application Information (Continued)



TL/H/8694-19

FIGURE 11. Eighth-Order multiple-feedback bandpass filter using two MF8s. The circuit shown accepts a TTL-level clock signal and has a clock-to-center-frequency ratio of 100:1.

1.5 TRACKING AND CASCADED SECOND-ORDER BANDPASS FILTERS

The individual second-order bandpass stages may be used as "stand-alone" filters without adding external feedback resistors. The clock frequency and Q logic voltages set the center frequency and bandwidth of both second-order bandpass filters, so the two filters will have equivalent responses. Thus, they may be used as separate "tracking" filters for two different signal sources as in *Figure 2a*, or cascaded as in *Figure 2b*. For individual or cascaded second-order bandpass filters, the −3 dB bandwidth and the amplitude response are given by the following two equations:

$$BW(-3) = \frac{f_0}{Q}\sqrt{2^{(1/N)} - 1} \qquad (1)$$

$$H(s) = \left[2 \times \frac{\frac{w_0}{Q}s}{s^2 + \frac{w_0}{Q}s + w_0^2} \right]^N \qquad (2)$$

where

BW(−3) = the −3 dB bandwidth of the overall filter

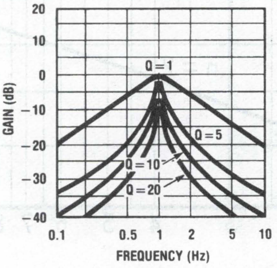
Q = the Q of each second order bandpass stage

f_0 = the center frequency of the filter in Hertz

w_0 = $2\pi f_0$ = the center frequency of the filter in radians per second

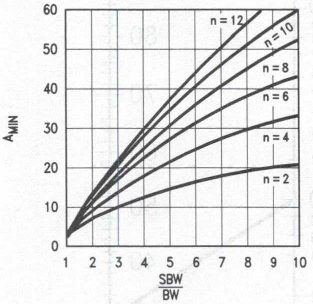
N = the number of cascaded second-order stages = $\frac{n}{2}$

H(s) = the overall filter transfer function



TL/H/8694-20

FIGURE 12. H(s) For second-order bandpass filters with various values of Q. H_0 normalized in each case to 0 dB.



TL/H/8694-21

FIGURE 13. Design Nomograph for Cascaded Identical Second-Order Bandpass Filters

H(s) for a second order bandpass filter is plotted in *Figure 12.* Curves are shown for several different values of Q. Center frequency is normalized to 1 Hz and center-frequency gain is normalized to 0 dB.

To find the necessary order n for cascaded second-order bandpass filters using the nomograph in *Figure 13*, first determine the −3 dB bandwidth BW(−3), stopband width SBW, and minimum stopband attenuation A_{min}. Draw a vertical line up from SBW/BW(−3), and a horizontal line across from A_{min}. The required order is shown on the curve just above the point of intersection of the two lines. Remember that each second-order filter section will have a center frequency gain of 2, so the overall gain of a cascaded filter will be 2^N.

Cascading filters in this way may provide acceptable performance when minimum external parts count is very important, but much greater flexibility and better performance will be obtained by using the feedback techniques described in 1.4.

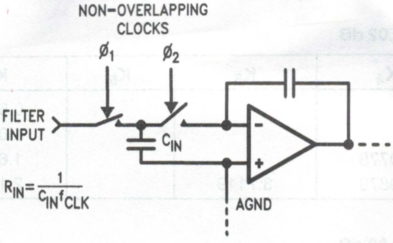
1.6 INPUT IMPEDANCE

The input to each filter block is a switched-capacitor circuit as shown in *Figure 14*. During the first half of a clock cycle, the input capacitor charges to the input voltage V_{in}, and during the second half-cycle, its charge is transferred to a feedback capacitor. The input impedance approximates a resistor of value

$$R_{in} \cong \frac{1}{C_{in} f_{CLK}}.$$

C_{in} depends on the value of Q selected by the Q logic pins, and varies from about 1 pF to about 5 pF. For a worst-case calculation of R_{in}, assume C_{in} = 5 pF. Thus,

$$R_{in}(\min) \cong \frac{1}{5 \times 10^{-12} f_{CLK}}$$



TL/H/8694–22

FIGURE 14. Simplified MF8 Input Stage

At the maximum clock frequency of 1 MHz, this gives $R_{in} \cong$ 200k. Note that R_{in} increases as f_{CLK} decreases, so the input impedance should never be less than this number. Source impedance should be low enough that the gain isn't significantly affected.

1.7 OUTPUT DRIVE

The filter outputs can typically drive a 5 kΩ load resistor to over ±4V peak-to-peak. Load resistors smaller than 5 kΩ should not be used. The operational amplifier can drive the minimum recommended load resistance of 5 kΩ to at least ±3.5V.

1.8 SAMPLED-DATA SYSTEM CONSIDERATIONS

Aliasing

The MF8 is a sampled-data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF8's sampling frequency is the same as its clock frequency). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled-data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2$ + 10 Hz will cause the system to respond as though the input frequency was $f_s/2$ − 10 Hz. This phen known as "aliasing". Aliasing can be reduced or e by limiting the input signal spectrum to less than $f_s/2$. in some cases require the use of a bandwidth-limiting ahead o simple passive RC network will generally suffice) F8 attenuate unwanted high-frequency signals. Howe frequency is much greater than the center usually not be necessary.

Output Steps

Another charac data circuits is that the output voltage cha lock cycle, resulting in a discontinuous The "steps" are smaller when the ratio is 100:1 than when the ratio is

Clock Frequency Limitations

The performance characteristics of a ter depend on the switching (clock) freq clock frequencies (below 10 Hz), the intern gin to discharge slightly between clock cycles. very small parasitic leakage currents. At very low quencies, the time between clock cycles is relativel allowing the capacitors to discharge enough to affect filters' output offset voltage and gain. This effect becomes stronger at elevated operating temperatures.

At higher clock frequencies, performance deviations are primarily due to the reduced time available for the internal integrating op amps to settle. For this reason, the clock waveform's duty cycle should be as close as possible to 50%, especially at higher frequencies. Filter Q shows more variation from the nominal values at higher frequencies, as indicated in the typical performance curves. This is the reason for the different maximum limits on Q accuracy at f_{CLK} = 250 kHz and f_{CLK} = 100 kHz in the table of performance specifications.

Center Frequency Accuracy

Ideally, the ratio f_{CLK}/f_0 should be precisely 100 or 50, depending on the logic voltage on pin 10. However, as Table I shows, this ratio will change slightly depending on the Q selected. As the table shows, the largest errors occur at the lowest values of Q.

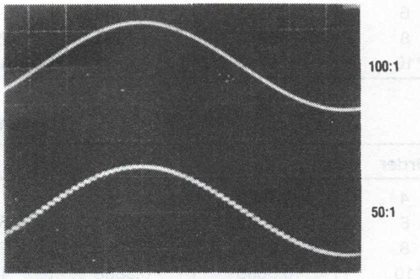


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FIGURE 15. Output Waveform of MF8 Showing Sampling Steps

2.0 Design Tables

BUTTERWORTH RIPPLE 3 dB

Order	K0	K2	K3	K4	K5	K6	KQ
4	2.0000	4.0000					1.4142
[illegible]	2.3704	2.6667	[illegible]				1.5000
8	2.9142	[illegible]	5.8284	14.3145			1.5307
10	[illegible]	[illegible]	[illegible]	6.9094	27.2014		1.5451
*12	[illegible]	[illegible]	3.5800	4.3198	11.5043	49.0673	1.5529

CHEBYSHEV RIPPLE 0.01 dB

Order	K0	K2	K3	K4	K5	K6	KQ
[illegible]	1.9041	3.6339					0.4489
[illegible]	1.8277	1.8450	6.6170				0.9438
[illegible]	1.4856	0.9919	3.1209	5.0414			1.4257
*10	1.0171	0.5740	1.7484	1.2943	4.8814		1.8908

CHEBYSHEV RIPPLE 0.02 dB

Order	K0	K2	K3	K4	K5	K6	KQ
4	1.8644	3.4922					0.5393
6	1.7024	1.6787	6.0772				1.0849
8	1.2893	0.8707	2.7661	4.0779			1.6106
*10	0.8163	0.4934	1.5155	0.9879	3.7119		2.1179

CHEBYSHEV RIPPLE 0.03 dB

Order	K0	K2	K3	K4	K5	K6	KQ
4	1.8341	3.3871					0.6016
6	1.6183	1.5713	5.7231				1.1808
8	1.1688	0.7977	2.5491	3.5270			1.7362
*10	0.7034	0.4467	1.3786	0.8252	3.0938		2.2724

CHEBYSHEV RIPPLE 0.04 dB

Order	K0	K2	K3	K4	K5	K6	KQ
4	1.8085	3.3009					0.6508
6	1.5535	1.4908	5.4548				1.2560
8	1.0814	0.7454	2.3919	3.1471			1.8348
*10	0.6264	0.4139	1.2818	0.7181	2.6883		2.3940

CHEBYSHEV RIPPLE 0.05 dB

Order	K0	K2	K3	K4	K5	K6	KQ
4	1.7860	3.2268					0.6923
6	1.5002	1.4260	5.2373				1.3191
8	1.0129	0.7046	2.2685	2.8609			1.9175
*10	0.5686	0.3888	1.2072	0.6402	2.3938		2.4961

CHEBYSHEV RIPPLE 0.06 dB

Order	K0	K2	K3	K4	K5	K6	KQ
4	1.7657	3.1612					0.7285
6	1.4548	1.3717	5.0536				1.3741
8	0.9566	0.6713	2.1670	2.6336			1.9897
*10	0.5230	0.3685	1.1467	0.5800	2.1666		2.5852

1.0 Application Information (Continued)

tant, but much greater flexibility and better performance will be obtained by using the feedback techniques described in 1.4.

1.6 INPUT IMPEDANCE

The input to each filter block is a switched-capacitor circuit as shown in *Figure 14*. During the first half of a clock cycle, the input capacitor charges to the input voltage V_{in}, and during the second half-cycle, its charge is transferred to a feedback capacitor. The input impedance approximates a resistor of value

$$R_{in} \cong \frac{1}{C_{in} f_{CLK}}.$$

C_{in} depends on the value of Q selected by the Q logic pins, and varies from about 1 pF to about 5 pF. For a worst-case calculation of R_{in}, assume C_{in} = 5 pF. Thus,

$$R_{in}(\text{min}) \cong \frac{1}{5 \times 10^{-12} f_{CLK}}$$

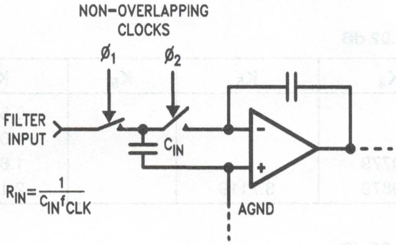

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FIGURE 14. Simplified MF8 Input Stage

At the maximum clock frequency of 1 MHz, this gives $R_{in} \cong$ 200k. Note that R_{in} increases as f_{CLK} decreases, so the input impedance should never be less than this number. Source impedance should be low enough that the gain isn't significantly affected.

1.7 OUTPUT DRIVE

The filter outputs can typically drive a 5 kΩ load resistor to over ±4V peak-to-peak. Load resistors smaller than 5 kΩ should not be used. The operational amplifier can drive the minimum recommended load resistance of 5 kΩ to at least ±3.5V.

1.8 SAMPLED-DATA SYSTEM CONSIDERATIONS

Aliasing

The MF8 is a sampled-data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF8's sampling frequency is the same as its clock frequency). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled-data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2 + 10$ Hz will cause the system to respond as though the input frequency was $f_s/2 - 10$ Hz. This phenomenon is known as "aliasing". Aliasing can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter (a simple passive RC network will generally suffice) ahead of the MF8 to attenuate unwanted high-frequency signals. However, since the clock frequency is much greater than the center frequency, this will usually not be necessary.

Output Steps

Another characteristic of sampled-data circuits is that the output voltage changes only once every clock cycle, resulting in a discontinuous output signal (*Figure 15*). The "steps" are smaller when the clock-to-center-frequency ratio is 100:1 than when the ratio is 50:1.

Clock Frequency Limitations

The performance characteristics of a switched-capacitor filter depend on the switching (clock) frequency. At very low clock frequencies (below 10 Hz), the internal capacitors begin to discharge slightly between clock cycles. This is due to very small parasitic leakage currents. At very low clock frequencies, the time between clock cycles is relatively long, allowing the capacitors to discharge enough to affect the filters' output offset voltage and gain. This effect becomes stronger at elevated operating temperatures.

At higher clock frequencies, performance deviations are primarily due to the reduced time available for the internal integrating op amps to settle. For this reason, the clock waveform's duty cycle should be as close as possible to 50%, especially at higher frequencies. Filter Q shows more variation from the nominal values at higher frequencies, as indicated in the typical performance curves. This is the reason for the different maximum limits on Q accuracy at f_{CLK} = 250 kHz and f_{CLK} = 100 kHz in the table of performance specifications.

Center Frequency Accuracy

Ideally, the ratio f_{CLK}/f_0 should be precisely 100 or 50, depending on the logic voltage on pin 10. However, as Table I shows, this ratio will change slightly depending on the Q selected. As the table shows, the largest errors occur at the lowest values of Q.

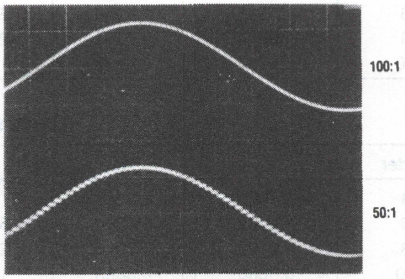

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FIGURE 15. Output Waveform of MF8 Showing Sampling Steps

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters

BUTTERWORTH RIPPLE 3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	2.0000	4.0000					1.4142
6	2.3704	2.6667	9.1429				1.5000
8	2.9142	2.0000	5.8284	14.3145			1.5307
10	3.6340	1.6000	4.4112	6.9094	27.2014		1.5451
*12	4.5635	1.3333	3.5800	4.3198	11.5043	49.0673	1.5529

CHEBYSHEV RIPPLE 0.01 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.9041	3.6339					0.4489
6	1.8277	1.8450	6.6170				0.9438
8	1.4856	0.9919	3.1209	5.0414			1.4257
*10	1.0171	0.5740	1.7484	1.2943	4.8814		1.8908

CHEBYSHEV RIPPLE 0.02 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.8644	3.4922					0.5393
6	1.7024	1.6787	6.0772				1.0849
8	1.2893	0.8707	2.7661	4.0779			1.6106
*10	0.8163	0.4934	1.5155	0.9879	3.7119		2.1179

CHEBYSHEV RIPPLE 0.03 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.8341	3.3871					0.6016
6	1.6183	1.5713	5.7231				1.1808
8	1.1688	0.7977	2.5491	3.5270			1.7362
*10	0.7034	0.4467	1.3786	0.8252	3.0938		2.2724

CHEBYSHEV RIPPLE 0.04 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.8085	3.3009					0.6508
6	1.5535	1.4908	5.4548				1.2560
8	1.0814	0.7454	2.3919	3.1471			1.8348
*10	0.6264	0.4139	1.2818	0.7181	2.6883		2.3940

CHEBYSHEV RIPPLE 0.05 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7860	3.2268					0.6923
6	1.5002	1.4260	5.2373				1.3191
8	1.0129	0.7046	2.2685	2.8609			1.9175
*10	0.5686	0.3888	1.2072	0.6402	2.3938		2.4961

CHEBYSHEV RIPPLE 0.06 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7657	3.1612					0.7285
6	1.4548	1.3717	5.0536				1.3741
8	0.9566	0.6713	2.1670	2.6336			1.9897
*10	0.5230	0.3685	1.1467	0.5800	2.1666		2.5852

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE .07 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7471	3.1020					0.7609
6	1.4150	1.3249	4.8943				1.4232
8	0.9089	0.6431	2.0808	2.4466			2.0543
*10	0.4856	0.3516	1.0959	0.5316	1.9842		2.6649

CHEBYSHEV RIPPLE .08 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7298	3.0478					0.7905
6	1.3795	1.2837	4.7534				1.4679
8	0.8675	0.6187	2.0060	2.2887			2.1130

CHEBYSHEV RIPPLE .09 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7136	2.9978					0.8177
6	1.3475	1.2469	4.6271				1.5090
8	0.8311	0.5973	1.9400	2.1529			2.1671

CHEBYSHEV RIPPLE 0.1 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.6983	2.9512					0.8430
6	1.3183	1.2137	4.5125				1.5473
8	0.7986	0.5782	1.8809	2.0343			2.2176

CHEBYSHEV RIPPLE 0.2 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.5757	2.5998					1.0378
6	1.1128	0.9894	3.7271				1.8413
8	0.5891	0.4551	1.4954	1.3309			2.6057

CHEBYSHEV RIPPLE 0.3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.4833	2.3575					1.1804
6	0.9835	0.8560	3.2501				2.0568
*8	0.4732	0.3861	1.2760	0.9885			2.8914

CHEBYSHEV RIPPLE 0.4 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.4067	2.1698					1.2988
6	0.8888	0.7618	2.9088				2.2363
*8	0.3956	0.3391	1.1250	0.7792			3.1299

CHEBYSHEV RIPPLE 0.5 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.3405	2.0161					1.4029
6	0.8143	0.6897	2.6447				2.3944
*8	0.3389	0.3040	1.0114	0.6365			3.3406

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE 0.6 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.2816	1.8857					1.4975
6	0.7530	0.6316	2.4305				2.5385
*8	0.2952	0.2762	0.9212	0.5326			3.5329

CHEBYSHEV RIPPLE 0.7 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.2283	1.7727					1.5852
6	0.7012	0.5834	2.2515				2.6724
*8	0.2601	0.2535	0.8471	0.4535			3.7119

CHEBYSHEV RIPPLE 0.8 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.1797	1.6731					1.6678
6	0.6564	0.5424	2.0983				2.7989
*8	0.2314	0.2344	0.7846	0.3913			3.8811

CHEBYSHEV RIPPLE 0.9 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.1347	1.5841					1.7464
6	0.6171	0.5068	1.9650				2.9194
*8	0.2073	0.2181	0.7309	0.3413			4.0426

CHEBYSHEV RIPPLE 1.0 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.0930	1.5039					1.8219
6	0.5822	0.4756	1.8475				3.0354
*8	0.1869	0.2038	0.6840	0.3002			4.1981

CHEBYSHEV RIPPLE 1.1 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.0539	1.4310					1.8949
6	0.5509	0.4479	1.7428				3.1476
*8	0.1693	0.1913	0.6426	0.2660			4.3487

CHEBYSHEV RIPPLE 1.2 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.0173	1.3643					1.9657
6	0.5226	0.4231	1.6487				3.2567
*8	0.1540	0.1801	0.6056	0.2372			4.4952

CHEBYSHEV RIPPLE 1.3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.9828	1.3029					2.0348
6	0.4969	0.4006	1.5634				3.3633
*8	0.1406	0.1701	0.5724	0.2125			4.6385

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE 1.4 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.9501	1.2461					2.1024
6	0.4733	0.3803	1.4857				3.4678

CHEBYSHEV RIPPLE 1.5 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.9192	1.1934					2.1688
6	0.4515	0.3616	1.4145				3.5705

CHEBYSHEV RIPPLE 1.6 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8897	1.1443					2.2341
6	0.4315	0.3445	1.3490				3.6717

CHEBYSHEV RIPPLE 1.7 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8617	1.0983					2.2986
6	0.4128	0.3287	1.2883				3.7717

CHEBYSHEV RIPPLE 1.8 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8350	1.0553					2.3624
6	0.3955	0.3141	1.2321				3.8706

CHEBYSHEV RIPPLE 1.9 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8095	1.0148					2.4255
6	0.3793	0.3005	1.1797				3.9687

CHEBYSHEV RIPPLE 2.0 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7850	0.9767					2.4881
6	0.3641	0.2878	1.1308				4.0660

CHEBYSHEV RIPPLE 2.1 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7616	0.9407					2.5503
6	0.3498	0.2759	1.0850				4.1628

CHEBYSHEV RIPPLE 2.2 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7391	0.9067					2.6122
6	0.3364	0.2648	1.0420				4.2591

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE 2.3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7176	0.8744					2.6737
6	0.3237	0.2544	1.0016				4.3550

CHEBYSHEV RIPPLE 2.4 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6968	0.8438					2.7350
6	0.3118	0.2446	0.9635				4.4507

CHEBYSHEV RIPPLE 2.5 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6769	0.8148					2.7962
6	0.3005	0.2353	0.9275				4.5462

CHEBYSHEV RIPPLE 2.6 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6577	0.7871					2.8573
6	0.2897	0.2265	0.8935				4.6415

CHEBYSHEV RIPPLE 2.7 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6392	0.7607					2.9183
6	0.2796	0.2182	0.8612				4.7368

CHEBYSHEV RIPPLE 2.8 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6213	0.7356					2.9792
6	0.2699	0.2104	0.8306				4.8322

CHEBYSHEV RIPPLE 2.9 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6041	0.7116					3.0402
6	0.2607	0.2029	0.8016				4.9276

CHEBYSHEV RIPPLE 3.0 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.5875	0.6886					3.1013
6	0.2519	0.1959	0.7739				5.0231

Note: Multiple feedback loop filters of higher order than those specified in the tables will oscillate due to phase shift at the output of the summing amplifier. This phase shift is not the fault of the MF8; it is inherent in this type of multiple feedback loop topology. In addition, all filters marked with an asterisk (*) will be unstable for $Q \le 1$, due to phase shifts caused by the MF8's switched-capacitor design approach.

National Semiconductor Corporation

MF10 Universal Monolithic Dual Switched Capacitor Filter

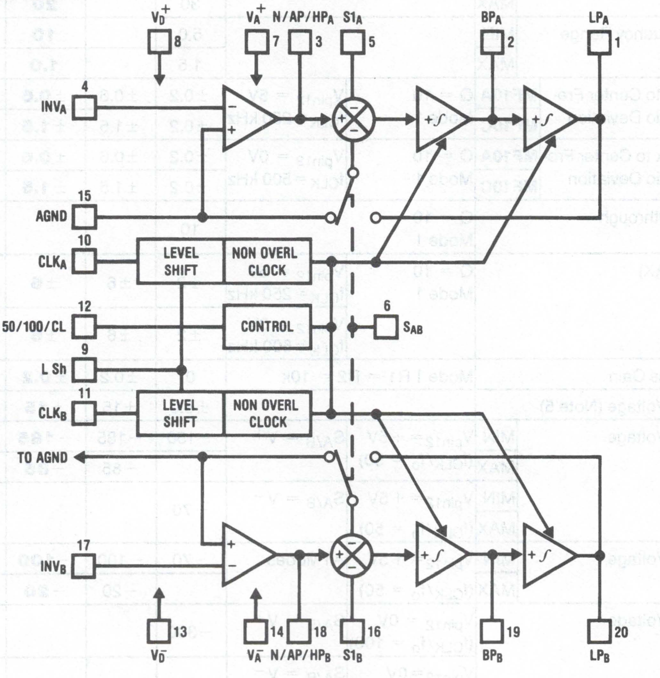
General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- f_o × Q range up to 200 kHz
- Operation up to 30 kHz
- 20-pin 0.3″ wide Dual-In-Line package
- 20-pin Surface Mount (SO) wide-body package

System Block Diagram



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Order Number MF10AJ or MF10CCJ
See NS Package Number J20A

Order Number MF10CCWM
See NS Package Number M20B

Order Number MF10ACN or MF10CCN
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	14V
Voltage at Any Pin	$V^+ + 0.3V$ $V^- - 0.3V$
Input Current at any pin (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
Power Dissipation (Note 3)	500 mW
Storage Temperature	150°C
ESD Susceptability (Note 11)	2000V

Soldering Information

N Package: 10 sec.	260°C
J Package: 10 sec.	300°C
SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (appendix D) for other methods of soldering surface mount devices.

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
MF10ACN, MF10CCN	$0°C \le T_A \le 70°C$
MF10CCWM	$0°C \le T_A \le 70°C$
MF10CCJ	$-40°C \le T_A \le 85°C$
MF10AJ	$-55°C \le T_A \le 125°C$

Electrical Characteristics $V^+ = +5.00V$ and $V^- = -5.00V$ unless otherwise specified.

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions		MF10ACN, MF10CCN, MF10CCWM			MF10CCJ, MF10AJ			Units
					Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ - V^-$	Supply Voltage	MIN					**8**			**8**	V
		MAX					**14**			**14**	V
I_s	Maximum Supply Current		Clock Applied to Pins 10 & 11 No Input Signal		8	12	**12**	8	**12**		mA
f_o	Center Frequency Range	MIN	$f_o \times Q < 200$ kHz		0.1		**0.2**	0.1		**0.2**	Hz
		MAX			30		**20**	30		**20**	kHz
f_{CLK}	Clock Frequency Range	MIN			5.0		**10**	5.0		**10**	Hz
		MAX			1.5		**1.0**	1.5		**1.0**	MHz
f_{CLK}/f_o	50:1 Clock to Center Frequency Ratio Deviation	**MF10A**	Q = 10 Mode 1	$V_{pin12} = 5V$ $f_{CLK} = 250$ kHz	±0.2	±0.6	±**0.6**	±0.2	±**1.0**		%
		MF10C			±0.2	±1.5	±**1.5**	±0.2	±**1.5**		%
f_{CLK}/f_o	100:1 Clock to Center Frequency Ratio Deviation	**MF10A**	Q = 10 Mode 1	$V_{pin12} = 0V$ $f_{CLK} = 500$ kHz	±0.2	±0.6	±**0.6**	±0.2	±**1.0**		%
		MF10C			±0.2	±1.5	±**1.5**	±0.2	±**1.5**		%
	Clock Feedthrough		Q = 10 Mode 1		10			10			mV
	Q Error (MAX) (Note 4)		Q = 10 Mode 1	$V_{pin12} = 5V$ $f_{CLK} = 250$ kHz	±2	±6	±**6**	±2	±**6**		%
				$V_{pin12} = 0V$ $f_{CLK} = 500$ kHz	±2	±6	±**6**	±2	±**6**		%
H_{OLP}	DC Lowpass Gain		Mode 1 R1 = R2 = 10k		0	±0.2	±**0.2**	0	±**0.2**		dB
V_{os1}	DC Offset Voltage (Note 5)				±5.0	±15	±**15**	±5.0	±**15**		mV
V_{os2}	DC Offset Voltage (Note 5)	MIN	$V_{pin12} = +5V$	$S_{A/B} = V^+$	−150	−185	−**185**	−150	−**185**		mV
		MAX	$(f_{CLK}/f_o = 50)$			−85	−**85**		−**85**		
		MIN	$V_{pin12} = +5V$	$S_{A/B} = V^-$	−70			−70			mV
		MAX	$(f_{CLK}/f_o = 50)$								
V_{os3}	DC Offset Voltage (Note 5)	MIN	$V_{pin12} = +5V$	All Modes	−70	−100	−**100**	−70	−**100**		mV
		MAX	$(f_{CLK}/f_o = 50)$			−20	−**20**		−**20**		
V_{os2}	DC Offset Voltage (Note 5)		$V_{pin12} = 0V$ $(f_{CLK}/f_o = 100)$	$S_{A/B} = V^+$	−300			−300			mV
			$V_{pin12} = 0V$ $(f_{CLK}/f_o = 100)$	$S_{A/B} = V^-$	−140			−140			mV
V_{os3}	DC Offset Voltage (Note 5)		$V_{pin12} = 0V$ $(f_{CLK}/f_o = 100)$	All Modes	−140			−140			mV

Electrical Characteristics (Continued) $V^+ = +5.00V$ and $V^- = -5.00V$ unless otherwise specified.

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions	MF10ACN, MF10CCN, MF10CCWM			MF10CCJ, MF10AJ			Units
				Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
V_{out}	Minimum Output Voltage Swing	BP, LP PINS	RL = 5k	±4.25	±3.8	**±3.8**	±4.25	**±3.8**		V
		N/AP/HP PIN	RL = 3.5k	±4.25	±3.8	**±3.8**	±4.25	**±3.6**		V
GBW	Op Amp Gain BW Product			2.5			2.5			MHz
SR	Op Amp Slew Rate			7			7			V/μs
	Dynamic Range (Note 6)		$V_{pin12} = +5V$ ($f_{CLK}/f_o = 50$)	83			83			dB
			$V_{pin12} = 0V$ ($f_{CLK}/f_o = 100$)	80			80			dB
I_{sc}	Maximum Output Short Circuit Current (Note 7)	Source		20			20			mA
		Sink		3.0			3.0			mA

Logic Input Characteristics **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter		Conditions	MF10ACN, MF10CCN, MF10CCWM			MF10CCJ, MF10AJ			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CMOS Clock Input Voltage	MIN Logical "1"	$V^+ = +5V$, $V^- = -5V$, $V_{LSh} = 0V$		+3.0	**+3.0**		**+3.0**		V
	MAX Logical "0"			−3.0	**−3.0**		**−3.0**		V
	MIN Logical "1"	$V^+ = +10V$, $V^- = 0V$, $V_{LSh} = +5V$		+8.0	**+8.0**		**+8.0**		V
	MAX Logical "0"			+2.0	**+2.0**		**+2.0**		V
TTL Clock Input Voltage	MIN Logical "1"	$V^+ = +5V$, $V^- = -5V$, $V_{LSh} = 0V$		+2.0	**+2.0**		**+2.0**		V
	MAX Logical "0"			+0.8	**+0.8**		**+0.8**		V
	MIN Logical "1"	$V^+ = +10V$, $V^- = 0V$, $V_{LSh} = 0V$		+2.0	**+2.0**		**+2.0**		V
	MAX Logical "0"			+0.8	**+0.8**		**+0.8**		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF10ACN/CCN when board mounted is 55°C/W. For the MF10AJ/CCJ, this number increases to 95°C/W and for the MF10CCWM this number is 66°C/W.

Note 4: The accuracy of the Q value is a function of the center frequency (f_o). This is illustrated in the curves under the heading "Typical Peformance Characteristics".

Note 5: V_{os1}, V_{os2}, and V_{os3} refer to the internal offsets as discussed in the Applications Information section 3.4.

Note 6: For ±5V supplies the dynamic range is referenced to 2.82V rms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μV rms for the MF10 with a 50:1 CLK ratio and 280 μV rms for the MF10 with a 100:1 CLK ratio.

Note 7: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

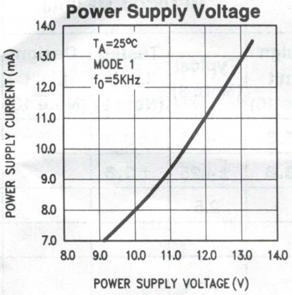
Note 8: Typicals are at 25°C and represent most likely parametric norm.

Note 9: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

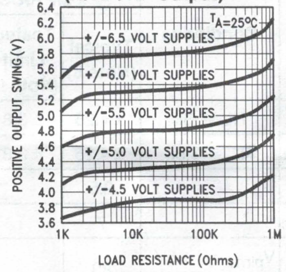
Note 10: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

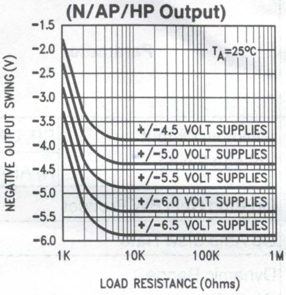
Typical Performance Characteristics



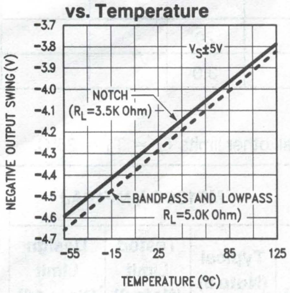
Power Supply Current vs. Power Supply Voltage



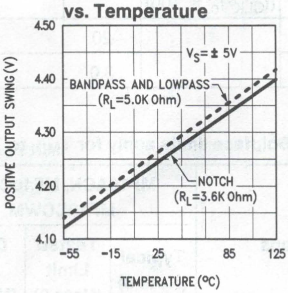
Positive Output Voltage Swing vs. Load Resistance (N/AP/HP Output)



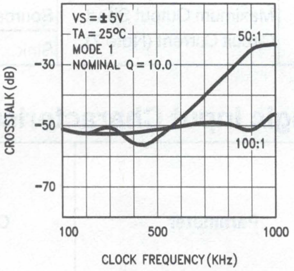
Negative Output Voltage Swing vs. Load Resistance (N/AP/HP Output)



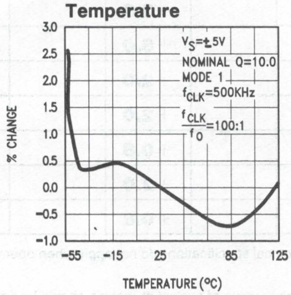
Negative Output Swing vs. Temperature



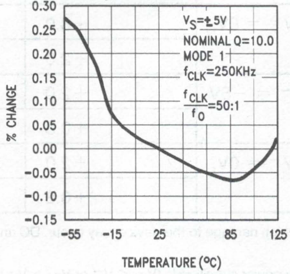
Positive Output Swing vs. Temperature



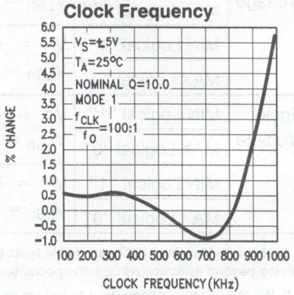
Crosstalk vs. Clock Frequency



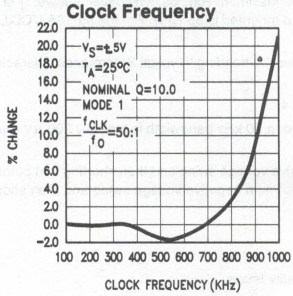
Q Deviation vs. Temperature



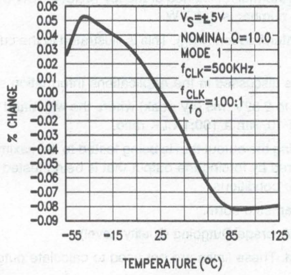
Q Deviation vs. Temperature



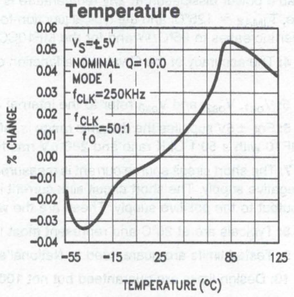
Q Deviation vs. Clock Frequency



Q Deviation vs. Clock Frequency



f_{clk}/f_o Deviation vs. Temperature

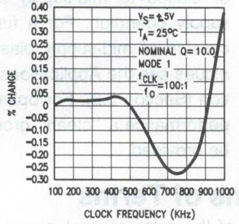


f_{clk}/f_o Deviation vs. Temperature

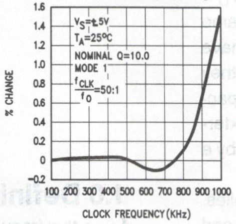
TL/H/5645-14

Typical Performance Characteristics (Continued)

f_{CLK}/f_o Deviation vs. Clock Frequency

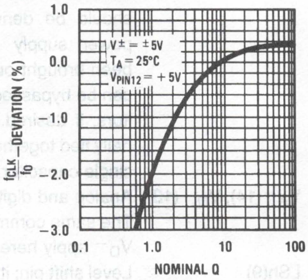


f_{CLK}/f_o Deviation vs. Clock Frequency



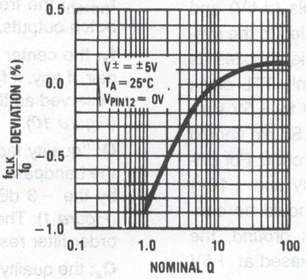
TL/H/5645–15

Deviation of $\frac{f_{CLK}}{f_o}$ vs. Nominal Q



TL/H/5645–16

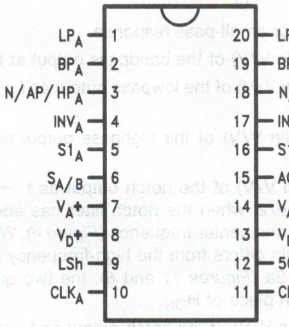
Deviation of $\frac{f_{CLK}}{f_o}$ vs. Nominal Q



TL/H/5645–17

Connection Diagram

Surface Mount and Dual-In-Line Package



TL/H/5645–18

Top View

Pin Descriptions

LP(1,20), BP(2,19), N/AP/HP(3,18)	The second order lowpass, bandpass and notch/allpass/highpass outputs. These outputs can typically sink 1.5 mA and source 3 mA. Each output typically swings to within 1 V of each supply.
INV(4,17)	The inverting input of the summing op-amp of each filter. These are high impedance inputs, but the non-inverting input is internally tied to AGND, making INV_A and INV_B behave like summing junctions (low impedance, current inputs).
S1(5,16)	S1 is a signal input pin used in the allpass filter configurations (see modes 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).
$S_{A/B}$(6)	This pin activates a switch that connects one of the inputs of each filter's second summer to either AGND ($S_{A/B}$ tied to V−) or to the lowpass (LP) output ($S_{A/B}$ tied to V+). This offers the flexibility needed for configuring the filter in its various modes of operation.

Pin Descriptions (Continued)

$V_A+(7)$, $V_D+(8)$	Analog positive supply and digital positive supply. These pins are internally connected through the IC substrate and therefore V_A+ and V_D+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.
$V_A-(14)$, $V_D-(13)$	Analog and digital negative supplies. The same comments as for V_A- and V_D- apply here.
LSh(9)	Level shift pin; it accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the MF10 can be driven with CMOS clock levels (±5V) and the LSh pin should be tied to the system ground. If the same supplies as above are used but only TTL clock levels, derived from 0V to +5V supply, are available, the LSh pin should be tied to the system ground. For single supply operation (0V and +10V) the V_A-, V_D- pins should be connected to the system ground, the AGND pin should be biased at +5V and the LSh pin should also be tied to the system ground for TTL clock levels. LSh should be biased at +5V for CMOS clock levels in 10V single-supply applications.
CLKA(10), CLKB(11)	Clock inputs for each switched capacitor filter building block. They should both be of the same level (TTL or CMOS). The level shift (LSh) pin description discusses how to accommodate their levels. The duty cycle of the clock should be close to 50% especially when clock frequencies above 200 kHz are used. This allows the maximum time for the internal op-amps to settle, which yields optimum filter operation.
50/100/CL(12)	By tying this pin high a 50:1 clock-to-filter-center-frequency ratio is obtained. Tying this pin at mid-supplies (i.e., analog ground with dual supplies) allows the filter to operate at a 100:1 clock-to-center-frequency ratio. When the pin is tied low (i.e., negative supply with dual supplies), a simple current limiting circuit is triggered to limit the overall supply current down to about 2.5 mA. The filtering action is then aborted.
AGND(15)	This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.

1.0 Definitions of Terms

f_{CLK}: the frequency of the external clock signal applied to pin 10 or 11.

f_o: center frequency of the second order function complex pole pair. f_o is measured at the bandpass outputs of the MF10, and is the frequency of maximum bandpass gain. (*Figure 1*).

f_{notch}: the frequency of minimum (ideally zero) gain at the notch outputs.

f_z: the center frequency of the second order complex zero pair, if any. If f_z is different from f_o and if Q_z is high, it can be observed as the frequency of a notch at the allpass output. (*Figure 10*).

Q: "quality factor" of the 2nd order filter. Q is measured at the bandpass outputs of the MF10 and is equal to f_o divided by the −3 dB bandwidth of the 2nd order bandpass filter (*Figure 1*). The value of Q determines the shape of the 2nd order filter responses as shown in *Figure 6*.

Q_z: the quality factor of the second order complex zero pair, if any. Q_Z is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q_Z} + \omega_o^2\right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

where $Q_Z = Q$ for an all-pass response.

H_{OBP}: the gain (in V/V) of the bandpass output at $f = f_o$.

H_{OLP}: the gain (in V/V) of the lowpass output as f ⟶ 0 Hz (*Figure 2*).

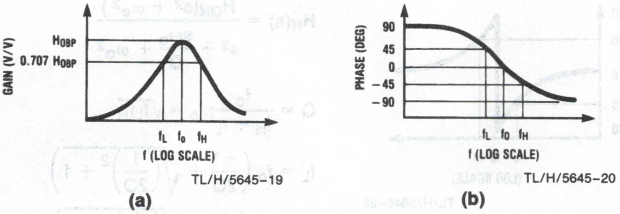
H_{OHP}: the gain (in V/V) of the highpass output as f ⟶ $f_{clk}/2$ (*Figure 3*).

H_{ON}: the gain (in V/V) of the notch output as f ⟶ 0 Hz and as f ⟶ $f_{clk}/2$, when the notch filter has equal gain above and below the center frequency (*Figure 4*). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (*Figures 11* and *8*), the two quantities below are used in place of H_{ON}.

H_{ON1}: the gain (in V/V) of the notch output as f ⟶ 0 Hz.

H_{ON2}: the gain (in V/V) of the notch output as f ⟶ $f_{clk}/2$.

1.0 Definitions of Terms (Continued)



(a) (b)

$$H_{BP}(s) = \frac{H_{OBP}s}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

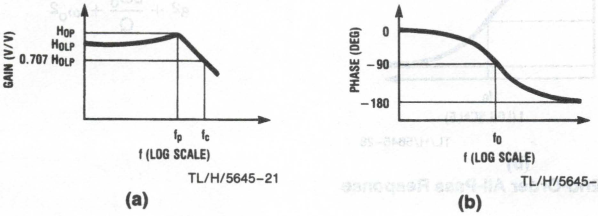
$$Q = \frac{f_o}{f_H - f_L};\ f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$\omega_o = 2\pi f_o$$

FIGURE 1. 2nd-Order Bandpass Response



(a) (b)

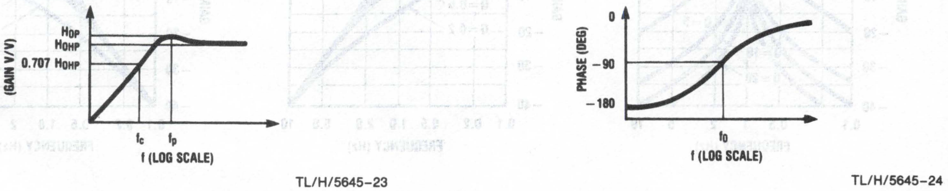
$$H_{LP}(s) = \frac{H_{OLP}\omega_o^2}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_o\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 2. 2nd-Order Low-Pass Response



(a) (b)

$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

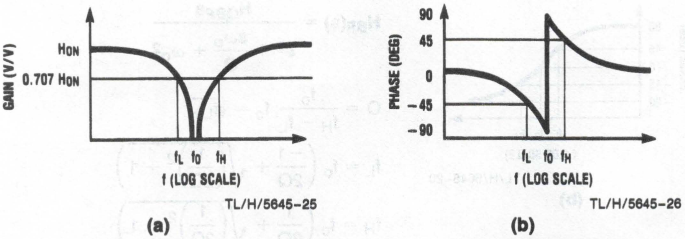
$$f_c = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_p = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 3. 2nd-Order High-Pass Response

1.0 Definitions of Terms (Continued)



TL/H/5645–25

(a)

TL/H/5645–26

(b)

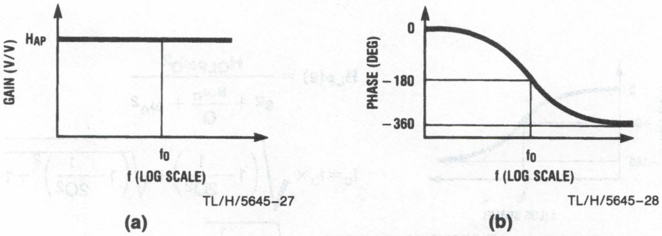
$$H_N(s) = \frac{H_{ON}(s^2 + \omega_o^2)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$Q = \frac{f_o}{f_H - f_L};\ f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

FIGURE 4. 2nd-Order Notch Response



TL/H/5645–27

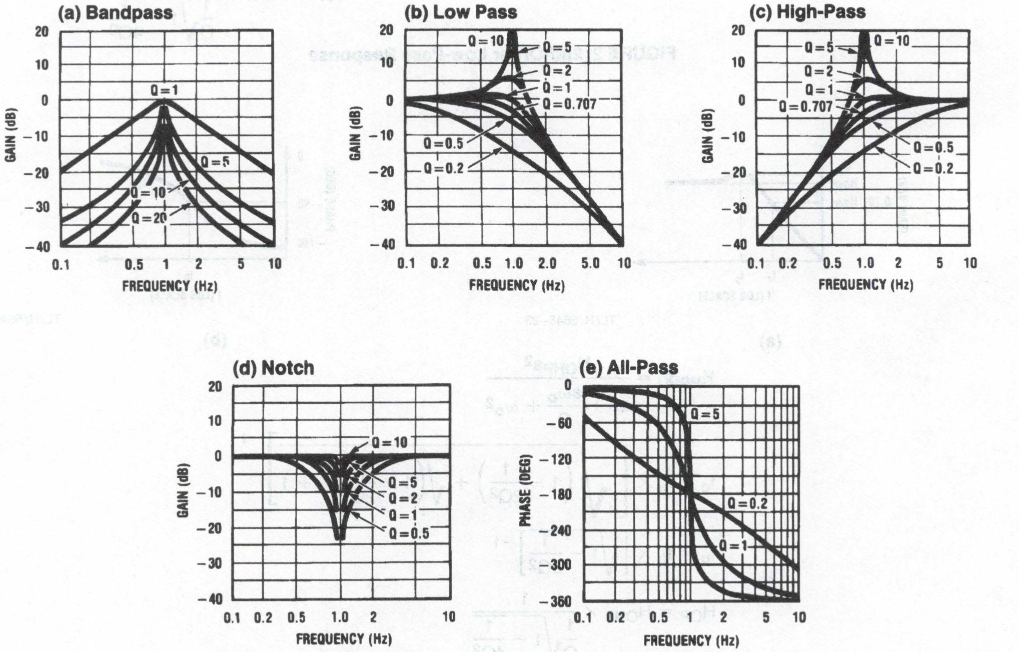
(a)

TL/H/5645–28

(b)

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q} + \omega_o^2\right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

FIGURE 5. 2nd-Order All-Pass Response



TL/H/5645–29

FIGURE 6. Response of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.

2.0 Modes of Operation

The MF10 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach is appropriate. Since this is cumbersome, and since the MF10 closely approximates continuous filters, the following discussion is based on the well known frequency domain. Each MF10 can produce a full 2nd order function. See Table 1 for a summary of the characteristics of the various modes.

MODE 1: Notch 1, Bandpass, Lowpass Outputs:

$f_{notch} = f_o$ **(See *Figure 7*)**

f_o = center frequency of the complex pole pair

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

f_{notch} = center frequency of the imaginary zero pair = f_o.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_o$) $= -\frac{R3}{R1}$

H_{ON} = Notch output gain as $\left.\begin{matrix} f \rightarrow 0 \\ f \rightarrow f_{CLK}/2 \end{matrix}\right\} = \frac{-R_2}{R_1}$

$Q = \frac{f_o}{BW} = \frac{R3}{R2}$

= quality factor of the complex pole pair

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$$H_{OLP} = \frac{H_{OBP}}{Q} \text{ or } H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q.$$

$$H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)}$$

MODE 1a: Non-Inverting BP, LP (See *Figure 8*)

$f_o = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

$H_{OLP} = -1$; $H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OBP_1} = -\frac{R3}{R2}$

$H_{OBP_2} = 1$ (non-inverting)

Circuit dynamics: $H_{OBP_1} = Q$

Note: V_{IN} should be driven from a low impedance (<1 kΩ) source.

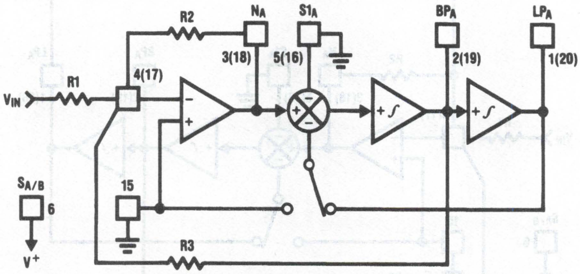
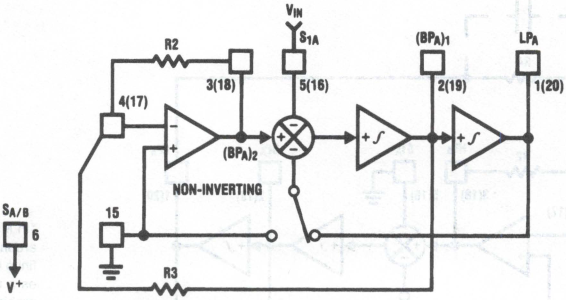


FIGURE 7. MODE 1



TL/H/5645–4

FIGURE 8. MODE 1a

2.0 Modes of Operation (Continued)

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_o$

(See *Figure 9*)

$$f_o = \text{center frequency} = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \text{quality factor of the complex pole pair} = \frac{\sqrt{R2/R4+1}}{R2/R3}$$

$$H_{OLP} = \text{Lowpass output gain (as } f \rightarrow 0) = -\frac{R2/R1}{R2/R4+1}$$

$$H_{OBP} = \text{Bandpass output gain (at } f = f_o) = -R3/R1$$

$$H_{ON_1} = \text{Notch output gain (as } f \rightarrow 0) = -\frac{R2/R1}{R2/R4+1}$$

$$H_{ON_2} = \text{Notch output gain} \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = \sqrt{H_{ON_1}\,H_{ON_2}}$

MODE 3: Highpass, Bandpass, Lowpass Outputs

(See *Figure 10*)

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \text{quality factor of the complex pole pair} = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = \text{Highpass gain} \left(\text{at } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_o) = -\frac{R3}{R1}$$

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\frac{R4}{R1}$$

Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$; $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q$

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP(peak)} \cong Q \times H_{OHP}$ (for high Q's)

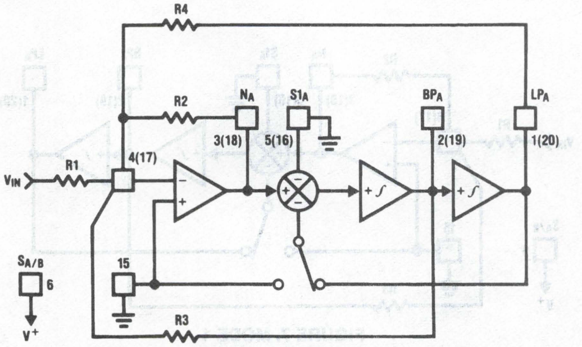


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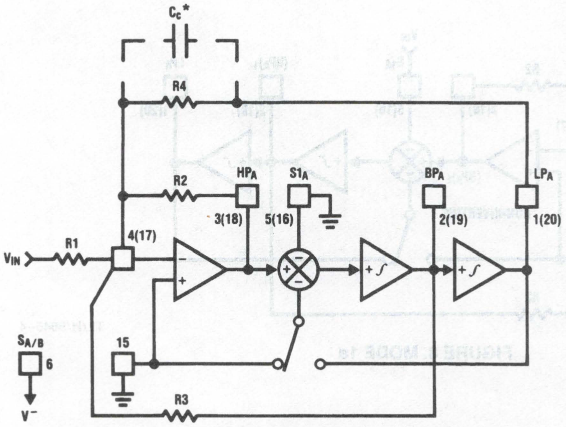
FIGURE 9. MODE 2



*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enchancement. If this is a problem, connect a small capacitor (10 pF − 100 pF) across R4 to provide some phase lead.

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FIGURE 10. MODE 3

2.0 Modes of Operation (Continued)

MODE 3a: HP, BP, LP and Notch with External Op Amp (See *Figure 11*)

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

$$f_n = \text{notch frequency} = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$$

$$H_{ON} = \text{gain of notch at } f = f_o = \left\| Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right) \right\|$$

$$H_{n1} = \text{gain of notch (as } f \longrightarrow 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{n2} = \text{gain of notch } \left(\text{as } f \longrightarrow \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP}$$

MODE 4: Allpass, Bandpass, Lowpass Outputs (See *Figure 12*)

$$f_o = \text{center frequency} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50};$$

$$f_z^* = \text{center frequency of the complex zero} \approx f_o$$

$$Q = \frac{f_o}{BW} = \frac{R3}{R2};$$

$$Q_z = \text{quality factor of complex zero pair} = \frac{R3}{R1}$$

For AP output make R1 = R2

$$H_{OAP}^* = \text{Allpass gain } \left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$$

$$H_{OLP} = \text{Lowpass gain (as } f \longrightarrow 0) = -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_o) = -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$$

Circuit dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)Q$

*Due to the sampled data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4 dB peaking around f_o of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

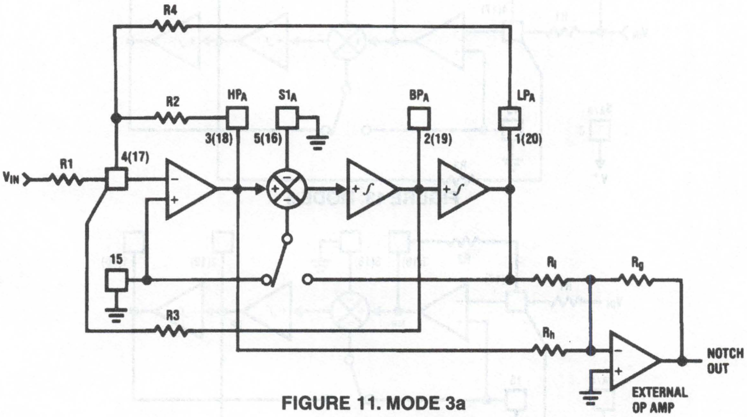

FIGURE 11. MODE 3a

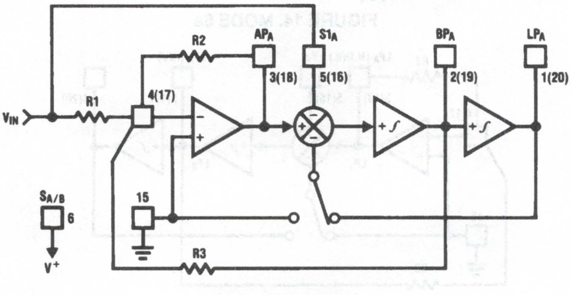

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FIGURE 12. MODE 4

2.0 Modes of Operation (Continued)

MODE 5: Numerator Complex Zeros, BP, LP (See *Figure 13*)

$$f_O = \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1 + R2/R4} \times \frac{R3}{R2}$$

$$Q_Z = \sqrt{1 - R1/R4} \times \frac{R3}{R1}$$

$$H_{O_{z1}} = \text{gain at C.Z. output (as } f \rightarrow 0 \text{ Hz)} = \frac{-R2(R4 - R1)}{R1(R2 + R4)}$$

$$H_{O_{z2}} = \text{gain at C.Z. output} \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{-R2}{R1}$$

$$H_{OBP} = -\left(\frac{R2}{R1} + 1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = -\left(\frac{R2 + R1}{R2 + R4}\right) \times \frac{R4}{R1}$$

MODE 6a: Single Pole, HP, LP Filter (See *Figure 14*)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See *Figure 15*)

f_c = cutoff frequency of LP outputs

$$\cong \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

H_{OLP_1} = 1 (non-inverting)

$$H_{OLP_2} = -\frac{R3}{R2}$$

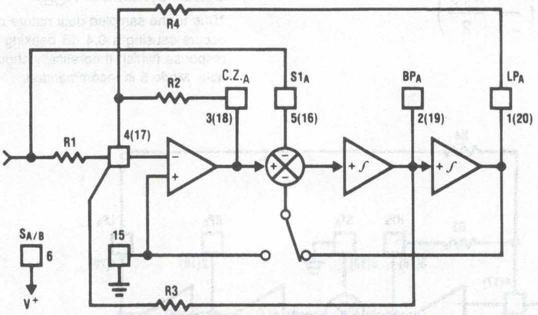
R4
R2
C.Z.A
S1A
BPA
LPA
3(18)
5(16)
2(19)
1(20)
R1
4(17)
VIN
SA/B
6
15
V+
R3

FIGURE 13. MODE 5

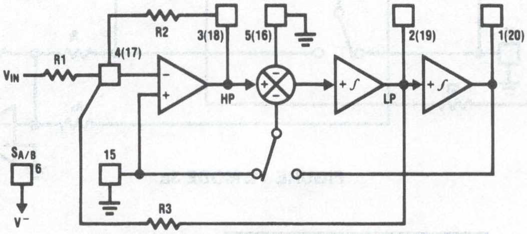
R2
3(18)
5(16)
2(19)
1(20)
R1
4(17)
VIN
HP
LP
15
SA/B
6
V−
R3

FIGURE 14. MODE 6a

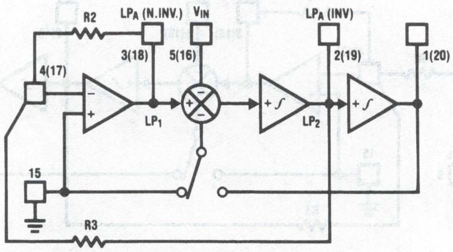
R2
LPA (N.INV.)
VIN
LPA (INV)
3(18)
5(16)
2(19)
1(20)
4(17)
LP1
LP2
15
R3

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FIGURE 15. MODE 6b

2.0 Modes of Operation (Continued)

TABLE I. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks. Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

Mode	BP	LP	HP	N	AP	Number of resistors	Adjustable f_{CLK}/f_o	Notes
1	*	*		*		3	No	
1a	(2) $H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} + 1$				2	No	May need input buffer. Poor dynamics for high Q.
2	*	*		*		3	Yes (above $f_{CLK}/50$ or $f_{CLK}/100$)	
3	*	*	*			4	Yes	Universal State-Variable Filter. Best general-purpose mode.
3a	*	*	*	*		7	Yes	As above, but also includes resistor-tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$.
5	*	*			*	4		Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$.
6a		*	*			3		Single pole.
6b		(2) $H_{OLP1} = +1$ $H_{OLP2} = \frac{-R3}{R2}$				2		Single pole.

3.0 Applications Information

The MF10 is a general-purpose dual second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input (f_{CLK}). By connecting pin 12 to the appropriate DC voltage, the filter center frequency f_0 can be made equal to either $f_{CLK}/100$ or $f_{CLK}/50$. f_0 can be very accurately set (within ±6%) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the f_{CLK}/f_0 ratio can be altered by external resistors as in *Figures 9, 10, 11, 13, 14* and *15.* The filter Q and gain are determined by external resistors.

All of the five second-order filter types can be built using either section of the MF10. These are illustrated in *Figures 1* through *5* along with their transfer functions and some related equations. *Figure 6* shows the effect of Q on the shapes of these curves. When filter orders greater than two are desired, two or more MF10 sections can be cascaded.

3.1 DESIGN EXAMPLE

In order to design a second-order filter section using the MF10, we must define the necessary values of three parameters: f_0, the filter section's center frequency; H_0, the passband gain; and the filter's Q. These are determined by the characteristics required of the filter being designed.

As an example, let's assume that a system requires a fourth-order Chebyshev low-pass filter with 1 dB ripple, unity gain at dc, and 1000 Hz cutoff frequency. As the system order is four, it is realizable using both second-order sections of an MF10. Many filter design texts (and National's Switched Capacitor Filter Handbook) include tables that list the characteristics (f_0 and Q) of each of the second-order filter sections needed to synthesize a given higher-order filter. For the Chebyshev filter defined above, such a table yields the following characteristics:

$f_{0A} = 529$ Hz $\qquad Q_A = 0.785$

$f_{0B} = 993$ Hz $\qquad Q_B = 3.559$

For unity gain at dc, we also specify:

$H_{0A} = 1$

$H_{0B} = 1$

The desired clock-to-cutoff-frequency ratio for the overall filter of this example is 100 and a 100 kHz clock signal is available. Note that the required center frequencies for the two second-order sections will not be obtainable with clock-to-center-frequency ratios of 50 or 100. It will be necessary to adjust $\frac{f_{CLK}}{f_0}$ externally. From Table I, we see that Mode 3 can be used to produce a low-pass filter with resistor-adjustable center frequency.

3.0 Applications Information (Continued)

In most filter designs involving multiple second-order stages, it is best to place the stages with lower Q values ahead of stages with higher Q, especially when the higher Q is greater than 0.707. This is due to the higher relative gain at the center frequency of a higher-Q stage. Placing a stage with lower Q ahead of a higher-Q stage will provide some attenuation at the center frequency and thus help avoid clipping of signals near this frequency. For this example, stage A has the lower Q (0.785) so it will be placed ahead of the other stage.

For the first section, we begin the design by choosing a convenient value for the input resistance: $R_{1A} = 20k$. The absolute value of the passband gain H_{OLPA} is made equal to 1 by choosing R_{4A} such that: $R_{4A} = -H_{OLPA}R_{1A} = R_{1A} = 20k$. If the 50/100/CL pin is connected to mid-supply for nominal 100:1 clock-to-center-frequency ratio, we find R_{2A} by:

$$R_{2A} = R_{4A}\frac{f_{0A}^2}{(f_{CLK}/100)^2} = 2 \times 10^4 \times \frac{(529)^2}{(1000)^2} = 5.6k \text{ and}$$

$$R_{3A} = Q_A\sqrt{R_{2A}R_{4A}} = 0.785\sqrt{5.6 \times 10^3 \times 2 \times 10^4} = 8.3k$$

The resistors for the second section are found in a similar fashion:

$$R_{1B} = 20k$$

$$R_{4B} = R_{1B} = 20k$$

$$R_{2B} = R_{4B}\frac{f_{0B}^2}{(f_{CLK}/100)^2} = 20k\,\frac{(993)^2}{(1000)^2} = 19.7k$$

$$R_{3B} = Q_B\sqrt{R_{2B}R_{4B}} = 3.559\sqrt{1.97 \times 10^4 \times 2 \times 10^4} = 70.6k$$

The complete circuit is shown in *Figure 16* for split ±5V power supplies. Supply bypass capacitors are highly recommended.

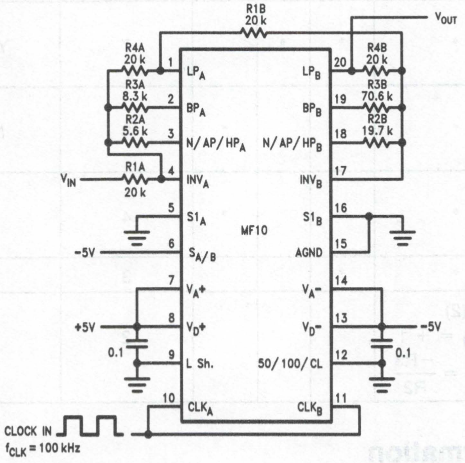
R1B
20 k
V_OUT
R4A
20 k
R3A
8.3 k
R2A
5.6 k
R1A
V_IN
20 k
R4B
20 k
R3B
70.6 k
R2B
19.7 k
1 LP_A
2 BP_A
3 N/AP/HP_A
4 INV_A
5 S1_A
6 S_A/B
7 V_A+
8 V_D+
9 L Sh.
10 CLK_A
20 LP_B
19 BP_B
18 N/AP/HP_B
17 INV_B
16 S1_B
15 AGND
14 V_A−
13 V_D−
12 50/100/CL
11 CLK_B
MF10
−5V
+5V
0.1
−5V
0.1
CLOCK IN
f_CLK = 100 kHz

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FIGURE 16. Fourth-order Chebyshev low-pass filter from example in 3.1. ±5V power supply. 0–5V TTL or −5V ±5V CMOS logic levels.

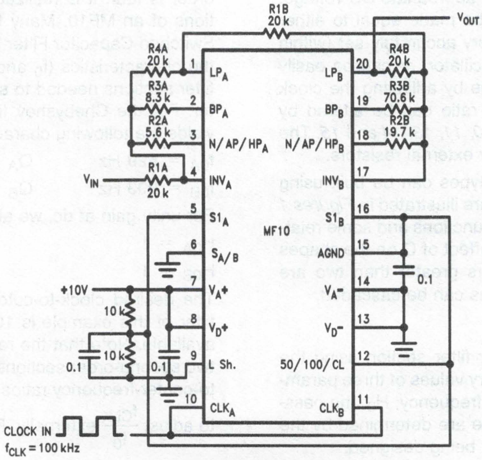
R1B
20 k
V_OUT
R4A
20 k
R3A
8.3 k
R2A
5.6 k
R1A
V_IN
20 k
R4B
20 k
R3B
70.6 k
R2B
19.7 k
1 LP_A
2 BP_A
3 N/AP/HP_A
4 INV_A
5 S1_A
6 S_A/B
7 V_A+
8 V_D+
9 L Sh.
10 CLK_A
20 LP_B
19 BP_B
18 N/AP/HP_B
17 INV_B
16 S1_B
15 AGND
14 V_A−
13 V_D−
12 50/100/CL
11 CLK_B
MF10
+10V
10 k
10 k
0.1
0.1
0.1
CLOCK IN
f_CLK = 100 kHz

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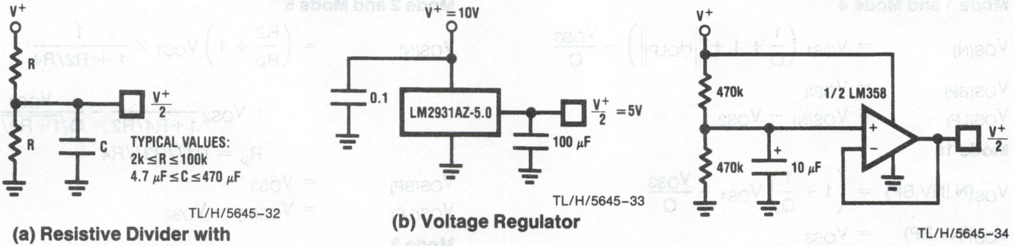
FIGURE 17. Fourth-order Chebyshev low-pass filter from example in 3.1. Single +10V power supply. 0–5V TTL logic levels. Input signals should be referred to half-supply or applied through a coupling capacitor.

3.0 Applications Information (Continued)



(a) Resistive Divider with Decoupling Capacitor

(b) Voltage Regulator

(c) Operational Amplifier with Divider

FIGURE 18. Three Ways of Generating $\frac{V^+}{2}$ for Single-Supply Operation

3.2 SINGLE SUPPLY OPERATION

The MF10 can also operate with a single-ended power supply. *Figure 17* shows the example filter with a single-ended power supply. $V_A{}^+$ and $V_D{}^+$ are again connected to the positive power supply (8 to 14 volts), and $V_A{}^-$ and $V_D{}^-$ are connected to ground. The A_{GND} pin must be tied to $V^+/2$ for single supply operation. This half-supply point should be very "clean", as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor (*Figure 18a*), or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier (*Figures 18b* and *18c*). The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1µF.

3.3 DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the MF10, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the MF10 are able to swing to within about 1 volt of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the MF10 is operating on ±5 volts, for example, the outputs will clip at about $8V_{p\text{-}p}$. The maximum input voltage multiplied by the filter gain should therefore be less than $8V_{p\text{-}p}$.

Note that if the filter Q is high, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain (*Figure 6*). As an example, a lowpass filter with a Q of 10 will have a 20 dB peak in its amplitude response at f_o. If the nominal gain of the filter H_{OLP} is equal to 1, the gain at f_o will be 10. The maximum input signal at f_o must therefore be less than 800 $mV_{p\text{-}p}$ when the circuit is operated on ±5 volt supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 (*Figure 7*). The notch output will be very small at f_o, so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at f_o and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying *Figures 7* through *15* are equations labeled "circuit dynamics", which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

3.4 OFFSET VOLTAGE

The MF10's switched capacitor integrators have a higher equivalent input offset voltage than would be found in a typical continuous-time active filter integrator. *Figure 19* shows an equivalent circuit of the MF10 from which the output dc offsets can be calculated. Typical values for these offsets with $S_{A/B}$ tied to V^+ are:

V_{os1} = opamp offset = ±5mV

V_{os2} = −150 mV @ 50:1 −300 mV @ 100:1

V_{os3} = −70 mV @ 50:1 −140 mV @ 100:1

When $S_{A/B}$ is tied to V^-, V_{os2} will approximately halve. The dc offset at the BP output is equal to the input offset of the lowpass integrator (V_{os3}). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

3.0 Applications Information (Continued)

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + \left\|H_{OLP}\right\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 1a

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right)V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{Rp} + 1\right)V_{OS1} \times \frac{1}{1 + R2/R4} + V_{OS2}\frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}};$$

$$R_p = R1//R3//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

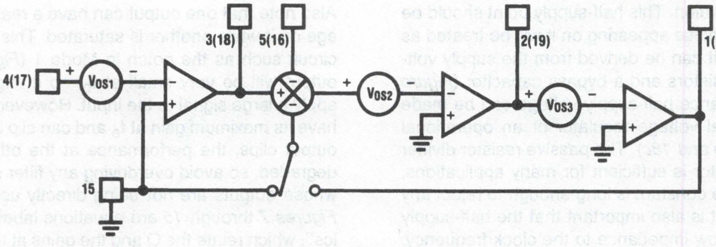
Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

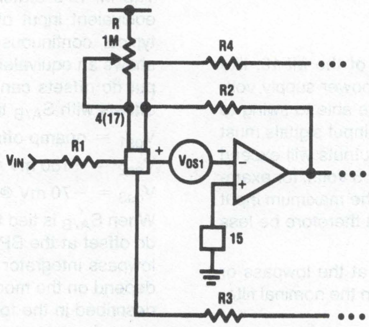
$$V_{OS(LP)} = V_{OS1}\left[1 + \frac{R4}{R_p}\right] - V_{OS2}\left(\frac{R4}{R2}\right) - V_{OS3}\left(\frac{R4}{R3}\right)$$

$$R_p = R1//R2//R3$$


3(18)
5(16)
2(19)
1(20)
4(17)
VOS1
VOS2
VOS3
15
+
−

TL/H/5645-12

FIGURE 19. MF10 Offset Voltage Sources


5V SUPPLY
R
1M
R4
R2
4(17)
VIN
R1
VOS1
15
R3

TL/H/5645-13

FIGURE 20. Method for Trimming V_{OS}

3.0 Applications Information (Continued)

For most applications, the outputs are AC coupled and DC offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower ac signal levels, and clipping at any of the outputs will cause gain nonlinearities and will change f_o and Q. When operating in Mode 3, offsets can become excessively large if R_2 and R_4 are used to make f_{CLK}/f_o significantly higher than the nominal value, especially if Q is also high. An extreme example is a bandpass filter having unity gain, a Q of 20, and $f_{CLK}/f_o = 250$ with pin 12 tied to ground (100:1 nominal). R_4/R_2 will therefore be equal to 6.25 and the offset voltage at the lowpass output will be about +1V. Where necessary, the offset voltage can be adjusted by using the circuit of *Figure 20*. This allows adjustment of V_{os1}, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ($V_{os(BP)}$ in modes 1a and 3, for example).

3.5 SAMPLED DATA SYSTEM CONSIDERATIONS

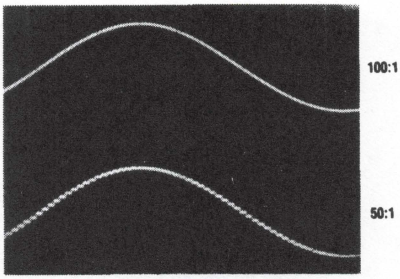
The MF10 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF10's sampling frequency is the same as its clock frequency.) If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2 + 100$ Hz will cause the system to respond as though the input frequency was $f_s/2 - 100$ Hz. This phenomenon is known as "aliasing", and can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter ahead of the MF10 to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in "steps" in the output voltage which occur at the clock rate. (*Figure 21*) If necessary, these can be "smoothed" with a simple R-C low-pass filter at the MF10 output.

The ratio of f_{CLK} to f_c (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise sensitive applications, however, a ratio of 50:1 may be better as it will result in 3 dB lower output noise. The 50:1 ratio also results in lower DC offset voltages, as discussed in 3.4.

The accuracy of the f_{CLK}/f_o ratio is dependent on the value of Q. This is illustrated in the curves under the heading "Typical Performance Characteristics". As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in f_{CLK}/f_o will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

It should also be noted that the product of Q and f_o should be limited to 300 kHz when $f_o < 5$ kHz, and to 200 kHz for $f_o > 5$ kHz.



TL/H/5645-35

FIGURE 21. The Sampled-Data Output Waveform

Section 2

Analog Switches/ Multiplexers

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***Devices Not Covered In Last Publication**

Analog Switch Definition of Terms

R_{ON}: Resistance between the output and the input of an addressed channel.

I_S: Current at any switch input. This is leakage current when the switch is ON.

I_D: Current at any switch input going into the switch. This is leakage current when the switch is OFF.

C_S: Capacitance between any open terminal "S" and ground.

C_D: Capacitance between any open terminal "D" and ground.

$I_D - I_S$: Leakage current that flows from the closed switch into the body. This leakage is the difference between the current I_D going into the switch and the current I_S going out of the switch.

t_{RAN}: Delay time when switching from one address state to another.

t_{ON}: Delay time between the 50% points of an enable input and the switch ON condition.

t_{OFF}: Delay time between the 50% points of the enable input and the switch OFF condition.

National
Semiconductor
Corporation

Analog Switch/Multiplexer Selection Guide

Part Number	Function	Logic Input	V_S (Typ)	T_{ON}/T_{OFF} ns (Typ)	R_{ON} Ω
AH5011	QUAD SPST	TTL, CMOS	—	150/300	100
AH5012		TTL, CMOS	—	150/300	150
CD4016		CMOS	±7.5	20/40	850
CD4066		CMOS	±7.5	25/50	280
LF11201/LF13201		TTL	±15	90/500	200
LF11202/LF13202		TTL	±15	90/500	200
LF11331/LF13331		TTL	±15	90/500	200
LF11332/LF13332		TTL	±15	90/500	200
LF11333/LF13333		TTL	±15	90/500	200
MM74HC4016		CMOS	±12	5/8	40
AH5020	DUAL SPDT	TTL, CMOS	—	150/300	150
CD4053	TRIPLE SPDT	CMOS	±7.5	160/75	300
MM74HC4053		CMOS	±6.0	15/16	40
AH5009	4-CHANNEL	TTL, CMOS	—	150/300	100
AH5010		TTL, CMOS	—	150/300	150
CD4052	4-CHANNEL DIFFERENTIAL	CMOS	±7.5	160/75	300
CD4529B		CMOS	±7.5	50	350
LF13509		TTL, CMOS	±18	1600/200	350
MM74HC4052		CMOS	±6.0	15/16	40
CD4051	8-CHANNEL	CMOS	±7.5	160/75	300
CD4529B		CMOS	±7.5	50	350
LF13508		TTL, CMOS	±18	1600/200	350
MM74HC4051		CMOS	±6.0	15/16	40

National Semiconductor

AH0014/AH0014C DPDT/ AH0015/AH0015C Quad SPST/ AH0019/AH0019C Dual DPST-TTL/DTL Compatible MOS Analog Switches

General Description

This series of TTL/DTL compatible MOS analog switches feature high speed with internal level shifting and driving. The package contains two monolithic integrated circuit chips: the MOS analog chip consists of four MOS analog switch transistors; the second chip is a bipolar I.C. gate and level shifter. The series is available in hermetic dual-in-line package.

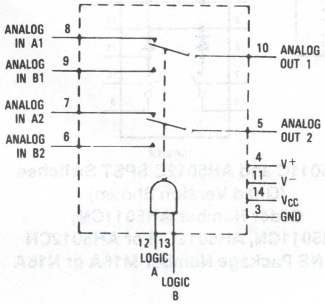
These switches are particularly suited for use in both military and industrial applications such as commutators in data acquisition systems, multiplexers, A/D and D/A converters, long time constant integrators, sample and hold circuits, modulators/demodulators, and other analog signal switching applications.

The AH0014, AH0015 and AH0019 are specified for operation over the −55°C to +125°C military temperature range. The AH0014C, AH0015C and AH0019C are specified for operation over the −25°C to +85°C temperature range.

Features

- Large analog voltage switching ±10V
- Fast switching speed 500 ns
- Operation over wide range of power supplies
- Low ON resistance 200Ω
- High OFF resistance $10^{11}\Omega$
- Analog signals in excess of 25 MHz
- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

Block and Connection Diagrams


ANALOG IN A1
8
ANALOG IN B1
9
ANALOG IN A2
7
ANALOG IN B2
6
10
ANALOG OUT 1
5
ANALOG OUT 2
4
V+
11
V−
14
VCC
3
GND
12
13
LOGIC A
LOGIC B

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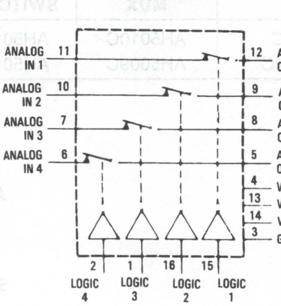
Note: All logic inputs shown at logic "1".

Order Number AH0014D or AH0014CD
See NS Package Number D14D

Quad SPST

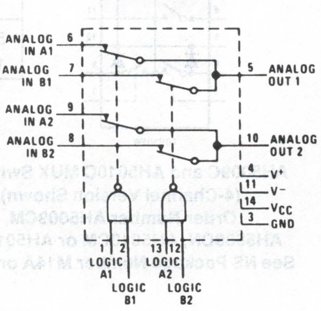

ANALOG IN 1
11
ANALOG IN 2
10
ANALOG IN 3
7
ANALOG IN 4
6
12
ANALOG OUT 1
9
ANALOG OUT 2
8
ANALOG OUT 3
5
ANALOG OUT 4
4
V+
13
V−
14
VCC
3
GND
2
1
16
15
LOGIC 4
LOGIC 3
LOGIC 2
LOGIC 1

TL/H/5563-2

Note: All logic inputs shown at logic "1".

Order Number AH0015D or AH0015CD
See NS Package Number D16C

Dual DPST


ANALOG IN A1
6
ANALOG IN B1
7
ANALOG IN A2
9
ANALOG IN B2
8
5
ANALOG OUT 1
10
ANALOG OUT 2
4
V+
11
V−
14
VCC
3
GND
1
2
13
12
LOGIC A1
LOGIC A2
LOGIC B1
LOGIC B2

TL/H/5563-3

Note: All logic inputs shown at logic "1".

Order Number AH0019D or AH0019CD
See NS Package Number D14D

National Semiconductor Corporation

AH5009, AH5010, AH5011, AH5012 Monolithic Analog Current Switches

General Description

A versatile family of monolithic JFET analog switches economically fulfills a wide variety of multiplexing and analog switching applications.

Even numbered switches may be driven directly from standard 5V logic, whereas the odd numbered switches are intended for applications utilizing 10V or 15V logic. The monolithic construction guarantees tight resistance match and track.

For voltage switching applications see LF13331, LF13332, and LF13333 Analog Switch Family, or the CMOS Analog Switch Family.

Applications

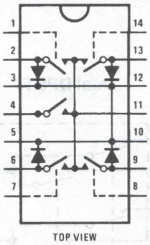
- A/D and D/A converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

Features

■ Interfaces with standard TTL and CMOS	
■ "ON" resistance match	2Ω
■ Low "ON" resistance	100Ω
■ Very low leakage	50 pA
■ Large analog signal range	±10V peak
■ High switching speed	150 ns
■ Excellent isolation between channels	80 dB at 1 kHz

Connection and Schematic Diagrams (All switches shown are for logical "1" input)

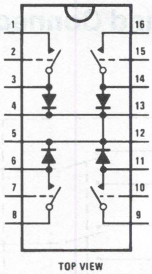
Dual-In-Line Package



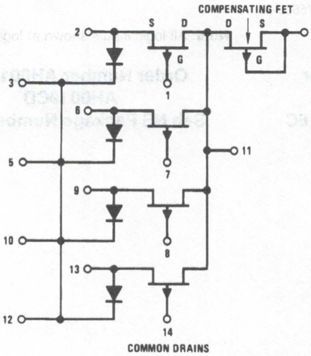
AH5009C and AH5010C MUX Switches (4-Channel Version Shown)
Order Number AH5009CM, AH5009CN, AH5010CM or AH5010CN
See NS Package Number M14A or N14A

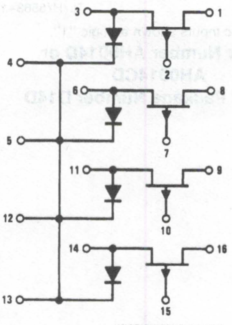
LOGIC DRIVE	4 CHANNEL MUX	4 SPST SWITCHES
5V LOGIC	AH5010C	AH5012C
15V LOGIC	AH5009C	AH5011C

Dual-In-Line Package



AH5011C and AH5012C SPST Switches (Quad Version Shown)
Order Number AH5011CM, AH5011CN, AH5012CM or AH5012CN
See NS Package Number M16A or N16A





TL/H/5659-1

Note: All diode cathodes are internally connected to the substrate.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage	
AH5009/AH5010/AH5011/AH5012	30V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA
Drain Current	30 mA
Soldering Information:	
N Package 10 sec	300°C
SO Package Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Power Dissipation	500 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics AH5010 and AH5012 (Notes 2 and 3)

Symbol	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	$4.5V \leq V_{GD} \leq 11V$, $V_{SD} = 0.7V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V$, $V_{GS} = 3.8V$ $T_A = 85°C$	0.02	0.2 10	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 1$ mA $T_A = 85°C$	0.08	1 200	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 2$ mA $T_A = 85°C$	0.13	5 10	nA μA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = -2$ mA $T_A = 85°C$	0.1	10 20	nA μA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 0.35V$, $I_S = 2$ mA $T_A = +85°C$	90	150 240	Ω Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} = 0$, $I_D = 1$ mA	4	20	Ω
T_{ON}	Turn "ON" Time	See AC Test Circuit	150	500	ns
T_{OFF}	Turn "OFF" Time	See AC Test Circuit	300	500	ns
CT	Cross Talk	See AC Test Circuit	120		dB

Electrical Characteristics AH5009 and AH5011 (Notes 2 and 3)

Symbol	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	$11V \leq V_{GD} \leq 15V$, $V_{SD} = 0.7V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V$, $V_{GS} = 10.3V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 1$ mA $T_A = 85°C$	0.04	0.5 100	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 2$ mA $T_A = 85°C$		2 1	nA μA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = -2$ mA $T_A = 85°C$		5 2	nA μA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 1.5V$, $I_S = 2$ mA $T_A = 85°C$	60	100 160	Ω Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} =$, $I_D = 1$ mA		10	Ω
T_{ON}	Turn "ON" Time	See AC Test Circuit	150	50	ns
T_{OFF}	Turn "OFF" Time	See AC Test Circuit	300	500	ns
CT	Cross Talk	See AC Test Circuit. f = 100 Hz.	120		dB

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Test conditions 25°C unless otherwise noted.

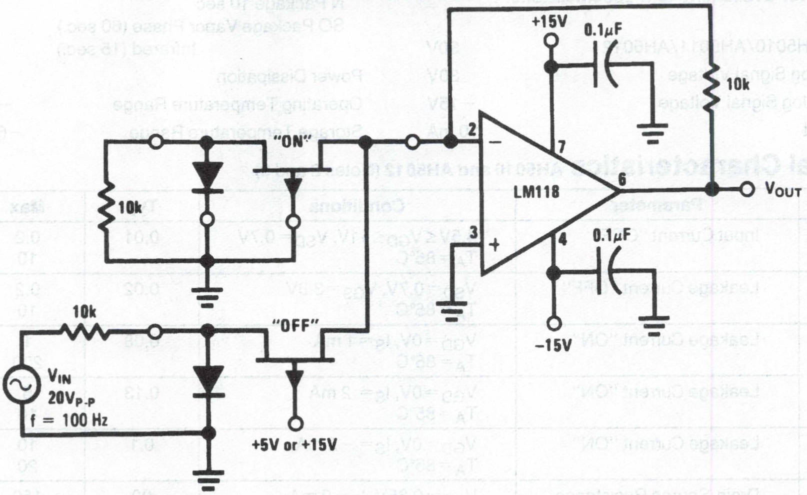
Note 3: "OFF" and "ON" notation refers to the conduction state of the FET switch.

Note 4: Thermal Resistance:

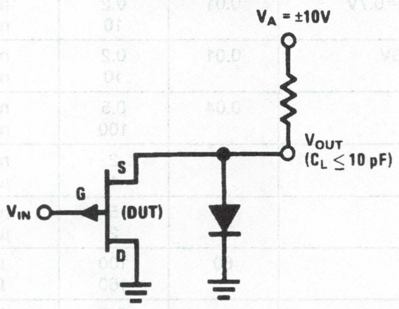
	θ_{JA}
N14A, N16A	92°C/W
M14A, M16A	115°C/W

Test Circuits and Switching Time Waveforms

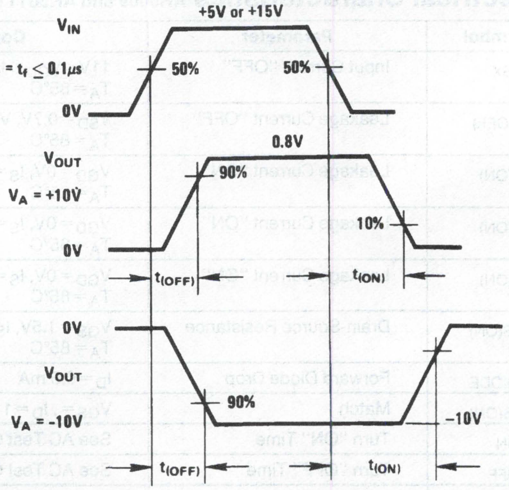
Cross Talk Test Circuit


+15V
0.1µF
10k
2
7
"ON"
10k
LM118
6
V_{OUT}
3
4
0.1µF
−15V
10k
"OFF"
V_{IN}
$20V_{P-P}$
f = 100 Hz
+5V or +15V

AC Test Circuit


V_A = ±10V
V_{OUT}
(C_L ≤ 10 pF)
S
G
V_{IN}
(DUT)
D

Time Waveforms



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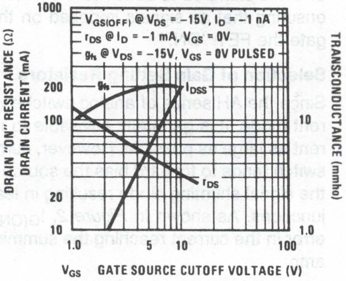
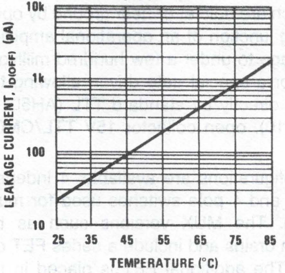
Typical Performance Characteristics

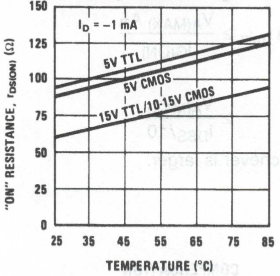
Parameter Interaction



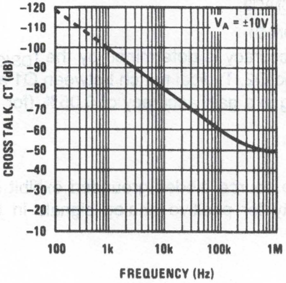
Leakage Current, $I_{D(OFF)}$ vs Temperature



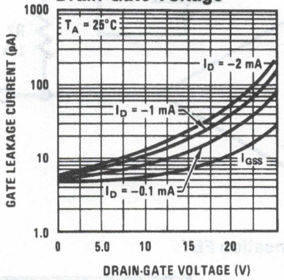
"ON" Resistance, $r_{DS(ON)}$ vs Temperature



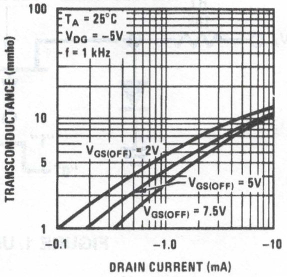
Cross Talk, CT vs Frequency



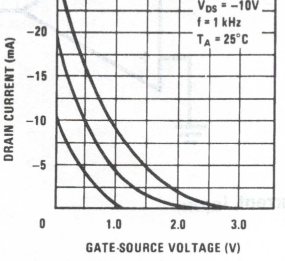
Leakage Current vs Drain-Gate Voltage



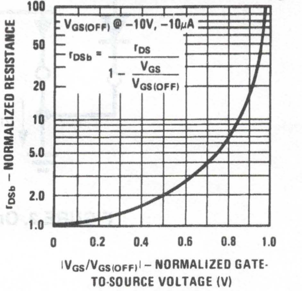
Transconductance vs Drain Current



Drain Current vs Bias Voltage



Normalized Drain Resistance vs Bias Voltage



TL/H/5659-3

Applications Information

Theory of Operation

The AH series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL (AH5010), 5V-10V CMOS (AH5010), open collector 15V TTL/CMOS (AH5009).

Two basic switch configurations are available: 4 independent switches (SPST) and 4 pole switches used for multiplexing (4 PST-MUX). The MUX versions such as the AH5009 offer common drains and include a series FET operated at $V_{GS} = 0V$. The additional FET is placed in the feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = \frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 4 ohms resulting in a gain accuracy of 0.05% (for R1 = R2 = 10 kΩ).

Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With $V_{IN} = 15V$ and the $V_A = 10V$, the source of Q1 is clamped to about 0.7V by the diode ($V_{GS} = 14.3V$) ensuring that ac signals imposed on the 10V input will not gate the FET "ON."

Selection of Gain Setting Resistors

Since the AH series of analog switches are operated in current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2*, $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

Combining the criteria from the above discussion yields:

$$R1_{min} \geq \frac{V_{A(MAX)}\, A_D}{I_{G(ON)}} \tag{2a}$$

or:

$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \tag{2b}$$

whichever is larger.

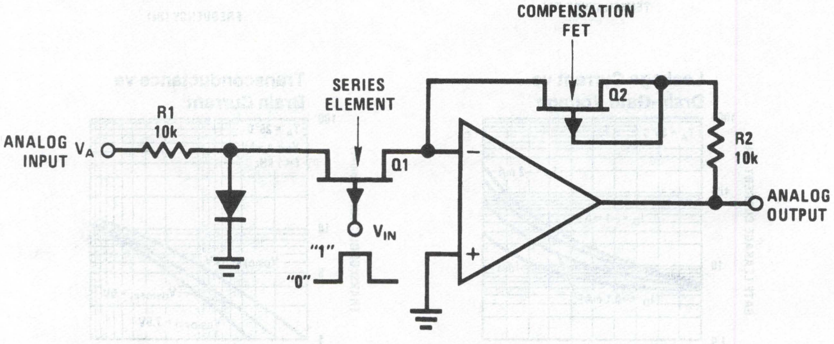


FIGURE 1. Use of Compensation FET

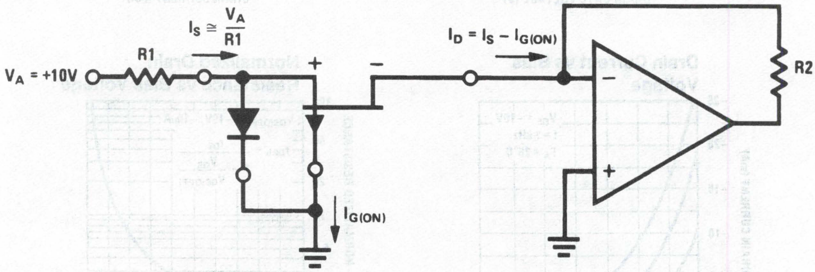


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FIGURE 2. On Leakage Current, $I_{G(ON)}$

Applications Information (Continued)

Where: $V_{A(MAX)}$ = Peak amplitude of the analog input signal

A_D = Desired accuracy

$I_{G(ON)}$ = Leakage at a given I_S

I_{DSS} = Saturation current of the FET switch

$\cong$ 20 mA

In a typical application, V_A might $= \pm 10V$, $A_D = 0.1\%$, $0°C \leq T_A \leq 85°C$. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{(10V)}{\left(\frac{20\ mA}{10}\right)} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong$ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\ \mu A$ at 85°C for the AH5010. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3*, the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\ A_D}{(N)\ I_{D(OFF)}}$$

Where: $V_{A(MIN)}$ = Minimum value of the analog input signal

A_D = Desired accuracy

N = Number of channels

$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)} \leq 10$ nA at 85°C for the AH5009. $R1_{(MAX)}$ is:

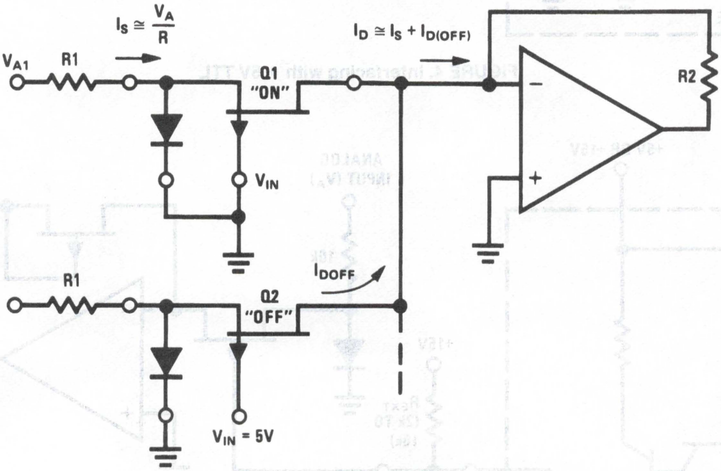
$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.

TTL Compatibility

The AH series can be driven with two different logic voltage swings: the even numbered part types are specified to be driven from standard 5V TTL logic and the odd numbered types from 15V open collector TTL.



TL/H/5659-5

FIGURE 3

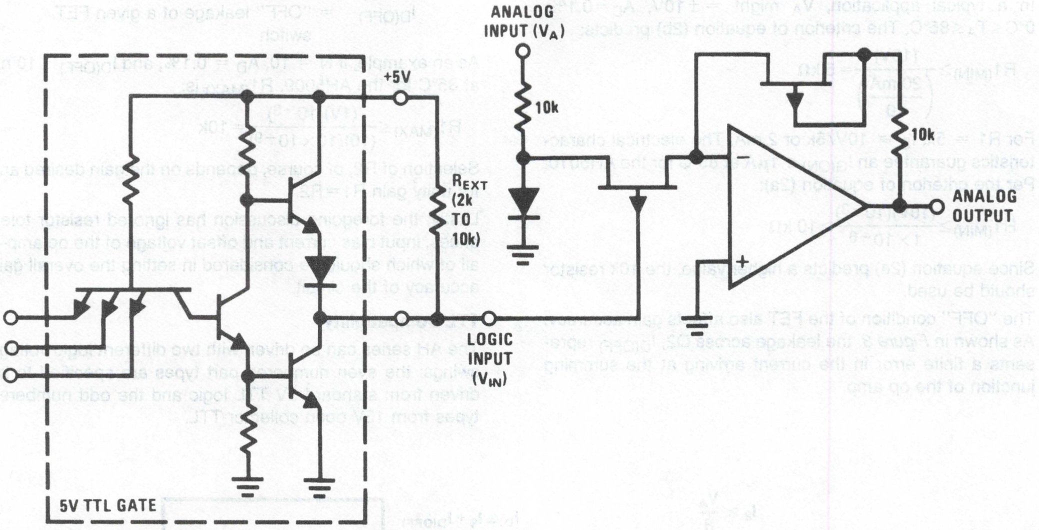
Applications Information (Continued)

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AH5010, a pull-up resistor, R_{EXT}, of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4.*

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in *Figure 5.* In both cases, $t_{(OFF)}$ is improved for lower values of R_{EXT} at the expense of power dissipation in the low state.

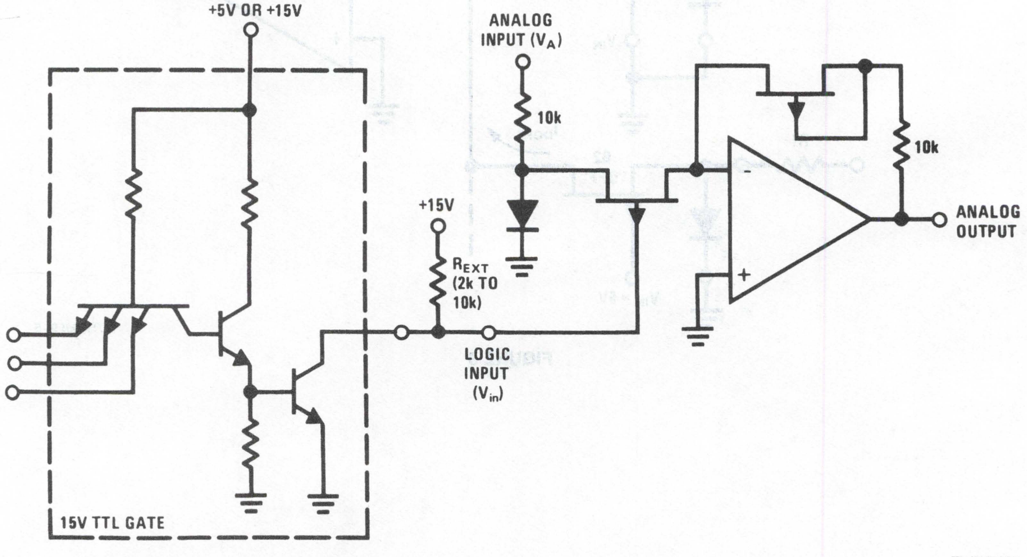
Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in *Figure 6.*



ANALOG INPUT (V_A)
+5V
10k
R_{EXT} (2k TO 10k)
10k
ANALOG OUTPUT
LOGIC INPUT (V_{IN})
5V TTL GATE

FIGURE 4. Interfacing with +5V TTL



+5V OR +15V
ANALOG INPUT (V_A)
10k
+15V
R_{EXT} (2k TO 10k)
10k
ANALOG OUTPUT
LOGIC INPUT (V_{in})
15V TTL GATE

TL/H/5659–6

FIGURE 5. Interfacing with +15V Open Collector TTL

Applications Information (Continued)

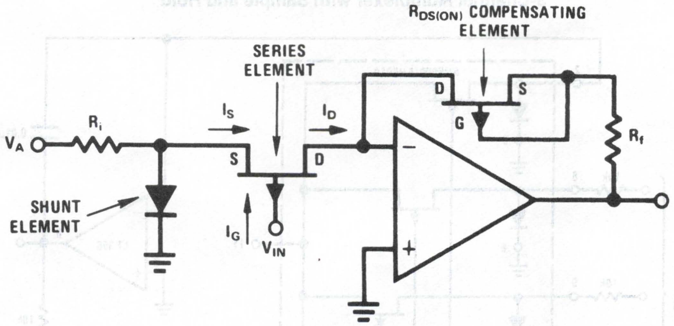
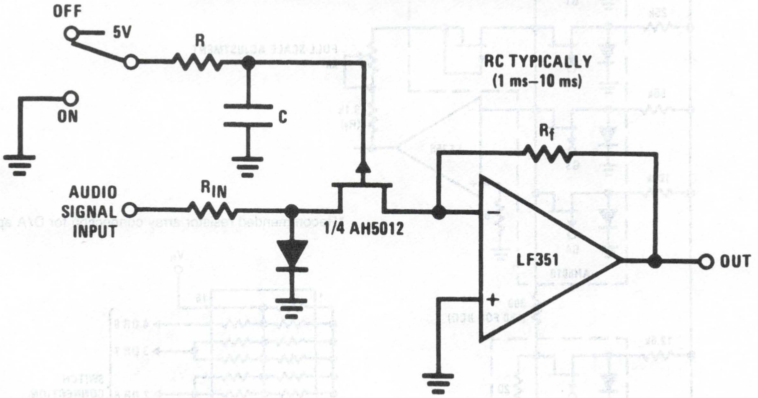

R_DS(ON) COMPENSATING ELEMENT
SERIES ELEMENT
I_S
I_D
D
S
G
R_i
V_A
R_f
S
D
SHUNT ELEMENT
I_G
V_IN

FIGURE 6. Definition of Terms

Typical Applications

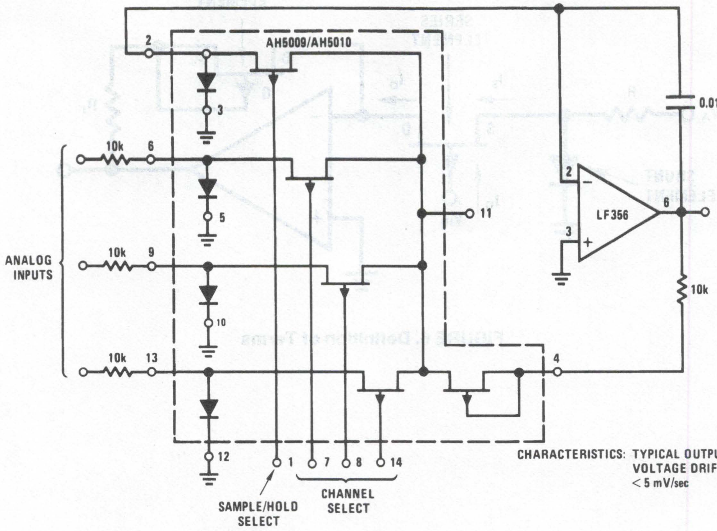
De-Glitched Switch for Noiseless Audio Switching


OFF
5V
R
ON
C
AUDIO SIGNAL INPUT
R_IN
1/4 AH5012
RC TYPICALLY (1 ms–10 ms)
R_f
LF351
OUT

TL/H/5659-7

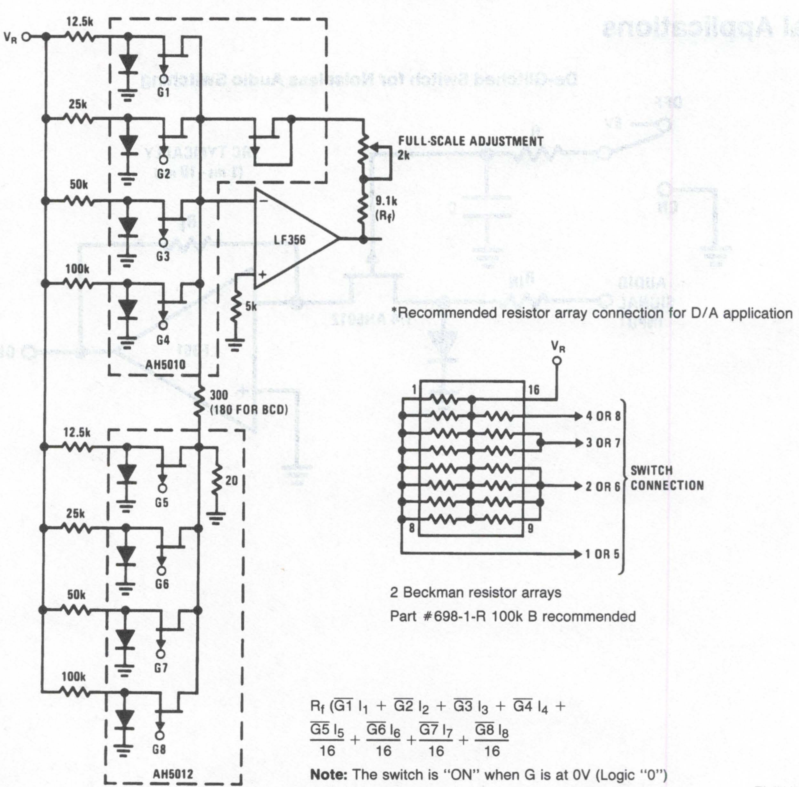
Typical Applications (Continued)

3-Channel Multiplexer with Sample and Hold


AH5009/AH5010
2
3
10k
6
5
11
ANALOG INPUTS
10k
9
10
10k
13
12
4
1
7
8
14
SAMPLE/HOLD SELECT
CHANNEL SELECT
0.01μF
2
3
LF356
6
10k

CHARACTERISTICS: TYPICAL OUTPUT VOLTAGE DRIFT < 5 mV/sec

8-Bit Binary (BCD) Multiplying D/A Converter*


V_R
12.5k
G1
25k
G2
50k
G3
100k
G4
AH5010
FULL-SCALE ADJUSTMENT
2k
9.1k
(R_f)
LF356
5k
300
(180 FOR BCD)
12.5k
G5
20
25k
G6
50k
G7
100k
G8
AH5012
V_R
1
16
8
9
4 OR 8
3 OR 7
2 OR 6
1 OR 5
SWITCH CONNECTION

*Recommended resistor array connection for D/A application

2 Beckman resistor arrays

Part #698-1-R 100k B recommended

$$R_f\left(\overline{G1}\,I_1 + \overline{G2}\,I_2 + \overline{G3}\,I_3 + \overline{G4}\,I_4 + \frac{\overline{G5}\,I_5}{16} + \frac{\overline{G6}\,I_6}{16} + \frac{\overline{G7}\,I_7}{16} + \frac{\overline{G8}\,I_8}{16}\right.$$

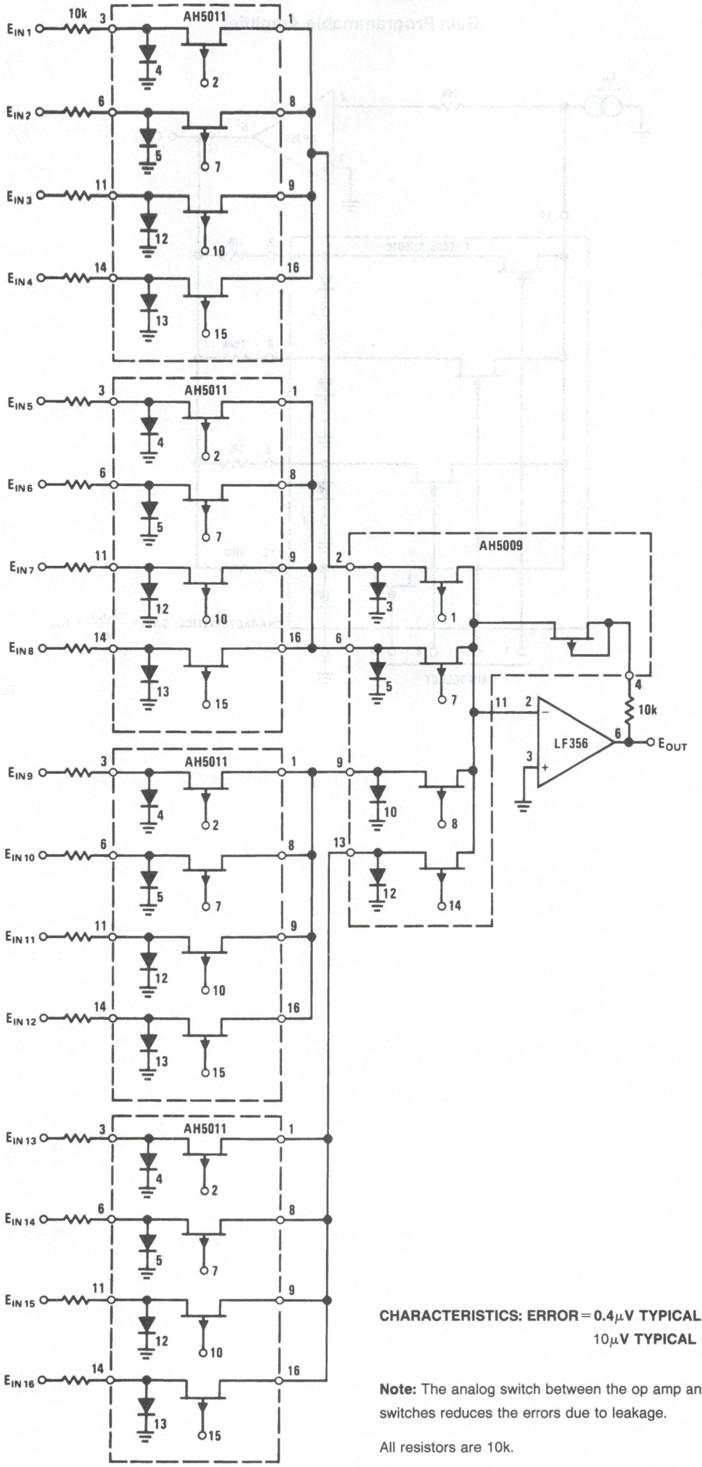
Note: The switch is "ON" when G is at 0V (Logic "0")

$$I = \frac{V_R}{R}$$

TL/H/5659-8

Typical Applications (Continued)

16-Channel Multiplexer



10k
E_{IN 1}
AH5011
AH5009
LF356
E_{OUT}
10k

CHARACTERISTICS: ERROR = $0.4\mu V$ TYPICAL @ 25°C
$10\mu V$ TYPICAL @ 70°C

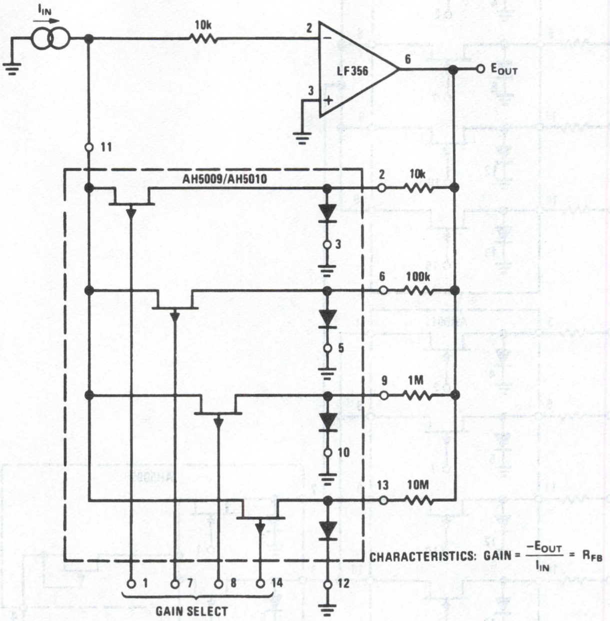
Note: The analog switch between the op amp and the 16 input switches reduces the errors due to leakage.

All resistors are 10k.

TL/H/5659-9

Typical Applications (Continued)

Gain Programmable Amplifier


I_{IN}
10k
2
LF356
3
6
E_{OUT}
11
AH5009/AH5010
2
10k
3
6
100k
5
9
1M
10
13
10M
1
7
8
14
12
GAIN SELECT

CHARACTERISTICS: GAIN = $\frac{-E_{OUT}}{I_{IN}} = R_{FB}$

TL/H/5659–10

National Semiconductor Corporation

AH5020C Monolithic Analog Current Switch

General Description

This versatile dual monolithic JFET analog switch economically fulfills a wide variety of multiplexing and analog switching applications.

These switches may be driven directly from standard 5V logic.

The monolithic construction guarantees tight resistance match and track.

Features

■ Interfaces with standard TTL	
■ "ON" resistance match	2Ω
■ Low "ON" resistance	150Ω
■ Very low leakage	50 pA
■ Large analog signal range	±10V peak
■ High switching speed	150 ns
■ Excellent isolation between channels	80 dB at 1 kHz

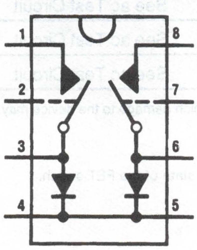
Applications

- A/D and D/A converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

For voltage switching applications see LF13201, LF13202, LF13331, LF13332, and LF13333 Analog Switch Family, or the CMOS Analog Switch Family.

Connection and Schematic Diagrams (All switches shown are for logical "1")

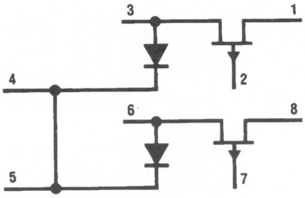
Dual-In-Line Package



TL/H/5166–1

Top View

Order Number AH5020CJ
See NS Package Number J08A



TL/H/5166–2

Note: All diode cathodes are internally connected to the substrate.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage	30V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA
Drain Current	30 mA
Power Dissipation	500 mW
Operating Temp. Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics (Notes 2 and 3)

Symbols	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	$V_{GD} = 4.5V, V_{SD} = 0.7V$ $V_{GD} = 11V, V_{SD} = 0.7V$ $T_A = 85°C, V_{GD} = 11V, V_{SD} = 0.7V$	0.01 0.01	0.1 0.2 10	nA nA nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V, V_{GS} = 3.8V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V, I_S = 1$ mA $T_A = 85°C$	0.08	1 200	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V, I_S = 2$ mA $T_A = 85°C$	0.13	5 10	nA µA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V, I_S = -2$ mA $T_A = 85°C$	0.1	10 20	nA µA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 0.5V, I_S = 2$ mA $T_A = +85°C$	90	150 240	Ω Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} = 0, I_D = 1$ mA	2	20	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Test conditions 25°C unless otherwise noted.

Note 3: "OFF" and "ON" notation refers to the conduction state of the FET switch.

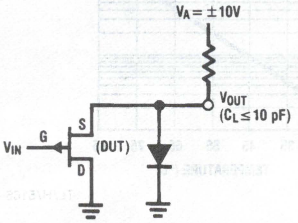
Note 4: Thermal Resistance:

θ_{JA} (Junction to Ambient) . . . . N/A

θ_{JC} (Junction to Case) . . . . N/A

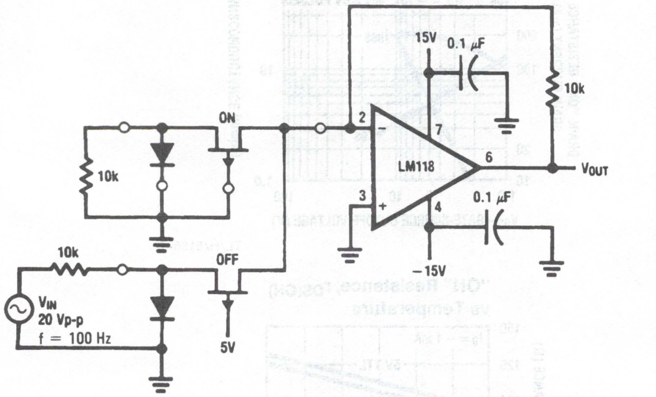
Test Circuits

AC Test Circuit


VA = ±10V
VOUT
(CL ≤ 10 pF)
G
S
D
VIN
(DUT)

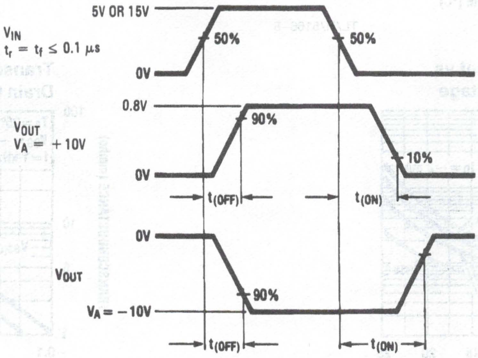
TL/H/5166-4

Cross Talk Test Circuit


15V
0.1 µF
10k
2
7
6
LM118
VOUT
3
4
0.1 µF
−15V
ON
10k
OFF
10k
VIN
20 Vp-p
f = 100 Hz
5V

TL/H/5166-3

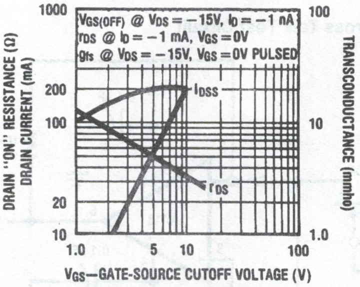
Switching Time Waveforms


5V OR 15V
VIN
tr = tf ≤ 0.1 µs
0V
50%
50%
0.8V
90%
VOUT
VA = +10V
0V
10%
t(OFF)
t(ON)
0V
VOUT
90%
VA = −10V
t(OFF)
t(ON)

TL/H/5166-5

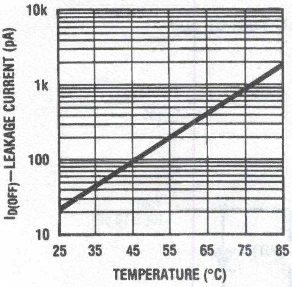
Typical Performance Characteristics

Parameter Interaction



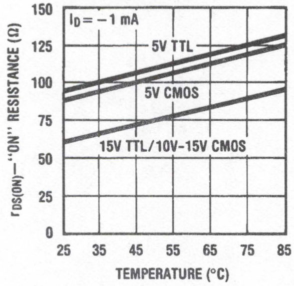
TL/H/5166–6

Leakage Current, $I_{D(OFF)}$ vs Temperature



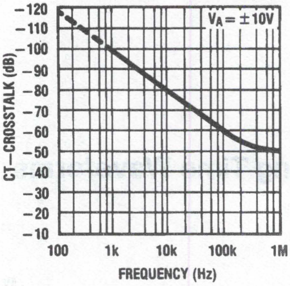
TL/H/5166–7

"ON" Resistance, $r_{DS(ON)}$ vs Temperature



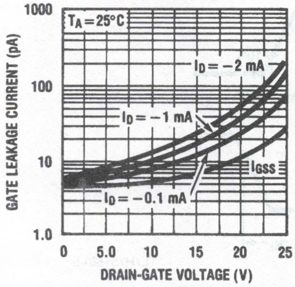
TL/H/5166–8

Cross Talk, CT vs Frequency



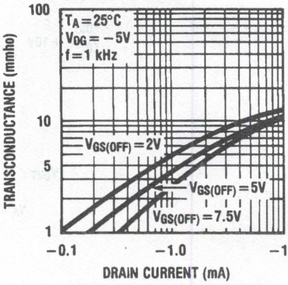
TL/H/5166–9

Leakage Current vs Drain-Gate Voltage



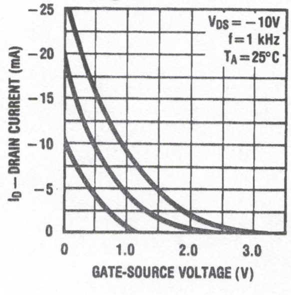
TL/H/5166–10

Transconductance vs Drain Current



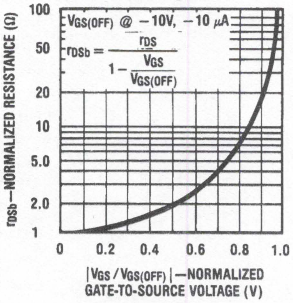
TL/H/5166–11

Drain Current vs Bias Voltage



TL/H/5166–12

Normalized Drain Resistance vs Bias Voltage



TL/H/5166–13

Applications Information

THEORY OF OPERATION

The AH5020 analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL.

If only one of the two switches in each package is used to apply an input signal to the input of an op amp, the other switch FET can be placed in the feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = -\frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 2Ω resulting in a gain accuracy of 0.02% (for R1 = R2 = 10 kΩ).

NOISE IMMUNITY

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With $V_{IN} = 15V$ and the $V_A = 10V$, the source of Q1 is clamped to about 0.7V by the diode ($V_{GS} = 14.3V$) ensuring that ac signals imposed on the 10V input will not gate the FET "ON".

SELECTION OF GAIN SETTING RESISTORS

Since the AH5020 analog switches are operated in current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2*, $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

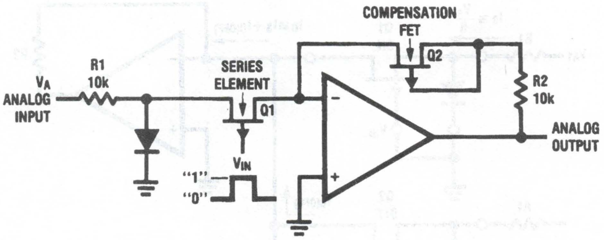
Combining the criteria from the above discussion yields:

$$R1_{(MIN)} \geq \frac{V_{A(MAX)}\, A_D}{I_{G(ON)}} \tag{2a}$$

or:

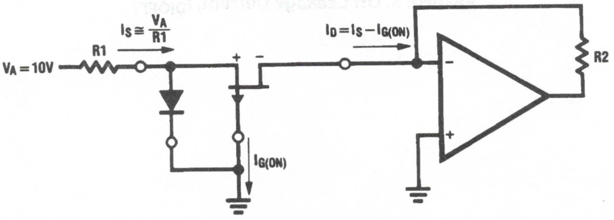
$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \tag{2b}$$

whichever is larger.



TL/H/5166-14

FIGURE 1. Use of Compensation FET



TL/H/5166-15

FIGURE 2. On Leakage Current, $I_{G(ON)}$

Applications Information (Continued)

Where $V_{A(MAX)}$ = Peak amplitude of the analog input signal

A_D = Desired accuracy

$I_{G(ON)}$ = Leakage at a given I_S

I_{DSS} = Saturation current of the FET switch = 20 mA

In a typical application, V_A might $= \pm 10V$, $A_D = 0.1\%$, $0°C \leq T_A \leq 85°C$. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{10V}{\dfrac{20\ mA}{10}} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong 10V/5k$ or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\mu A$ at 85°C for the AH5020. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3*, the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\ A_D}{(N)\ I_{D(OFF)}}$$

Where $V_{A(MIN)}$ = Minimum value for the analog input signal

A_D = Desired accuracy

N = Number of channels

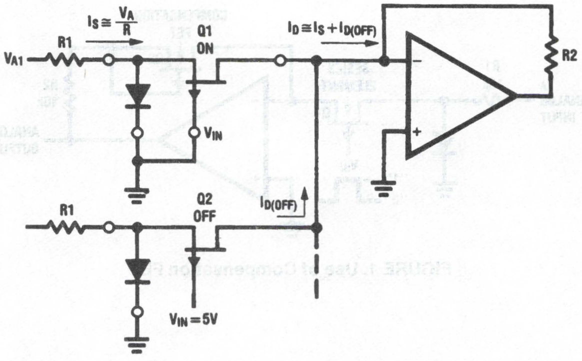
$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, $A_D = 0.1\%$, and $I_{D(OFF)} \leq 10$ nA at 85°C for the AH5020. $R1_{(MAX)}$ is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.



TL/H/5166-16

FIGURE 3. Off Leakage Current, $I_{D(OFF)}$

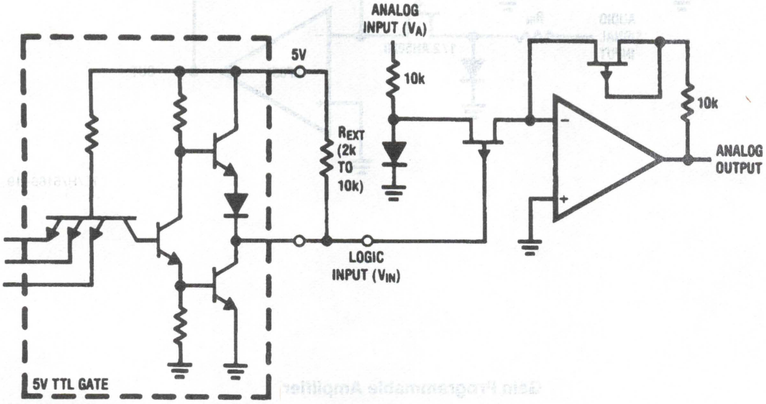
Applications Information (Continued)

TTL COMPATIBILITY

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the AH5020, a pull-up resistor, R_{EXT} of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4*.

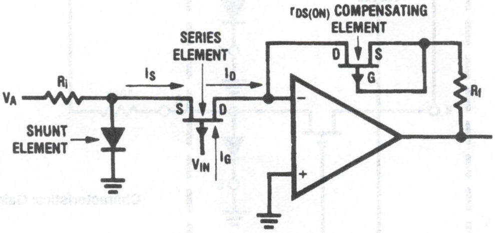
DEFINITION OF TERMS

The terms referred to in the electrical characteristics tables are as defined in *Figure 5*.


ANALOG
INPUT (V_A)
5V
10k
R_{EXT}
(2k
TO
10k)
10k
ANALOG
OUTPUT
LOGIC
INPUT (V_{IN})
5V TTL GATE

TL/H/5166-17

FIGURE 4. Interfacing with +5V TTL

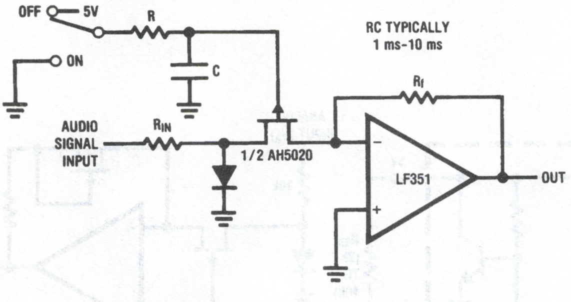

$r_{DS(ON)}$ COMPENSATING
ELEMENT
SERIES
ELEMENT
I_S
I_D
D
S
G
R_f
V_A
R_i
S
D
SHUNT
ELEMENT
V_{IN}
I_G

TL/H/5166-18

FIGURE 5. Definition of Terms

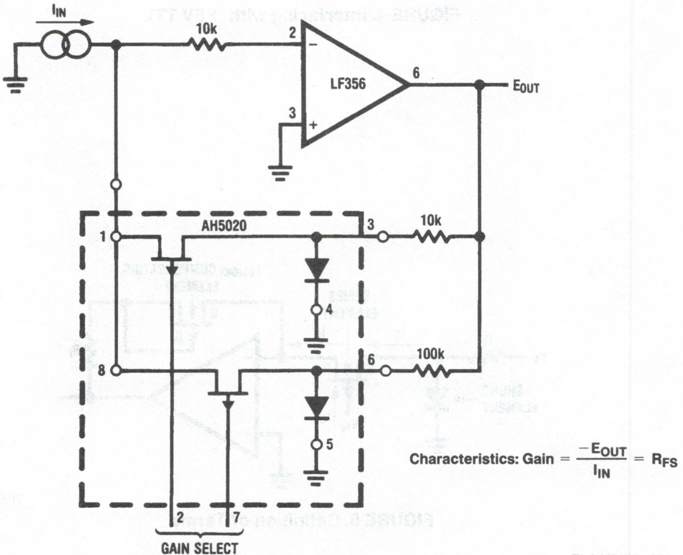
Typical Applications

Deglitched Switch for Noiseless Audio Switching


OFF
5V
R
ON
C
RC TYPICALLY
1 ms-10 ms
R_f
AUDIO
SIGNAL
INPUT
R_{IN}
1/2 AH5020
−
+
LF351
OUT

TL/H/5166-19

Gain Programmable Amplifier


I_{IN}
10k
2
−
LF356
6
E_{OUT}
3
+
AH5020
1
3
10k
4
8
6
100k
5
2
7
GAIN SELECT

$$\text{Characteristics: Gain} = \frac{-E_{OUT}}{I_{IN}} = R_{FS}$$

TL/H/5166-20

National Semiconductor Corporation

CD4016BM/CD4016BC Quad Bilateral Switch

General Description

The CD4016BM/CD4016BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4066BM/CD4066BC.

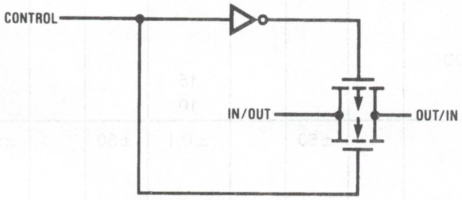
Features

- Wide supply voltage range 3V to 15V
- Wide range of digital and analog switching ±7.5 V_{PEAK}
- "ON" resistance for 15V operation 400Ω (typ.)
- Matched "ON" resistance over 15V signal input $\Delta R_{ON} = 10\Omega$ (typ.)
- High degree of linearity 0.4% distortion (typ.) @ $f_{IS} = 1$ kHz, $V_{IS} = 5$ $V_{p\text{-}p}$, $V_{DD} - V_{SS} = 10V$, $R_L = 10$ kΩ
- Extremely low "OFF" switch leakage 0.1 nA (typ.) @ $V_{DD} - V_{SS} = 10V$ $T_A = 25°C$
- Extremely high control input impedance $10^{12}\Omega$ (typ.)
- Low crosstalk between switches −50 dB (typ.) @ $f_{IS} = 0.9$ MHz, $R_L = 1$ kΩ
- Frequency response, switch "ON" 40 MHz (typ.)

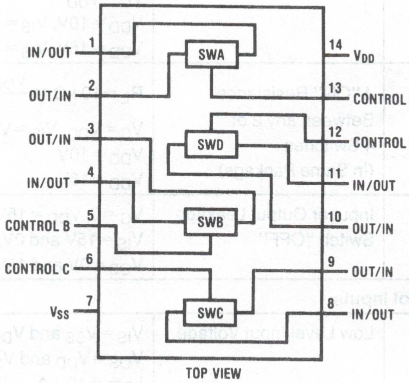
Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

Schematic and Connection Diagrams



Dual-In-Line Package



TL/F/5661–1

Cavity Dual-In-Line Package (J)
Order Number CD4016BMJ or CD4016BCJ
See NS Package Number J14A

Small Outline Package (M)
Order Number CD4016BCM
See NS Package Number M14A

Molded Dual-In-Line Package (N)
Order Number CD4016BMN or CD4016BCN
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to + 150°C
P_D Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4016BM	−55°C to +125°C
CD4016BC	−40°C to +85°C

DC Electrical Characteristics CD4016BM (Note 2)

Symbol	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		0.25		0.01	0.25		7.5	µA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		0.5		0.01	0.5		15	µA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		1.0		0.01	1.0		30	µA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ or V_{DD}								
		$V_{DD}=10V$		600		250	660		960	Ω
		$V_{DD}=15V$		360		200	400		600	Ω
		$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$								
		$V_{DD}=10V$, $V_{IS}=4.75$ to $5.25V$		1870		850	2000		2600	Ω
		$V_{DD}=15V$, $V_{IS}=7.25$ to $7.75V$		775		400	850		1230	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches (In Same Package)	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=10V$				15				Ω
		$V_{DD}=15V$				10				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C=0$, $V_{DD}=15V$ $V_{IS}=15V$ and $0V$, $V_{OS}=0V$ and $15V$		±50		±0.1	±50		±500	nA
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS}=V_{SS}$ and V_{DD} $V_{OS}=V_{DD}$ and V_{SS} $I_{IS}=\pm 10\ \mu A$								
		$V_{DD}=5V$		0.9			0.7		0.5	V
		$V_{DD}=10V$		0.9			0.7		0.5	V
		$V_{DD}=15V$		0.9			0.7		0.5	V
V_{IHC}	High Level Input Voltage	$V_{DD}=5V$	3.5		3.5			3.5		V
		$V_{DD}=10V$ (see Note 6 and	7.0		7.0			7.0		V
		$V_{DD}=15V$ *Figure 8*)	11.0		11.0			11.0		V
I_{IN}	Input Current	$V_{DD}-V_{SS}=15V$ $V_{DD}\geq V_{IS}\geq V_{SS}$ $V_{DD}\geq V_C\geq V_{SS}$		±0.1		$\pm 10^{-5}$	±0.1		±1.0	µA

DC Electrical Characteristics CD4016BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		1.0		0.01	1.0		7.5	µA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		2.0		0.01	2.0		15	µA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		4.0		0.01	4.0		30	µA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C=V_{DD}$, $V_{IS}=V_{SS}$ or V_{DD}								
		$V_{DD}=10V$		610		275	660		840	Ω
		$V_{DD}=15V$		370		200	400		520	Ω
		$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C=V_{DD}$								
		$V_{DD}=10V$, $V_{IS}=4.75$ to $5.25V$		1900		850	2000		2380	Ω
		$V_{DD}=15V$, $V_{IS}=7.25$ to $7.75V$		790		400	850		1080	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=10V$				15				Ω
	(In Same Package)	$V_{DD}=15V$				10				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C=0$, $V_{DD}=15V$ $V_{IS}=0V$ or $15V$, $V_{OS}=15V$ or $0V$		±50		±0.1	±50		±200	nA
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS}=V_{SS}$ and V_{DD} $V_{OS}=V_{DD}$ and V_{SS} $I_{IS}=\pm 10\ \mu A$								
		$V_{DD}=5V$		0.9			0.7		0.4	V
		$V_{DD}=10V$		0.9			0.7		0.4	V
		$V_{DD}=15V$		0.9			0.7		0.4	V
V_{IHC}	High Level Input Voltage	$V_{DD}=5V$	3.5		3.5			3.5		V
		$V_{DD}=10V$ (see Note 6 and	7.0		7.0			7.0		V
		$V_{DD}=15V$ *Figure 8*)	11.0		11.0			11.0		V
I_{IN}	Input Current	$V_{CC}-V_{SS}=15V$ $V_{DD}\geq V_{IS}\geq V_{SS}$ $V_{DD}\geq V_C\geq V_{SS}$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	µA

AC Electrical Characteristics $T_A=25°C$, $t_r=t_f=20$ ns and $V_{SS}=0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C=V_{DD}$, $C_L=50$ pF, (*Figure 1*) $R_L=200k$				
		$V_{DD}=5V$		58	100	ns
		$V_{DD}=10V$		27	50	ns
		$V_{DD}=15V$		20	40	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$R_L=1.0\ k\Omega$, $C_L=50$ pF, (*Figures 2* and *3*)				
		$V_{DD}=5V$		20	50	ns
		$V_{DD}=10V$		18	40	ns
		$V_{DD}=15V$		17	35	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time *Control Input to Signal* Output Logical Level to High Impedance	$R_L=1.0\ k\Omega$, $C_L=50$ pF, (*Figures 2* and *3*)				
		$V_{DD}=5V$		15	40	ns
		$V_{DD}=10V$		11	25	ns
		$V_{DD}=15V$		10	22	ns
	Sine Wave Distortion	$V_C=V_{DD}=5V$, $V_{SS}=-5$ $R_L=10\ k\Omega$, $V_{IS}=5\ V_{P-P}$, $f=1$ kHz, (*Figure 4*)		0.4		%

AC Electrical Characteristics (Continued)

$T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Frequency Response — Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5\ V_{P-P}$, $20\ Log_{10}\ V_{OS}/V_{OS}$ (1 kHz) − dB, (*Figure 4*)		40		MHz
	Feedthrough — Switch "OFF" (Frequency at −50 dB)	$V_{DD} = 5V$, $V_C = V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5\ V_{P-P}$, $20\ Log_{10}\ (V_{OS}/V_{IS}) = -50$ dB, (*Figure 4*)		1.25		MHz
	Crosstalk Between Any Two Switches (Frequency at −50 dB)	$V_{DD} = V_{C(A)} = 5V$; $V_{SS} = V_{C(B)} = -5V$, $R_L = 1\ k\Omega V_{IS(A)} = 5\ V_{P-P}$, $20\ Log_{10}\ (V_{OS(B)}/V_{OS(A)}) = -50$ dB, (*Figure 5*)		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\ k\Omega$ $R_{IN} = 1\ k\Omega$, $V_{CC} = 10V$ Square Wave, $C_L = 50$ pF (*Figure 6*)		150		mV_{P-P}
	Maximum Control Input	$R_L = 1\ k\Omega$, $C_L = 50$ pF, (*Figure 7*) $V_{OS(f)} = ½\ V_{OS}(1\ kHz)$				
		$V_{DD} = 5V$		6.5		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		9.0		MHz
C_{IS}	Signal Input Capacitance			4		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		4		pF
C_{IOS}	Feedthrough Capacitance	$V_C = 0V$		0.2		pF
C_{IN}	Control Input Capacitance			5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: If the switch input is held at V_{DD}, V_{IHC} is the control input level that will cause the switch output to meet the standard "B" series V_{OH} and I_{OH} output levels. If the analog switch input is connected to V_{SS}, V_{IHC} is the control input level — which allows the switch to *sink* standard "B" series $|I_{OH}|$, high level current, and still maintain a $V_{OL} \leq$ "B" series. These currents are shown in *Figure 8*.

Note 7: Refer to RETS4016BX for military specifications.

AC Test Circuits and Switching Time Waveforms

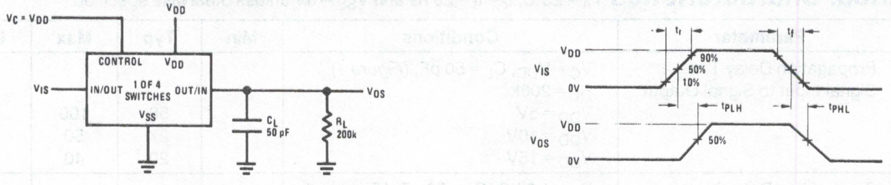


Figure 1. t_{PLH}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

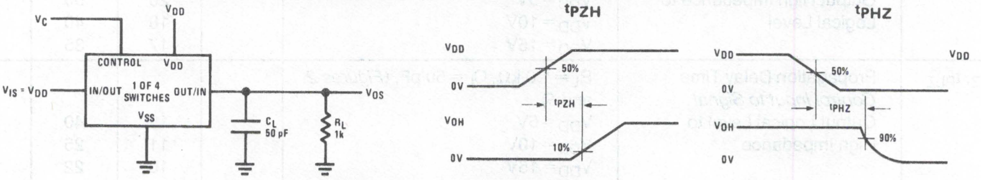


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FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

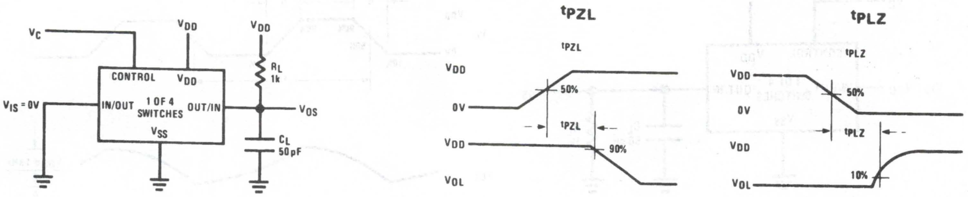
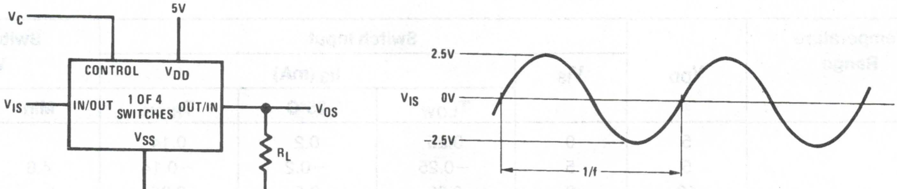

VC
VDD
VDD
CONTROL
VDD
VIS = 0V
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VSS
RL 1k
VOS
CL 50 pF
tPZL
tPZL
VDD
0V
50%
tPZL
VDD
90%
VOL
tPLZ
tPLZ
VDD
0V
50%
tPLZ
VDD
10%
VOL

FIGURE 3. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output


VC
5V
CONTROL
VDD
VIS
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS
VSS
RL
−5V
2.5V
VIS
0V
−2.5V
1/f

$V_C = V_{DD}$ for distortion and frequency response tests

$V_C = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

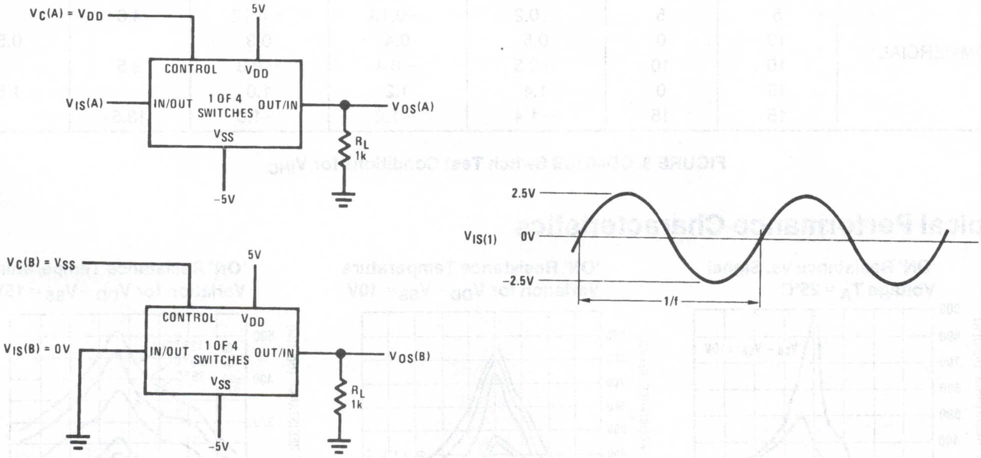

VC(A) = VDD
5V
CONTROL
VDD
VIS(A)
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS(A)
VSS
RL 1k
−5V
2.5V
VIS(1)
0V
−2.5V
1/f
VC(B) = VSS
5V
CONTROL
VDD
VIS(B) = 0V
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS(B)
VSS
RL 1k
−5V

FIGURE 5. Crosstalk Between Any Two Switches

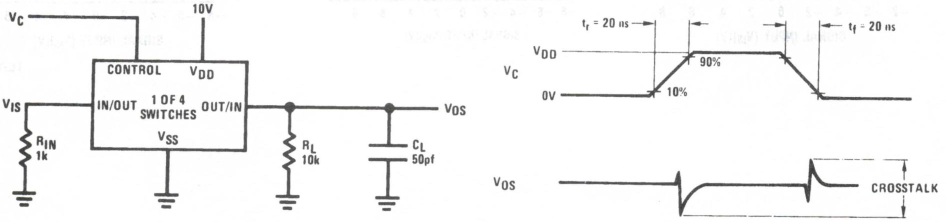

VC
10V
CONTROL
VDD
VIS
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS
VSS
RIN 1k
RL 10k
CL 50pf
tr = 20 ns
tf = 20 ns
VDD
VC
0V
90%
10%
VOS
CROSSTALK

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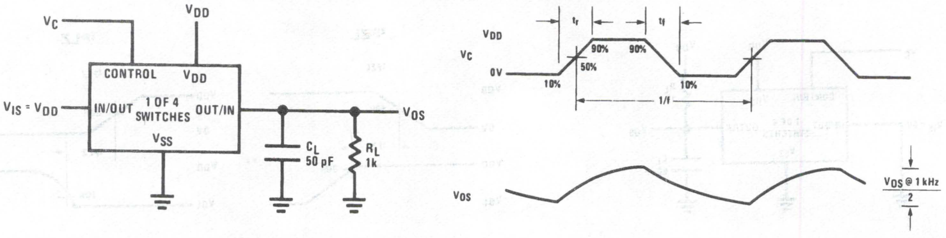
FIGURE 6. Crosstalk — Control to Input Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)


V_C
V_DD
CONTROL
V_DD
V_IS = V_DD
IN/OUT
1 OF 4 SWITCHES
OUT/IN
V_SS
C_L 50 pF
R_L 1k
V_OS
V_DD
V_C
0V
t_r
t_f
90%
90%
50%
10%
10%
1/f
V_OS
V_OS @ 1 kHz / 2

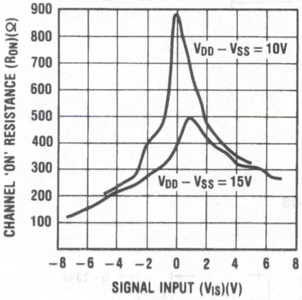
TL/F/5661-4

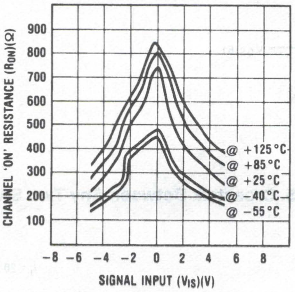
FIGURE 7. Maximum Control Input Frequency

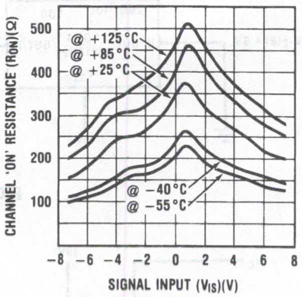
Temperature Range	V_{DD}	Switch Input				Switch Output V_{OS}(V)	
		V_{IS}	I_{IS} (mA)				
			T_{LOW}	25°C	T_{HIGH}	Min	Max
MILITARY	5	0	0.25	0.2	0.14		0.4
	5	5	−0.25	−0.2	−0.14	4.6	
	10	0	0.62	0.5	0.35		0.5
	10	10	−0.62	−0.5	−0.35	9.5	
	15	0	1.8	1.5	1.1		1.5
	15	15	−1.8	−1.5	−1.1	13.5	
COMMERCIAL	5	0	0.2	0.16	0.12		0.4
	5	5	−0.2	−0.16	−0.12	4.6	
	10	0	0.5	0.4	0.3		0.5
	10	10	−0.5	−0.4	−0.3	9.5	
	15	0	1.4	1.2	1.0		1.5
	15	15	−1.4	−1.2	−1.0	13.5	

FIGURE 8. CD4016B Switch Test Conditions for V_{IHC}

Typical Performance Characteristics


'ON' Resistance vs. Signal Voltage $T_A = 25°C$

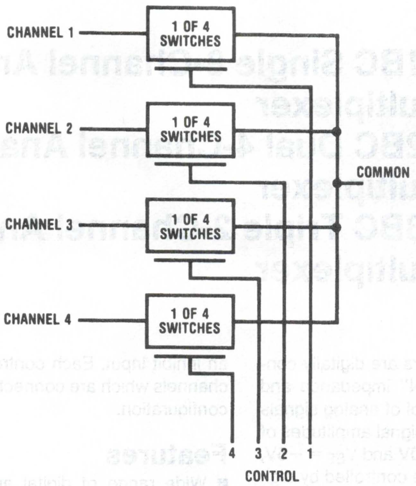

'ON' Resistance Temperature Variation for $V_{DD} - V_{SS} = 10V$


'ON' Resistance Temperature Variation for $V_{DD} - V_{SS} = 15V$

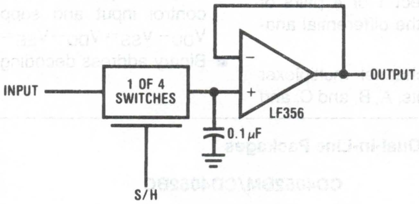
TL/F/5661-5

Typical Applications

4 Input Multiplexer


CHANNEL 1
1 OF 4 SWITCHES
CHANNEL 2
1 OF 4 SWITCHES
COMMON
CHANNEL 3
1 OF 4 SWITCHES
CHANNEL 4
1 OF 4 SWITCHES
4
3
2
1
CONTROL

Sample/Hold Amplifier


INPUT
1 OF 4 SWITCHES
−
+
OUTPUT
LF356
0.1 μF
S/H

TL/F/5661-6

Special Considerations

The CD4016B is composed of 4, two-transistor analog switches. These switches do not have any linearization or compensation circuitry for "R_{ON}" as do the CD4066B's. Because of this, the special operating considerations for the CD4066B do not apply to the CD4016B, but at low supply voltages, ≤5V, the CD4016B's on resistance becomes non-linear. It is recommended that at 5V, voltages on the in/out pins be maintained within about 1V of either V_{DD} or V_{SS}; and that at 3V the voltages on the in/out pins should be at V_{DD} or V_{SS} for reliable operation.

National
Semiconductor
Corporation

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15V_{p\text{-}p}$ can be achieved by digital signal amplitudes of 3–15V. For example, if $V_{DD}=5V$, $V_{SS}=0V$ and $V_{EE}=-5V$, analog signals from $-5V$ to $+5V$ can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs. A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

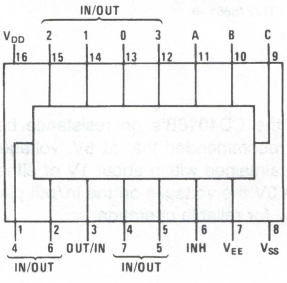
Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to $15V_{p\text{-}p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p\text{-}p}$ signal-input range for $V_{DD}-V_{EE}=15V$
- High "OFF" resistance: channel leakage of ±10 pA (typ.) at $V_{DD}-V_{EE}=10V$
- Logic level conversion for digital addressing signals of 3–15V ($V_{DD}-V_{SS}=3\text{–}15V$) to switch analog signals to 15 $V_{p\text{-}p}$ ($V_{DD}-V_{EE}=15V$)
- Matched switch characteristics: $\Delta R_{ON}=5\Omega$ (typ.) for $V_{DD}-V_{EE}=15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ.) at $V_{DD}-V_{SS}=V_{DD}-V_{EE}=10V$
- Binary address decoding on chip

Connection Diagrams

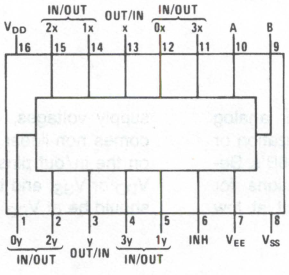
Dual-In-Line Packages

CD4051BM/CD4051BC



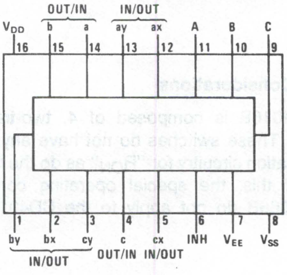
TOP VIEW

CD4052BM/CD4052BC



TOP VIEW

CD4053BM/CD4053BC



TOP VIEW

TL/F/5662–1

Cavity Dual-In-Line Package (J)
Order Number CD4051BMJ, CD4051BCJ, CD4052BMJ, CD4052BCJ, CD4053BMJ, or CD4053BCJ
See NS Package Number J16A

Small Outline Package (M)
Order Number CD4051BCM, CD4052BCM or CD4053BCM
See NS Package Number M16A

Molded Dual-In-Line Package (N)
Order Number CD4051BMN, CD4051BCN, CD4052BMN, CD4052BCN, CD4053BMN, or CD4053BCN
See NS Package Number N16E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 4)

V_{DD}	DC Supply Voltage	−0.5 Vdc to +18 Vdc
V_{IN}	Input Voltage	−0.5 Vdc to V_{DD}+0.5 Vdc
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	260°C

Recommended Operating Conditions

V_{DD}	DC Supply Voltage	+5 Vdc to +15 Vdc
V_{IN}	Input Voltage	0V to V_{DD} Vdc
T_A	Operating Temperature Range	
	4051BM/4052BM/4053BM	−55°C to +125°C
	4051BC/4052BC/4053BC	−40°C to +85°C

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		−55°C		+25°			+125°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD}=5V			5			5		150	µA
		V_{DD}=10V			10			10		300	µA
		V_{DD}=15V			20			20		600	µA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \leq V_{IS} \leq V_{DD}$)	R_L=10 kΩ (any channel selected)	V_{DD}=2.5V, V_{EE}=−2.5V or V_{DD}=5V, V_{EE}=0V		800		270	1050		1300	Ω
			V_{DD}=5V, V_{EE}=−5V or V_{DD}=10V, V_{EE}=0V		310		120	400		550	Ω
			V_{DD}=7.5V, V_{EE}=−7.5V or V_{DD}=15V, V_{EE}=0V		200		80	240		320	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	R_L=10 kΩ (any channel selected)	V_{DD}=2.5V, V_{EE}=−2.5V or V_{DD}=5V, V_{EE}=0V				10				Ω
			V_{DD}=5V, V_{EE}=−5V or V_{DD}=10V, V_{EE}=0V				10				Ω
			V_{DD}=7.5V, V_{EE}=−7.5V or V_{DD}=15V, V_{EE}=0V				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	V_{DD}=7.5V, V_{EE}=−7.5V O/I=±7.5V, I/O=0V			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit=7.5V	CD4051		±200		±0.08	±200		±2000	nA
		V_{DD}=7.5V, V_{EE}=−7.5V, O/I=0V,	CD4052		±200		±0.04	±200		±2000	nA
		I/O=±7.5V	CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	V_{EE}=V_{SS} R_L=1 kΩ to V_{SS} I_{IS}<2 µA on all OFF channels V_{IS}=V_{DD} thru 1 kΩ									
		V_{DD}=5V			1.5			1.5		1.5	V
		V_{DD}=10V			3.0			3.0		3.0	V
		V_{DD}=15V			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD}=5		3.5		3.5			3.5		V
		V_{DD}=10		7		7			7		V
		V_{DD}=15		11		11			11		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics (Note 2) (Continued)

Symbol	Parameter	Conditions		−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Units
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$	$V_{EE}=0V$		−0.1		-10^{-5}	−0.1		−1.0	µA
		$V_{DD}=15V$, $V_{IN}=15V$	$V_{EE}=0V$		0.1		10^{-5}	0.1		1.0	µA
I_{DD}	Quiescent Device Current	$V_{DD}=5V$			20			20		150	µA
		$V_{DD}=10V$			40			40		300	µA
		$V_{DD}=15V$			80			80		600	µA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \le V_{IS} \le V_{DD}$)	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$		850		270	1050		1200	Ω
			$V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$		330		120	400		520	Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$		210		80	240		300	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	$V_{DD}=7.5V$, O/I = ±7.5V,	$V_{EE}=-7.5V$ I/O = 0V		±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V $V_{DD}=7.5V$, $V_{EE}=-7.5V$, O/I = 0V I/O = ±7.5V	CD4051		±200		±0.08	±200		±2000	nA
			CD4052		±200		±0.04	±200		±2000	nA
			CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	$V_{EE}=V_{SS}$ $R_L=1\ k\Omega$ to V_{SS} $I_{IS}<2\ \mu A$ on all OFF Channels $V_{IS}=V_{DD}$ thru 1 kΩ $V_{DD}=5V$			1.5			1.5		1.5	V
		$V_{DD}=10V$			3.0			3.0		3.0	V
		$V_{DD}=15V$			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5$		3.5		3.5			3.5		V
		$V_{DD}=10$		7		7			7		V
		$V_{DD}=15$		11		11			11		V
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$	$V_{EE}=0V$		−0.1		-10^{-5}	−0.1		−1.0	µA
		$V_{DD}=15V$, $V_{IN}=15V$	$V_{EE}=0V$		0.1		10^{-5}	0.1		1.0	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

AC Electrical Characteristics

$T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

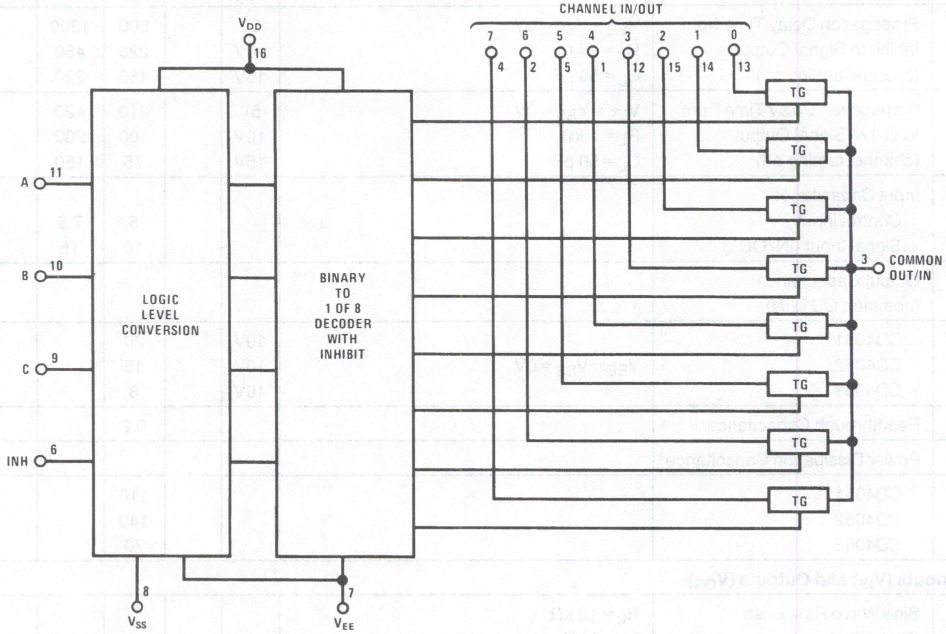
Symbol	Parameter	Conditions	V_{pp}	Min	Typ	Max	Units
t_{PZH} t_{PZL}	Propagation Delay Time from Inhibit to Signal Output (channel turning on)	$V_{EE} = V_{SS} = 0V$ $R_L = 1\ k\Omega$ $C_L = 50\ pF$	5V 10V 15V		600 225 160	1200 450 320	ns ns ns
t_{PHZ} t_{PLZ}	Propagation Delay Time from Inhibit to Signal Output (channel turning off)	$V_{EE} = V_{SS} = 0V$ $R_L = 1\ k\Omega$ $C_L = 50\ pF$	5V 10V 15V		210 100 75	420 200 150	ns ns ns
C_{IN}	Input Capacitance Control input Signal Input (IN/OUT)				 5 10	 7.5 15	 pF pF
C_{OUT}	Output Capacitance (common OUT/IN)						
	CD4051 CD4052 CD4053	$V_{EE} = V_{SS} = 0V$	10V 10V 10V		30 15 8		pF pF pF
C_{IOS}	Feedthrough Capacitance				0.2		pF
C_{PD}	Power Dissipation Capacitance						
	CD4051 CD4052 CD4053				110 140 70		pF pF pF
Signal Inputs (V_{IS}) and Outputs (V_{OS})							
	Sine Wave Response (Distortion)	$R_L = 10\ k\Omega$ $f_{IS} = 1$ kHz $V_{IS} = 5\ V_{p-p}$ $V_{EE} = V_{SI} = 0V$	10V		0.04		%
	Frequency Response, Channel "ON" (Sine Wave Input)	$R_L = 1\ k\Omega$, $V_{EE} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -3$ dB	10V		40		MHz
	Feedthrough, Channel "OFF"	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -40$ dB	10V		10		MHz
	Crosstalk Between Any Two Channels (frequency at 40 dB)	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p-p}$ $20 \log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 3)	10V		3		MHz
t_{PHL} t_{PLH}	Propagation Delay Signal Input to Signal Output	$V_{EE} = V_{SS} = 0V$ $C_L = 50\ pF$	5V 10V 15V		25 15 10	55 35 25	ns ns ns
Control Inputs, A, B, C and Inhibit							
	Control Input to Signal Crosstalk	$V_{EE} = V_{SS} = 0V$, $R_L = 10\ k\Omega$ at both ends of channel. Input Square Wave Amplitude = 10V	10V		65		mV (peak)
t_{PHL}, t_{PLH}	Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF")	$V_{EE} = V_{SS} = 0V$ $C_L = 50\ pF$	5V 10V 15V		500 180 120	1000 360 240	ns ns ns

Note 3: A, B are two arbitrary channels with A turned "ON" and B "OFF".

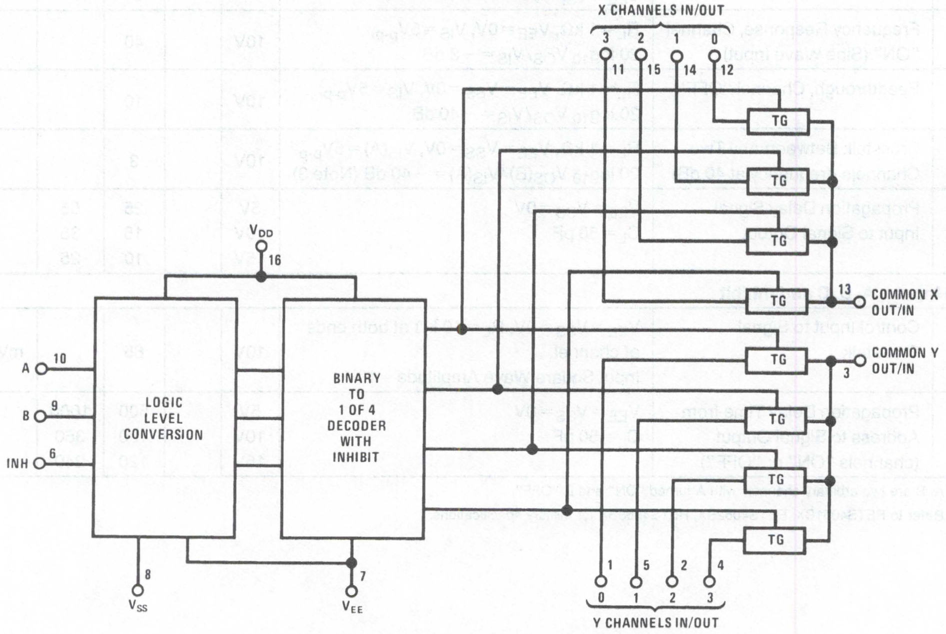
Note 4: Refer to RETS4051BX, RETS4052BX, RETS4053BX for military specifications.

Block Diagrams

CD4051BM/CD4051BC


CHANNEL IN/OUT
7
6
5
4
3
2
1
0
4
2
5
1
12
15
14
13
V_DD
16
A
11
B
10
C
9
INH
6
LOGIC LEVEL CONVERSION
BINARY TO 1 OF 8 DECODER WITH INHIBIT
TG
3
COMMON OUT/IN
8
V_SS
7
V_EE

CD4052BM/CD4052BC


X CHANNELS IN/OUT
3
2
1
0
11
15
14
12
V_DD
16
A
10
B
9
INH
6
LOGIC LEVEL CONVERSION
BINARY TO 1 OF 4 DECODER WITH INHIBIT
TG
13
COMMON X OUT/IN
COMMON Y OUT/IN
3
8
V_SS
7
V_EE
1
5
2
4
0
1
2
3
Y CHANNELS IN/OUT

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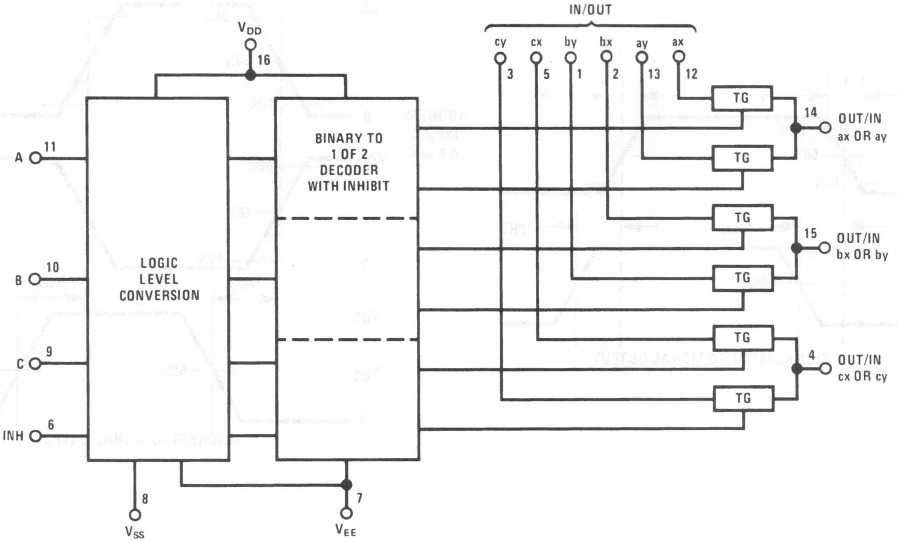
Block Diagrams (Continued)

CD4053BM/CD4053BC


IN/OUT
cy
cx
by
bx
ay
ax
3
5
1
2
13
12
V_{DD}
16
A
11
B
10
C
9
INH
6
LOGIC LEVEL CONVERSION
BINARY TO 1 OF 2 DECODER WITH INHIBIT
TG
14
OUT/IN ax OR ay
15
OUT/IN bx OR by
4
OUT/IN cx OR cy
8
V_{SS}
7
V_{EE}

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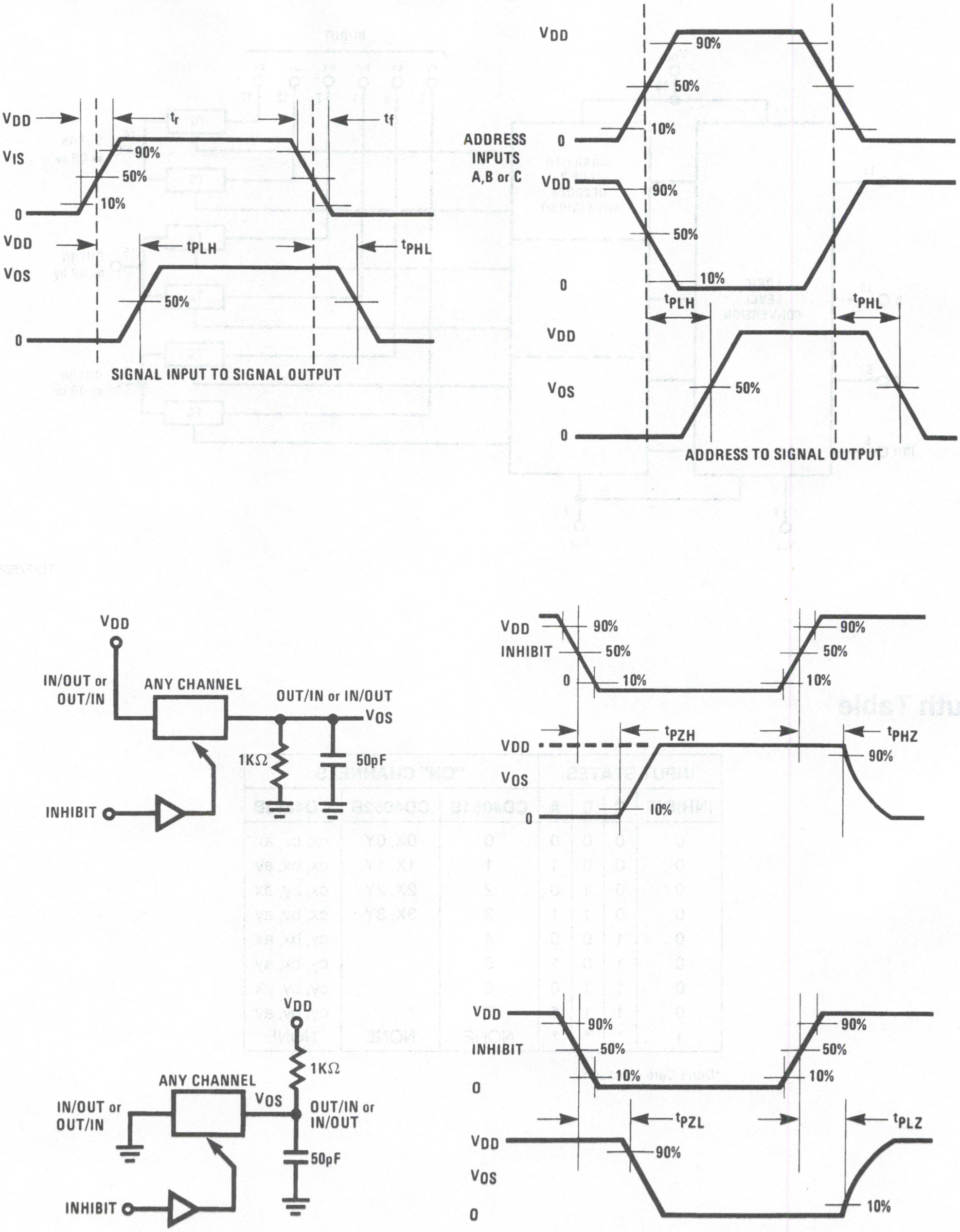
Truth Table

INPUT STATES				“ON” CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

*Don’t Care condition.

Switching Time Waveforms


VDD
VIS
0
tr
tf
90%
50%
10%
VDD
VOS
0
tPLH
tPHL
50%
SIGNAL INPUT TO SIGNAL OUTPUT
VDD
ADDRESS INPUTS A,B or C
0
VDD
0
90%
50%
10%
tPLH
tPHL
VDD
VOS
0
50%
ADDRESS TO SIGNAL OUTPUT
VDD
IN/OUT or OUT/IN
ANY CHANNEL
OUT/IN or IN/OUT
VOS
1KΩ
50pF
INHIBIT
VDD
INHIBIT
0
90%
50%
10%
tPZH
tPHZ
VDD
VOS
0
90%
10%
VDD
1KΩ
ANY CHANNEL
IN/OUT or OUT/IN
VOS
OUT/IN or IN/OUT
50pF
INHIBIT
VDD
INHIBIT
0
90%
50%
10%
tPZL
tPLZ
VDD
VOS
0
90%
10%

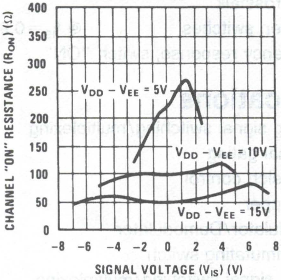
TL/F/5662-4

Special Considerations

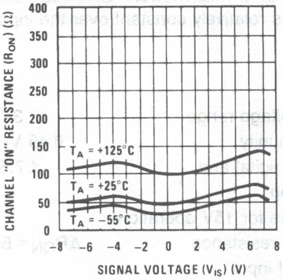
In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

Typical Performance Characteristics

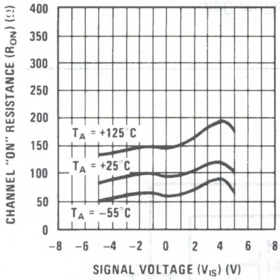
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



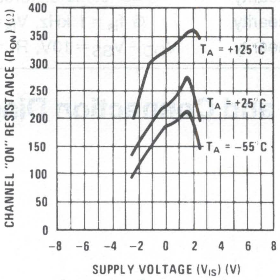
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$



TL/F/5662-5

National Semiconductor Corporation

CD4066BM/CD4066BC Quad Bilateral Switch

General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

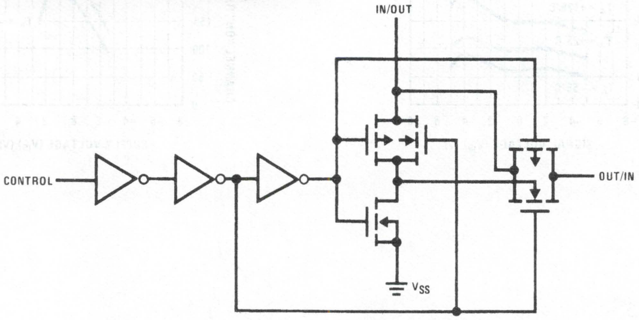
Features

- Wide supply voltage range 3V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Wide range of digital and analog switching ±7.5 V_{PEAK}
- "ON" resistance for 15V operation 80Ω
- Matched "ON" resistance over 15V signal input $\Delta R_{ON}=5\Omega$ (typ.)
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio 65 dB (typ.) @ $f_{is}=10$ kHz, $R_L=10$ kΩ
- High degree linearity 0.1% distortion (typ.)
  High degree linearity @ $f_{is}=1$ kHz, $V_{is}=5V_{p\text{-}p}$,
  High degree linearity $V_{DD}-V_{SS}=10V$, $R_L=10$ kΩ
- Extremely low "OFF" switch leakage 0.1 nA (typ.) @ $V_{DD}-V_{SS}=10V$, $T_A=25°C$
- Extremely high control input impedance $10^{12}\Omega$(typ.)
- Low crosstalk between switches −50 dB (typ.) @ $f_{is}=0.9$ MHz, $R_L=1$ kΩ
- Frequency response, switch "ON" 40 MHz (typ.)

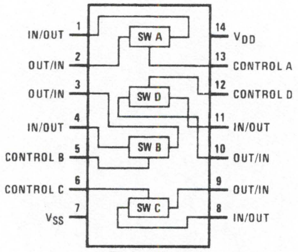
Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

Schematic and Connection Diagrams



Dual-In-Line Package



Top View

Cavity Dual-In-Line Package (J)
Order Number CD4066BMJ or CD4066BCJ
See NS Package Number J14A

Molded Dual-In-Line Package (N)
Order Number CD4066BMN or CD4066BCN
See NS Package Number N14A

Small Outline Package (M)
Order Number CD4066BCM
See NS Package Number M14A

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Absolute Maximum Ratings

(Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD}+0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

DC Electrical Characteristics CD4066BM (Note 2)

Symbol	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		0.25		0.01	0.25		7.5	μA
		$V_{DD}=10V$		0.5		0.01	0.5		15	μA
		$V_{DD}=15V$		1.0		0.01	1.0		30	μA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=5V$		800		270	1050		1300	Ω
		$V_{DD}=10V$		310		120	400		550	Ω
		$V_{DD}=15V$		200		80	240		320	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=10V$				10				Ω
		$V_{DD}=15V$				5				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C=0$ $V_{IS}=15V$ and 0V, $V_{OS}=0V$ and 15V		±50		±0.1	±50		±500	nA
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS}=V_{SS}$ and V_{DD} $V_{OS}=V_{DD}$ and V_{SS} $I_{IS}=\pm 10\ \mu A$								
		$V_{DD}=5V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10V$		3.0		4.5	3.0		3.0	V
		$V_{DD}=15V$		4.0		6.75	4.0		4.0	V
V_{IHC}	High Level Input Voltage	$V_{DD}=5V$	3.5		3.5	2.75		3.5		V
		$V_{DD}=10V$ (see note 6)	7.0		7.0	5.5		7.0		V
		$V_{DD}=15V$	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD}-V_{SS}=15V$ $V_{DD}\geq V_{IS}\geq V_{SS}$ $V_{DD}\geq V_C\geq V_{SS}$		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA

DC Electrical Characteristics CD4066BC (Note 2)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		1.0		0.01	1.0		7.5	μA
		$V_{DD}=10V$		2.0		0.01	2.0		15	μA
		$V_{DD}=15V$		4.0		0.01	4.0		30	μA

DC Electrical Characteristics (Continued) CD4066BC (Note 2)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C = V_{DD}$, V_{SS} to V_{DD}								
		$V_{DD} = 5V$		850		270	1050		1200	Ω
		$V_{DD} = 10V$		330		120	400		520	Ω
		$V_{DD} = 15V$		210		80	240		300	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any 2 of 4 Switches	$R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_{CC} = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
		$V_{DD} = 10V$				10				Ω
		$V_{DD} = 15V$				5				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C = 0$		±50		±0.1	±50		±200	nA
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS} = V_{SS}$ and V_{DD}								
		$V_{OS} = V_{DD}$ and V_{SS}								
		$I_{IS} = \pm 10\mu A$								
		$V_{DD} = 5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$		4.0		6.75	4.0		4.0	V
V_{IHC}	High Level Input Voltage	$V_{DD} = 5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$ (See note 6)	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD} - V_{SS} = 15V$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA
		$V_{DD} \geq V_{IS} \geq V_{SS}$								
		$V_{DD} \geq V_C \geq V_{SS}$								

AC Electrical Characteristics $T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C = V_{DD}$, $C_L = 50$ pF, (*Figure 1*)				
		$R_L = 200k$				
		$V_{DD} = 5V$		25	55	ns
		$V_{DD} = 10V$		15	35	ns
		$V_{DD} = 15V$		10	25	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, (*Figures 2* and *3*)				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, (*Figures 2* and *3*)				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
	Sine Wave Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$ $R_L = 10\ k\Omega$, $V_{IS} = 5V_{p\text{-}p}$, $f = 1$ kHz, (*Figure 4*)		0.1		%
	Frequency Response-Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5V_{p\text{-}p}$, $20\ \text{Log}_{10}\ V_{OS}/V_{OS}$ (1 kHz) − dB, (*Figure 4*)		40		MHz

AC Electrical Characteristics (Continued) $T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Feedthrough — Switch "OFF" (Frequency at −50 dB)	$V_{DD} = 5.0V$, $V_{CC} = V_{SS} = -5.0V$, $R_L = 1\ k\Omega$, $V_{IS} = 5.0V_{p-p}$, 20 Log_{10}, $V_{OS}/V_{IS} = -50$ dB, *(Figure 4)*		1.25		
	Crosstalk Between Any Two Switches (Frequency at −50 dB)	$V_{DD} = V_{C(A)} = 5.0V$; $V_{SS} = V_{C(B)} = 5.0V$, $R_L 1\ k\Omega$, $V_{IS(A)} = 5.0\ V_{p-p}$, 20 Log_{10}, $V_{OS(B)}/V_{IS(A)} = -50$ dB *(Figure 5)*		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\ k\Omega$, $R_{IN} = 1.0\ k\Omega$, $V_{CC} = 10V$ Square Wave, $C_L = 50$ pF *(Figure 6)*		150		mV_{p-p}
	Maximum Control Input	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, *(Figure 7)* $V_{OS(f)} = ½\ V_{OS}(1.0\ kHz)$				
		$V_{DD} = 5.0V$		6.0		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		8.5		MHz
C_{IS}	Signal Input Capacitance			8.0		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		8.0		pF
C_{IOS}	Feedthrough Capacitance	$V_C = 0V$		0.5		pF
C_{IN}	Control Input Capacitance			5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance in the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: Conditions for V_{IHC}: a) $V_{IS} = V_{DD}$, I_{OS} = standard B series I_{OH} b) $V_{IS} = 0V$, I_{OL} = standard B series I_{OL}.

Note 7: Refer to RETS4066BX for military specifications.

AC Test Circuits and Switching Time Waveforms

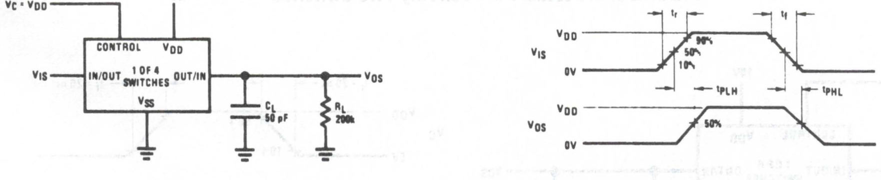
VC = VDD
VDD
CONTROL
VDD
VIS
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VSS
CL 50 pF
RL 200k
VOS
tr
tf
VDD
VIS
0V
90%
50%
10%
tPLH
tPHL
VDD
VOS
0V
50%

FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

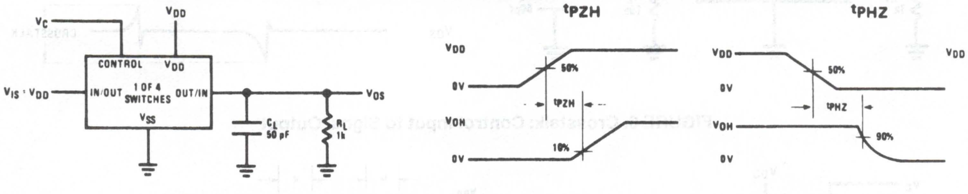
tPZH
tPHZ
VC
VDD
CONTROL
VDD
VIS = VDD
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VSS
CL 50 pF
RL 1k
VOS
VDD
0V
50%
tPZH
VOH
0V
10%
VDD
0V
50%
tPHZ
VOH
0V
90%
VDD

FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

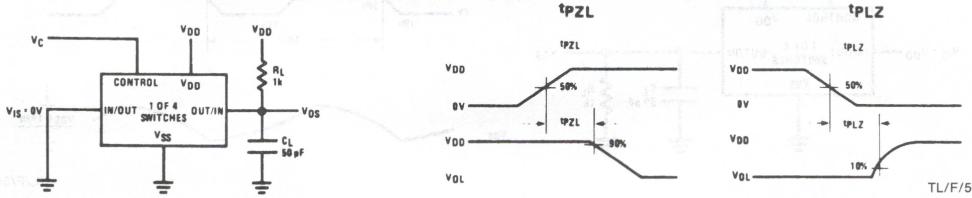
tPZL
tPLZ
VC
VDD
VDD
CONTROL
VDD
RL 1k
VIS = 0V
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS
VSS
CL 50 pF
tPZL
VDD
0V
50%
tPZL
VDD
VOL
90%
tPLZ
VDD
0V
50%
tPLZ
VDD
VOL
10%

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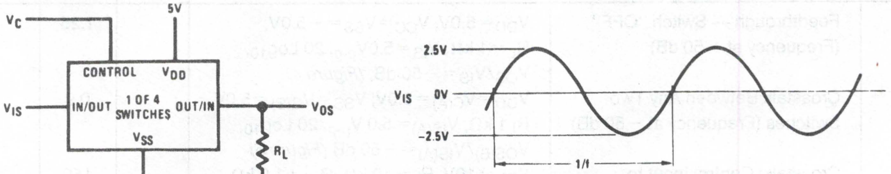
FIGURE 3. t_{PZL}, t_{PLZ} Propagtion Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)


VC
5V
CONTROL
VDD
VIS
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS
VSS
RL
−5V
2.5V
VIS
0V
−2.5V
1/f

$V_C = V_{DD}$ for distortion and frequency response tests
$V_C = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

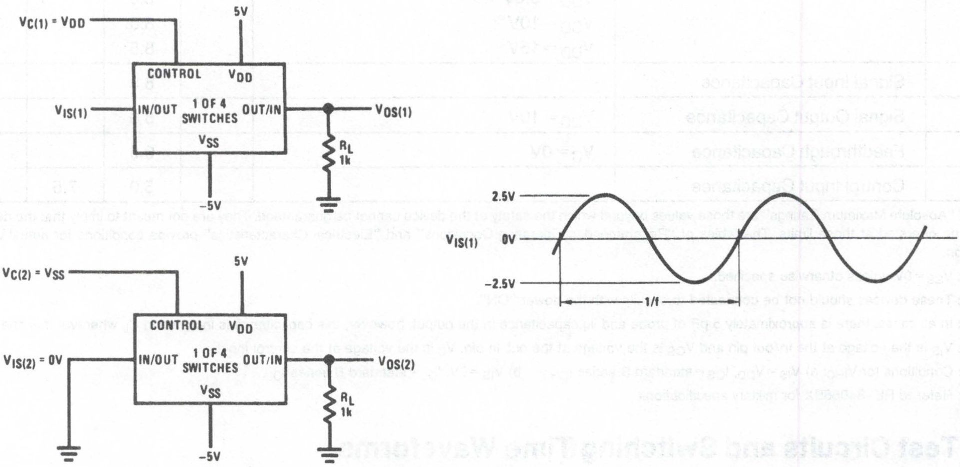

VC(1) = VDD
5V
CONTROL
VDD
VIS(1)
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS(1)
VSS
RL 1k
−5V
2.5V
VIS(1)
0V
−2.5V
1/f
VC(2) = VSS
5V
CONTROL
VDD
VIS(2) = 0V
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS(2)
VSS
RL 1k
−5V

FIGURE 5. Crosstalk Between Any Two Switches

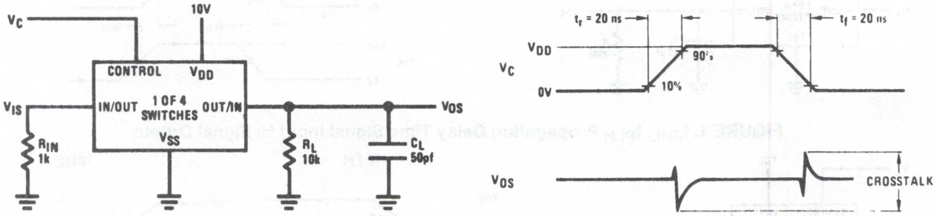

VC
10V
CONTROL
VDD
VIS
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS
RIN 1k
VSS
RL 10k
CL 50pf
tr = 20 ns
tf = 20 ns
VDD
VC
90%
0V
10%
VOS
CROSSTALK

FIGURE 6. Crosstalk: Control Input to Signal Output

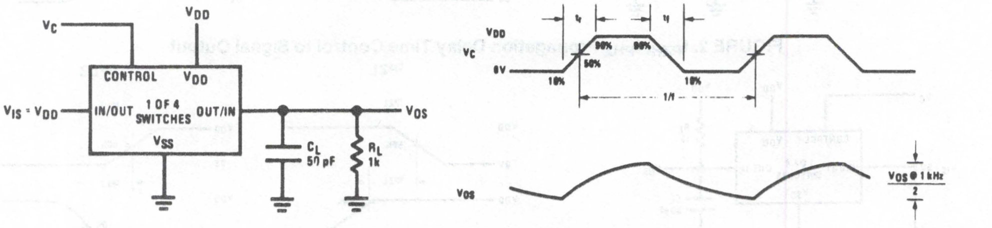

VC
VDD
CONTROL
VDD
VIS = VDD
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS
VSS
CL 50 pF
RL 1k
tr
tf
VDD
VC
90%
90%
50%
0V
10%
10%
1/f
VOS
VOS @ 1 kHz / 2

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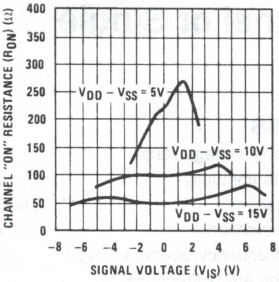
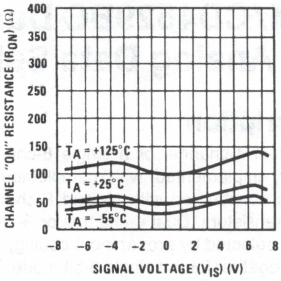
FIGURE 7. Maximum Control Input Frequency

Typical Performance Characteristics

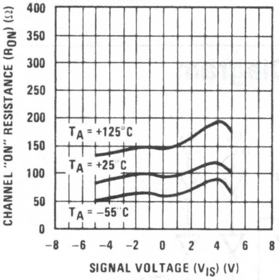
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



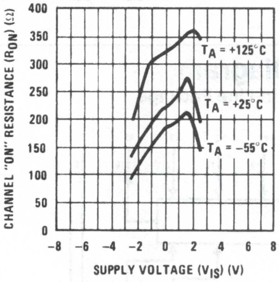
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 5V$



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Special Considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action of the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

National Semiconductor Corporation

CD4529BM/CD4529BC Dual 4-Channel or Single 8-Channel Analog Data Selector

General Description

The CD4529B is a dual 4-channel or a single 8-channel analog data selector, implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. Dual 4-channel or 8-channel mode operation is selected by proper input coding, with outputs Z and W tied together for the single 8-bit mode. The device is suitable for digital as well as analog applications, including various 1-of-4 and 1-of-8 data selector functions. Since the device is analog and bidirectional, it can also be used for dual binary to 1-of-4 or single 1-of-8 decoder applications.

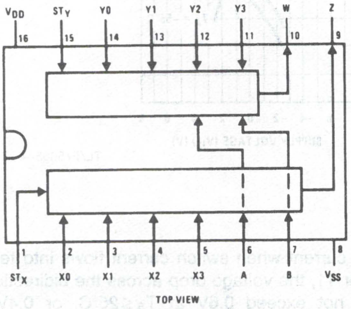
Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low quiescent power dissipation	0.005 μW/package (typ.) @ 5.0 V_{DC}

- ■ 10 MHz frequency operation (typ.)
- ■ Data paths are bidirectional
- ■ Linear ON resistance [120Ω (typ.) @ 15V]
- ■ TRI-STATE® outputs (high impedance disable strobe)
- ■ Plug-in replacement for MC14529B

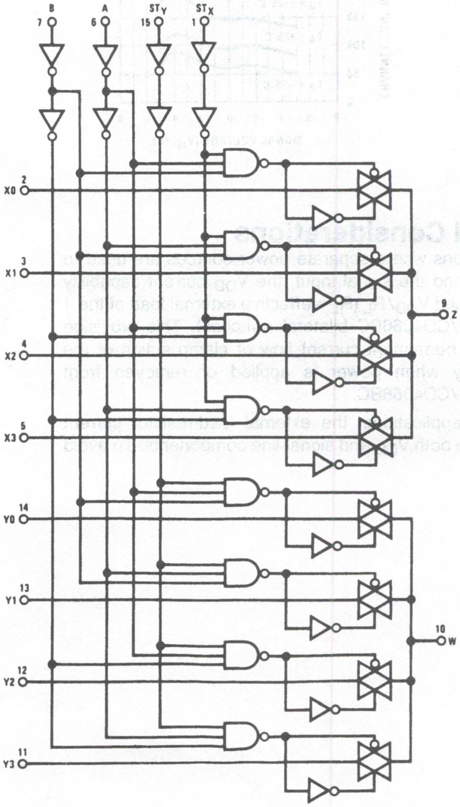
Connection Diagram

Dual-In-Line Package



Order Number CD4529BCJ, N or CD4529BMJ, W
See NS Package J16A, N16E, or W16A

Logic Diagram



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Truth Table

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	X	X	High Impedance (TRI-STATE)		

X = Don't care

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Notes 1 and 2)

V_{DD} DC Supply Voltage	$-0.5V$ to $+18V$
V_{IN} Input Voltage	$-0.5V$ to $V_{DD} + 0.5V$
T_S Storage Temperature Range	$-65°C$ to $+150°C$
P_D Package Dissipation	500 mW
T_L Lead Temp. (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

V_{DD} DC Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4529BM	$-55°C$ to $+125°C$
CD4529BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4529BM (Note 2)

Symbol	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		1.0		0.001	1.0		60	μA
		$V_{DD} = 10V$		1.0		0.002	1.0		60	μA
		$V_{DD} = 15V$		2.0		0.003	2.0		120	μA
V_{OL}	Low Level Output Voltage	$V_{IL} = 0V, V_{IH} = V_{DD}, \lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IL} = 0V, V_{IH} = V_{DD}, \lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	$V_{DD} = 5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	$V_{DD} = 5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD} = 15V$								
		$V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA
R_{ON}	ON Resistance	$V_{DD} = 5V, V_{SS} = -5V$								
		$V_{IN} = 5V$		400		165	480		640	Ω
		$V_{IN} = -5V$		400		100	480		640	Ω
		$V_{IN} = \pm 0.25V$		400		155	480		640	Ω
		$V_{DD} = 7.5V, V_{SS} = -7.5V$								
		$V_{IN} = 7.5V$		240		135	270		400	Ω
		$V_{IN} = -7.5V$		240		75	270		400	Ω
		$V_{IN} = \pm 0.25V$		240		100	270		400	Ω
		$V_{DD} = 10V, V_{SS} = 0V$								
		$V_{IN} = 10V$		400		165	480		640	Ω
		$V_{IN} = 0.25V$		400		100	480		640	Ω
		$V_{IN} = 5.6V$		400		160	480		640	Ω
		$V_{DD} = 15V, V_{SS} = 0V$								
		$V_{IN} = 15V$		250		135	270		400	Ω
		$V_{IN} = 0.25V$		250		75	270		400	Ω
		$V_{IN} = 9.3V$		250		110	270		400	Ω
I_{OFF}	Input to Output Leakage Current	$V_{SS} = -5V, V_{DD} = 5V, V_{IN} = 5V, V_{OUT} = -5V$		±125		±0.001	±125		±1250	nA
		$V_{SS} = -5V, V_{DD} = 5V, V_{IN} = -5V, V_{OUT} = 5V$		±125		±0.001	±125		±1250	nA
		$V_{SS} = -7.5V, V_{DD} = 7.5V, V_{IN} = 7.5V, V_{OUT} = -7.5V$		±250		±0.0015	±250		±2500	nA
		$V_{SS} = -7.5V, V_{DD} = 7.5V, V_{IN} = -7.5V, V_{OUT} = 7.5V$		±250		±0.0015	±250		±2500	nA

DC Electrical Characteristics CD4529BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5.0		0.001	5.0		70	μA
		$V_{DD} = 10V$		5.0		0.002	5.0		70	μA
		$V_{DD} = 15V$		10.0		0.003	10.0		140	μA
V_{OL}	Low Level Output Voltage	$V_{IL} = 0V$, $V_{IH} = V_{DD}$, $\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IL} = 0V$, $V_{IH} = V_{DD}$, $\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5.00		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.00		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.00		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	$V_{DD} = 5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	$V_{DD} = 5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD} = 15V$								
		$V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA
R_{ON}	ON Resistance	$V_{DD} = 5V$, $V_{SS} = -5V$								
		$V_{IN} = 5V$		410		165	480		560	Ω
		$V_{IN} = -5V$		410		100	480		560	Ω
		$V_{IN} = \pm 0.25V$		410		155	480		560	Ω
		$V_{DD} = 7.5V$, $V_{SS} = -7.5V$								
		$V_{IN} = 7.5V$		250		135	270		350	Ω
		$V_{IN} = -7.5V$		250		75	270		350	Ω
		$V_{IN} = \pm 0.25V$		250		100	270		350	Ω
		$V_{DD} = 10V$, $V_{SS} = 0V$								
		$V_{IN} = 10V$		410		165	480		560	Ω
		$V_{IN} = 0.25V$		410		100	480		560	Ω
		$V_{IN} = 5.6V$		410		160	480		560	Ω
		$V_{DD} = 15V$, $V_{SS} = 0V$								
		$V_{IN} = 15V$		250		135	270		350	Ω
		$V_{IN} = 0.25V$		250		75	270		350	Ω
		$V_{IN} = 9.3V$		250		110	270		350	Ω
I_{OFF}	Input-Output Leakage Current	$V_{SS} = -5V$, $V_{DD} = 5V$								
		$V_{IN} = 5V$, $V_{OUT} = -5V$		±125		±0.001	±125		±500	nA
		$V_{IN} = -5V$, $V_{OUT} = 5V$		±125		±0.001	±125		±500	nA
		$V_{SS} = -7.5V$, $V_{DD} = 7.5V$								
		$V_{IN} = 7.5V$, $V_{OUT} = -7.5V$		±250		±0.0015	±250		±1000	nA
		$V_{IN} = -7.5V$, $V_{OUT} = 7.5V$		±250		±0.0015	±250		±1000	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Switch OFF is defined as $|I_O| \leq 10\ \mu A$, switch ON as defined by R_{ON} specification.

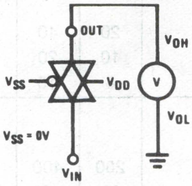
AC Characteristics CD4529BM/CD4539BC

$T_A = 25°C$, $R_L = 1\ k\Omega$, $t_r = t_f = 20$ ns, unless otherwise specified.

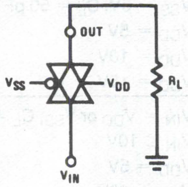
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	V_{IN} to V_{OUT} Propagation Delay	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		10	20	ns
		$V_{DD} = 15V$		8	15	ns
t_{PLH}, t_{PHL}	Control to Output Propagation Delay	$V_{IN} = V_{DD}$ or V_{SS}, $C_L = 50$ pF				
		$V_{IN} \leq 10V$				
		$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		50	120	ns
f_{MAX}	Maximum Control Input Pulse Frequency	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		5		MHz
		$V_{DD} = 10V$		10		MHz
		$V_{DD} = 15V$		12		MHz
	Crosstalk, Control to Output	$R_{OUT} = 10\ k\Omega$, $C_L = 50$ pF, $V_{SS} = 0$				
		$V_{DD} = 5V$		5.0		mV
		$V_{DD} = 10V$		5.0		mV
		$V_{DD} = 15V$		5.0		mV
	Noise Voltage	$f = 100$ Hz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		24		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		25		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		30		$nV/\sqrt{cycle}$
		$f = 100$ kHz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		15		$nV/\sqrt{cycle}$
	Sine Wave (Distortion)	$V_{IN} = 1.77$Vrms Centered at 0V, $R_L = 10\ k\Omega$, $f = 1$ kHz, $V_{SS} = -5V$, $V_{DD} = 5V$		0.36		%
I_{LOSS}	Insertion Loss,	$V_{IN} = 177$Vrms Centered				
		at 0V, $V_{SS} = -5V$, $V_{DD} = 5V$				
	$I_{LOSS} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$	$R_L = 1\ k\Omega$		2.0		dB
		$R_L = 10\ k\Omega$		0.8		dB
		$R_L = 100\ k\Omega$		0.25		dB
		$R_L = 1\ M\Omega$		0.01		dB
BW	Bandwidth, −3dB	$V_{IN} = 177$Vrms Centered				
		at 0 Vdc, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	35			MHz
		$R_L = 10\ k\Omega$	28			MHz
		$R_L = 100\ k\Omega$	27			MHz
		$R_L = 1\ M\Omega$	26			MHz
	Feedthrough and Crosstalk,	$V_{SS} = -5V$, $V_{DD} = 5V$				
	$20 \log_{10} \frac{V_{OUT}}{V_{IN}} = -50$ db	$R_L = 1\ k\Omega$	850			kHz
		$R_L = 10\ k\Omega$	100			kHz
		$R_L = 100\ k\Omega$	12			kHz
		$R_L = 1\ M\Omega$	1.5			Khz

Test Circuits and Switching Time Waveforms

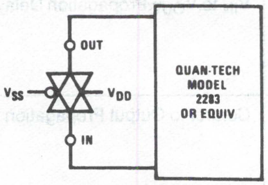
Output Voltage


OUT
V_{OH}
V_{SS}
V_{DD}
V
V_{OL}
V_{SS} = 0V
V_{IN}

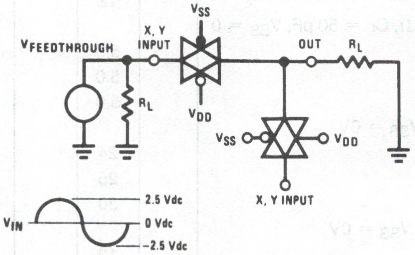
R_{ON} Characteristics


OUT
V_{SS}
V_{DD}
R_L
V_{IN}

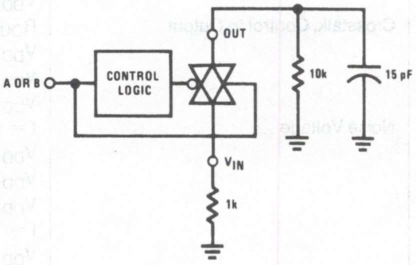
Noise Voltage


OUT
QUAN-TECH MODEL 2283 OR EQUIV
V_{SS}
V_{DD}
IN

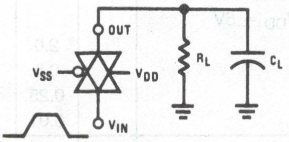
Frequency Response


V_{SS}
X, Y INPUT
$V_{FEEDTHROUGH}$
OUT
R_L
R_L
V_{DD}
V_{SS}
V_{DD}
X, Y INPUT
2.5 Vdc
V_{IN}
0 Vdc
−2.5 Vdc

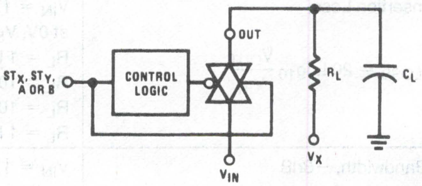
Crosstalk

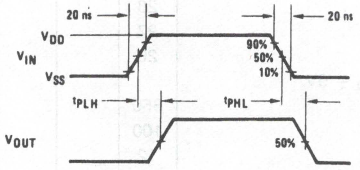

OUT
A OR B
CONTROL LOGIC
10k
15 pF
V_{IN}
1k

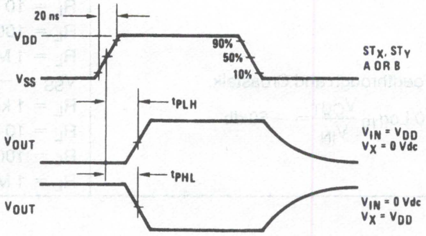
Propagation Delay


OUT
V_{SS}
V_{DD}
R_L
C_L
V_{IN}

Turn-ON Delay Time


OUT
ST_X, ST_Y, A OR B
CONTROL LOGIC
R_L
C_L
V_X
V_{IN}

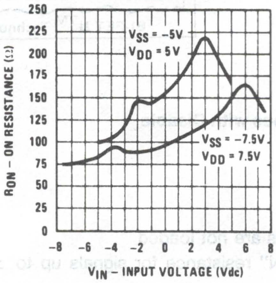

20 ns
20 ns
V_{DD}
V_{IN}
V_{SS}
90%
50%
10%
t_{PLH}
t_{PHL}
V_{OUT}
50%


20 ns
V_{DD}
90%
50%
10%
ST_X, ST_Y A OR B
V_{SS}
t_{PLH}
V_{OUT}
$V_{IN} = V_{DD}$
V_X = 0 Vdc
t_{PHL}
V_{OUT}
V_{IN} = 0 Vdc
$V_X = V_{DD}$

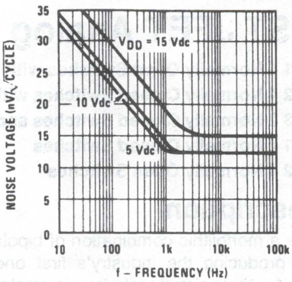
TL/F/5999–2

Typical Performance Characteristics

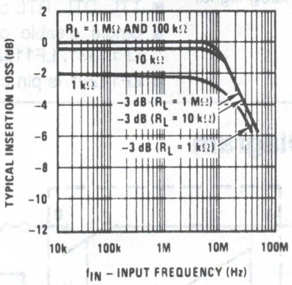
Typical R_{ON} vs V_{IN}



Typical Noise Characteristics

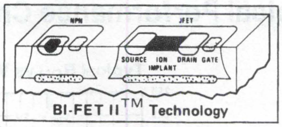


Typical Insertion Loss/ Bandwidth Characteristics



TL/F/5999-3

National Semiconductor Corporation


NPN
JFET
SOURCE
ION IMPLANT
DRAIN
GATE

BI-FET II™ Technology

Quad SPST JFET Analog Switches

LF11331, LF13331 4 Normally Open Switches with Disable
LF11332, LF13332 4 Normally Closed Switches with Disable
LF11333, LF13333 2 Normally Closed Switches and 2 Normally Open Switches with Disable
LF11201, LF13201 4 Normally Closed Switches
LF11202, LF13202 4 Normally Open Switches

General Description

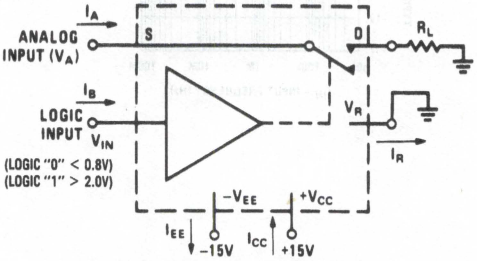
These devices are a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of ±10V. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-before-make action.

These devices operate from ±15V supplies and swing a ±10V analog signal. The JFET switches are designed for applications where a dc to medium frequency analog signal needs to be controlled.

Features

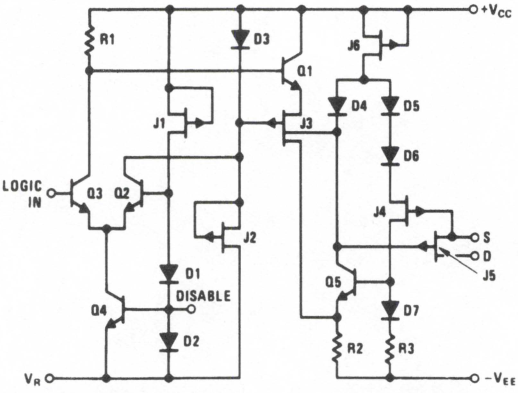
- Analog signals are not loaded
- Constant "ON" resistance for signals up to ±10V and 100 kHz
- Pin compatible with CMOS switches with the advantage of blow out free handling
- Small signal analog signals to 50 MHz
- Break-before-make action $t_{OFF} < t_{ON}$
- High open switch isolation at 1.0 MHz −50 dB
- Low leakage in "OFF" state <1.0 nA
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches in package on LF11331, LF11332, LF11333
- LF11201 is pin compatible with DG201

Test Circuit and Schematic Diagram


I_A
ANALOG INPUT (V_A)
S
D
R_L
I_B
LOGIC INPUT
V_{IN}
(LOGIC "0" < 0.8V)
(LOGIC "1" > 2.0V)
V_R
I_R
$-V_{EE}$
$+V_{CC}$
I_{EE}
−15V
I_{CC}
+15V

TL/H/5667-2

FIGURE 1. Typical Circuit for One Switch


+V_{CC}
R1
D3
Q1
J6
J1
J3
D4
D5
D6
LOGIC IN
Q3
Q2
J4
J2
S
D
J5
D1
DISABLE
Q5
D7
Q4
D2
R2
R3
V_R
−V_{EE}

TL/H/5667-12

FIGURE 2. Schematic Diagram (Normally Open)

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 1)

Supply Voltage ($V_{CC}-V_{EE}$)	36V
Reference Voltage	$V_{EE} \leq V_R \leq V_{CC}$
Logic Input Voltage	$V_R-4.0V \leq V_{IN} \leq V_R+6.0V$
Analog Voltage	$V_{EE} \leq V_A \leq V_{CC}+6V$; $V_A \leq V_{EE}+36V$
Analog Current	$\lvert I_A \rvert < 20$ mA
Power Dissipation (Note 2)	
Molded DIP (N Suffix)	500 mW
Cavity DIP (D Suffix)	900 mW
Operating Temperature Range	
LF11201, 2 and LF11331, 2, 3	−55°C to +125°C
LF13201, 2 and LF13331, 2, 3	0°C to +70°C
Storage Temperature	−65°C to +150°C
Soldering Information	
N and D Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF11331/2/3 LF11201/2			LF13331/2/3 LF13201/2			Units
			Min	Typ	Max	Min	Typ	Max	
R_{ON}	"ON" Resistance	$V_A=0$, $I_D=1$ mA $T_A=25°C$		150	200		150	250	Ω
				200	300		200	350	Ω
R_{ON} Match	"ON" Resistance Matching	$T_A=25°C$		5	20		10	50	Ω
V_A	Analog Range		±10	±11		±10	±11		V
$I_{S(ON)}+I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON," $V_S=V_D=\pm10V$ $T_A=25°C$		0.3	5		0.3	10	nA
				3	100		3	30	nA
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF," $V_S=+10V$, $V_D=-10V$ $T_A=25°C$		0.4	5		0.4	10	nA
				3	100		3	30	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF," $V_S=+10V$, $V_D=-10V$ $T_A=25°C$		0.1	5		0.1	10	nA
				3	100		3	30	nA
V_{INH}	Logical "1" Input Voltage		2.0			2.0			V
V_{INL}	Logical "0" Input Voltage				0.8			0.8	V
I_{INH}	Logical "1" Input Current	$V_{IN}=5V$ $T_A=25°C$		3.6	10		3.6	40	µA
					25			100	µA
I_{INL}	Logical "0" Input Current	$V_{IN}=0.8$ $T_A=25°C$			0.1			0.1	µA
					1			1	µA
t_{ON}	Delay Time "ON"	$V_S=\pm10V$, *(Figure 3)* $T_A=25°C$		500			500		ns
t_{OFF}	Delay Time "OFF"	$V_S=\pm10V$, *(Figure 3)* $T_A=25°C$		90			90		ns
$t_{ON}-t_{OFF}$	Break-Before-Make	$V_S=\pm10V$, *(Figure 3)* $T_A=25°C$		80			80		ns
$C_{S(OFF)}$	Source Capacitance	Switch "OFF," $V_S=\pm10V$ $T_A=25°C$		4.0			4.0		pF
$C_{D(OFF)}$	Drain Capacitance	Switch "OFF," $V_D=\pm10V$ $T_A=25°C$		3.0			3.0		pF
$C_{S(ON)}+C_{D(ON)}$	Active Source and Drain Capacitance	Switch "ON," $V_S=V_D=0V$ $T_A=25°C$		5.0			5.0		pF
$I_{SO(OFF)}$	"OFF" Isolation	*(Figure 4)*, (Note 4) $T_A=25°C$		−50			−50		dB
CT	Crosstalk	*(Figure 4)*, (Note 4) $T_A=25°C$		−65			−65		dB
SR	Analog Slew Rate	(Note 5) $T_A=25°C$		50			50		V/µs
I_{DIS}	Disable Current	*(Figure 5)*, (Note 6) $T_A=25°C$		0.4	1.0		0.6	1.5	mA
				0.6	1.5		0.9	2.3	mA
I_{EE}	Negative Supply Current	All Switches "OFF," $V_S=\pm10V$ $T_A=25°C$		3.0	5.0		4.3	7.0	mA
				4.2	7.5		6.0	10.5	mA
I_R	Reference Supply Current	All Switches "OFF," $V_S=\pm10V$ $T_A=25°C$		2.0	4.0		2.7	5.0	mA
				2.8	6.0		3.8	7.5	mA
I_{CC}	Positive Supply Current	All Switches "OFF," $V_S=\pm10V$ $T_A=25°C$		4.5	6.0		7.0	9.0	mA
				6.3	9.0		9.8	13.5	mA

Note 1: Refer to RETSF11201X, RETSF11331X, RETSF11332X and RETSF11333X for military specifications.

Note 2: For operating at high temperature the molded DIP products must be derated based on a +100°C maximum junction temperature and a thermal resistance of +150°C/W, devices in the cavity DIP are based on a +150°C maximum junction temperature and are derated at ±100°C/W.

Note 3: Unless otherwise specified, $V_{CC}=+15V$, $V_{EE}=-15V$, $V_R=0V$, and limits apply for $-55°C \leq T_A \leq +125°C$ for the LF11331/2/3 and the LF11201/2, $-25°C \leq T_A \leq +85°C$ for the LF13331/2/3 and the LF13201/2.

Note 4: These parameters are limited by the pin to pin capacitance of the package.

Note 5: This is the analog signal slew rate above which the signal is distorted as a result of finite internal slew rates.

Note 6: All switches in the device are turned "OFF" by saturating a transistor at the disable node as shown in *Figure 5*. The delay time will be approximately equal to the t_{ON} or t_{OFF} plus the delay introduced by the external transistor.

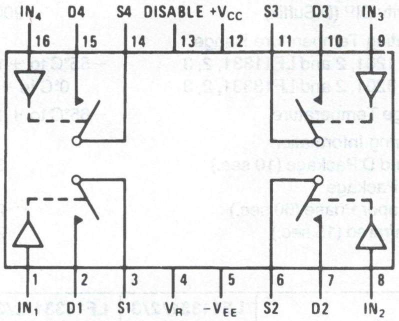
Note 7: This graph indicates the analog current at which 1% of the analog current is lost when the drain is positive with respect to the source.

Note 8: θ_{JA} (Typical) Thermal Resistance

Molded DIP (N)	85°C/W
Cavity DIP (D)	100°C/W
Small Outline (M)	105°C/W

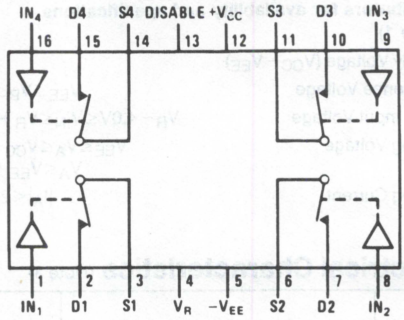
Connection Diagrams (Top View for SO and Dual-In-Line Packages) (All Switches Shown are For Logical "0")

LF11331/LF13331


IN$_4$
D4
S4
DISABLE
+V$_{CC}$
S3
D3
IN$_3$
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
IN$_1$
D1
S1
V$_R$
−V$_{EE}$
S2
D2
IN$_2$

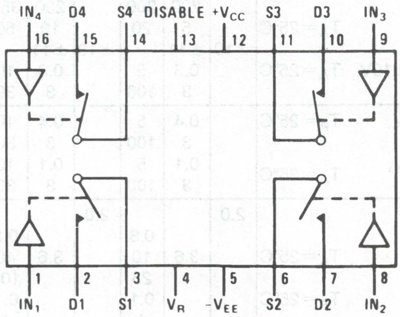
TL/H/5667-1

LF11332/LF13332


IN$_4$
D4
S4
DISABLE
+V$_{CC}$
S3
D3
IN$_3$
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
IN$_1$
D1
S1
V$_R$
−V$_{EE}$
S2
D2
IN$_2$

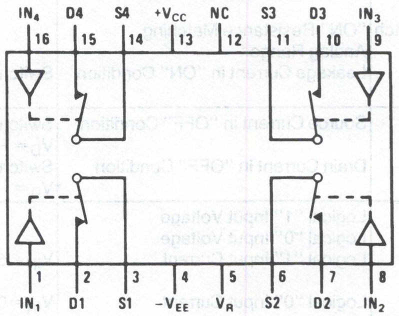
TL/H/5667-13

LF11333/LF13333


IN$_4$
D4
S4
DISABLE
+V$_{CC}$
S3
D3
IN$_3$
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
IN$_1$
D1
S1
V$_R$
−V$_{EE}$
S2
D2
IN$_2$

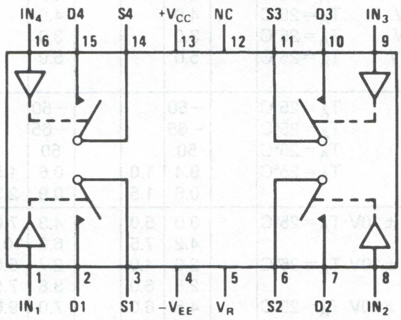
TL/H/5667-14

LF11201/LF13201


IN$_4$
D4
S4
+V$_{CC}$
NC
S3
D3
IN$_3$
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
IN$_1$
D1
S1
−V$_{EE}$
V$_R$
S2
D2
IN$_2$

TL/H/5667-15

LF11202/LF13202


IN$_4$
D4
S4
+V$_{CC}$
NC
S3
D3
IN$_3$
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
IN$_1$
D1
S1
−V$_{EE}$
V$_R$
S2
D2
IN$_2$

TL/H/5667-16

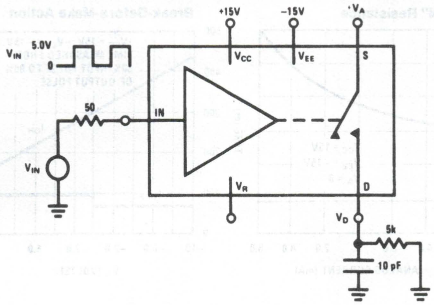
Order Number LF13201D, LF11201D, LF13202D, LF11202D, LF13331D, LF11331D, LF13332D, LF11332D, LF13333D or LF11333D
See NS Package Number D16C

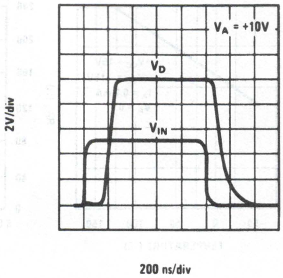
Order Number LF13201M, LF13202M, LF13331M, LF13332M or LF13333M
See NS Package Number M16A

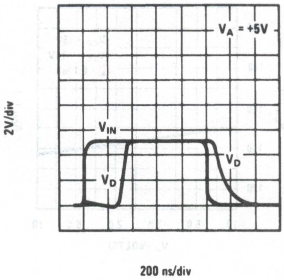
Order Number LF13201N, LF13202N, LF13331N, LF13332N or LF13333N
See NS Package Number N16A

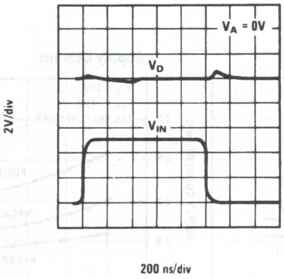
Test Circuit and Typical Performance Curves

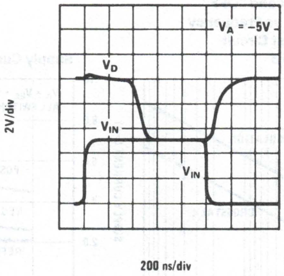
Delay Time, Rise Time, Settling Time, and Switching Transients

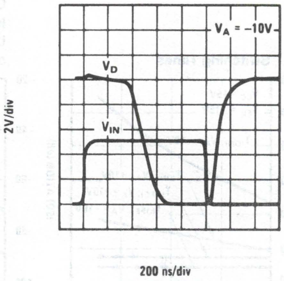

+15V
−15V
V_A
V_{IN}
5.0V
0
50
IN
V_{CC}
V_{EE}
S
V_R
D
V_D
5k
10 pF











TL/H/5667-3

Additional Test Circuits

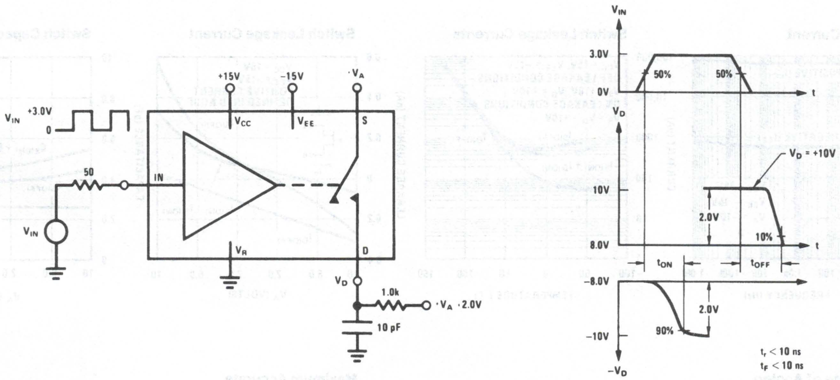
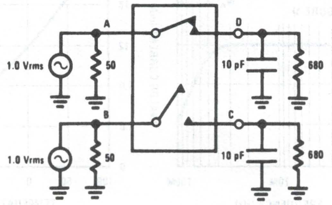

+15V
−15V
V_A
V_{IN}
+3.0V
0
50
IN
V_{CC}
V_{EE}
S
V_R
D
V_D
1.0k
V_A 2.0V
10 pF
V_{IN}
3.0V
50%
50%
0V
t
V_D
V_D = +10V
10V
2.0V
10%
8.0V
t
t_{ON}
t_{OFF}
−8.0V
2.0V
90%
−10V
$-V_D$
t_r < 10 ns
t_f < 10 ns

FIGURE 3. t_{ON}, t_{OFF} Test Circuit and Waveforms for a Normally Open Switch

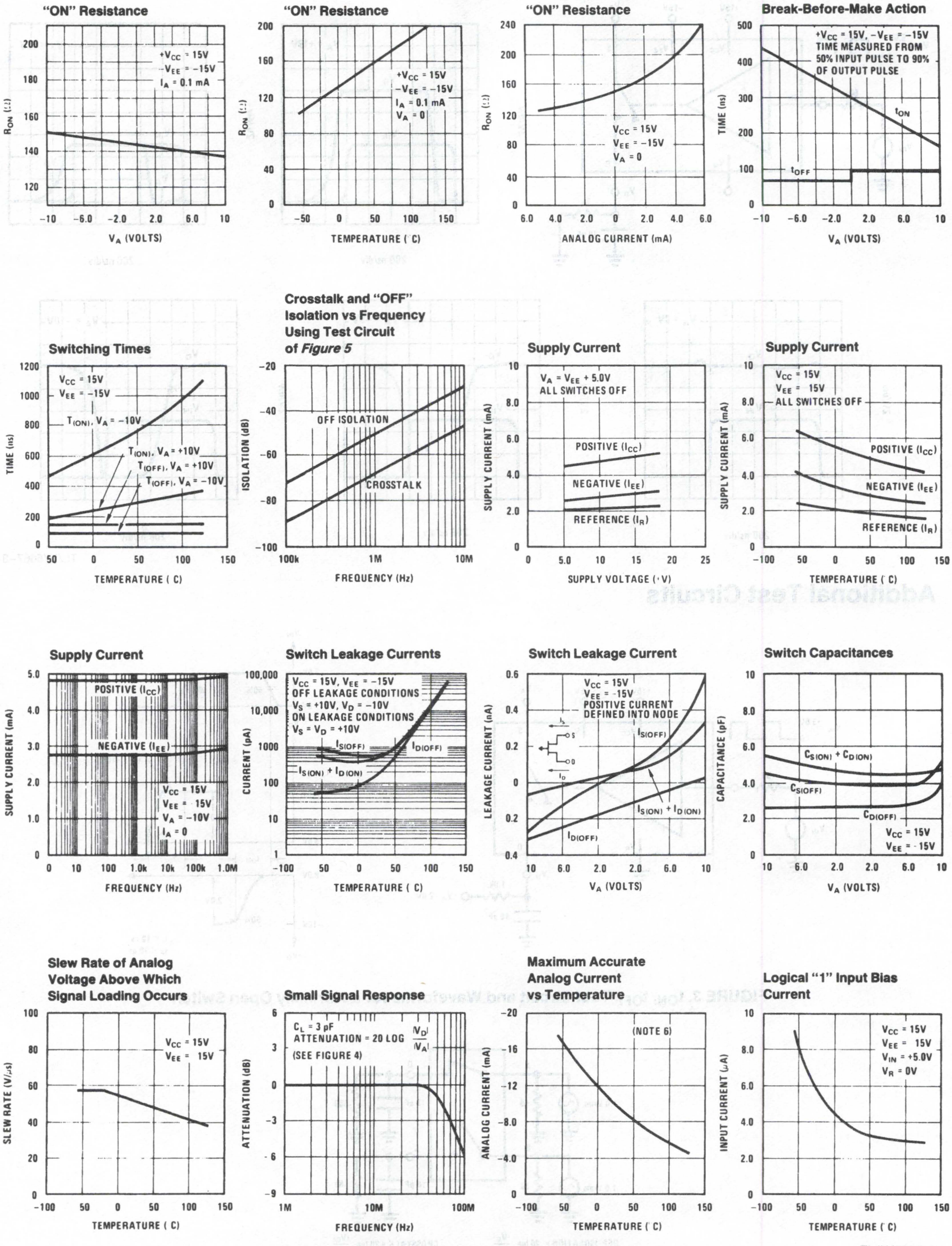

A
B
C
D
1.0 Vrms
50
1.0 Vrms
50
10 pF
680
10 pF
680

OFF ISOLATION = $20 \log \frac{|V_C|}{|V_B|}$ CROSSTALK = $20 \log \frac{|V_C|}{|V_A|}$

TL/H/5667-4

FIGURE 4. "OFF" Isolation, Crosstalk, Small Signal Response

Typical Performance Characteristics



TL/H/5667-5

Application Hints

GENERAL INFORMATION

These devices are monolithic quad JFET analog switches with "ON" resistances which are essentially independent of analog voltage or analog current. The leakage currents are typically less than 1 nA at 25°C in both the "OFF"and "ON" switch states and introduce negligible errors in most applications. Each switch is controlled by minimum TTL logic levels at its input and is designed to turn "OFF" faster than it will turn "ON." This prevents two analog sources from being transiently connected together during switching. The switches were designed for applications which require break-before-make action, no analog current loss, medium speed switching times and moderate analog currents.

Because these analog switches are JFET rather than CMOS, they do not require special handling.

LOGIC INPUTS

The logic input (IN), of each switch, is referenced to two forward diode drops (1.4V at 25°C) from the reference supply (V_R) which makes it compatible with DTL, RTL, and TTL logic families. For normal operation, the logic "0" voltage can range from 0.8V to −4.0V with respect to V_R and the logic "1" voltage can range from 2.0V to 6.0V with respect to V_R, provided V_{IN} is not greater than ($V_{CC}-2.5V$). If the input voltage is greater than (V_{CC} −2.5V), the input current will increase. If the input voltage exceeds 6.0V or −4.0V with respect to V_R, a resistor in series with the input should be used to limit the input current to less than 100μA.

ANALOG VOLTAGE AND CURRENT

Analog Voltage

Each switch has a constant "ON" resistance (R_{ON}) for analog voltages from ($V_{EE}+5V$) to ($V_{CC}-5V$). For analog voltages greater than ($V_{CC}-5V$), the switch will remain ON independent of the logic input voltage. For analog voltages less than ($V_{EE}+5V$), the ON resistance of the switch will increase. Although the switch will not operate normally when the analog voltage is out of the previously mentioned range, the source voltage can go to either ($V_{EE}+36V$) or ($V_{CC}+6V$), whichever is more positive, and can go as negative as V_{EE} without destruction. The drain (D) voltage can also go to either ($V_{EE}+36V$) or ($V_{CC}+6V$), whichever is more positive, and can go as negative as ($V_{CC}-36V$) without destruction.

Analog Current

With the source (S) positive with respect to the drain (D), the R_{ON} is constant for low analog currents, but will increase at higher currents (>5 mA) when the FET enters the saturation region. However, if the drain is positive with respect to the source and a small analog current loss at high analog currents (Note 6) is tolerable, a low R_{ON} can be maintained for analog currents greater than 5 mA at 25°C.

LEAKAGE CURRENTS

The drain and source leakage currents, in both the ON and the OFF states of each switch, are typically less than 1 nA at 25°C and less than 100 nA at 125°C. As shown in the typical curves, these leakage currents are Dependent on power supply voltages, analog voltage, analog current and the source to drain voltage.

DELAY TIMES

The delay time OFF (t_{OFF}) is essentially independent of both the analog voltage and temperature. The delay time ON (t_{ON}) will decrease as either ($V_{CC}-V_A$) decreases or the temperature decreases.

POWER SUPPLIES

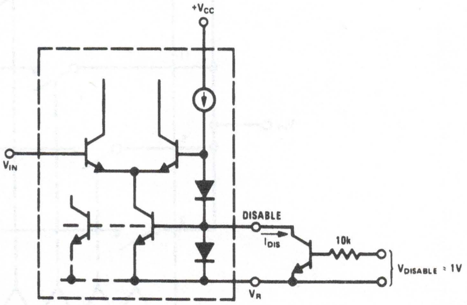
The voltage between the positive supply (V_{CC}) and either the negative supply (V_{EE}) or the reference supply (V_R) can be as much as 36V. To accommodate variations in input logic reference voltages, V_R can range from V_{EE} to ($V_{CC}-4.5V$). Care should be taken to ensure that the power supply leads for the device never become reversed in polarity or that the device is never inadvertantly installed backwards in a test socket. If one of these conditions occurs, the supplies would zener an internal diode to an unlimited current; and result in a destroyed device.

SWITCHING TRANSIENTS

When a switch is turned OFF or ON, transients will appear at the load due to the internal transient voltage at the gate of the switch JFET being coupled to the drain and source by the junction capacitances of the JFET. The magnitude of these transients is dependent on the load. A lower value R_L produces a lower transient voltage. A negative transient occurs during the delay time ON, while a positive transient occurs during the delay time OFF. These transients are relatively small when compared to faster switch families.

DISABLE NODE

This node can be used, as shown in *Figure 5*, to turn all the switches in the unit off independent of logic inputs. Normally, the node floats freely at an internal diode drop (≈0.7V) above V_R. When the external transistor in *Figure 5* is saturated, the node is pulled very close to V_R and the unit is disabled. Typically, the current from the node will be less than 1 mA. This feature is not available on the LF11201 or LF11202 series.

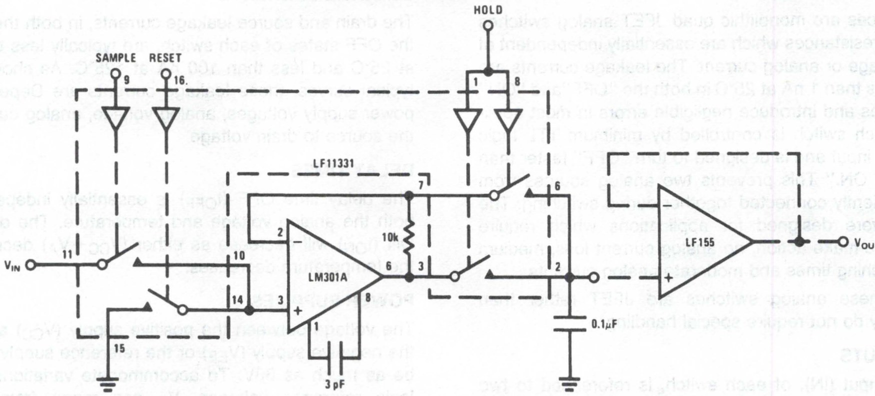


TL/H/5667–6

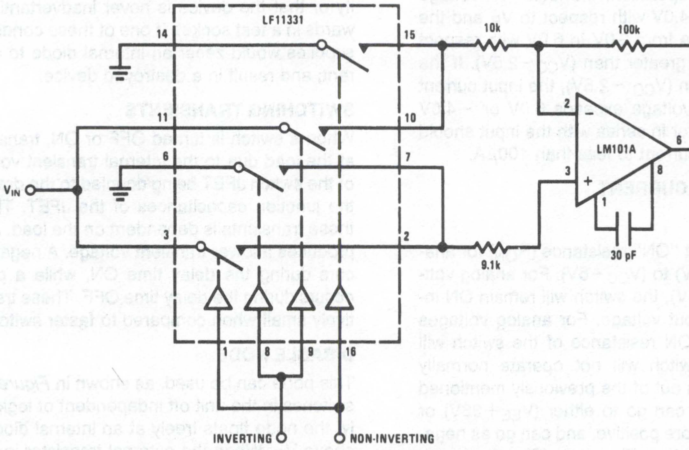
FIGURE 5. Disable Function

Typical Applications

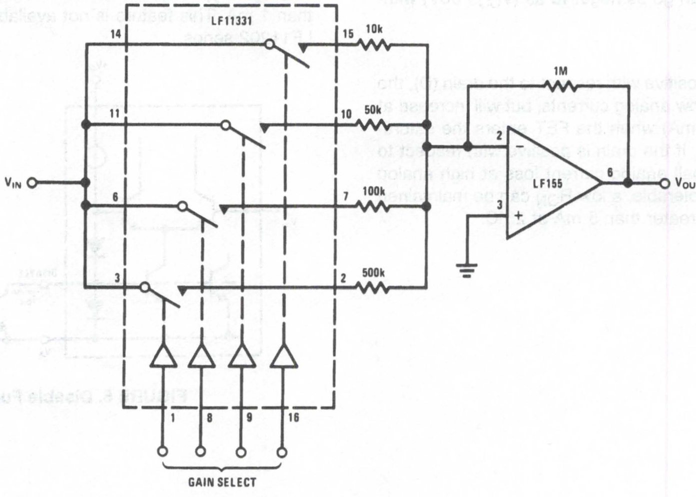
Sample and Hold with Reset


HOLD
SAMPLE
RESET
9
16.
1
8
LF11331
7
10k
6
2
LM301A
3
10
11
V_{IN}
14
15
3 pF
LF155
V_{OUT}
0.1µF

Programmable Inverting Non-Inverting Operational Amplifier


LF11331
14
15
10k
100k
11
10
6
7
V_{IN}
LM101A
V_{OUT}
3
2
9.1k
30 pF
1
8
16
INVERTING
NON-INVERTING

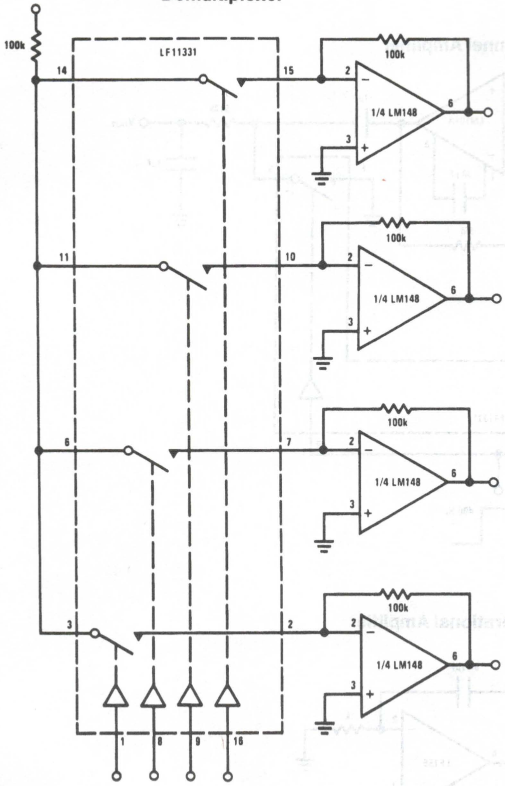
Programmable Gain Operational Amplifier


LF11331
14
15
10k
11
10
50k
1M
V_{IN}
6
7
100k
LF155
V_{OUT}
3
2
500k
1
8
9
16
GAIN SELECT

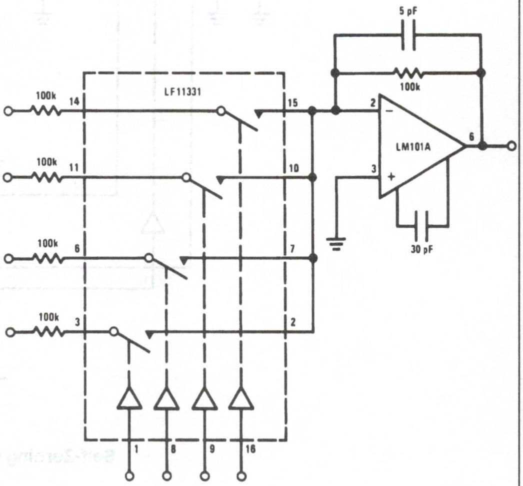
TL/H/5667-7

Typical Applications (Continued)

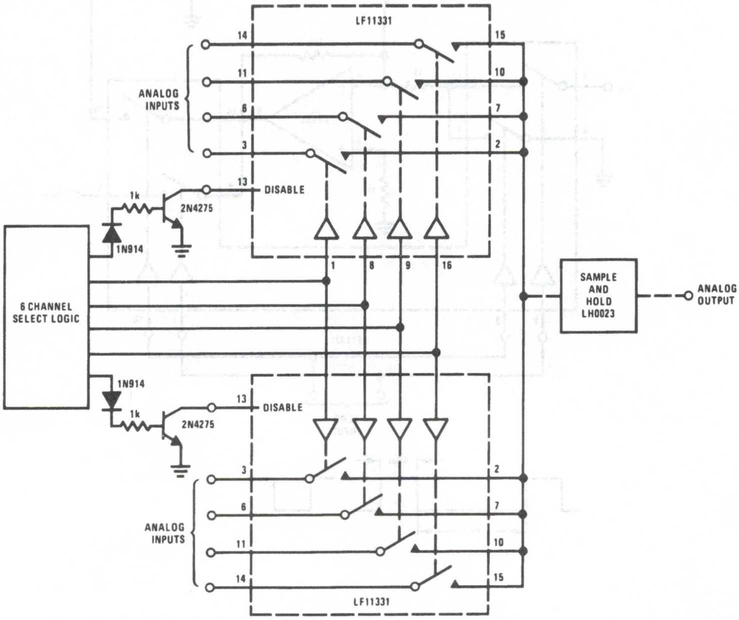
Demultiplexer


100k
LF11331
14
15
100k
2
3
6
1/4 LM148
11
10
6
7
3
2
1
8
9
16

Multiplexer/Mixer


5 pF
100k
LF11331
100k
14
100k
11
100k
6
100k
3
15
10
7
2
2
3
6
LM101A
30 pF
1
8
9
16

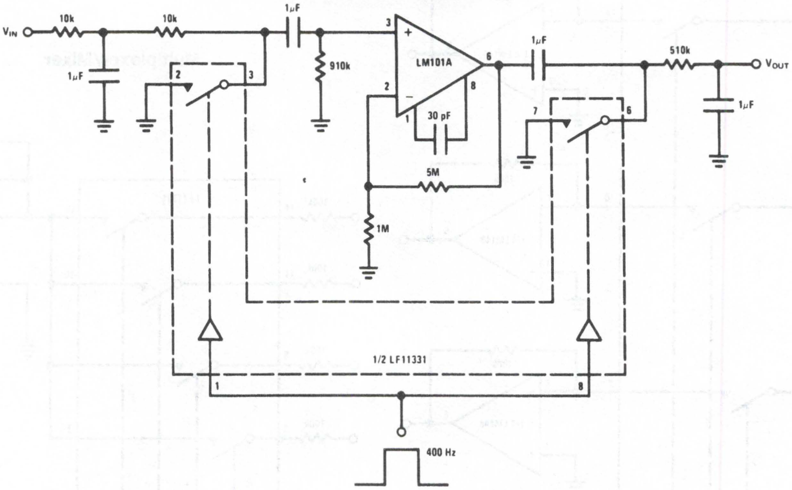
8-Channel Analog Commutator with 6-Channel Select Logic


LF11331
14
11
6
3
15
10
7
2
ANALOG INPUTS
13
DISABLE
1k
2N4275
1N914
6 CHANNEL SELECT LOGIC
1
8
9
16
SAMPLE AND HOLD LH0023
ANALOG OUTPUT
1N914
1k
2N4275
13
DISABLE
3
6
11
14
ANALOG INPUTS
2
7
10
15
LF11331

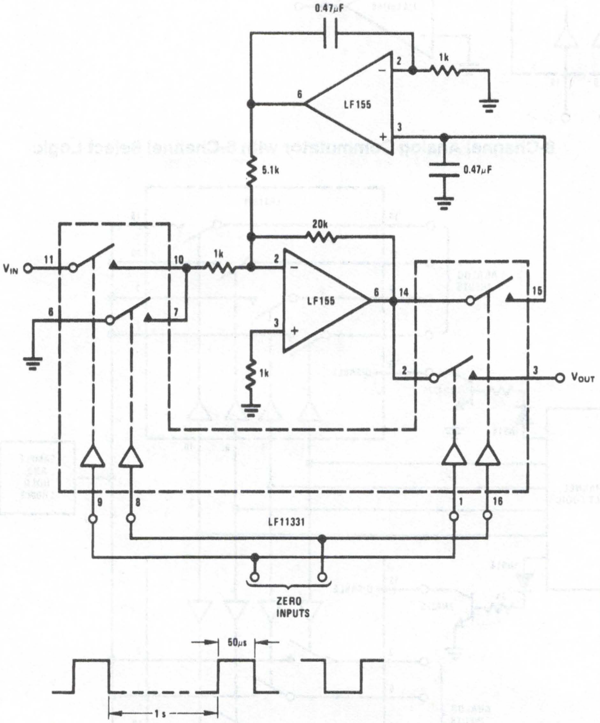
TL/H/5667–8

Typical Applications (Continued)

Chopper Channel Amplifier


V_{IN}
10k
10k
1μF
1μF
910k
3
+
LM101A
6
2
−
8
1
30 pF
5M
1M
1μF
510k
V_{OUT}
1μF
2
3
7
6
1/2 LF11331
1
8
400 Hz

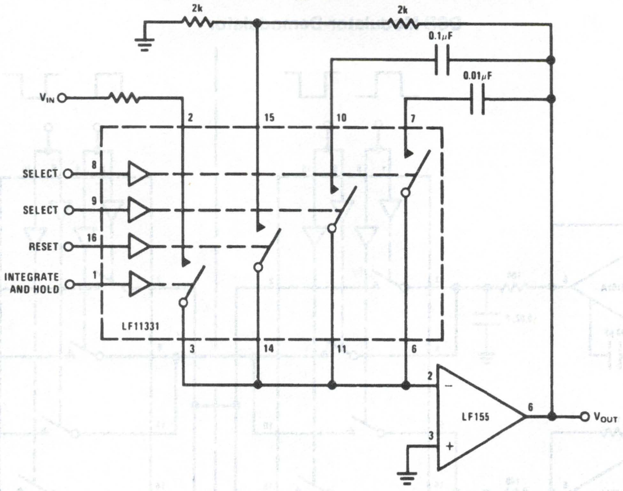
Self-Zeroing Operational Amplifier


0.47μF
1k
2
−
6
LF155
3
+
0.47μF
5.1k
20k
V_{IN}
11
10
1k
2
−
6
LF155
3
+
14
15
1k
6
7
2
3
V_{OUT}
9
8
LF11331
1
16
ZERO INPUTS
50μs
1 s

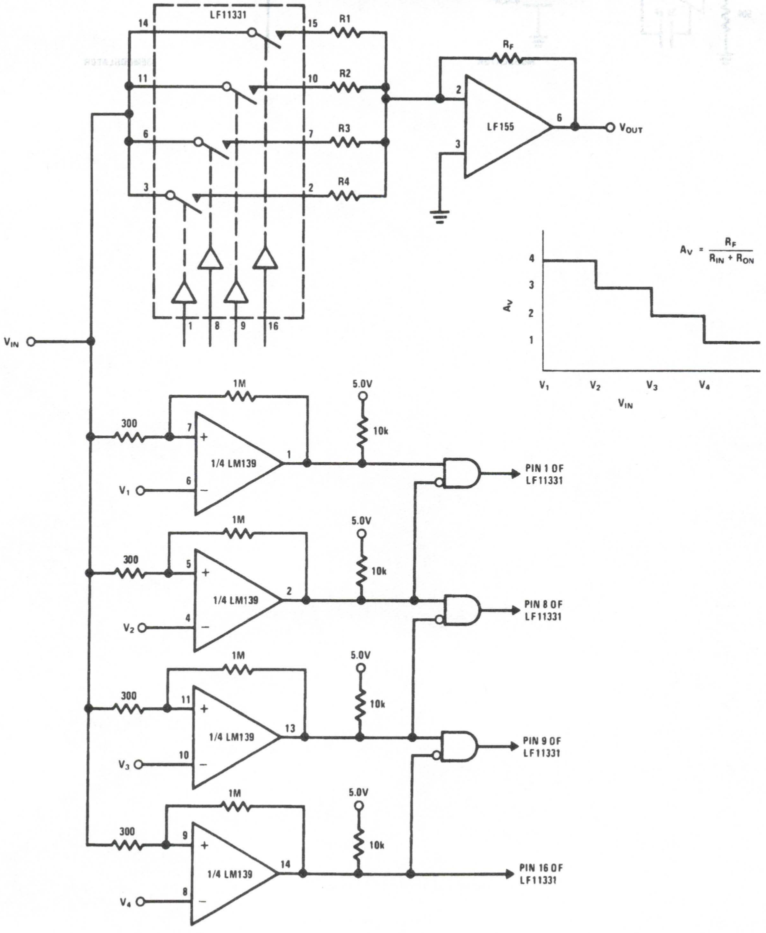
TL/H/5667–9

Typical Applications (Continued)

Programmable Integrator with Reset and Hold


2k
2k
0.1μF
0.01μF
V_{IN}
2
15
10
7
SELECT
8
SELECT
9
RESET
16
INTEGRATE AND HOLD
1
LF11331
3
14
11
6
2
LF155
3
6
V_{OUT}

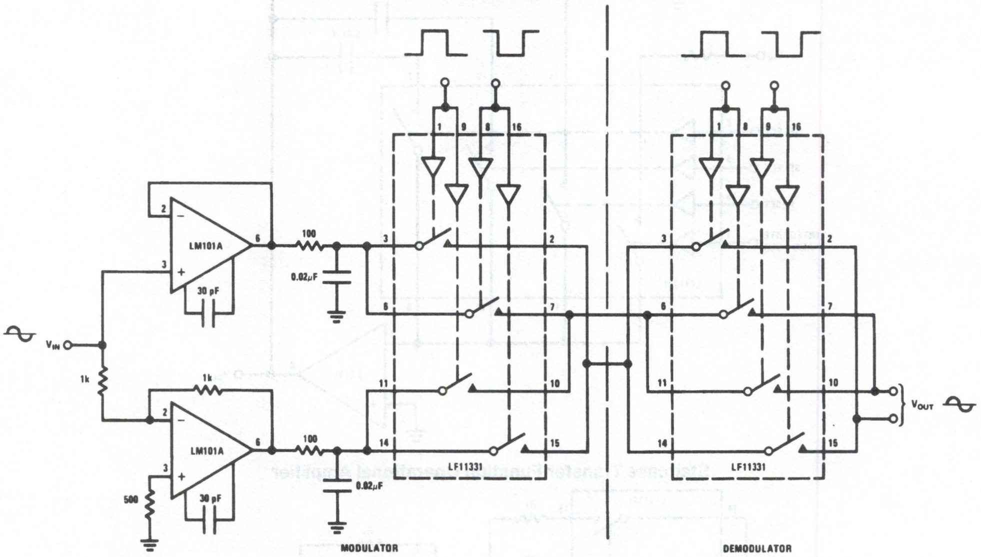
Staircase Transfer Function Operational Amplifier


LF11331
14
15
R1
11
10
R2
6
7
R3
3
2
R4
R_F
2
LF155
3
6
V_{OUT}
1
8
9
16
V_{IN}
$A_V = \frac{R_F}{R_{IN} + R_{ON}}$
4
3
2
1
A_V
V_1
V_2
V_3
V_4
V_{IN}
1M
5.0V
300
7
1/4 LM139
1
10k
6
V_1
PIN 1 OF LF11331
1M
5.0V
300
5
1/4 LM139
2
10k
4
V_2
PIN 8 OF LF11331
1M
5.0V
300
11
1/4 LM139
13
10k
10
V_3
PIN 9 OF LF11331
1M
5.0V
300
9
1/4 LM139
14
10k
8
V_4
PIN 16 OF LF11331

TL/H/5667-10

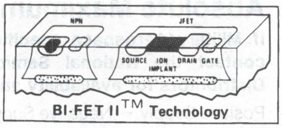
Typical Applications (Continued)

DSB Modulator-Demodulator


V_{IN}
1k
1k
500
LM101A
LM101A
30 pF
30 pF
100
100
0.02µF
0.02µF
LF11331
LF11331
MODULATOR
DEMODULATOR
V_{OUT}
1
9
8
16
3
2
6
7
11
10
14
15

TL/H/5667-11

National Semiconductor Corporation



LF13508 8-Channel Analog Multiplexer
LF13509 4-Channel Differential Analog Multiplexer

General Description

The LF13508 is an 8-channel analog multiplexer which connects the output to 1 of the 8 analog inputs depending on the state of a 3-bit binary address. An enable control allows disconnecting the output, thereby providing a package select function.

This device is fabricated with National's BI-FET technology which provides ion-implanted JFETs for the analog switch on the same chip as the bipolar decode and switch drive circuitry. This technology makes possible low constant "ON" resistance with analog input voltage variations. This device does not suffer from latch-up problems or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action.

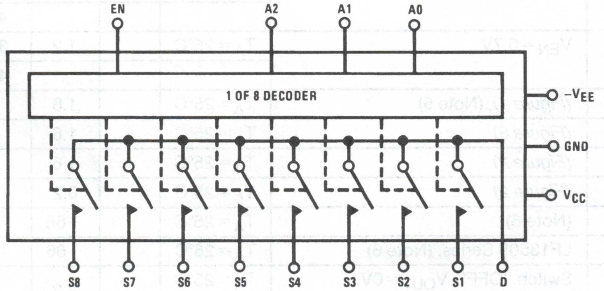
The LF13509 is a 4-channel differential analog multiplexer. A 2-bit binary address will connect a pair of independent analog inputs to one of any 4 pairs of independent analog outputs. The device has all the features of the LF13508 series and should be used whenever differential analog inputs are required.

Features

- JFET switches rather than CMOS
- No static discharge blow-out problem
- No SCR latch-up problems
- Analog signal range 11V, −15V
- Constant "ON" resistance for analog signals between −11V and 11V
- "ON" resistance 380 Ω typ
- Digital inputs compatible with TTL and CMOS
- Output enable control
- Break-before-make action: $t_{OFF} = 0.2\ \mu s$; $t_{ON} = 2\ \mu s$ typ
- Lower leakage devices available

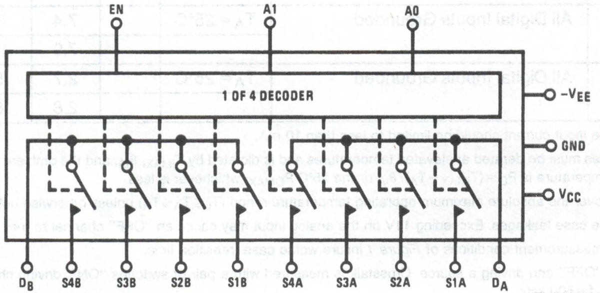
Functional Diagrams and Truth Tables

LF13508



EN	A2	A1	A0	SWITCH ON
H	L	L	L	S1
H	L	L	H	S2
H	L	H	L	S3
H	L	H	H	S4
H	H	L	L	S5
H	H	L	H	S6
H	H	H	L	S7
H	H	H	H	S8
L	X	X	X	NONE

LF13509



EN	A1	A0	SWITCH PAIR ON
L	X	X	None
H	L	L	S1
H	L	H	S2
H	H	L	S3
H	H	H	S4

TL/H/5668–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply − Negative Supply ($V_{CC}-V_{EE}$)	36V
Positive Analog Input Voltage (Note 1)	V_{CC}
Negative Analog Input Voltage (Note 1)	$-V_{EE}$
Positive Digital Input Voltage	V_{CC}
Negative Digital Input Voltage	−5V
Analog Switch Current	$\lvert I_S \rvert < 10$ mA

Power Dissipation (P_D at 25°C) (Notes 2 & 7)		
Molded DIP (N)	P_D	500 mW
Cavity DIP (D)	P_D	900 mW
Maximum Junction Temperature (T_{jMAX})		100°C
Operating Temperature Range		$0°C \le T_A \le +70°C$
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		300°C

Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions		LF13508 LF13509			Units
				Min	Typ	Max	
R_{ON}	"ON" Resistance	$V_{OUT}=0V$, $I_S=100\ \mu A$	$T_A=25°C$		380	650	Ω
					500	850	Ω
ΔR_{ON}	ΔR_{ON} with Analog Voltage Swing	$-10V \le V_{OUT} \le +10V$, $I_S=100\ \mu A$	$T_A=25°C$		0.01	1	%
R_{ON} Match	R_{ON} Match Between Switches	$V_{OUT}=0V$, $I_S=100\ \mu A$	$T_A=25°C$		20	150	Ω
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF", $V_S=11$, $V_D=-11$, (Note 4)	$T_A=25°C$			5	nA
					0.09	50	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF", $V_S=11$, $V_D=-11$, (Note 4)	$T_A=25°C$			20	nA
					0.6	500	nA
$I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON" $V_D=11V$, (Note 4)	$T_A=25°C$			20	nA
					1	500	nA
V_{INH}	Digital "1" Input Voltage			2.0			V
V_{INL}	Digital "0" Input Voltage					0.7	V
I_{INL}	Digital "0" Input Current	$V_{IN}=0.7V$	$T_A=25°C$		1.5	30	μA
						40	μA
$I_{INL(EN)}$	Digital "0" Enable Current	$V_{EN}=0.7V$	$T_A=25°C$		1.2	30	μA
						40	μA
t_{TRAN}	Switching Time of Multiplexer	*(Figure 1)*, (Note 5)	$T_A=25°C$		1.8		μs
t_{OPEN}	Break-Before-Make	*(Figure 3)*	$T_A=25°C$		1.6		μs
$t_{ON(EN)}$	Enable Delay "ON"	*(Figure 2)*	$T_A=25°C$		1.6		μs
$t_{OFF(EN)}$	Enable Delay "OFF"	*(Figure 2)*	$T_A=25°C$		0.2		μs
$I_{SO(OFF)}$	"OFF" Isolation	(Note 6)	$T_A=25°C$		−66		dB
CT	Crosstalk	LF13509 Series, (Note 6)	$T_A=25°C$		−66		dB
$C_{S(OFF)}$	Source Capacitance ("OFF")	Switch "OFF", $V_{OUT}=0V$, $V_S=0V$	$T_A=25°C$		2.2		pF
$C_{D(OFF)}$	Drain Capacitance ("OFF")	Switch "OFF", $V_{OUT}=0V$, $V_S=0V$	$T_A=25°C$		11.4		pF
I_{CC}	Positive Supply Current	All Digital Inputs Grounded	$T_A=25°C$		7.4	12	mA
					7.9	15	mA
I_{EE}	Negative Supply Current	All Digital Inputs Grounded	$T_A=25°C$		2.7	5	mA
					2.8	6	mA

Note 1: If the analog input voltage exceeds this limit, the input current should be limited to less than 10 mA.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D=(T_{jMAX}-T_A)/\theta_{jA}$ or the 25°C P_{DMAX}, whichever is less.

Note 3: These specifications apply for $V_S=\pm15V$ and over the absolute maximum operating temperature range ($T_L \le T_A \le T_H$) unless otherwise noted.

Note 4: Conditions applied to leakage tests insure worse case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".

Note 5: Lots are sample tested to this parameter. The measurement conditions of *Figure 1* insure worse case transition time.

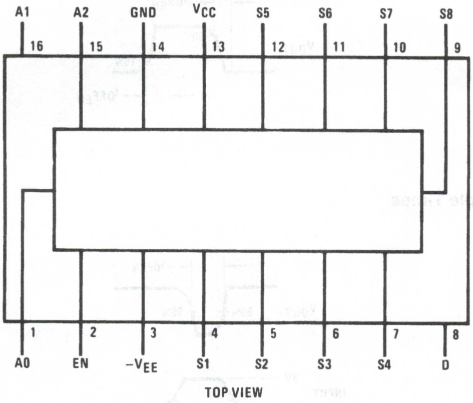
Note 6: "OFF" isolation is measured with all switches "OFF" and driving a source. Crosstalk is measured with a pair of switches "ON", driving channel A and measuring channel B. $R_L=200$, $C_L=7$ pF, $V_S=3$ Vrms, f=500 kHz.

Note 7: Thermal Resistance θ_{jA} (Junction to Ambient)

Molded DIP (N)	150°C/W
Cavity DIP (D)	100°C/W

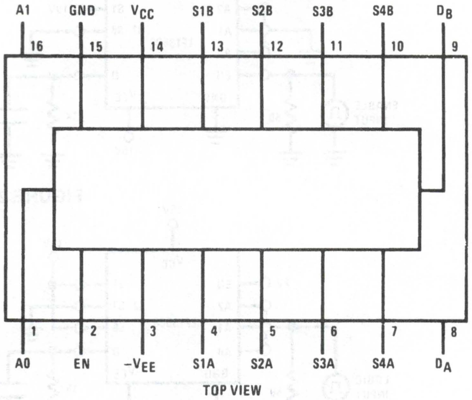
Connection Diagrams

LF13508
Dual-In-Line Package


A1
A2
GND
V_{CC}
S5
S6
S7
S8
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
A0
EN
$-V_{EE}$
S1
S2
S3
S4
D
TOP VIEW

Order Number LF13508D
See NS Package Number D16C
Order Number LF13508N
See NS Package Number N16A

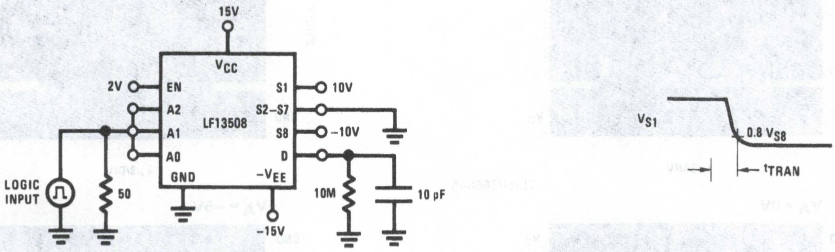
LF13509
Dual-In-Line Package


A1
GND
V_{CC}
S1B
S2B
S3B
S4B
D_B
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
A0
EN
$-V_{EE}$
S1A
S2A
S3A
S4A
D_A
TOP VIEW

TL/H/5668-2

Order Number LF13509D
See NS Package Number D16C
Order Number LF13509N
See NS Package Number N16A

AC Test Circuits and Switching Time Waveforms


15V
V_{CC}
2V
EN
A2
A1
A0
LF13508
GND
S1
S2–S7
S8
D
$-V_{EE}$
10V
−10V
LOGIC INPUT
50
−15V
10M
10 pF
V_{S1}
$0.8\ V_{S8}$
t_{TRAN}

TL/H/5668-3

FIGURE 1. Transition Time

AC Test Circuit and Switching Time Waveforms (Continued)

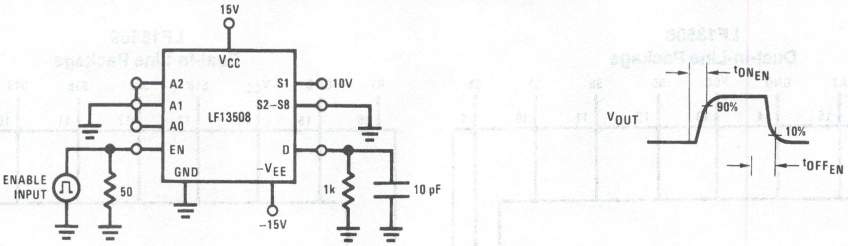
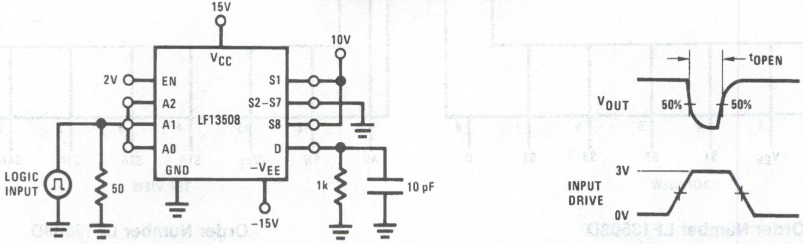

15V
V_{CC}
A2
A1
A0
EN
GND
LF13508
S1
S2–S8
D
$-V_{EE}$
10V
ENABLE INPUT
50
1k
10 pF
−15V
V_{OUT}
$t_{ON_{EN}}$
90%
10%
$t_{OFF_{EN}}$

FIGURE 2. Enable Times

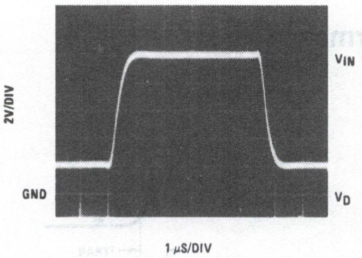

15V
V_{CC}
2V
EN
A2
A1
A0
GND
LF13508
S1
S2–S7
S8
D
$-V_{EE}$
10V
LOGIC INPUT
50
1k
10 pF
−15V
t_{OPEN}
V_{OUT}
50%
50%
3V
INPUT DRIVE
0V

TL/H/5668-4

FIGURE 3. Break-Before-Make

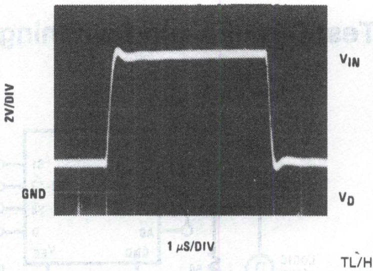
Transition Times and Transients

V_A = 10V



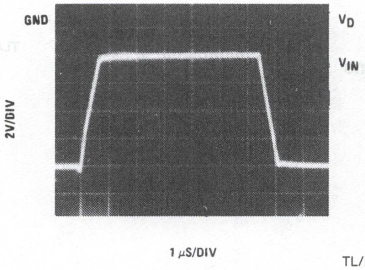
TL/H/5668-5

V_A = 5V



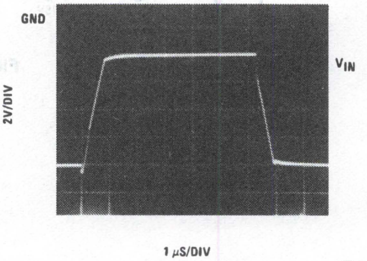
TL/H/5668-6

V_A = 0V



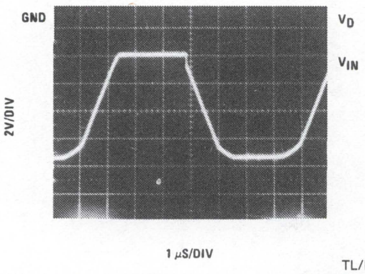
TL/H/5668-7

V_A = −5V



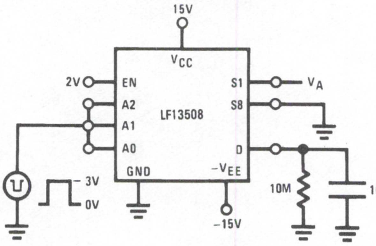
TL/H/5668-8

V_A = −10V



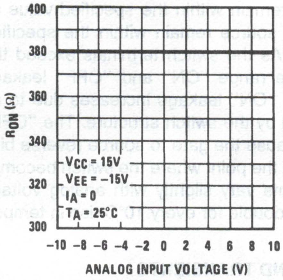
TL/H/5668-9

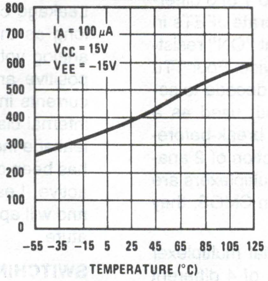
Test Circuit

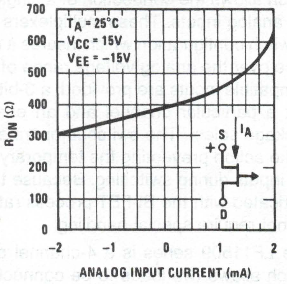

15V
V_{CC}
2V
EN
A2
A1
A0
GND
LF13508
S1
S8
D
$-V_{EE}$
V_A
3V
0V
10M
10 pF
−15V

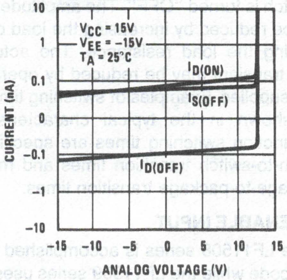
TL/H/5668-10

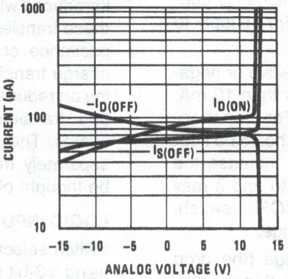
Typical Performance Characteristics

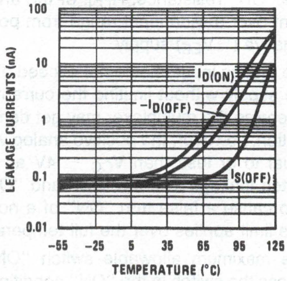

"ON" Resistance

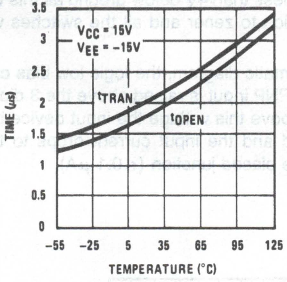

"ON" Resistance

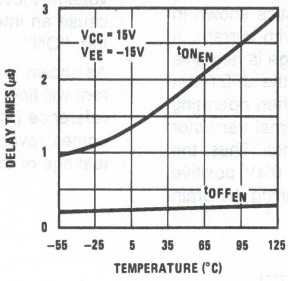

"ON" Resistance

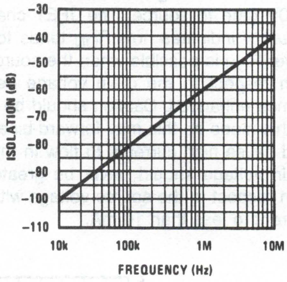

Switch Leakage Currents

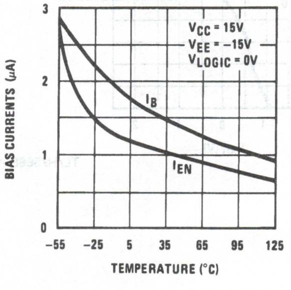

Switch Leakage Currents

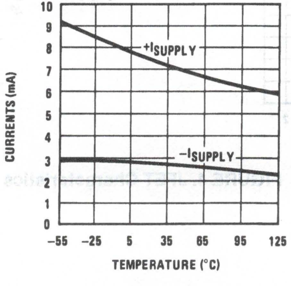

Switch Leakage Currents

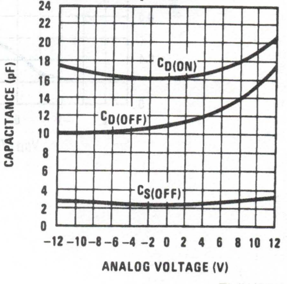

Switching Times (Figures 1 and 3)


Enable Delay Times (Figure 2)


"OFF" Isolation and Crosstalk


Bias Currents


Supply Currents


Switch Capacitances

TL/H/5668–11

Application Hints

The LF11508 series is an 8-channel analog multiplexer which allows the connection of a single load to 1 of 8 different analog inputs. These multiplexers incorporate JFETs in a switch configuration which insures a constant "ON" resistance over the analog voltage range of the device. Four TTL compatible inputs are provided; a 3-bit binary decode to select a particular channel and an enable input used as a package select. The switches operate with a break-before-make action preventing the temporary connection of 2 analog inputs during switching. Because these multiplexers are fabricated with the BI-FET process rather than CMOS, they do not require special handling.

The LF11509 series is a 4-channel differential multiplexer which allows two loads to be connected to 1 of 4 different pairs of analog inputs. The LF11509 series also has all the features of the LF11508.

ANALOG VOLTAGE AND CURRENT

The "ON" resistance, R_{ON}, of the analog switches is constant over a wide input range from positive (V_{CC}) supply to negative ($-V_{EE}$) supply.

The analog input should not exceed either positive or negative supply without limiting the current to less than 10 mA; otherwise the multiplexer may get damaged. For proper operation, however, the positive analog voltage should be kept equal to or less than $V_{CC} - 4V$ as this will increase the switch leakage in both "ON" and "OFF" state and it may also cause a false turn "ON" of a normally "OFF" switch. This limit applies over the full temperature range.

The maximum allowable switch "ON" voltage (the drop across the switch in the "ON" condition) is ±0.4V over temperature. If this number is to exceed the input current should be limited to 10 mA.

The "ON" resistance of the multiplexing switches varies slightly with analog current because they are JFETs running at 0V gate to source. The JFET characteristics shown in *Figure 4* indicates how R_{ON} tends to vary with current. A lower R_{ON} is possible when the source voltage is negative with respect to the drain voltage because the JFET becomes enhanced. Caution should be used when operating in this mode as this may forward-bias an internal transistor and cause high currents to flow in the switches. Thus, the drain voltage should never be greater than 0.4V positive with respect to the source voltage without limiting the drain current to less than 10 mA.

LEAKAGE CURRENTS

Leakage currents will remain within the specified value as long as the drain and source remain within the specified analog voltage range. As the switch terminals exceed the positive analog voltage range "ON" and "OFF" leakage currents increase. The "ON" leakage increases due to an internal clamp required by the switch structure. The "OFF" leakage increases because the gate to source reverse bias has been decreased to the point where the switch becomes active. Leakage currents vary slightly with analog voltage and will approximately double for every 10°C rise in temperature.

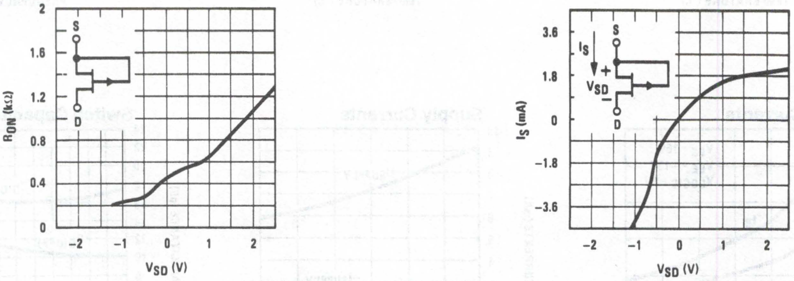
SWITCHING TIMES AND TRANSIENTS

These multiplexers operate with a break-before-make switch action. The turn off time is much faster than the turn on time to guarantee this feature over the full range of analog input voltage and temperature. Switching transients are introduced when a switch is turned "OFF". The amplitude of these transients may be reduced by increasing the load capacitance or decreasing the load resistance. The actual charge transfer in the transient may be reduced by operating on reduced power supplies. Examples of switching times and transients are shown in the typical characteristic curves. The enable function switching times are specified separately from switch-to-switch transition times and may be thought of as package-to-package transition times.

LOGIC INPUTS AND ENABLE INPUT

Switch selection in the LF11508 series is accomplished by using a 3-bit binary decode while the LF11509 series uses a 2-bit decode. These binary logic inputs are compatible with both TTL and CMOS logic voltage levels. The maximum positive voltage applied to these inputs may exceed V_{CC} but should not exceed $-V_{EE}+36V$. The maximum negative voltage should not be less than 4V below ground as this will cause an internal device to zener and all the switches will turn "ON".

As shown in the schematic diagram, the logic low bias current will flow until the PNP input is raised above the 3 diode reference (≈2.1V). Above this voltage the input device becomes reverse biased and the input current drops to the leakage of the reverse biased junction (<0.1 μA).



TL/H/5668-12

FIGURE 4. JFET Characteristics

Typical Applications

DATA ACQUISITION SYSTEM

A SIMPLIFIED SYSTEM DISCUSSION

Analog multiplexers (MUX) are usually used for multi-channel Data Acquisition Units (DAU). *Figure 5* shows a system in which 8 different analog inputs are sampled and converted into digital words for further processing. The sample and hold circuit is optional, depending on input speed requirements and on A/D converter speed.

Parameters characterizing the system are:

System Channels: The number of multiplexer channels.

Accuracy: The conversion accuracy of each individual sample with the system operating at the throughput rate.

Speed or Throughput Rate: Number of samples/second/channel the system can handle.

For a discussion on system structure, addressing mode and processor interfacing, see application note AN-159.

A. ACCURACY CONSIDERATIONS

1. Multiplexer's Influence on System Accuracy *(Figure 6)*.

   a. The error, (E), caused by the finite "ON" resistance, R_{ON}, of the multiplexing switches is given by:

$$E(\%) = \frac{100}{1 + R_{IN}/(R_{ON} + R_S + \Delta R_{ON})} \quad \text{where:}$$

R_{IN} = following stage input impedance

ΔR_{ON} = "ON" resistance modulation which is negligible for JFET switches like the LF11508

Example: Let $R_{ON} = 450\ \Omega$, $\Delta R_{ON} = 0$, $R_S = 0$, $T_A = 25°C$ and allowable $E = 0.01\%$ which is equivalent to 1/2 LSB in a 12-bit system:

$$R_{IN}\Big|_{min} = \frac{R_{ON}(100 - E)}{E} = 4.5\ M\Omega$$

Note that if temperature effects are included, some gain (or full scale) drift will occur; but effects on linearity are small.

   b. Multiplexer settling time (t_s):

$t_{s(ON)}$: is the time required for the MUX output to settle within a predetermined accuracy, as shown in Table I.

C_S *(Figure 6):* MUX output capacitance + following stage input capacitance + any stray capacitance at this node.

TABLE I.

ERROR %	BITS	$t_{s(ON)}$ TO 1/2 LSB
0.2	8	6.2t
0.05	10	7.6t
0.01	12	9t
0.0008	16	11.8t

$$t = C_S (R_{ON} + R_S) \parallel R_{IN}$$

$t_{s(OFF)}$: is the time it takes to discharge C_S within a tolerable error. The "OFF" settling time should be taken into account for bipolar inputs where its effects will appear as a worse case of doubling of the $t_{s(ON)}$.

2. Sample and Hold Influence on System Accuracy

   The sample and hold, if used, also introduces errors into the system accuracy due to:

   - Offset voltage of sample and hold
   - Droop rate in the Hold mode
   - T_A: Aperture time or time delay between the time of a digital Hold command and the actual Hold occurance
   - Taq: Acquisition time or time it takes to acquire an analog input and settle within a predetermined error band
   - Hold step: Error created during the Sample to Hold mode caused by an undesirable charge injected into the Hold capacitor C_h.

   For more details on sample and hold errors, see the LF198/LF298/LF398 data sheet.

3. A/D Converter Influence on System Accuracy

   The "accuracy" of the A/D converter is the best possible system accuracy. In most data acquisition systems, the A/D converter is the most expensive single component, so its error will often dominate system error. Care should be taken that MUX, S/H and input source errors do not exceed system error requirements when *added* to A/D errors. For instance, if an 8-bit accuracy system is desired and an 8-bit A/D converter is used, the accuracy of the MUX and S/H should be far better than 8 bits.

For details on A/D converter specifications, see AN-156.

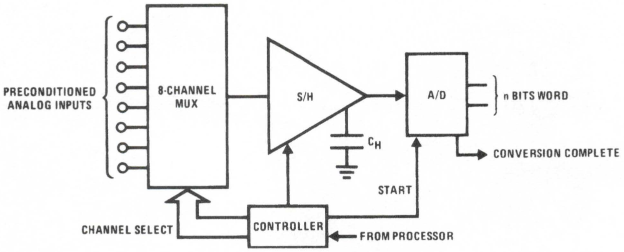


FIGURE 5. Random-Addressed, Multiplexed DAU

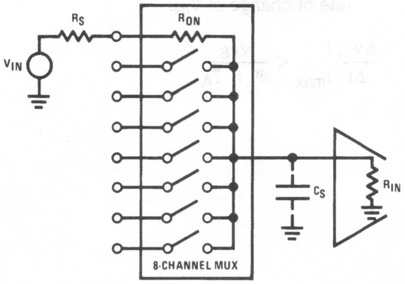


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FIGURE 6. 8-Channel MUX

Typical Applications (Continued)

B. SPEED CONSIDERATIONS

In the system of *Figure 5* with the S/H omitted, if n-bit accuracy is desired, the change of the analog input voltage should be less than ±1/2 LSB over the A/D conversion time T_C. In other words, the analog input slew rate, (rate of change of input voltage), will cause a slew-induced error and its magnitude, with respect to the total system error, will depend on the particular application.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{\pm 1/2\ \text{LSB}}{T_C} = \frac{V_{FS}}{2^n \times T_C}$$

where V_{FS} is the full scale voltage of the A/D. Note that slew induced errors are not affected by the MUX switch time since we can let the unit settle before starting conversion.

Example: Let $T_C = 40\ \mu s$ (MM4357), $V_{FS} = 10V$ and $n = 8$.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{1 mV}{\mu s}$$

which is a very small number. A 10 Vp-p sine wave of a frequency greater than 32 Hz will have higher slew rate than this. The maximum throughput rate of the above 8-channel system would be calculated using both the A/D conversion time and the sum of MUX switch "ON" time and settling time, i.e.:

$$\text{Th. R}\left.\right|_{max} = \frac{1}{8(T_C + T_{MUX})} = 3\text{k samples/sec/channel}$$

$$T_{MUX} = T_{ON} + T_{S(ON)}$$

Also notice that Nyquist sampling criteria would allow each channel to have a signal bandwidth of 1.5 kHz max, while the slew limit dictates a maximum frequency of 32 Hz. If the input signal has a peak-to-peak voltage less than 10V, the allowable maximum input frequency can be calculated by:

$$f_{MAX} = \frac{(\text{Slew Rate})max}{\pi\ \text{Vp-p}}$$

On the other hand, if the input voltage is not band-limited a low pass filter with an attenuation of 30 dB or better at 1.5 kHz, should be connected in front of the MUX.

1. Improving System Speed with a Sample and Hold

   The system speed can be improved by using the S/H shown in *Figure 5.* This allows a much greater rate of change of V_{IN}.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{V_{FS}}{2^n \times T_A}$$

where T_A is the aperture time of the S/H. This represents an input slew rate improvement by a factor: T_C/T_A. Here again, the slew rate error is not affected by the acquisition time of the Sample and Hold since conversion will start after the S/H has settled. *An important thing to notice is that the sample and hold errors will add to the total system error budget; therefore, the inequality of the $\Delta V_{IN}/\Delta t$ expression should become more stringent.*

Example: $T_C = 40\ \mu s$, $T_A = 0.5\ \mu s$, $n = 8$: $T_C/T_A = 80$

So the use of a S/H allows a speed improvement by nearly two orders of magnitude.

The maximum throughput rate can be calculated by:

$$\text{Th. R}\left.\right|_{max} = \frac{1}{8(T_A + \text{Taq} + T_C)}$$

Notice that T_{MUX} does not affect the $\Delta V_{IN}/\Delta t$ expression *nor the throughput rate* of the system since it may be switched and settled while the Sample and Hold is in the Hold mode. This is true, provided that: $T_{MUX} < T_A + T_C$.

C. SYSTEM EXAMPLE *(Figure 7)*

The LF398 S/H with a 1000 pF hold capacitor, has an acquisition time of 4 μs to 0.1% (1/4 LSB error for 8 bits) and an aperture time of less than 200 μs. On the other hand, after the hold command, the output will settle to ±0.05 mV in 1 μs. This, together with the acquisition time, introduces approximately a ±1/4 LSB error. Allowing another 1/4 LSB error for hold step and gain non-linearity, the maximum slew error ($\Delta V_{IN}/\Delta t$) should not exceed 1/4 LSB or:

$$\frac{\Delta V_{IN}}{\Delta t} \leq \frac{1}{4} \times \frac{1}{256} \times \frac{1}{T_A} \approx 5\text{mV}/\mu s$$

(which is the maximum slew rate of a 5 V peak sine wave. Also notice that, due to the above input slew restrictions, the analog delay caused by the finite BW of the S/H and the digital delay caused by the response time of the controller will be negligible. The maximum throughput rate of the system is:

$$\text{Th. R}\left.\right|_{max} = \frac{1}{8(5 + 40)10^{-6}} = 2800\ \text{samples/sec/ch.}$$

If the system speed requirements are relaxed, but the A/D converter is still too slow, then an inexpensive S/H can be built by using just a capacitor and a low cost FET input op amp as shown in *Figure 8.*

Typical Applications (Continued)

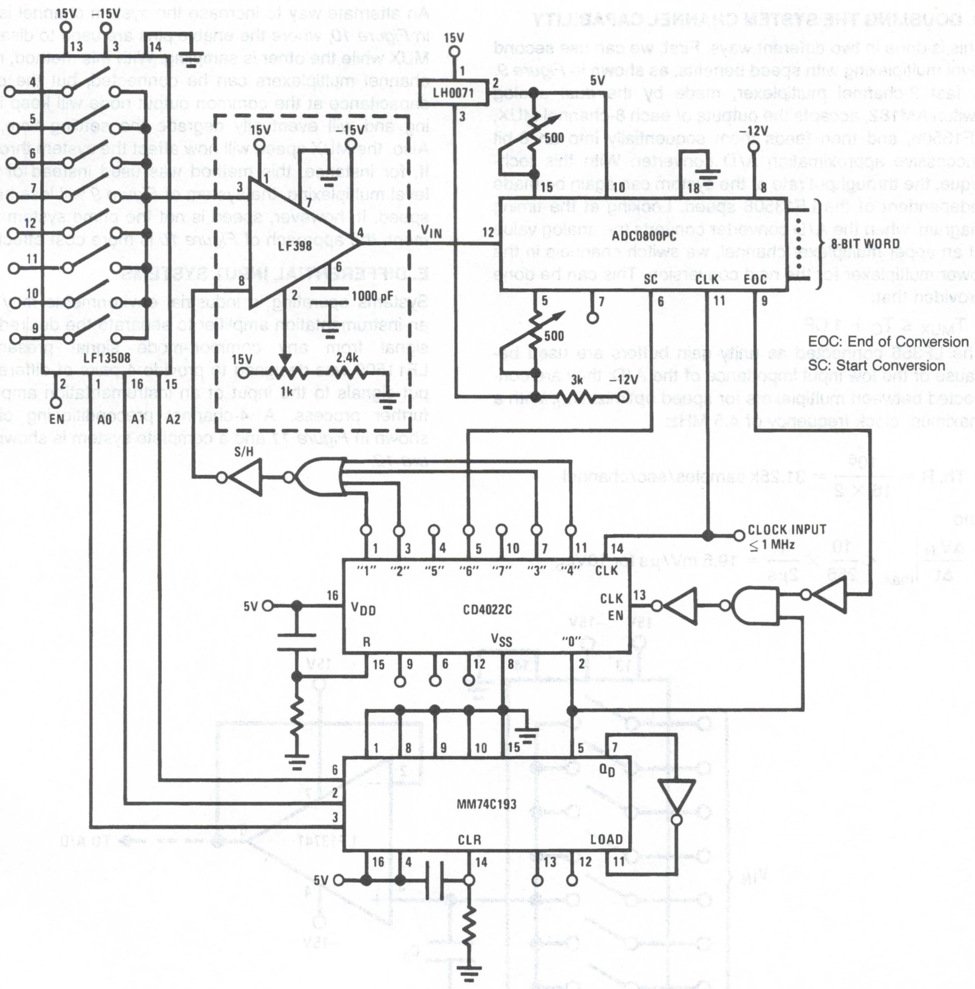

15V
−15V
13
3
14
4
5
6
7
12
11
10
9
2
1
16
15
EN
A0
A1
A2
LF13508
15V
1
LH0071
2
3
5V
15V
−15V
3
1
7
LF398
4
V_{IN}
8
6
2
1000 pF
15V
2.4k
1k
500
−12V
15
10
18
8
12
ADC0800PC
8-BIT WORD
SC
CLK
EOC
5
7
6
11
9
500
3k
−12V
EOC: End of Conversion
SC: Start Conversion
S/H
CLOCK INPUT
≤ 1 MHz
1
3
4
5
10
7
11
14
"1"
"2"
"5"
"6"
"7"
"3"
"4"
CLK
5V
16
V_{DD}
CD4022C
CLK
13
EN
R
V_{SS}
"0"
15
9
6
12
8
2
1
8
9
10
15
5
7
6
Q_D
2
MM74C193
3
CLR
LOAD
16
4
14
13
12
11
5V

FIGURE 7a. Sequentially Multiplexed DAU with Sample and Hold

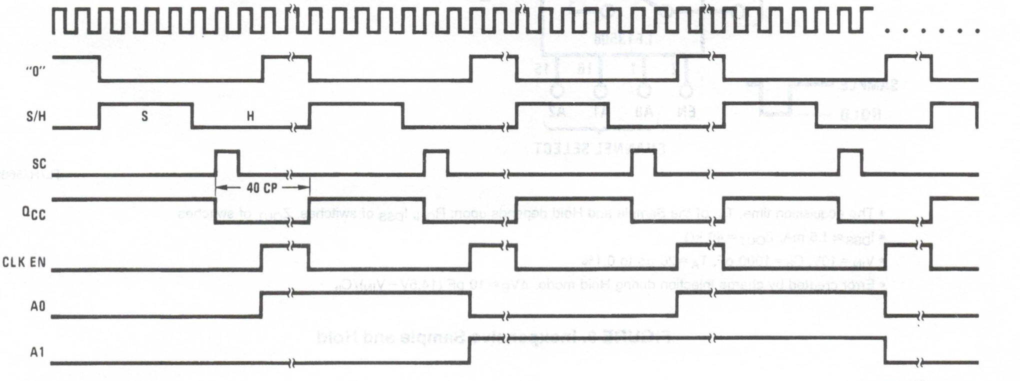

"0"
S/H
S
H
SC
40 CP
Q_{CC}
CLK EN
A0
A1
A2
TL/H/5668–14

FIGURE 7b. Timing Diagram

Typical Applications (Continued)

D. DOUBLING THE SYSTEM CHANNEL CAPABILITY

This is done in two different ways. First, we can use second level multiplexing with speed benefits, as shown in *Figure 9.* A fast 2-channel multiplexer, made by the dual analog switch AM182, accepts the outputs of each 8-channel MUX, LF13508, and then feeds them sequentially into an 8-bit successive approximation A/D converter. With this technique, the throughput rate of the system can again be made independent of the LF13508 speed. Looking at the timing diagram, when the A/D converter converts the analog value of an upper multiplexer channel, we switch channels in the lower multiplexer for the next conversion. This can be done provided that:

$$T_{MUX} \leq T_C + 1\ CP$$

The LF356 connected as unity gain buffers are used because of the low input impedance of the A/D; they are connected between multiplexers for speed optimization. With a maximum clock frequency of 4.5 MHz:

$$\text{Th. R} = \frac{10^6}{16 \times 2} = 31.25\text{k samples/sec/channel}$$

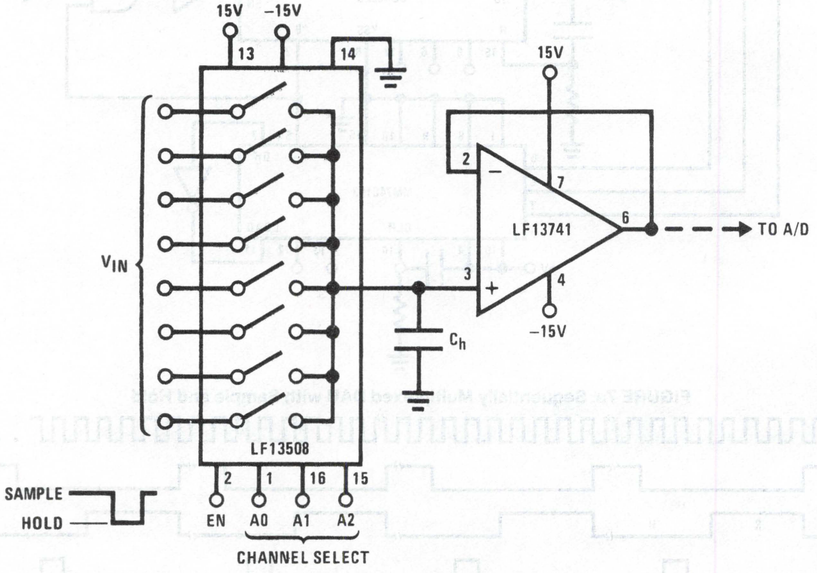
and

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{10}{256} \times \frac{1}{2\mu s} = 19.5\ mV/\mu s \text{ for } 10V_{FS}$$

An alternate way to increase the system channel is shown in *Figure 10,* where the enable pins are used to disable one MUX while the other is sampling. With this method, many 8-channel multiplexers can be connected, but the parasitic capacitance at the common output node will keep increasing and will eventually degrade the settling time, $t_{s(ON)}$. Also, the MUX speed will now affect the system throughput. If, for instance, this method was used instead of second level multiplexing, the system of *Figure 9* will lose half of its speed. If, however, speed is not the prime system requirement, the approach of *Figure 10* is more cost effective.

E. DIFFERENTIAL INPUT SYSTEMS

Systems operating in industrial environments may require an instrumentation amplifier to separate the desired analog signal from any common-mode signal present. The LF11509 was designed to provide 4 pairs of differential input signals to the input of an instrumentation amplifier for further process. A 4-channel preconditioning circuit is shown in *Figure 11* and a complete system is shown in *Figure 12.*



TL/H/5668–15

- The acquisition time, T_A, of the Sample and Hold depends upon: R_{ON}, I_{DSS} of switches, Z_{OUT} of switches
- $I_{DSS} \cong 1.5$ mA, $Z_{OUT} = 40$ kΩ
- $V_{IN} = 10V$, $C_h = 1000$ pF, $T_A = 20\ \mu s$ to 0.1%
- Error created by charge injection during Hold mode: $\Delta V_E \cong 10\ pF\ (14.5V - V_{IN})/C_h$

FIGURE 8. Inexpensive Sample and Hold

Typical Applications (Continued)

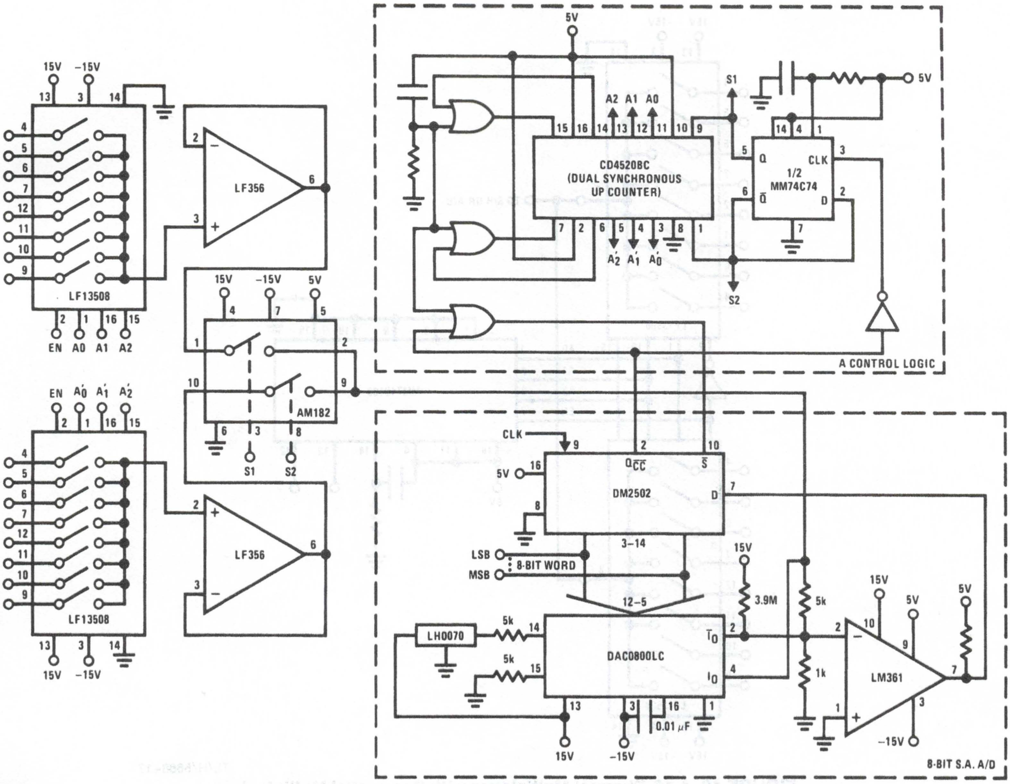
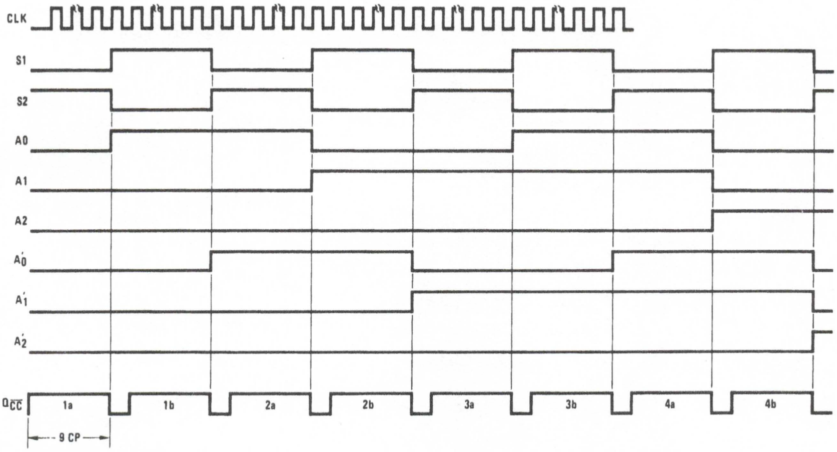

15V
−15V
13
3
14
4
5
6
7
12
11
10
9
LF13508
2
1
16
15
EN
A0
A1
A2
LF356
2
3
6
−
+
15V
−15V
5V
4
7
5
1
2
10
9
6
3
8
AM182
S1
S2
EN
A'0
A'1
A'2
LF13508
LF356
5V
A2
A1
A0
15
16
14
13
12
11
10
9
CD4520BC
(DUAL SYNCHRONOUS
UP COUNTER)
7
2
6
5
4
3
8
1
A'2
A'1
A'0
S1
S2
5V
14
4
1
Q
CLK
1/2
MM74C74
Q̄
D
3
2
6
7
A CONTROL LOGIC
CLK
9
2
10
16
5V
8
Q̄CC
S̄
D
DM2502
3–14
12–5
LSB
MSB
8-BIT WORD
15V
3.9M
5k
1k
LH0070
5k
14
5k
15
DAC0800LC
I̅O
IO
13
3
16
1
0.01 μF
15V
−15V
LM361
15V
5V
5V
10
9
7
2
1
3
−15V
8-BIT S.A. A/D

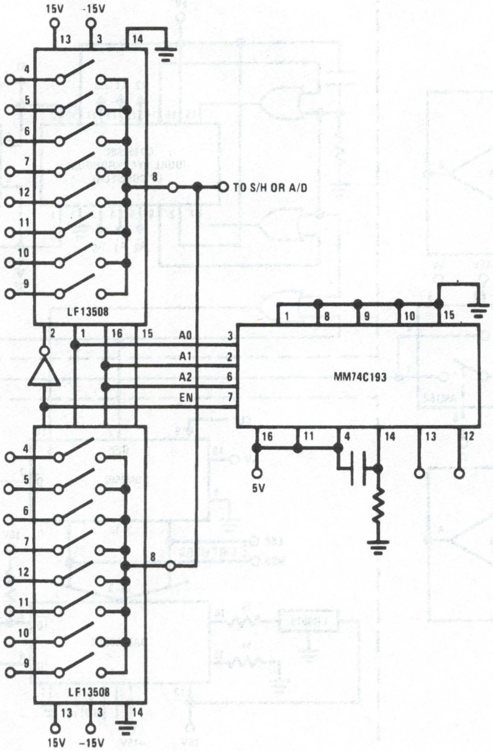
FIGURE 9a. A Fast 16-Channel DAU with Second Level Multiplexing


CLK
S1
S2
A0
A1
A2
A'0
A'1
A'2
QCC
1a
1b
2a
2b
3a
3b
4a
4b
9 CP

TL/H/5668–16

FIGURE 9b. Timing Diagram

Typical Applications (Continued)

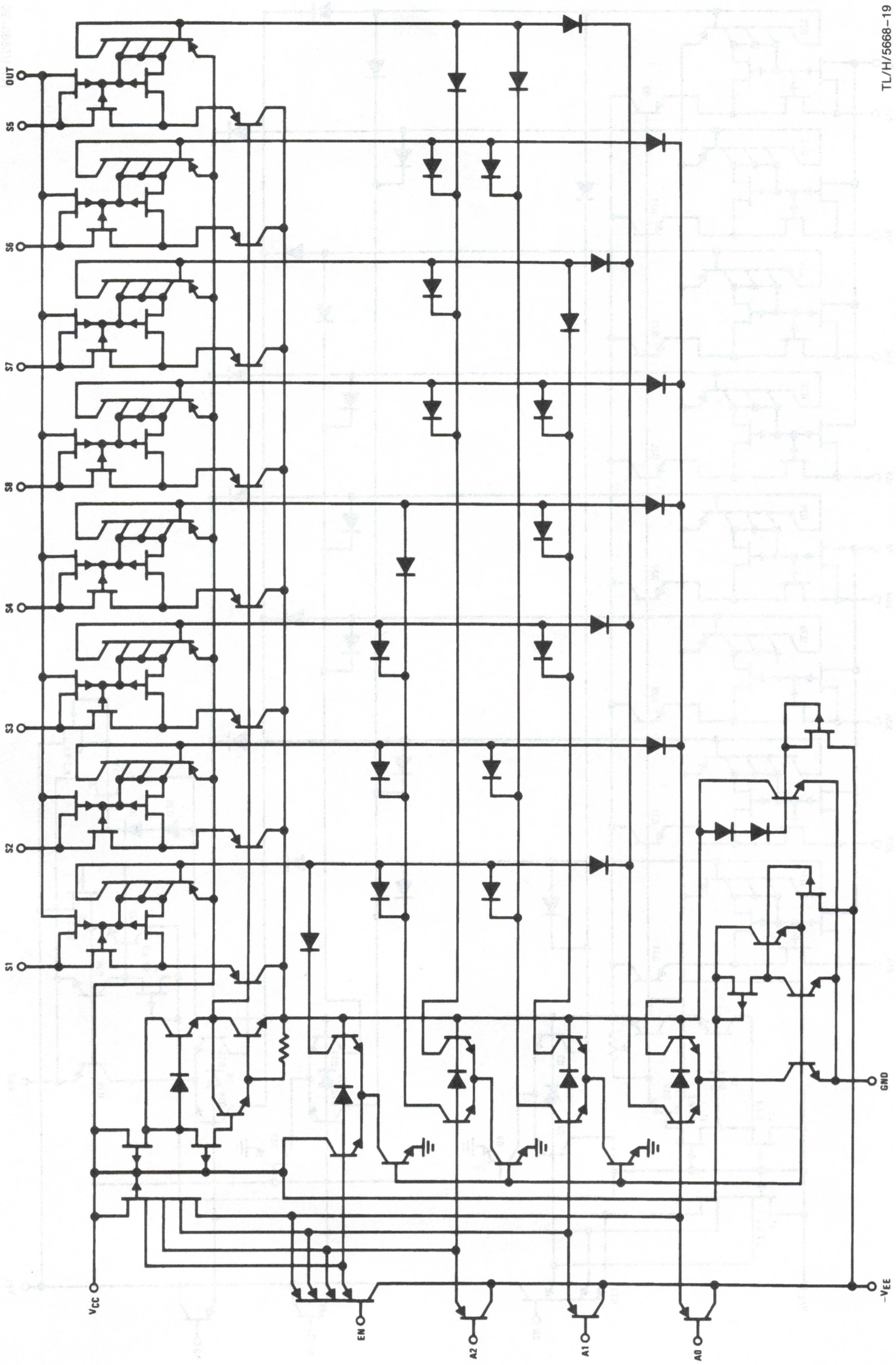

15V
-15V
13
3
14
4
5
6
7
12
11
10
9
8
TO S/H OR A/D
LF13508
2
1
16
15
A0
A1
A2
EN
3
2
6
7
1
8
9
10
15
MM74C193
16
11
4
14
13
12
5V
LF13508
13
3
14
15V
-15V

TL/H/5668-17

FIGURE 10. A 16-Channel Multiplexer with Sequential Multiplexing

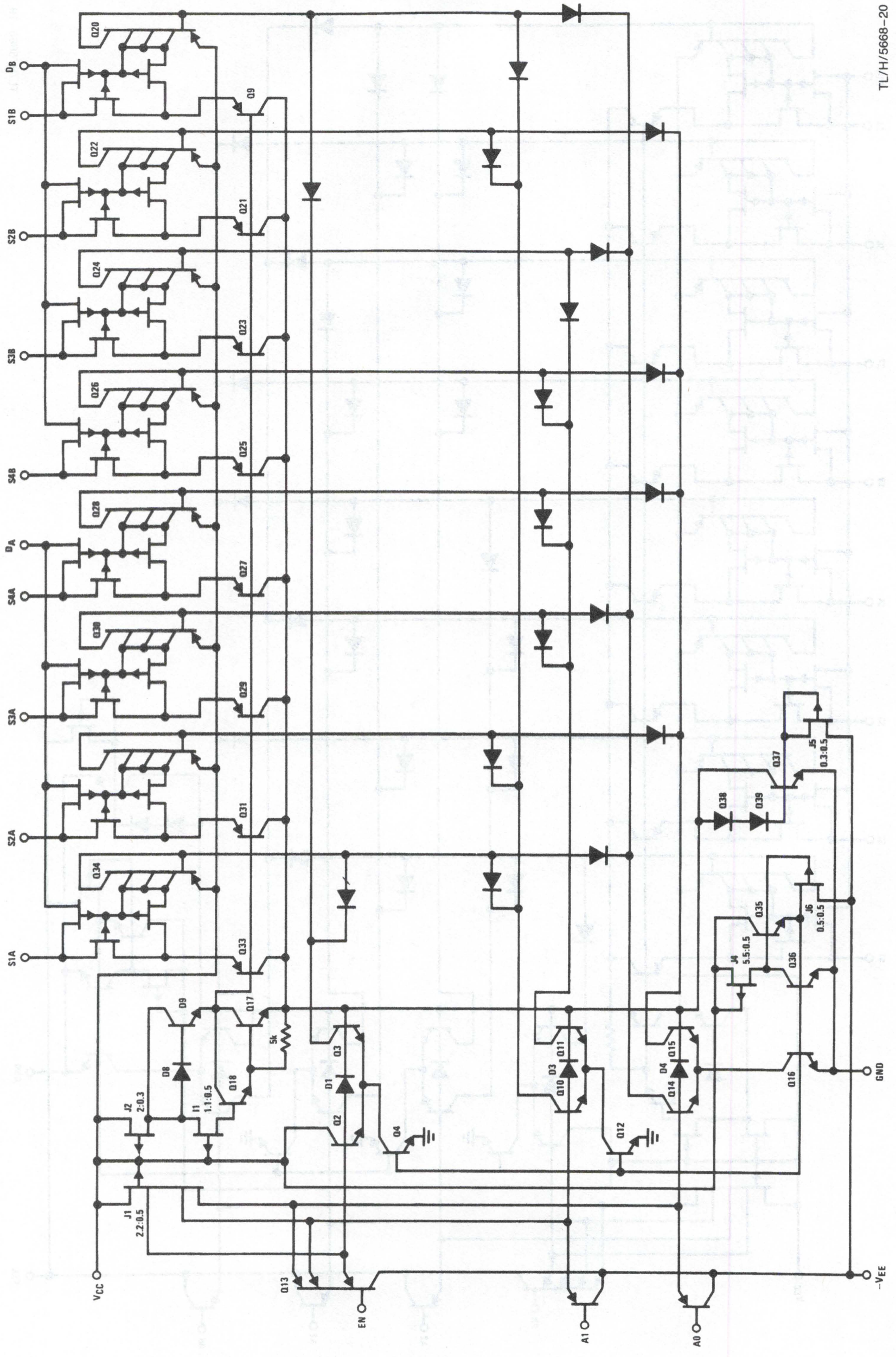
Schematic Diagrams

LF13508


TL/H/5668-19
OUT
S5
S6
S7
S8
S4
S3
S2
S1
V_{CC}
EN
A2
A1
A0
GND
$-V_{EE}$

Schematic Diagrams (Continued)

LF13509


Q20
DB
S1B
Q9
Q22
S2B
Q21
Q24
S3B
Q23
Q26
S4B
Q25
Q28
DA
S4A
Q27
Q30
S3A
Q29
S2A
Q31
Q34
S1A
Q33
D9
Q17
D8
Q18
5k
Q3
D1
Q2
Q4
J2
2:0.3
I1
1.1:0.5
J1
2.2:0.5
VCC
Q13
EN
Q11
D3
Q10
Q12
A1
Q15
D4
Q14
A0
Q16
GND
−VEE
Q38
Q39
Q37
J5
0.3:0.5
Q35
J4
5.5:0.5
J6
0.5:0.5
Q36

TL/H/5668-20

National Semiconductor Corporation

microCMOS

MM54HC4016/MM74HC4016 Quad Analog Switch

General Description

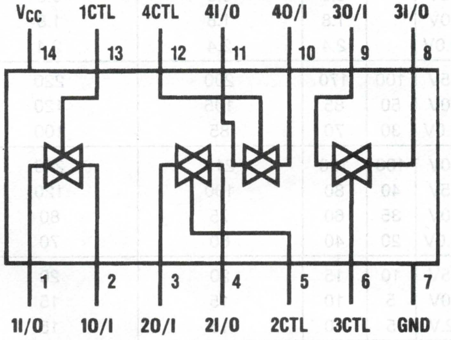
These devices are digitally controlled analog switches implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. The '4016 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 50Ω typ.
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Connection Diagram

Dual-In-Line Package



TL/F/5350–1

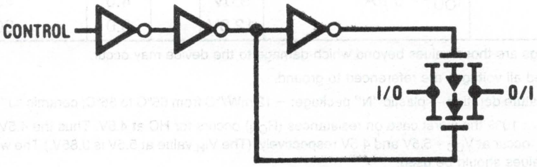
Top View

Order Number MM54HC4016J or MM74HC4016J, N
See NS Package J14A or N14A

Truth Table

Input	Switch
CTL	I/O–O/I
L	"OFF"
H	"ON"

Schematic Diagram



TL/F/5350–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	6.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			9.0V		1.8	1.8	1.8	V
			12.0V		2.4	2.4	2.4	V
R_{ON}	Maximum 'ON' Resistance (See Note 5)	$V_{CTL}=V_{IH}$, I_S=1.0 mA $V_{IS}=V_{CC}$ to GND (Figure 1)	4.5V	100	170	200	220	Ω
			9.0V	50	85	105	120	Ω
			12.0V	30	70	85	100	Ω
		$V_{CTL}=V_{IH}$, I_S=1.0 mA $V_{IS}=V_{CC}$ or GND (Figure 1)	2.0V	100	180	215	240	Ω
			4.5V	40	80	100	120	Ω
			9.0V	35	60	75	80	Ω
			12.0V	20	40	60	70	Ω
R_{ON}	Maximum 'ON' Resistance Matching	$V_{CTL}=V_{IH}$ $V_{IS}=V_{CC}$ to GND	4.5V	10	15	20	20	Ω
			9.0V	5	10	15	15	Ω
			12.V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch 'OFF' Leakage Current	$V_{OS}=V_{CC}$ or GND V_{IS}=GND or V_{CC} $V_{CTL}=V_{IL}$ (Figure 2)	6.0V		±60	±600	±600	nA
			9.0V		±80	±800	±800	nA
			12.0V		±100	±1000	±1000	nA
I_{IZ}	Maximum Switch 'ON' Leakage Current	$V_{OS}=V_{CC}$ or GND $V_{CTL}=V_{IH}$ (Figure 3)	6.0V		±40	±150	±150	nA
			9.0V		±50	±200	±200	nA
			12.0V		±60	±300	±300	nA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA
			9.0V		4.0	40	80	μA
			12.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so these values should be used.

Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics V_{CC} = 2.0V–12.0V, C_L = 50 pF (unless otherwise specified), (Notes 6 and 7)

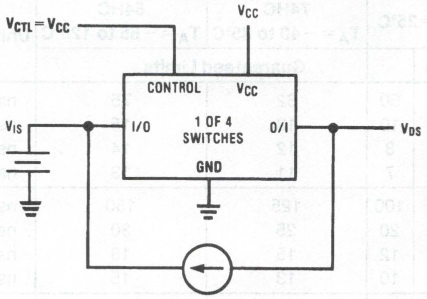
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V 4.5V 9.0V 12.0V	25 5 4 3	50 10 8 7	62 13 12 11	75 15 14 13	ns ns ns ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	2.0V 4.5V 9.0V 12.0V	32 8 6 5	100 20 12 10	125 25 15 13	150 30 18 15	ns ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	R_L = 1 kΩ	2.0V 4.5V 9.0V 12.0V	45 15 10 8	168 36 32 30	210 45 40 38	252 54 48 45	ns ns ns ns
	Minimum Frequency Response (Figure 7) 20 log (V_{OS}/V_{IS}) = −3 dB	R_L = 600Ω, V_{IS} = 2V_{PP} at (V_{CC}/2) (Notes 6 & 7)	4.5V 9.0V	40 100				MHz MHz
	Control to Switch Feedthrough Noise (Figure 8)	R_L = 600Ω, F = 1 MHz C_L = 50 pF (Notes 7 & 8)	4.5V 9.0V	100 250				mV mV
	Crosstalk Between any Two Switches (Figure 9)	R_L = 600Ω, F = 1 MHz	4.5V 9.0V	−52 −50				dB dB
	Switch OFF Signal Feedthrough Isolation (Figure 10)	R_L = 600Ω, F = 1 MHz V_{CTL} = V_{IL} (Notes 7 & 8)	4.5V 9.0V	−42 −44				dB dB
THD	Sinewave Harmonic Distortion (Figure 11)	R_L = 10 kΩ, C_L = 50 pF, F = 1 kHz V_{IS} = 4V_{PP} V_{IS} = 8V_{PP}	4.5V 9.0V	0.013 0.008				% %
C_{IN}	Maximum Control Input Capacitance			5				pF
C_{IN}	Maximum Switch Input Capacitance			15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND		5				pF
C_{PD}	Power Dissipation Capacitance	(per switch)		15				pF

Note 6: Adjust 0 dBm for F = 1 kHz (Null R_L/R_{ON} Attenuation)

Note 7: V_{IS} is centered at V_{CC}/2

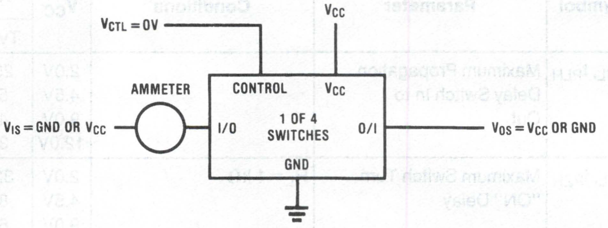
Note 8: Adjust input for 0 dBm

AC Test Circuits and Switching Time Waveforms


V_CTL = V_CC
V_CC
CONTROL
V_CC
V_IS
I/O
1 OF 4
SWITCHES
O/I
V_OS
GND

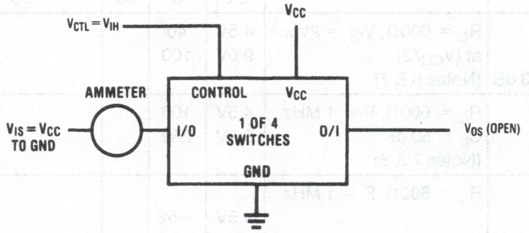
TL/F/5350-3

FIGURE 1. "ON" Resistance


V_CTL = 0V
V_CC
AMMETER
CONTROL
V_CC
V_IS = GND OR V_CC
I/O
1 OF 4
SWITCHES
O/I
V_OS = V_CC OR GND
GND

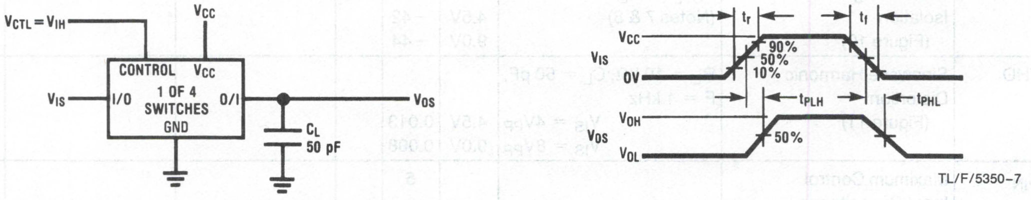
TL/F/5350-4

FIGURE 2. "OFF" Channel Leakage Current


V_CTL = V_IH
V_CC
AMMETER
CONTROL
V_CC
V_IS = V_CC TO GND
I/O
1 OF 4
SWITCHES
O/I
V_OS (OPEN)
GND

TL/F/5350-5

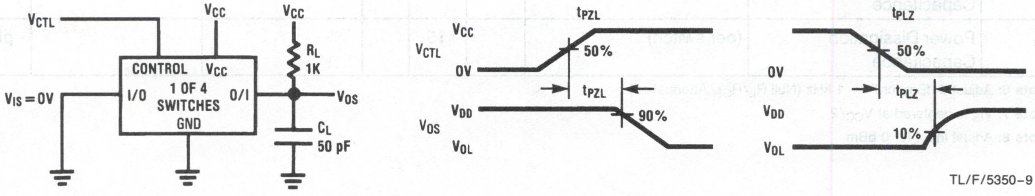
FIGURE 3. "ON" Channel Leakage Current


V_CTL = V_IH
V_CC
CONTROL
V_CC
V_IS
I/O
1 OF 4
SWITCHES
O/I
GND
V_OS
C_L
50 pF
t_r
t_f
V_CC
V_IS
0V
90%
50%
10%
t_PLH
t_PHL
V_OH
V_OS
V_OL
50%

TL/F/5350-6

TL/F/5350-7

FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output


V_CTL
V_CC
V_CC
R_L
1K
CONTROL
V_CC
V_IS = 0V
I/O
1 OF 4
SWITCHES
O/I
V_OS
GND
C_L
50 pF
t_PZL
V_CC
V_CTL
0V
50%
t_PZL
V_DD
V_OS
V_OL
90%
t_PLZ
50%
0V
t_PLZ
V_DD
10%
V_OL

TL/F/5350-8

TL/F/5350-9

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

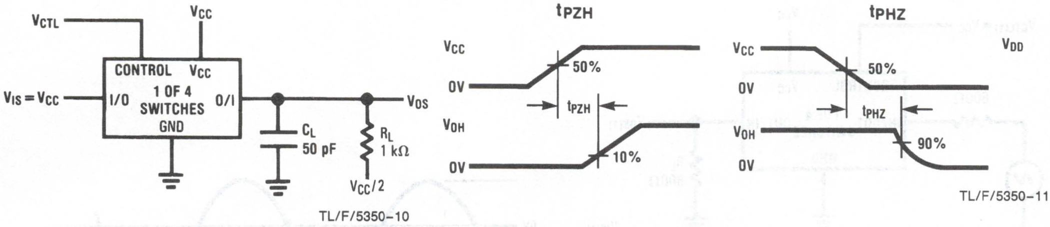

V_{CTL}
VCC
CONTROL
VCC
VIS = VCC
I/O
1 OF 4
SWITCHES
O/I
GND
VOS
CL
50 pF
RL
1 kΩ
VCC/2
TL/F/5350-10
tPZH
VCC
50%
0V
tPZH
VOH
10%
0V
tPHZ
VCC
50%
0V
tPHZ
VOH
90%
0V
VDD
TL/F/5350-11

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

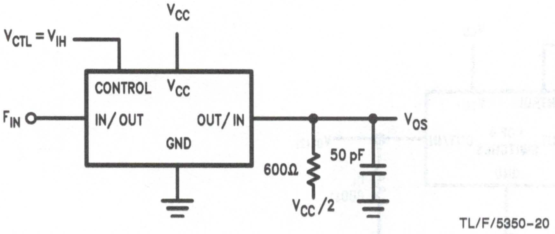

VCC
VCTL = VIH
CONTROL
VCC
FIN
IN/OUT
OUT/IN
GND
VOS
600Ω
50 pF
VCC/2
TL/F/5350-20

FIGURE 7. Frequency Response

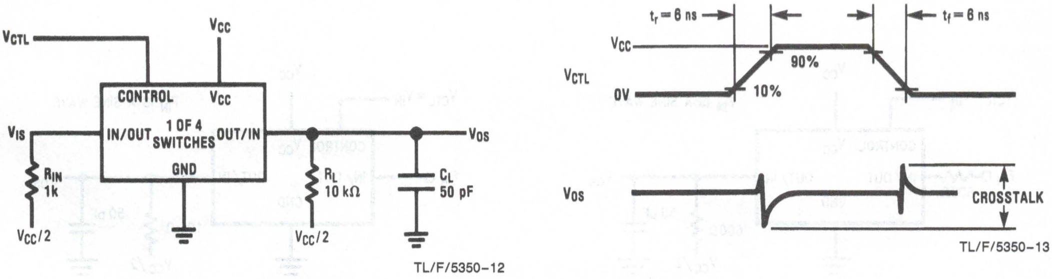

VCTL
VCC
CONTROL
VCC
VIS
IN/OUT
1 OF 4
SWITCHES
OUT/IN
GND
VOS
RIN
1k
VCC/2
RL
10 kΩ
VCC/2
CL
50 pF
TL/F/5350-12
tr = 6 ns
tf = 6 ns
VCC
90%
VCTL
0V
10%
VOS
CROSSTALK
TL/F/5350-13

FIGURE 8. Crosstalk: Control Input to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

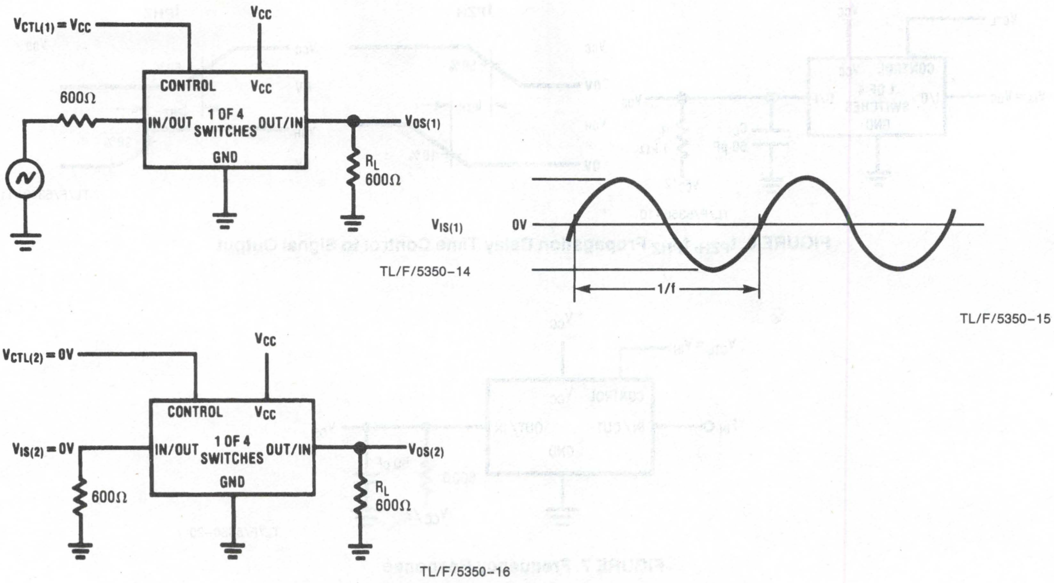

VCTL(1) = VCC
VCC
CONTROL
VCC
600Ω
IN/OUT
1 OF 4
SWITCHES
OUT/IN
VOS(1)
GND
RL
600Ω
VIS(1)
0V
1/f
TL/F/5350-14
TL/F/5350-15
VCTL(2) = 0V
VCC
CONTROL
VCC
VIS(2) = 0V
IN/OUT
1 OF 4
SWITCHES
OUT/IN
VOS(2)
GND
600Ω
RL
600Ω
TL/F/5350-16

FIGURE 9. Crosstalk Between Any Two Switches

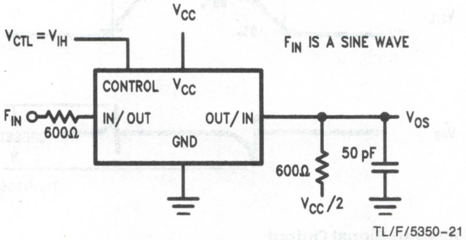

VCTL = VIH
VCC
FIN IS A SINE WAVE
CONTROL
VCC
FIN
600Ω
IN/ OUT
OUT/ IN
VOS
GND
600Ω
50 pF
VCC/2
TL/F/5350-21

FIGURE 10. Switch OFF Signal Feedthrough Isolation

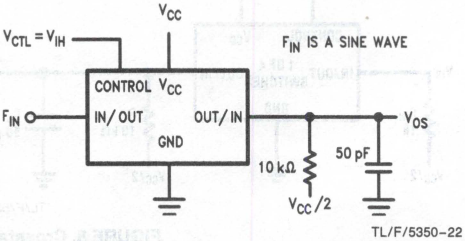
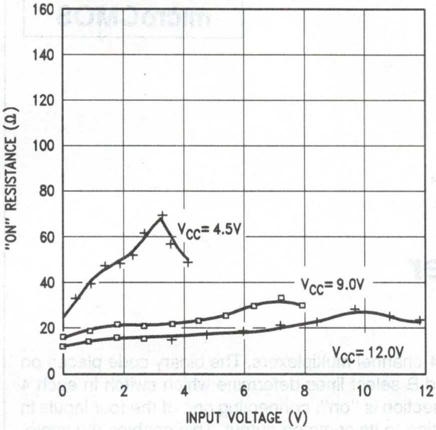

VCTL = VIH
VCC
FIN IS A SINE WAVE
CONTROL
VCC
FIN
IN/ OUT
OUT/ IN
VOS
GND
10 kΩ
50 pF
VCC/2
TL/F/5350-22

FIGURE 11. Sinewave Distortion

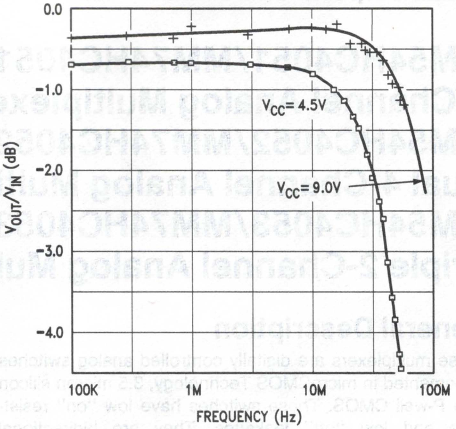
Typical Performance Characteristics

Typical "On" Resistance



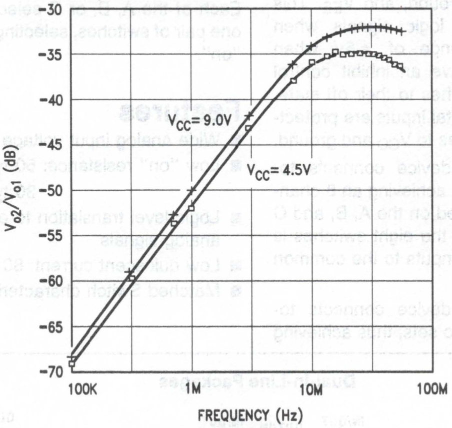
TL/F/5350-19

Typical Frequency Response



TL/F/5350-23

Typical Crosstalk Between Any Two Switches



TL/F/5350-24

National
Semiconductor
Corporation

PRELIMINARY

microCMOS

MM54HC4051/MM74HC4051
8-Channel Analog Multiplexer
MM54HC4052/MM74HC4052
Dual 4-Channel Analog Multiplexer
MM54HC4053/MM74HC4053
Triple 2-Channel Analog Multiplexer

General Description

These multiplexers are digitally controlled analog switches implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the on resistance and increases switch linearity. These devices allow control of up to ±6V (peak) analog signals with digital control signals of 0 to 6V. Three supply pins are provided for V_{CC}, ground, and V_{EE}. This enables the connection of 0–5V logic signals when V_{CC}=5V and an analog input range of ±5V when V_{EE}=5V. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

MM54HC4051/MM74HC4051: This device connects together the outputs of 8 switches, thus achieving an 8 channel Multiplexer. The binary code placed on the A, B, and C select lines determines which one of the eight switches is "on", and connects one of the eight inputs to the common output.

MM54HC4052/MM74HC4052: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4-channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is "on", connecting one of the four inputs in each section to its common output. This enables the implementation of a 4-channel differential multiplexer.

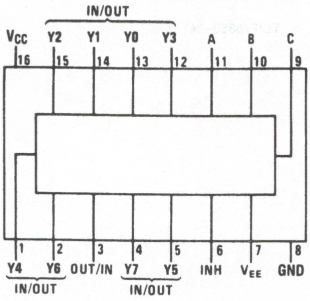
MM54HC4053/MM74HC4053: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of 3 single-pole-double throw configurations. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be "on".

Features

- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Logic level translation to enable 5V logic with ±5V analog signals
- Low quiescent current: 80 μA maximum (74HC)
- Matched Switch characteristic

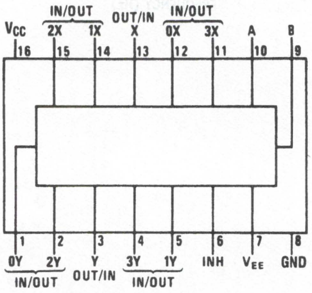
Connection Diagrams

Dual-In-Line Packages



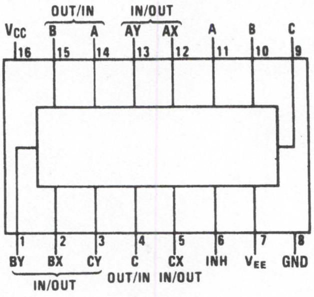
TL/F/5353–1

Top View



TL/F/5353–2

Top View



TL/F/5353–3

Top View

Order Number MM54HC4051J, MM54HC4052J, MM54HC4053J,
MM74HC4051J, N, MM74HC4052J, N or MM74HC4053J, N
See NS Package J16A or N16E

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
Output Current, per pin (I_{OUT})	±25 mA
V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
Supply Voltage (V_{EE})		0	−6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage			2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
R_{ON}	Maximum "ON" Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=1.0 mA V_{IS}=V_{CC} to V_{EE} (Figure 1)	GND	4.5V	40	200	250	300	Ω
			−4.5V	4.5V	30	100	125	150	Ω
			−6.0V	6.0V	20	90	112	135	Ω
		V_{CTL}=V_{IH}, I_S=1.0 mA V_{IS}=V_{CC} or V_{EE} (Figure 1)	GND	2.0V	100	230	290	350	Ω
			GND	4.5V	40	110	138	165	Ω
			−4.5V	4.5V	20	90	110	135	Ω
			−6.0V	6.0V	15	80	100	120	Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL}=V_{IH} V_{IS}=V_{CC} to GND	GND	4.5V	10	15	20	20	Ω
			−4.5V	4.5V	5	10	15	15	Ω
			−6.0V	6.0V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND V_{CC}=2−6V				±0.1	±1.0	±1.0	µA
I_{IZ}	Maximum Switch "OFF" Leakage Current (Switch Input)	V_{OS}=V_{CC} or GND V_{IS}=GND or V_{CC} V_{INH}=V_{IH} (Figure 2)	GND	6.0V		±60	±600	±600	nA
			−6.0V	6.0V		±100	±1000	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	HC4051 V_{OS}=V_{CC} or GND V_{INH}=V_{IL} (Figure 3)	GND	6.0V					µA
			−6.0V	6.0V					µA
		HC4052 V_{OS}=V_{CC} or GND V_{INH}=V_{IL} (Figure 3)	GND	6.0V					µA
			−6.0V	6.0V					µA
		HC4053 V_{OS}=V_{CC} or GND V_{INH}=V_{IL} (Figure 3)	GND	6.0V					µA
			−6.0V	6.0V					µA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}−V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

DC Electrical Characteristics (Note 4) (Continued)

Symbol	Parameter		Conditions	V_{EE}	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
						Typ		Guaranteed Limits		
I_{IZ}	Maximum Switch "OFF" Leakage Current (Common Pin)	HC4051	$V_{OS}=V_{CC}$ or GND $V_{IS}=$ GND or V_{CC} $V_{INH}=V_{IH}$	GND	6.0V					μA
				−6.0V	6.0V					μA
		HC4052	$V_{OS}=V_{CC}$ or GND $V_{IS}=$ GND or V_{CC} $V_{INH}=V_{IH}$	GND	6.0V					μA
				−6.0V	6.0V					μA
		HC4053	$V_{OS}=V_{CC}$ or GND $V_{IS}=$ GND or V_{CC} $V_{INH}=V_{IH}$	GND	6.0V					μA
				−6.0V	6.0V					μA
I_{CC}	Maximum Quiescent Supply Current		$V_{IN}=V_{CC}$ or GND $I_{OUT}=0$ μA	GND	6.0V		8	80	160	μA
				−6.0V	6.0V		16	160	320	μA

AC Electrical Characteristics $V_{CC}=2.0V–6.0V$ $V_{EE}=0V–6V$, $C_L=50$ pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	2.0V	25	50	62	75	ns
			GND	4.5V	5	10	13	15	ns
			−4.5V	4.5V	4	8	12	14	ns
			−6.0V	6.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	$R_L=1$ kΩ	GND	2.0V	92				ns
			GND	4.5V	18				ns
			−4.5V	4.5V	16				ns
			−6.0V	6.0V	15				ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay		GND	2.0V	65				ns
			GND	4.5V	28				ns
			−4.5V	4.5V	18				ns
			−6.0V	6.0V	16				
f_{MAX}	Minimum Switch Frequency Response 20 log $(V_I/V_O)=3$ dB		GND	4.5V	30				MHz
			−4.5V	4.5V	35				MHz
	Cross Talk Control to Switch	(Figure 7)	−4.5V	4.5V	180				mV_{P-P}
	Cross Talk Between any Two Switches (Frequency at −50 dB)	(Figure 8)	−4.5V	4.5V					MHz
	Feed Through, Switch Input to Output	F = 5 MHz							dB
		F = 10 MHz							dB
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input			15				pF
		4051 Common			90				
		4052 Common			45				
		4053 Common			30				
C_{IN}	Maximum Feedthrough Capacitance				5				pF

Truth Tables

'4051

Input				"ON" Channel
Inh	C	B	A	
H	X	X	X	None
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7

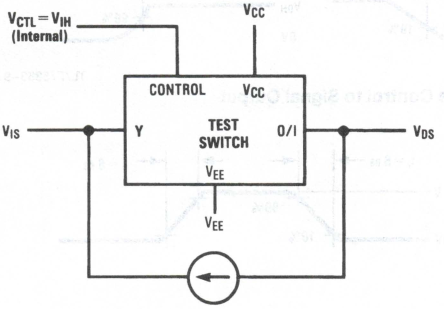
'4052

Inputs			"ON" Channels	
Inh	B	A	X	Y
H	X	X	None	None
L	L	L	0X	0Y
L	L	H	1X	1Y
L	H	L	2X	2Y
L	H	H	3X	3Y

'4053

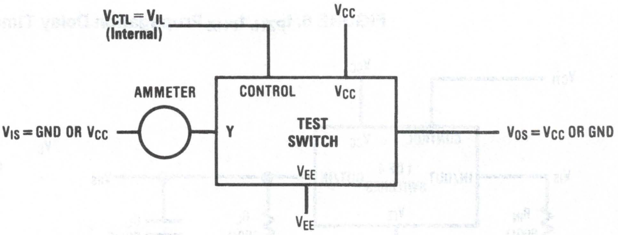
Input				"ON" Channels		
Inh	C	B	A	C	b	a
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AY
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AY
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AY
L	H	H	H	CY	BY	AY

AC Test Circuits and Switching Time Waveforms


$V_{CTL} = V_{IH}$ (Internal)
V_{CC}
CONTROL
V_{CC}
TEST SWITCH
V_{IS}
Y
0/I
V_{OS}
V_{EE}
V_{EE}

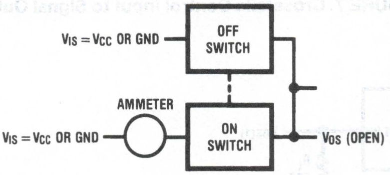
TL/F/5353-4

FIGURE 1. "ON" Resistance


$V_{CTL} = V_{IL}$ (Internal)
V_{CC}
AMMETER
CONTROL
V_{CC}
V_{IS} = GND OR V_{CC}
Y
TEST SWITCH
V_{OS} = V_{CC} OR GND
V_{EE}
V_{EE}

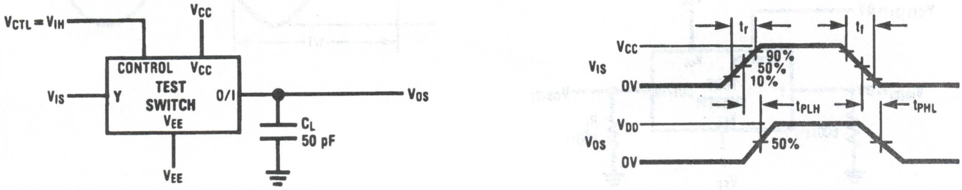
TL/F/5353-5

FIGURE 2. "OFF" Channel Leakage Current


V_{IS} = V_{CC} OR GND
OFF SWITCH
AMMETER
V_{IS} = V_{CC} OR GND
ON SWITCH
V_{OS} (OPEN)

TL/F/5353-6

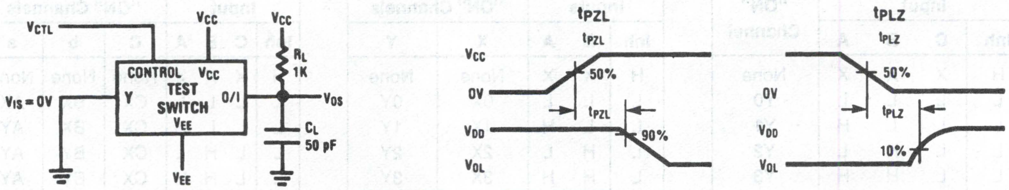
FIGURE 3. "ON" Channel Leakage Current


$V_{CTL} = V_{IH}$
V_{CC}
CONTROL
V_{CC}
TEST SWITCH
V_{IS}
Y
0/I
V_{EE}
V_{OS}
C_L 50 pF
V_{EE}
t_r
t_f
V_{CC}
V_{IS}
0V
90%
50%
10%
t_{PLH}
t_{PHL}
V_{DD}
V_{OS}
0V
50%

TL/F/5353-7

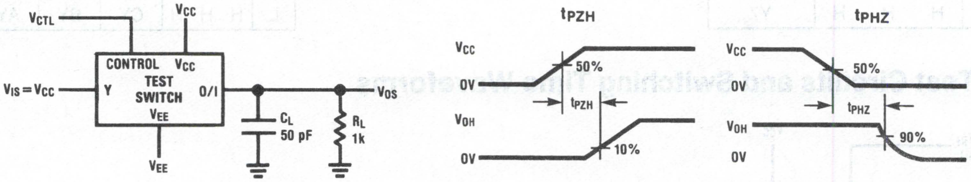
FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)


VCTL
VIS = 0V
CONTROL
VCC
TEST SWITCH
Y
O/I
VEE
VCC
VCC
RL 1K
VOS
CL 50 pF
tPZL
VCC
0V
50%
tPZL
VDD
90%
VOL
tPLZ
50%
0V
tPLZ
VDD
10%
VOL

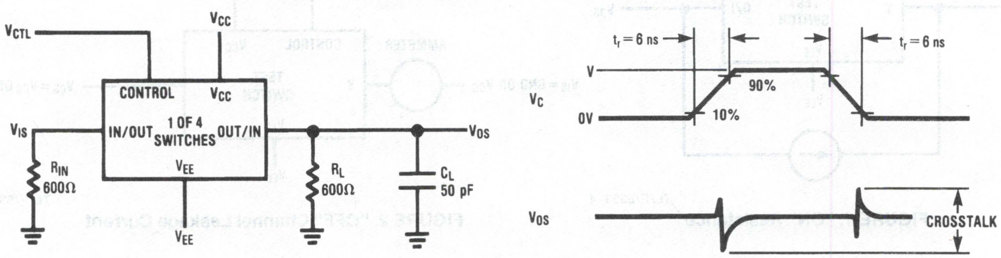
TL/F/5353-8

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output


VCTL
VCC
VIS = VCC
CONTROL
VCC
TEST SWITCH
Y
O/I
VEE
VEE
CL 50 pF
RL 1k
VOS
tPZH
VCC
0V
50%
tPZH
VOH
0V
10%
tPHZ
VCC
0V
50%
tPHZ
VOH
0V
90%
VDD

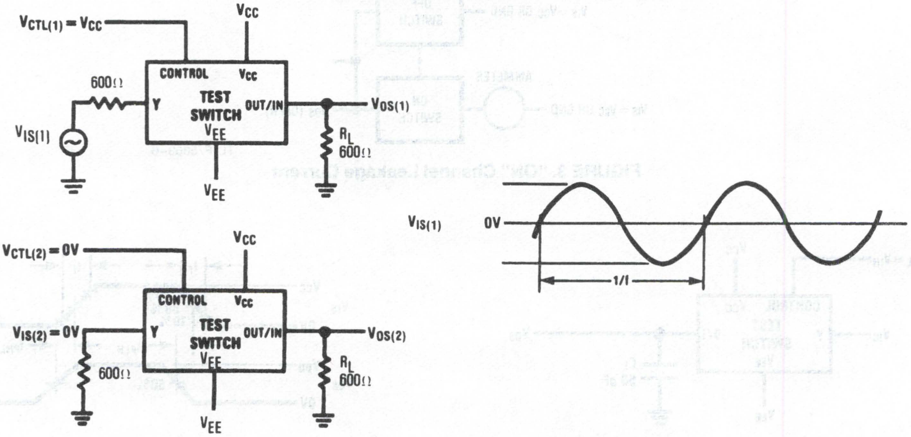
TL/F/5353-9

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay TIme Control to Signal Output


VCTL
VCC
CONTROL
VCC
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VEE
VIS
RIN 600Ω
RL 600Ω
CL 50 pF
VOS
VEE
tr = 6 ns
tf = 6 ns
V
VC
0V
90%
10%
VOS
CROSSTALK

TL/F/5353-10

FIGURE 7. Crosstalk: Control Input to Signal Output

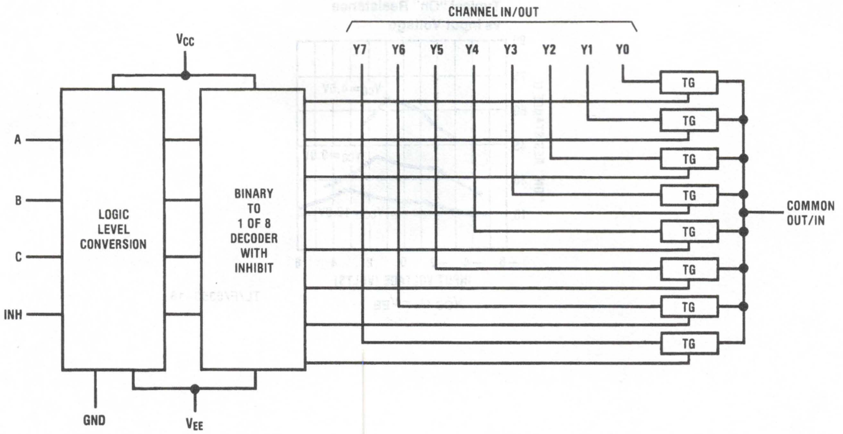

VCTL(1) = VCC
VCC
CONTROL
VCC
600Ω
VIS(1)
Y
TEST SWITCH
OUT/IN
VEE
VOS(1)
RL 600Ω
VEE
VIS(1)
0V
1/f
VCTL(2) = 0V
VCC
CONTROL
VCC
VIS(2) = 0V
Y
TEST SWITCH
OUT/IN
VEE
VOS(2)
600Ω
RL 600Ω
VEE

TL/F/5353-11

FIGURE 8. Crosstalk Between Any Two Switches

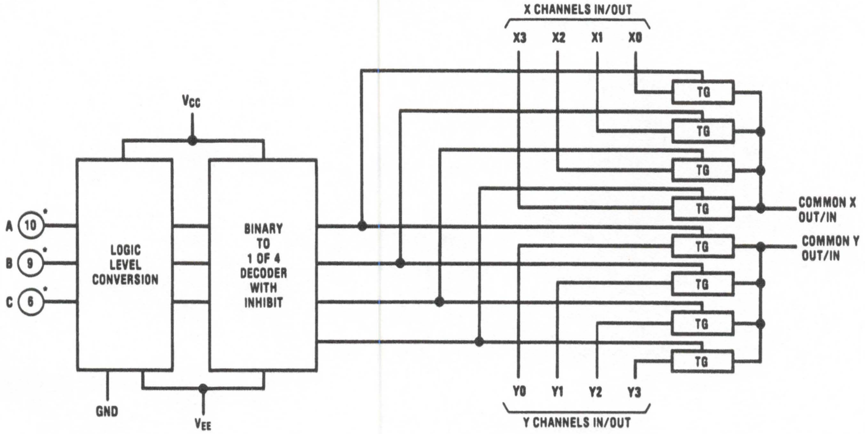
Logic Diagrams

MM54HC4051/MM74HC4051


CHANNEL IN/OUT
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
Vcc
A
B
C
INH
LOGIC LEVEL CONVERSION
BINARY TO 1 OF 8 DECODER WITH INHIBIT
TG
COMMON OUT/IN
GND
VEE

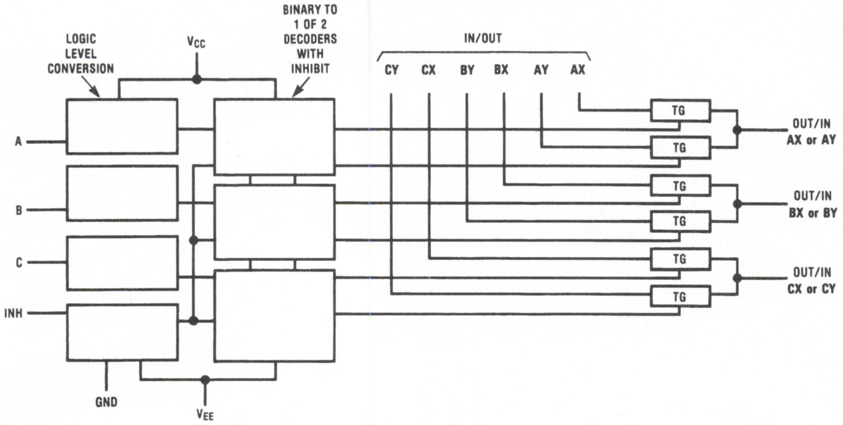
TL/F/5353-19

MM54HC4052/MM74HC4052


X CHANNELS IN/OUT
X3
X2
X1
X0
Vcc
A 10
B 9
C 6
LOGIC LEVEL CONVERSION
BINARY TO 1 OF 4 DECODER WITH INHIBIT
TG
COMMON X OUT/IN
COMMON Y OUT/IN
GND
VEE
Y0
Y1
Y2
Y3
Y CHANNELS IN/OUT

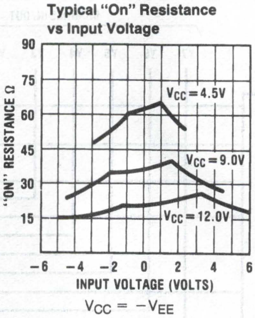
TL/F/5353-20

MM54HC4053/MM74HC4053


LOGIC LEVEL CONVERSION
Vcc
BINARY TO 1 OF 2 DECODERS WITH INHIBIT
IN/OUT
CY
CX
BY
BX
AY
AX
A
B
C
INH
TG
OUT/IN AX or AY
OUT/IN BX or BY
OUT/IN CX or CY
GND
VEE

TL/F/5353-21

Typical Performance Characteristics



TL/F/5353-18

National Semiconductor Corporation

microCMOS

MM54HC4066/MM74HC4066 Quad Analog Switch

General Description

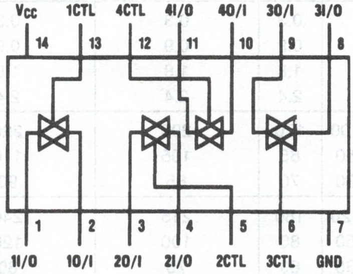
These devices are digitally controlled analog switches utilizing microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the '4066 switches contain linearization circuitry which lowers the "on" resistance and increases switch linearity. The '4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 30 typ. ('4066)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Connection Diagram

Dual-In-Line Package



TL/F/5355–1

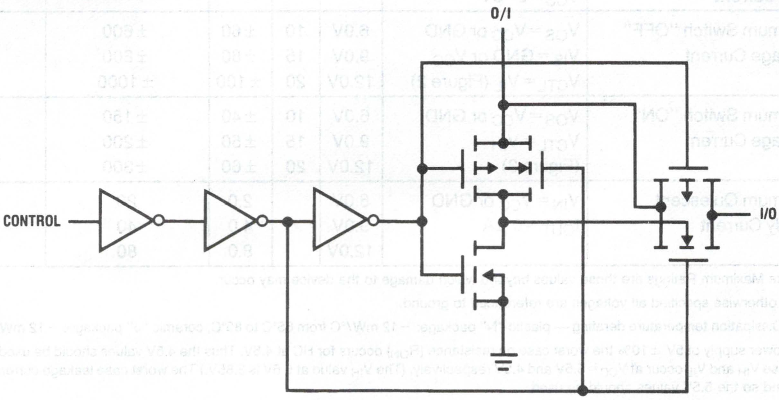
Top View

Order Number MM54HC4066J or MM74HC4066J, N
See NS Package J14A or N14A

Truth Table

Input	Switch
CTL	I/O–O/I
L	"OFF"
H	"ON"

Schematic Diagram



TL/F/5355–2

2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	12	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=9.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	5.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			9.0V		1.8	1.8	1.8	V
			12.0V		2.4	2.4	2.4	V
R_{ON}	Maximum "ON" Resistance (See Note 5)	$V_{CTL}=V_{IH}$, I_S=1.0 mA $V_{IS}=V_{CC}$ to GND (Figure 1)	4.5V	100	170	200	220	Ω
			9.0V	50	85	105	110	Ω
			12.0	30	70	85	90	Ω
		$V_{CTL}=V_{IH}$, I_S=1.0 mA $V_{IS}=V_{CC}$ or GND (Figure 1)	2.0V	120	180	215	240	Ω
			4.5V	50	80	100	120	Ω
			9.0V	35	60	75	80	Ω
			12.0V	20	40	60	70	Ω
R_{ON}	Maximum "ON" Resistance Matching	$V_{CTL}=V_{IH}$ $V_{IS}=V_{CC}$ to GND	4.5V	10	15	20	20	Ω
			9.0V	5	10	15	15	Ω
			12.0V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	$V_{IN}=V_{CC}$ or GND V_{CC}=2–6V			±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	$V_{OS}=V_{CC}$ or GND V_{IS}=GND or V_{CC} $V_{CTL}=V_{IL}$ (Figure 2)	6.0V	10	±60	±600	±600	nA
			9.0V	15	±80	±800	±800	nA
			12.0V	20	±100	±1000	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	$V_{OS}=V_{CC}$ or GND $V_{CTL}=V_{IH}$ (Figure 3)	6.0V	10	±40	±150	±150	nA
			9.0V	15	±50	±200	±200	nA
			12.0V	20	±60	±300	±300	nA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA
			9.0V		4.0	40	80	μA
			12.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistance (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

$V_{CC}=2.0V–6.0V$ $V_{EE}=0V–12V$, $C_L=50$ pF (unless otherwise specified)

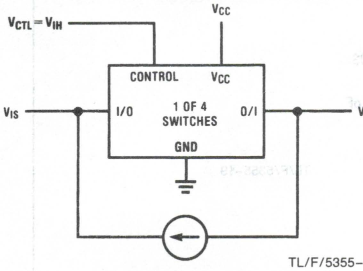
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V	25	50	30	75	ns
			4.5V	5	10	13	15	ns
			9.0V	4	8	10	12	ns
			12.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	$R_L=1$ kΩ	2.0V	30	100	125	150	ns
			4.5V	12	20	25	30	ns
			9.0V	6	12	15	18	ns
			12.0V	5	10	13	15	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	$R_L=1$ kΩ	2.0V	60	168	210	252	ns
			4.5V	25	36	45	54	ns
			9.0V	20	32	40	48	ns
			12.0V	15	30	38	45	
	Minimum Frequency Response (Figure 7) $20\log(V_O/V_I)=-3$ dB	$R_L=600Ω$ $V_{IS}=2$ V_{PP} at $(V_{CC}/2)$ (Notes 6 & 7)	4.5V	40				MHz
			9.0V	100				MHz
	Crosstalk Between any Two Switches (Figure 8)	$R_L=600Ω$, F = 1 MHz (Notes 7 & 8)	4.5V	−52				dB
			9.0V	−50				dB
	Peak Control to Switch Feedthrough Noise (Figure 9)	$R_L=600Ω$, F = 1 MHz $C_L=50$ pF	4.5V	100				mV
			9.0V	250				mV
	Switch OFF Signal Feedthrough Isolation (Figure 10)	$R_L=600Ω$, F = 1 MHz $V_{(CT)}$ V_{IL} (Notes 7 & 8)	4.5V	−42				dB
			9.0V	−44				dB
THD	Total Harmonic Distortion (Figure 11)	$R_L=10$ kΩ, $C_L=50$ pF, F = 1 kHz $V_{IS}=4$ V_{PP}	4.5V	.013				%
		$V_{IS}=8$ V_{PP}	9.0V	.008				%
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			20				pF
C_{IN}	Maximum Feedthrough Capacitance	$V_{CTL}=GND$		0.5				pF
C_{PD}	Power Dissipation Capacitance			15				pF

Note 6: Adjust 0 dBm for F = 1 kHz (Null R_L/R_{ON} Attenuation).

Note 7: V_{IS} is centered at $V_{CC}/2$.

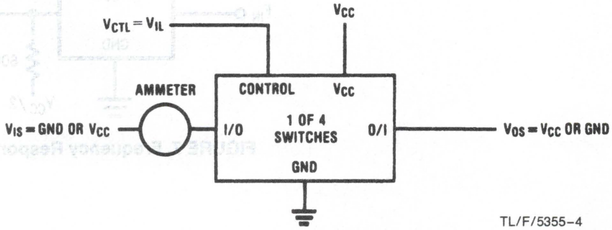
Note 8: Adjust input for 0 dBm.

AC Test Circuits and Switching Time Waveforms



TL/F/5355-3

FIGURE 1. "ON" Resistance



TL/F/5355-4

FIGURE 2. "OFF" Channel Leakage Current

AC Test Circuits and Switching Time Waveforms (Continued)

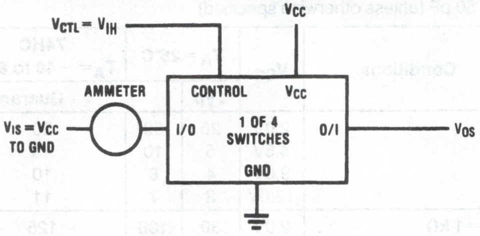

$V_{CTL} = V_{IH}$
V_{CC}
AMMETER
CONTROL
V_{CC}
$V_{IS} = V_{CC}$ TO GND
I/O
1 OF 4 SWITCHES
O/I
V_{OS}
GND
TL/F/5355-5

FIGURE 3. "ON" Channel Leakage Current

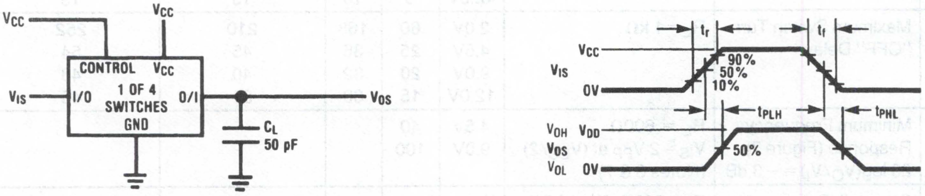

$V_{CTL} = V_{CC}$
V_{CC}
CONTROL
V_{CC}
V_{IS}
I/O
1 OF 4 SWITCHES
O/I
GND
V_{OS}
C_L 50 pF
t_r
t_f
V_{CC}
V_{IS}
0V
90%
50%
10%
t_{PLH}
t_{PHL}
V_{OH} V_{DD}
V_{OS}
V_{OL} 0V
50%
TL/F/5355-6

FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

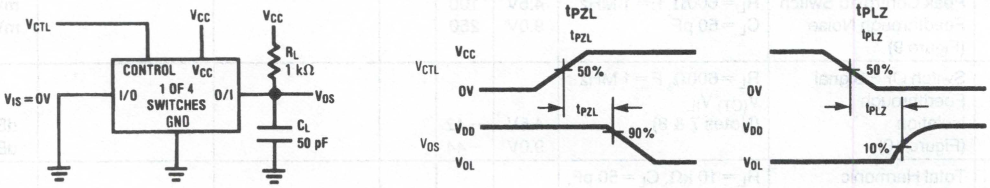

V_{CTL}
V_{CC}
V_{CC}
R_L 1 kΩ
CONTROL
V_{CC}
$V_{IS} = 0V$
I/O
1 OF 4 SWITCHES
O/I
GND
V_{OS}
C_L 50 pF
t_{PZL}
t_{PZL}
V_{CC}
V_{CTL}
0V
50%
t_{PZL}
V_{DD}
V_{OS}
90%
V_{OL}
t_{PLZ}
t_{PLZ}
50%
0V
t_{PLZ}
V_{DD}
10%
V_{OL}
TL/F/5355-7

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

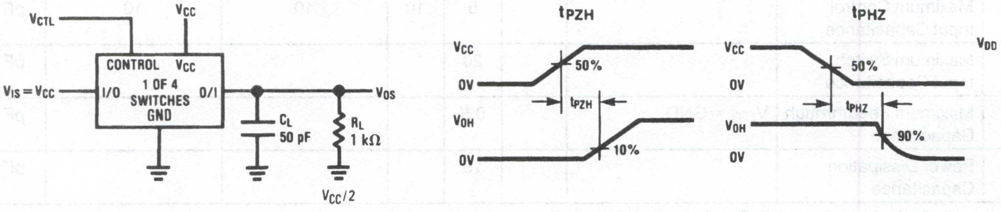

V_{CTL}
V_{CC}
CONTROL
V_{CC}
$V_{IS} = V_{CC}$
I/O
1 OF 4 SWITCHES
O/I
GND
V_{OS}
C_L 50 pF
R_L 1 kΩ
$V_{CC}/2$
t_{PZH}
V_{CC}
50%
0V
t_{PZH}
V_{OH}
10%
0V
t_{PHZ}
V_{CC}
V_{DD}
50%
0V
t_{PHZ}
V_{OH}
90%
0V
TL/F/5355-8

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

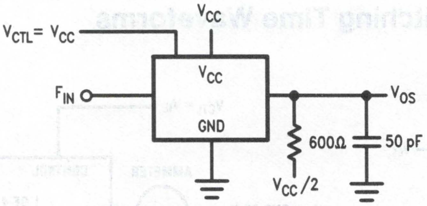
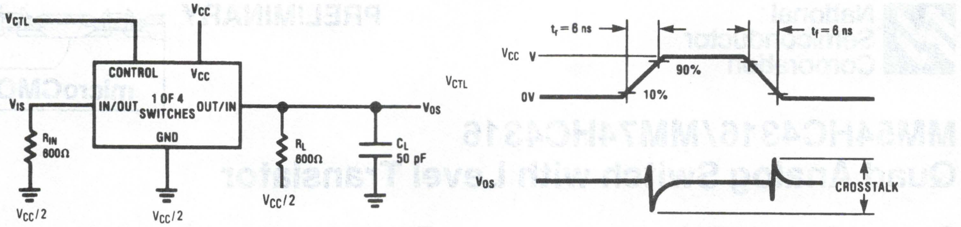
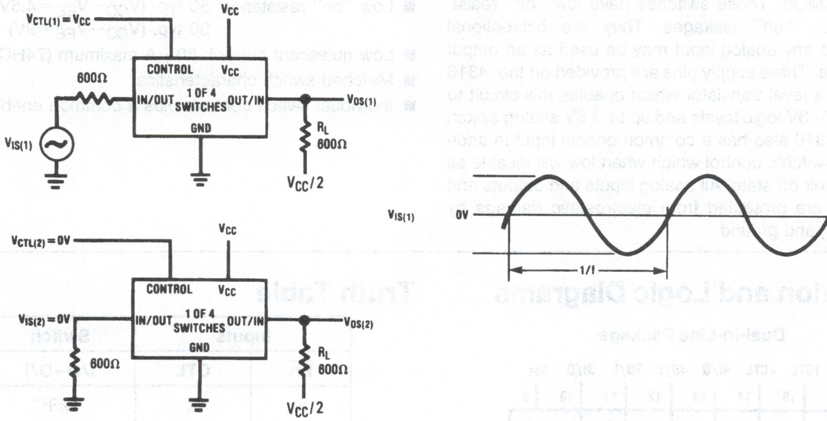

$V_{CTL} = V_{CC}$
V_{CC}
V_{CC}
F_{IN}
GND
V_{OS}
600Ω
50 pF
$V_{CC}/2$
TL/F/5355-19

FIGURE 7. Frequency Response


VCTL
VCC
CONTROL
VCC
VIS
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS
RIN 600Ω
GND
RL 600Ω
CL 50 pF
VCC/2
VCC/2
VCC/2
tr = 6 ns
tf = 6 ns
VCC
90%
VCTL
0V
10%
VOS
CROSSTALK

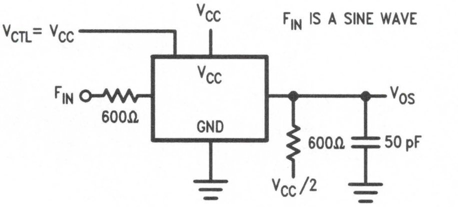
TL/F/5355-9

FIGURE 8. Crosstalk: Control Input to Signal Output


VCTL(1) = VCC
VCC
CONTROL
VCC
600Ω
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS(1)
GND
RL 600Ω
VIS(1)
VCC/2
VIS(1)
0V
1/f
VCTL(2) = 0V
VCC
CONTROL
VCC
VIS(2) = 0V
IN/OUT
1 OF 4 SWITCHES
OUT/IN
VOS(2)
GND
600Ω
RL 600Ω
VCC/2

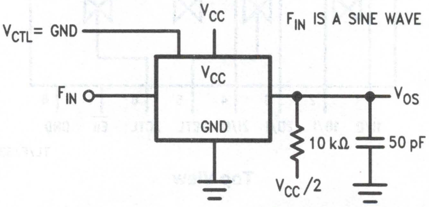
TL/F/5355-10

FIGURE 9. Crosstalk Between Any Two Switches


VCTL = VCC
VCC
FIN IS A SINE WAVE
VCC
FIN
600Ω
GND
VOS
600Ω
50 pF
VCC/2

TL/F/5355-20

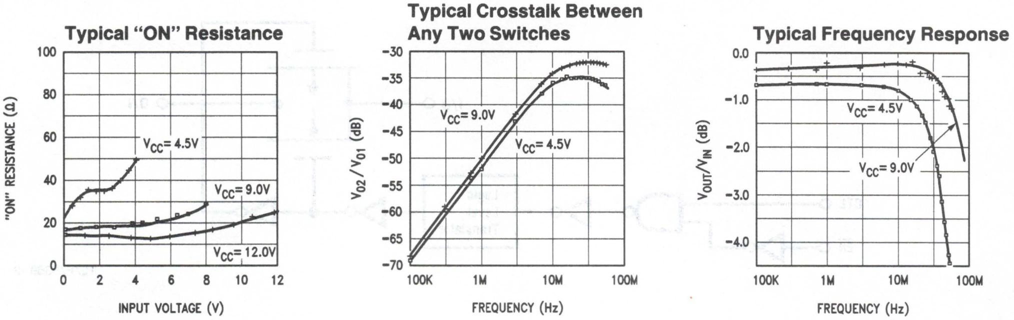
FIGURE 10. Switch OFF Signal Feedthrough Isolation


VCTL = GND
VCC
FIN IS A SINE WAVE
VCC
FIN
GND
VOS
10 kΩ
50 pF
VCC/2

TL/F/5355-21

FIGURE 11. Sinewave Distortion

Typical Performance Characteristics


Typical "ON" Resistance

Typical Crosstalk Between Any Two Switches

Typical Frequency Response

TL/F/5355-18

MM54HC4316/MM74HC4316

National Semiconductor Corporation

PRELIMINARY

microCMOS

MM54HC4316/MM74HC4316
Quad Analog Switch with Level Translator

General Description

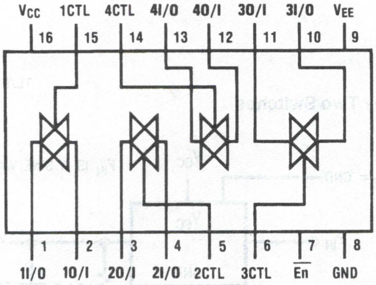
These devices are digitally controlled analog switches implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the '4316 to implement a level translator which enables this circuit to operate with 0–6V logic levels and up to ±6V analog switch levels. The '4316 also has a common enable input in addition to each switch's control which when low will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 20 ns
- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls plus a common enable

Connection and Logic Diagrams

Dual-In-Line Package



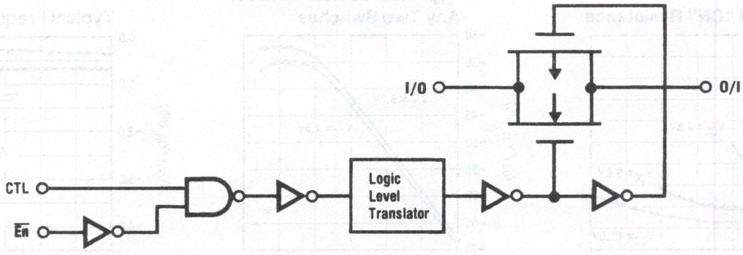
TL/F/5369–1

Top View

Order Number MM54HC4316J or MM74HC4316J,N
See NS Package J16A or N16E

Truth Table

Inputs		Switch
$\overline{En}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"



TL/F/5369–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
Supply Voltage (V_{EE})		0	−6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns
	V_{CC}=12.0V		250	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage			2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
R_{ON}	Minimum "ON" Resistance (See Note 5)	$V_{CTL}=V_{IH}$, I_S=1.0 mA	GND	4.5V	100	170	200	220	Ω
		$V_{IS}=V_{CC}$ to V_{EE}	−4.5V	4.5V	40	85	105	110	Ω
		(Figure 1)	−6.0V	6.0V	30	70	85	90	Ω
			GND	2.0V	100	180	215	240	Ω
		$V_{CTL}=V_{IH}$, I_S=1.0 mA	GND	4.5V	40	80	100	120	Ω
		$V_{IS}=V_{CC}$ or V_{EE}	−4.5V	4.5V	50	60	75	80	Ω
		(Figure 1)	−6.0V	6.0V	20	40	60	70	Ω
R_{ON}	Maximum "ON" Resistance Matching	$V_{CTL}=V_{IH}$	GND	4.5V	10	15	20	20	Ω
		$V_{IS}=V_{CC}$ to GND	−4.5V	4.5V	5	10	15	15	Ω
			−6.0V	6.0V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	$V_{IN}=V_{CC}$ or GND	GND	6.0V		±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	$V_{OS}=V_{CC}$ or GND V_{IS}=GND or V_{CC} $V_{CTL}=V_{IL}$ (Fig 2)	GND	6.0V		±60	±600	±600	nA
			−6.0V	6.0V		±100	±1000	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	$V_{OS}=V_{CC}$ or GND $V_{CTL}=V_{IH}$ (Figure 3)	GND	6.0V		±40	±150	±150	nA
			−6.0V	6.0V		±60	±300	±300	nA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND I_{OUT}=0 μA	GND	6.0V		2.0	20	40	μA
			−6.0V	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V, V_{EE} = 0V–6V, C_L = 50 pF (unless otherwise specified)

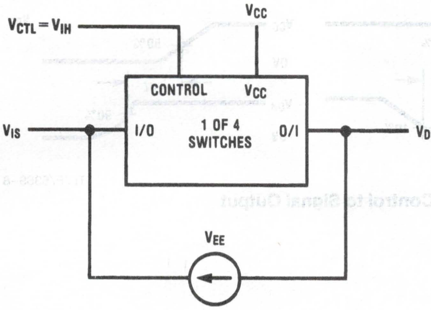
Symbol	Parameter	Conditions	V_{EE}	V_{CC}	$T_A = +25°C$		74HC $T_A = -40°C$ to $+85°C$	54HC $T_A = -55°C$ to $+125°C$	Units
					Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	2.0V	25	50	63	75	ns
			GND	4.5V	5	10	13	15	ns
			−4.5V	4.5V	4	8	12	14	ns
			−6.0V	6.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay (Control)	$R_L = 1\ k\Omega$	GND	2.0V	30	165	206	250	ns
			GND	4.5V	20	35	43	53	ns
			−4.5V	4.5V	15	32	39	48	ns
			−6.0V	6.0V	14	30	37	45	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay (Control)	$R_L = 1\ k\Omega$	GND	2.0V	45	250	312	375	ns
			GND	4.5V	25	50	63	75	ns
			−4.5V	4.5V	20	44	55	66	ns
			−6.0V	6.0V	20	44	55	66	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay (Enable)		GND	2.0V	35	205	256	308	ns
			GND	4.5V	20	41	52	62	ns
			−4.5V	4.5V	19	38	48	57	ns
			−6.0V	6.0V	18	36	45	54	ns
t_{PLZ}, t_{PHZ}	Maximum Switch Turn "OFF" Delay (Enable)		GND	2.0V	58	265	330	400	ns
			GND	4.5V	28	53	67	79	ns
			−4.5V	4.5V	23	47	59	70	ns
			−6.0V	6.0V	21	47	59	70	ns
	Minimum Frequency Response (*Figure 7*) 20 log (V_{OS}/V_{IS}) = −3 dB	$R_L = 600\Omega$, $V_{IS} = 2V_{PP}$ at (V_{CC}–V_{EE}/2) (Notes 6, 7)	0V	4.5	40				MHz
			−4.5V	4.5V	100				MHz
	Control to Switch Feedthrough Noise (*Figure 8*)	$R_L = 600\Omega$, F = 1 MHz C_L = 50 pF (Notes 7, 8)	0V	4.5V	100				mV
			−4.5V	4.5V	250				mV
	Crosstalk Between any Two Switches (*Figure 9*)	$R_L = 600\Omega$, F = 1 MHz	0V	4.5V	−52				dB
			−4.5V	4.5V	−50				dB
	Switch OFF Signal Feedthrough Isolation (*Figure 10*)	$R_L = 600\Omega$, F = 1 MHz $V_{CTL} = V_{IL}$, (Notes 7, 8)	0V	4.5V	−42				dB
			−4.5V	4.5V	−44				dB
THD	Sinewave Harmonic Distortion (Figure 11)	$R_L = 10\ K\Omega$, C_L = 50 pF, F = 1 KHz $V_{IS} = 4V_{PP}$	0V	4.5V	0.013				%
		$V_{IS} = 8V_{PP}$	−4.5V	4.5V	0.008				%
C_{IN}	Maximum Control Input Capacitance				5				pF
C_{IN}	Maximum Switch Input Capacitance				35				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND			0.5				pF
C_{PD}	Power Dissipation Capacitance				15				pF

Note 6: Adjust 0 dBm for F = 1 KHz (Null R_L/Ron Attenuation).

Note 7: V_{IS} is centered at V_{CC}–V_{EE}/2.

Note 8: Adjust for 0 dBm.

AC Test Circuits and Switching Time Waveforms


$V_{CTL} = V_{IH}$
V_{CC}
CONTROL
V_{CC}
V_{IS}
I/O
1 OF 4
SWITCHES
O/I
V_{OS}
V_{EE}

TL/F/5369-3

FIGURE 1. "ON" Resistance

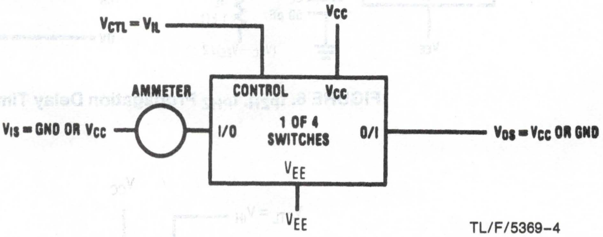

$V_{CTL} = V_{IL}$
V_{CC}
AMMETER
CONTROL
V_{CC}
V_{IS} = GND OR V_{CC}
I/O
1 OF 4
SWITCHES
O/I
V_{OS} = V_{CC} OR GND
V_{EE}
V_{EE}

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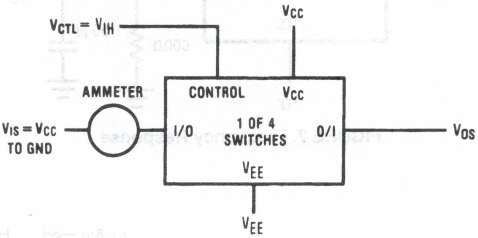
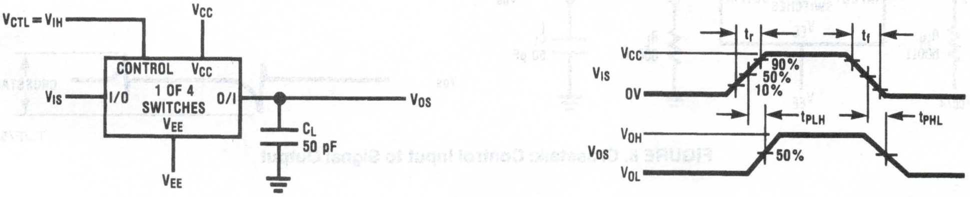
FIGURE 2. "OFF" Channel Leakage Current


$V_{CTL} = V_{IH}$
V_{CC}
AMMETER
CONTROL
V_{CC}
$V_{IS} = V_{CC}$
TO GND
I/O
1 OF 4
SWITCHES
O/I
V_{OS}
V_{EE}
V_{EE}

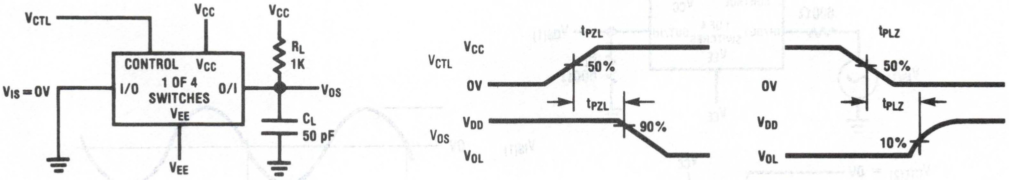
TL/F/5369-5

FIGURE 3. "ON" Channel Leakage Current


$V_{CTL} = V_{IH}$
V_{CC}
CONTROL
V_{CC}
V_{IS}
I/O
1 OF 4
SWITCHES
O/I
V_{EE}
V_{OS}
C_L
50 pF
V_{EE}
t_r
t_f
V_{CC}
V_{IS}
0V
90%
50%
10%
t_{PLH}
t_{PHL}
V_{OH}
V_{OS}
V_{OL}
50%

TL/F/5369-6

FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output


V_{CTL}
V_{CC}
V_{CC}
R_L
1K
CONTROL
V_{CC}
$V_{IS} = 0V$
I/O
1 OF 4
SWITCHES
V_{EE}
O/I
V_{OS}
C_L
50 pF
V_{EE}
t_{PZL}
V_{CC}
V_{CTL}
50%
0V
t_{PZL}
V_{DD}
90%
V_{OS}
V_{OL}
t_{PLZ}
50%
0V
t_{PLZ}
V_{DD}
10%
V_{OL}

TL/F/5369-7

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

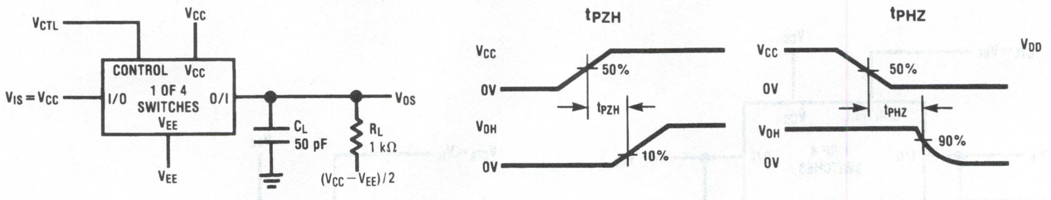

V_{CTL}
V_{CC}
CONTROL
V_{CC}
$V_{IS} = V_{CC}$
I/O
1 OF 4
SWITCHES
O/I
V_{EE}
V_{EE}
C_L
50 pF
R_L
1 kΩ
$(V_{CC} - V_{EE})/2$
V_{OS}
t_{PZH}
V_{CC}
0V
50%
t_{PZH}
V_{OH}
0V
10%
t_{PHZ}
V_{CC}
0V
50%
t_{PHZ}
V_{DD}
V_{OH}
0V
90%

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FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

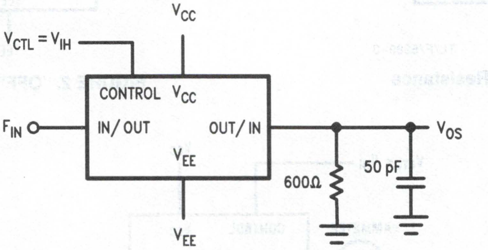
V_{CC}
$V_{CTL} = V_{IH}$
CONTROL
V_{CC}
F_{IN}
IN/OUT
OUT/IN
V_{EE}
V_{EE}
600Ω
50 pF
V_{OS}

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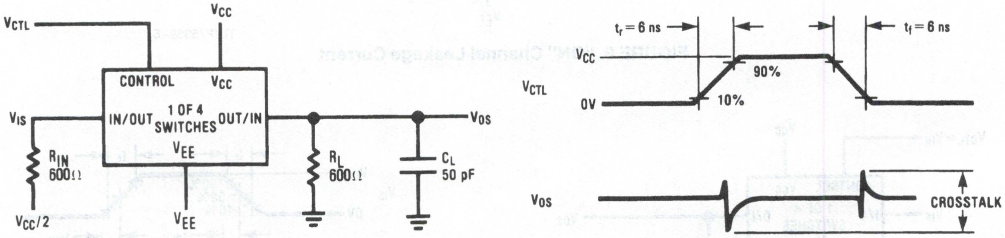
FIGURE 7. Frequency Response


V_{CTL}
V_{CC}
CONTROL
V_{CC}
V_{IS}
IN/OUT
1 OF 4
SWITCHES
OUT/IN
V_{EE}
R_{IN}
600Ω
$V_{CC}/2$
V_{EE}
R_L
600Ω
C_L
50 pF
V_{OS}
$t_r = 6$ ns
$t_f = 6$ ns
V_{CC}
V_{CTL}
0V
90%
10%
V_{OS}
CROSSTALK

TL/F/5369-9

FIGURE 8. Crosstalk: Control Input to Signal Output

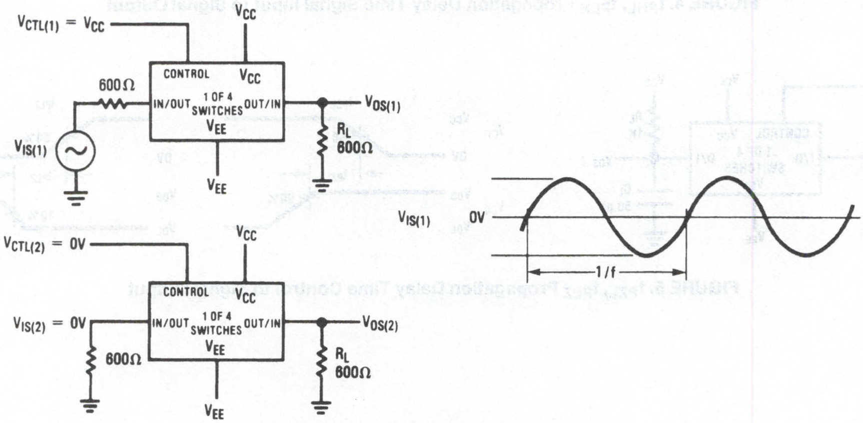

$V_{CTL(1)} = V_{CC}$
V_{CC}
CONTROL
V_{CC}
600Ω
IN/OUT
1 OF 4
SWITCHES
OUT/IN
V_{EE}
$V_{IS(1)}$
V_{EE}
$V_{OS(1)}$
R_L
600Ω
$V_{IS(1)}$
0V
1/f
$V_{CTL(2)} = 0V$
V_{CC}
CONTROL
V_{CC}
$V_{IS(2)} = 0V$
IN/OUT
1 OF 4
SWITCHES
OUT/IN
V_{EE}
600Ω
V_{EE}
$V_{OS(2)}$
R_L
600Ω

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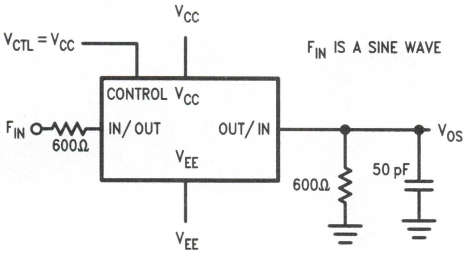
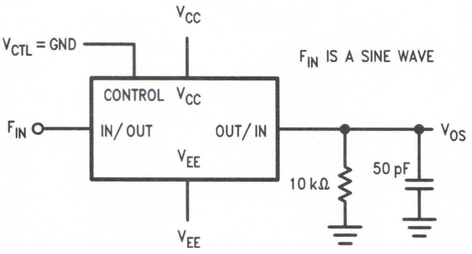
FIGURE 9: Crosstalk Between Any Two Switches

AC Test Circuits and Switching Time Waveforms (Continued)


V_CC
V_CTL = V_CC
F_IN IS A SINE WAVE
CONTROL V_CC
F_IN
600Ω
IN/OUT
OUT/IN
V_OS
V_EE
600Ω
50 pF
V_EE

TL/F/5369-19

FIGURE 10. Switch OFF Signal Feedthrough Isolation

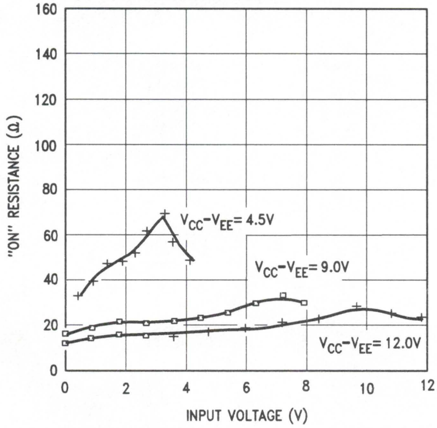

V_CC
V_CTL = GND
F_IN IS A SINE WAVE
CONTROL V_CC
F_IN
IN/OUT
OUT/IN
V_OS
V_EE
10 kΩ
50 pF
V_EE

TL/F/5369-20

FIGURE 11. Sinewave Distortion

Typical Performance Characteristics

Typical "ON" Resistance



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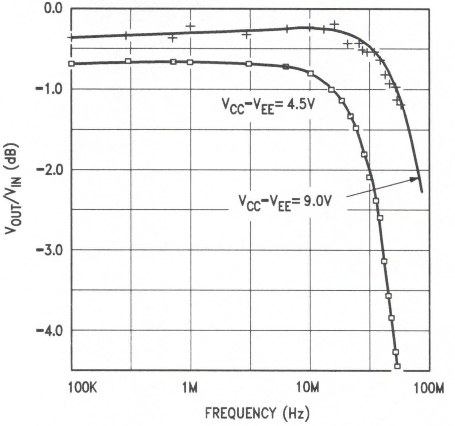
Typical Crosstalk Between Any Two Switches



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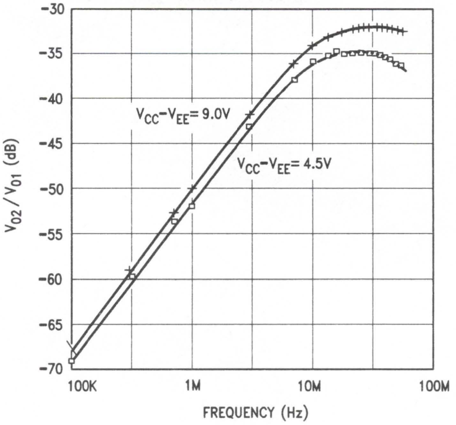
Typical Frequency Response



TL/F/5369-23

Section 3

Analog-to-Digital Converters

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***Devices Not Covered In Last Publication**

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Definition Of Terms
A/D Converters

Conversion Time: The time required for a complete measurement by an analog-to-digital converter.

DC Common-Mode Error: This specification applies to ADCs with differential inputs. It is the change in the output code that occurs when the analog voltages on the two inputs are changed by an equal amount. It is expressed in LSBs.

Differential Nonlinearity: Ideally, any two adjacent digital codes correspond to measured analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. For example, a DAC with a 1.5 LSB output change for a 1 LSB digital code change exhibits ½ LSB differential non-linearity. Differential non-linearity may be expressed in fractional bits or as a percentage of full scale. A differential non-linearity greater than 1 LSB will lead to a non-monotonic transfer function in a DAC and missing codes in an ADC.

Gain Error (Full Scale Error): For an ADC, the difference (usually expressed in LSBs) between the input voltage that should ideally produce a full scale output code and the actual input voltage that produces that code. For DACs, it is the difference between the output voltage (or current) with full scale input code and the ideal voltage (or current) that should exist with a full scale input code.

Gain Temperature Coefficient (Full Scale Temperature Coefficient): Change in gain error divided by change in temperature. Usually expressed in parts per million per degree Celsius (ppm/°C).

Integral Nonlinearity (Linearity Error): Worst case deviation from the line between the endpoints (zero and full scale). Can be expressed as a percentage of full scale or in fractions of an LSB.

LSB (Least-Significant Bit): In a binary coded system this is the bit that carries the smallest value or weight. Its value is the full scale voltage (or current) divided by 2^n, where n is the resolution of the converter.

Missing Codes: When an incremental increase or decrease in input voltage causes the converter to increment or decrement its numeric output by more than one LSB the converter is said to exhibit "missing codes". If there are missing codes, there is a numeric value on the output on the converter which cannot be reached by any input voltage value.

Monotonicity: A monotonic function has a slope whose sign does not change. A monotonic DAC has an output that changes in the same direction (or remains constant) for each increase in the input code. The converse is true for decreasing codes.

MSB (Most Significant Bit): In a binary coded system this is the bit that has the largest value or weight. Its value is one half of full scale.

Multiplying DAC: In a sense, every DAC is a multiplying DAC since the output voltage (or current) is equal to the reference voltage times a constant determined by the digital input code divided by 2^n (n is the number of bits of resolution). In a two quadrant multiplying DAC the reference voltage or the digital input code can change the output voltage polarity. If both the reference voltage and the digital code change the output voltage polarity four quadrant multiplication exists.

Offset Error (Zero Error): In a DAC, this is the output voltage that exists when the input digital code is set to give an ideal output of zero volts. In the case of an ADC, this is the difference between the ideal input voltage (½ LSB) and the actual input voltage that is needed to make the transition from zero to 1 LSB. All the digital codes in the transfer curve are offset by the same value. Many converters allow nulling of offset with an external potentiometer. Offset error is usually expressed in LSBs.

Power Supply Rejection (Power Supply Sensitivity): The sensitivity of a converter to changes in the dc power supply voltages.

Quantizing Error: The error inherent in all A/D conversions. Since even an "ideal" converter has finite resolution, any analog voltage that falls between two adjacent output codes will result in an output code that is inaccurate by up to ½ LSB.

Ratiometric Operation: Many A/D applications require a stable and accurate reference voltage against which the input voltage is compared. This approach results in an **absolute conversion**. Some applications, however, use transducers or other signal sources whose output voltages are proportional to some external reference. In these **ratiometric** applications, the reference for the signal source should be connected to the reference input of the converter. Thus, any variations in the source reference voltage will also change the converter reference voltage and produce an accurate conversion.

Resolution: The smallest analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in bits, where the number of analog levels is equal to 2^n. As an example, a 12-bit converter divides the analog signal into $2^{12} = 4096$ discrete voltage (or current) levels.

Settling Time: The time from a change in input code until a DAC's output signal remains within ±½ LSB (or some other specified tolerance) of the final value.

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A/D Converter Selection Guide

Part No.	Resolution (Bits)	Absolute Accuracy (Max)	Conversion Time	Input Voltage Range	Output Logic Levels	Supplies (V)	Temperature Range*			Package	Comments
							M	I	C		
A/D CONVERTER											
ADC0800	8	±2 LSB	50 µs	±5V	TTL, TRI-STATE	+5, −12	•		•	18-Pin DIP	
ADC0801	8	±¼ LSB	110 µs	5V	TTL, TRI-STATE	+5	•	•		20-Pin DIP	Differential Input
ADC0802	8	±½ LSB	110 µs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin SO 20-Pin PCC	Differential Input
ADC0803	8	±½ LSB	110 µs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin SO 20-Pin PCC	Differential Input
ADC0804	8	±1 LSB	110 µs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP 20-Pin SO 20-Pin PCC	Differential Input
ADC0805	8	±1 LSB	110 µs	5V	TTL, TRI-STATE	+5		•		20-Pin DIP	Ratiometric Operation
ADC0808	8	±½ LSB	100 µs	5V	TTL, TRI-STATE	+5	•	•		28-Pin DIP 28-Pin PCC	8-Channel MUX
ADC0809	8	±1 LSB	100 µs	5V	TTL, TRI-STATE	+5		•		28-Pin DIP 28-Pin PCC	8-Channel MUX
ADC0811B	8	±½ LSB	32 µs	5V	TTL	+5		•	•	20-Pin DIP 20-Pin PCC	11-Channel Serial I/O
ADC0811C	8	±1 LSB	32 µs	5V	TTL	+5		•	•	20-Pin DIP 20-Pin PCC	11-Channel Serial I/O
ADC0816	8	±½ LSB	100 µs	5V	TTL, TRI-STATE	+5	•	•		40-Pin DIP	16-Channel MUX
ADC0817	8	±1 LSB	100 µs	5V	TTL, TRI-STATE	+5		•		40-Pin DIP	16-Channel MUX
ADC0819B	8	±½ LSB	16 µs	5V	TTL	+5		•	•	28-Pin DIP 28-Pin PCC	19-Channel Serial I/O
ADC0819C	8	±1 LSB	16 µs	5V	TTL	+5		•	•	28-Pin DIP 28-Pin PCC	19-Channel Serial I/O
ADC0820B	8	±½ LSB	1.2 µs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin SO 20-Pin PCC	Built-In Track and Hold Function
ADC0820C	8	±1 LSB	1.2 µs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin SO 20-Pin PCC	Built-In Track and Hold Function

A/D Converter Selection Guide (Continued)

Part No.	Resolution (Bits)	Absolute Accuracy (Max)	Conversion Time	Input Voltage Range	Output Logic Levels	Supplies (V)	Temperature Range*			Package	Comments
							M	I	C		
A/D CONVERTER (Continued)											
ADC0829B	8	±½ LSB	100 µs	5V	TTL, TRI-STATE	+5		•		28-Pin DIP	Additional Digital Input Capability
ADC0829C	8	±1 LSB	100 µs	5V	TTL, TRI-STATE	+5		•		28-Pin DIP	Additional Digital Input Capability
ADC0831B	8	±½ LSB	32 µs	5V	TTL	+5		•	•	8-Pin DIP	Serial I/O
ADC0831C	8	±1 LSB	32 µs	5V	TTL	+5		•	•	8-Pin DIP	Serial I/O
ADC0832B	8	±½ LSB	32 µs	5V	TTL	+5		•	•	8-Pin DIP	2-Channel Serial I/O
ADC0832C	8	±1 LSB	32 µs	5V	TTL	+5		•	•	8-Pin DIP	2-Channel Serial I/O
ADC0833B	8	±½ LSB	32 µs	5V	TTL	+5		•	•	14-Pin DIP	4-Channel Serial I/O
ADC0833C	8	±1 LSB	32 µs	5V	TTL	+5		•	•	14-Pin DIP	4-Channel Serial I/O
ADC0834B	8	±½ LSB	32 µs	5V	TTL	+5		•	•	14-Pin DIP	4-Channel Serial I/O
ADC0834C	8	±1 LSB	32 µs	5V	TTL	+5		•	•	14-Pin DIP	4-Channel Serial I/O
ADC0838B	8	±½ LSB	32 µs	5V	TTL	+5		•	•	20-Pin DIP 20-Pin PCC	8-Channel Serial I/O
ADC0838C	8	±1 LSB	32 µs	5V	TTL	+5		•	•	20-Pin DIP 20-Pin PCC	8-Channel Serial I/O
ADC0841B	8	±½ LSB	40 µs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP 20-Pin PCC	Differential Input, Internal Clock
ADC0841C	8	±1 LSB	40 µs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP 20-Pin PCC	Differential Input, Internal Clock
ADC0844B	8	±½ LSB	40 µs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	4-Channel MUX, Internal Clock
ADC0844C	8	±1 LSB	40 µs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	4-Channel MUX, Internal Clock
ADC0848B	8	±½ LSB	40 µs	5V	TTL, TRI-STATE	+5		•	•	28-Pin DIP 28-Pin PCC	8-Channel MUX, Internal Clock
ADC0848C	8	±1 LSB	40 µs	5V	TTL, TRI-STATE	+5		•	•	28-Pin DIP 28-Pin PCC	8-Channel MUX, Internal Clock
ADC1001C	10	±1 LSB	200 µs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	8-Bit Bus Compatible, Differential Input
ADC1005B	10	±½ LSB	50 µs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin PCC	8-Bit Bus Compatible, Differential Input

A/D Converter Selection Guide (Continued)

Part No.	Resolution (Bits)	Absolute Accuracy (Max)	Conversion Time	Input Voltage Range	Output Logic Levels	Supplies (V)	Temperature Range* M	Temperature Range* I	Temperature Range* C	Package	Comments
A/D CONVERTER (Continued)											
ADC1005C	10	±1 LSB	50 µs	5V	TTL, TRI-STATE	+5	●	●	●	20-Pin DIP 20-Pin PCC	8-Bit Bus Compatible, Differential Input
ADC1021C	10	±1 LSB	200 µs	5V	TTL, TRI-STATE	+5		●	●	24-Pin DIP	Differential Input
ADC1025B	10	±½ LSB	50 µs	5V	TTL, TRI-STATE	+5	●	●	●	24-Pin DIP 28-Pin PCC	Differential Input
ADC1025C	10	±1 LSB	50 µs	5V	TTL, TRI-STATE	+5	●	●	●	24-Pin DIP 28-Pin PCC	Differential Input
ADC1205B	12+sign	±½ LSB	100 µs	±5V	TTL, TRI-STATE	+5, ±5		●	●	24-Pin DIP	8-Bit Bus Compatible, Differential Input
ADC1205C	12+sign	±1 LSB	100 µs	±5V	TTL, TRI-STATE	+5, ±5		●	●	24-Pin DIP	8-Bit Bus Compatible, Differential Input
ADC1210	12	±¾ LSB	200 µs	10.2V	CMOS	+5 to ±15	●	●		24-Pin DIP	
ADC1211	12	±2 LSB	200 µs	10.2V	CMOS	+5 to ±5	●	●		24-Pin DIP	
ADC1225B	12+sign	±½ LSB	100 µs	±5V	TTL, TRI-STATE	+5, ±5		●	●	28-Pin DIP	Differential Input
ADC1225C	12+sign	±1 LSB	100 µs	±5V	TTL, TRI-STATE	+5, ±5		●	●	28-Pin DIP	Differential Input
ADC3511	3½-Digit	0.05%	200 ms	2V	TTL, TRI-STATE	+5			●	24-Pin DIP	Integrating µP Compatible
ADC3711	3¾-Digit	0.05%	400 ms	2V	TTL, TRI-STATE	+5			●	24-Pin DIP	Integrating µP Compatible
LM131	V-F	0.01%	N/A	V_{CC} − 2V	Open Collector	+5 to +40	●	●	●	8-Pin DIP or TO-99 Can	Voltage-to-Frequency Converter 100 kHz Max
DIGITAL VOLTMETER											
ADD3501	3½-Digit	0.05%	200 ms	2V	7-Segment LED Drive	+5			●	28-Pin DIP	3½-Digit LED DVM
ADD3701	3½-Digit	0.05%	400 ms	2V	7-Segment LED Drive	+5			●	28-Pin DIP	3¾-Digit LED DVM

*Temperature ranges: "M" is −55°C to +125°C ambient; "I" is −40°C to +85°C or −25°C to +85°C; "C" is 0°C to +70°C.

National Semiconductor Corporation

ADC0800 8-Bit A/D Converter

General Description

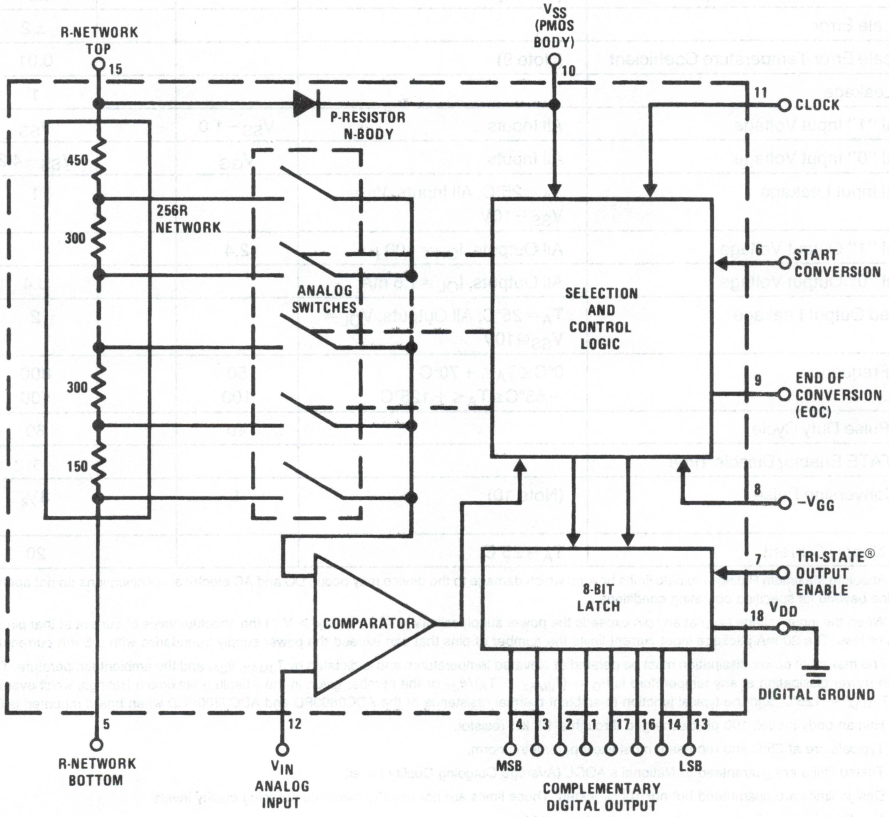
The ADC0800 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE® to permit bussing on common data lines.

The ADC0800PD is specified over −55°C to +125°C and the ADC0800PCD is specified over 0°C to 70°C.

Features

- Low cost
- ±5V, 10V input ranges
- No missing codes
- Ratiometric conversion
- TRI-STATE outputs
- Fast $T_C = 50\ \mu s$
- Contains output latches
- TTL compatible
- Supply voltages 5 V_{DC} and −12 V_{DC}
- Resolution 8 bits
- Linearity ±1 LSB
- Conversion speed 40 clock periods
- Clock range 50 to 800 kHz

Block Diagram



R-NETWORK TOP
15
V_SS (PMOS BODY)
10
P-RESISTOR N-BODY
11
CLOCK
450
256R NETWORK
300
300
150
ANALOG SWITCHES
SELECTION AND CONTROL LOGIC
6
START CONVERSION
9
END OF CONVERSION (EOC)
8
−V_GG
7
TRI-STATE® OUTPUT ENABLE
8-BIT LATCH
18
V_DD
COMPARATOR
DIGITAL GROUND
5
R-NETWORK BOTTOM
12
V_IN ANALOG INPUT
4 3 2 1 17 16 14 13
MSB
LSB
COMPLEMENTARY DIGITAL OUTPUT

TL/H/5670–1

(00000000 = + full-scale)

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	$V_{SS}-22V$
Supply Voltage (V_{GG})	$V_{SS}-22V$
Voltage at Any Input	$V_{SS}+0.3V$ to $V_{SS}-22V$
Input Current at Any Pin (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
Power Dissipation (Note 3)	875 mW
ESD Susceptibility (Note 4)	500V
Storage Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0800PD	$-55°C \le T_A \le +125°C$
ADC0800PCD	$0°C \le T_A \le +70°C$

Electrical Characteristics

These specifications apply for $V_{SS}=5.0\ V_{DC}$, $V_{GG}=-12.0\ V_{DC}$, $V_{DD}=0\ V_{DC}$, a reference voltage of 10.000 V_{DC} across the on-chip R-network ($V_{R\text{-}NETWORK\ TOP}=5.000\ V_{DC}$ and $V_{R\text{-}NETWORK\ BOTTOM}=-5.000\ V_{DC}$), and a clock frequency of 800 kHz. For all tests, a 475Ω resistor is used from pin 5 to $V_{R\text{-}NETWORK\ BOTTOM}=-5\ V_{DC}$. Unless otherwise noted, these specifications apply over an ambient temperature range of −55°C to +125°C for the ADC0800PD and 0°C to +70°C for the ADC0800PCD.

Parameter	Conditions	Min	Typ	Max	Units
Non-Linearity	$T_A=25°C$, (Note 8) Over Temperature, (Note 8)			±1 ±2	LSB LSB
Differential Non-Linearity				±½	LSB
Zero Error				±2	LSB
Zero Error Temperature Coefficient	(Note 9)			0.01	%/°C
Full-Scale Error				±2	LSB
Full-Scale Error Temperature Coefficient	(Note 9)			0.01	%/°C
Input Leakage				1	μA
Logical "1" Input Voltage	All Inputs	$V_{SS}-1.0$		V_{SS}	V
Logical "0" Input Voltage	All Inputs	V_{GG}		$V_{SS}-4.2$	V
Logical Input Leakage	$T_A=25°C$, All Inputs, $V_{IL}=V_{SS}-10V$			1	μA
Logical "1" Output Voltage	All Outputs, $I_{OH}=100\ \mu A$	2.4			V
Logical "0" Output Voltage	All Outputs, $I_{OL}=1.6$ mA			0.4	V
Disabled Output Leakage	$T_A=25°C$, All Outputs, $V_{OL}=V_{SS}$@10V			2	μA
Clock Frequency	$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	50 100		800 500	kHz kHz
Clock Pulse Duty Cycle		40		60	%
TRI-STATE Enable/Disable Time				1	μs
Start Conversion Pulse	(Note 10)	1		3½	Clock Periods
Power Supply Current	$T_A=25°C$			20	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the ADC0800PD and ADC0800PCD when board mounted is 66°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

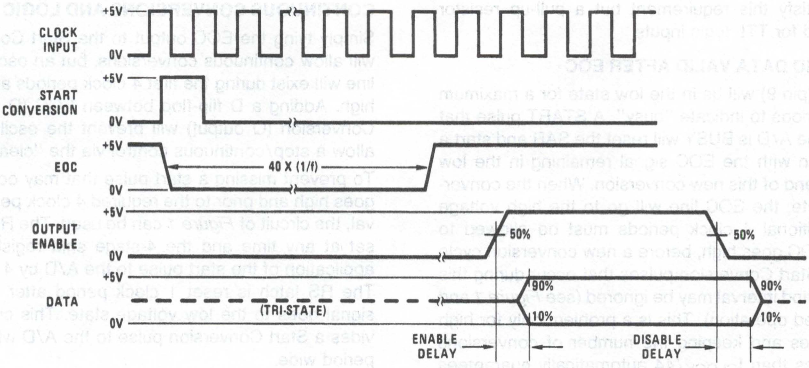
Note 7: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 8: Non-linearity specifications are based on best straight line.

Note 9: Guaranteed by design only.

Note 10: Start conversion pulse duration greater than 3½ clock periods will cause conversion errors.

Timing Diagram



TL/H/5670–2

Data is complementary binary (full scale is all "0's" output).

Application Hints

OPERATION

The ADC0800 contains a network with 256-300Ω resistors in series. Analog switch taps are made at the junction of each resistor and at each end of the network. In operation, a reference (10.00V) is applied across this network of 256 resistors. An analog input (V_{IN}) is first compared to the center point of the ladder via the appropriate switch. If V_{IN} is larger than $V_{REF}/2$, the internal logic changes the switch points and now compares V_{IN} and ¾ V_{REF}. This process, known as successive approximation, continues until the best match of V_{IN} and V_{REF}/N is made. N now defines a specific tap on the resistor network. When the conversion is complete, the logic loads a binary word corresponding to this tap into the output latch and an end of conversion (EOC) logic level appears. The output latches hold this data valid until a new conversion is completed and new data is loaded into the latches. The data transfer occurs in about 200 ns so that valid data is present virtually all the time in the latches. The data outputs are activated when the Output Enable is high, and in TRI-STATE when Output Enable is low. The Enable Delay time is approximately 200 ns. Each conversion requires 40 clock periods. The device may be operated in the free running mode by connecting the Start Conversion line to the End of Conversion line. However, to ensure start-up under all possible conditions, an external Start Conversion pulse is required during power up conditions.

REFERENCE

The reference applied across the 256 resistor network determines the analog input range. $V_{REF} = 10.00V$ with the top of the R-network connected to 5V and the bottom connected to −5V gives a ±5V range. The reference can be level shifted between V_{SS} and V_{GG}. However, the voltage, applied to the top of the R-network (pin 15), must not exceed V_{SS}, to prevent forward biasing the on-chip parasitic silicon diodes that exist between the P-diffused resistors (pin 15) and the N-type body (pin 10, V_{SS}). Use of a standard logic power supply for V_{SS} can cause problems, both due to initial voltage tolerance and changes over temperature. A solution is to power the V_{SS} line (15 mA max drain) from the output of the op amp that is used to bias the top of the R-network (pin 15). The analog input voltage and the voltage that is applied to the bottom of the R-network (pin 5) must be at least 7V above the $-V_{GG}$ supply voltage to ensure adequate voltage drive to the analog switches.

Other reference voltages may be used (such as 10.24V). If a 5V reference is used, the analog range will be 5V and accuracy will be reduced by a factor of 2. Thus, for maximum accuracy, it is desirable to operate with at least a 10V reference. For TTL logic levels, this requires 5V and −5V for the R-network. CMOS can operate at the 10 V_{DC} V_{SS} level and a single 10 V_{DC} reference can be used. All digital voltage levels for both inputs and outputs will be from ground to V_{SS}.

ANALOG INPUT AND SOURCE RESISTANCE CONSIDERATIONS

The lead to the analog input (pin 12) should be kept as short as possible. Both noise and digital clock coupling to this input can cause conversion errors. To minimize any input errors, the following source resistance considerations should be noted:

For $R_S \leq 5k$	No analog input bypass capacitor required, although a 0.1 μF input bypass capacitor will prevent pickup due to unavoidable series lead inductance.
For $5k < R_S \leq 20k$	A 0.1 μF capacitor from the input (pin 12) to ground should be used.
For $R_S > 20k$	Input buffering is necessary.

If the overall converter system requires lowpass filtering of the analog input signal, use a 20 kΩ or less series resistor for a passive RC section or add an op amp RC active lowpass filter (with its inherent low output resistance) to ensure accurate conversions.

CLOCK COUPLING

The clock lead should be kept away from the analog input line to reduce coupling.

LOGIC INPUTS

The logical "1" input voltage swing for the Clock, Start Conversion and Output Enable should be ($V_{SS} - 1.0V$).

Application Hints (Continued)

CMOS will satisfy this requirement but a pull-up resistor should be used for TTL logic inputs.

RE-START AND DATA VALID AFTER EOC

The EOC line (pin 9) will be in the low state for a maximum of 40 clock periods to indicate "busy". A START pulse that occurs while the A/D is BUSY will reset the SAR and start a new conversion with the EOC signal remaining in the low state until the end of this new conversion. When the conversion is complete, the EOC line will go to the high voltage state. An additional 4 clock periods must be allowed to elapse after EOC goes high, before a new conversion cycle is requested. Start Conversion pulses that occur during this last 4 clock period interval may be ignored (see *Figure 1* and *2* for high speed operation). This is a problem only for high conversion rates and keeping the number of conversions per second less than $f_{CLOCK}/44$ automatically guarantees proper operation. For example, for an 800 kHz clock, approximately 18,000 conversions per second are allowed. The transfer of the new digital data to the output is initiated when EOC goes to the high voltage state.

POWER SUPPLIES

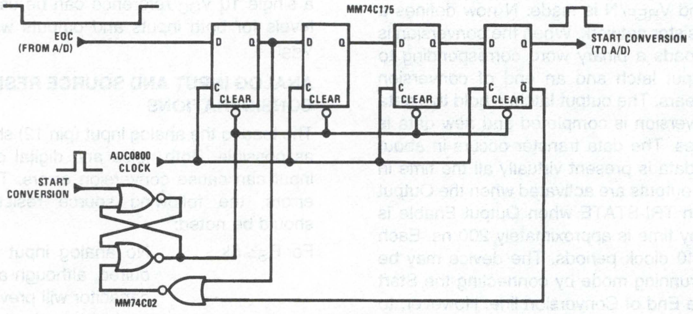
Standard supplies are $V_{SS}=+5V$, $V_{GG}=-12V$ and $V_{DD}=0V$. Device accuracy is dependent on stability of the reference voltage and has slight sensitivity to V_{SS}—V_{GG}. V_{DD} has no effect on accuracy. Noise spikes on the V_{SS} and V_{GG} supplies can cause improper conversion; therefore, filtering each supply with a 4.7 μF tantalum capacitor is recommended.

CONTINUOUS CONVERSIONS AND LOGIC CONTROL

Simply tying the EOC output to the Start Conversion input will allow continuous conversions, but an oscillation on this line will exist during the first 4 clock periods after EOC goes high. Adding a D flip-flop between EOC (D input) to Start Conversion (Q output) will prevent the oscillation and will allow a stop/continuous control via the "clear" input.

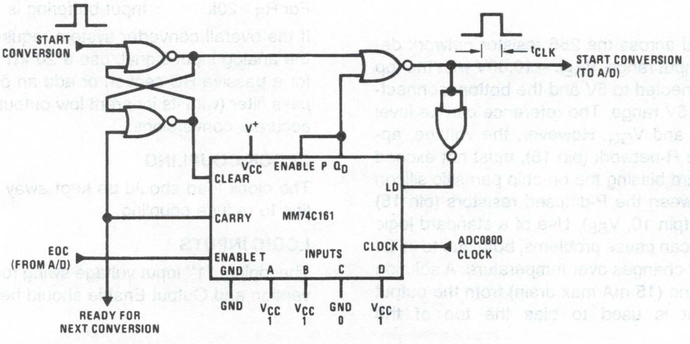
To prevent missing a start pulse that may occur after EOC goes high and prior to the required 4 clock period time interval, the circuit of *Figure 1* can be used. The RS latch can be set at any time and the 4-stage shift register delays the application of the start pulse to the A/D by 4 clock periods. The RS latch is reset 1 clock period after the A/D EOC signal goes to the low voltage state. This circuit also provides a Start Conversion pulse to the A/D which is 1 clock period wide.

A second control logic application circuit is shown in *Figure 2*. This allows an asynchronous start pulse of arbitrary length less than T_C, to continuously convert for a fixed high level and provides a single clock period start pulse to the A/D. The binary counter is loaded with a count of 11 when the start pulse to the A/D appears. Counting is inhibited until the EOC signal from the A/D goes high. A carry pulse is then generated 4 clock periods after EOC goes high and is used to reset the input RS latch. This carry pulse can be used to indicate that the conversion is complete, the data has transferred to the output buffers and the system is ready for a new conversion cycle.



TL/H/5670–3

FIGURE 1. Delaying an Asynchronous Start Pulse



TL/H/5670–10

FIGURE 2. A/D Control Logic

Application Hints (Continued)

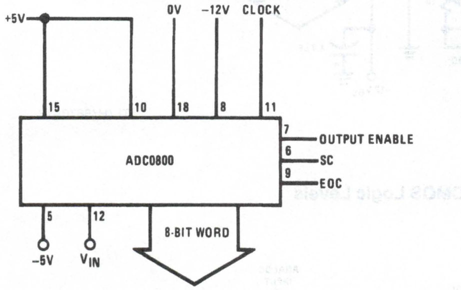
ZERO AND FULL-SCALE ADJUSTMENT

Zero Adjustment: This is the offset voltage required at the bottom of the R-network (pin 5) to make the 11111111 to 11111110 transition when the input voltage is ½ LSB (20 mV for a 10.24V scale). In most cases, this can be accomplished by having a 1 kΩ pot on pin 5. A resistor of 475Ω can be used as a non-adjustable best approximation from pin 5 to ground.

Full-Scale Adjustment: This is the offset voltage required at the top of the R-network (pin 15) to make the 00000001 to 00000000 transition when the input voltage is 1 ½ LSB from full-scale (60 mV less than full-scale for a 10.24V scale). This voltage is guaranteed to be within ±2 LSB for the ADC0800 without adjustment. In most cases, adjustment can be accomplished by having a 1 kΩ pot on pin 15.

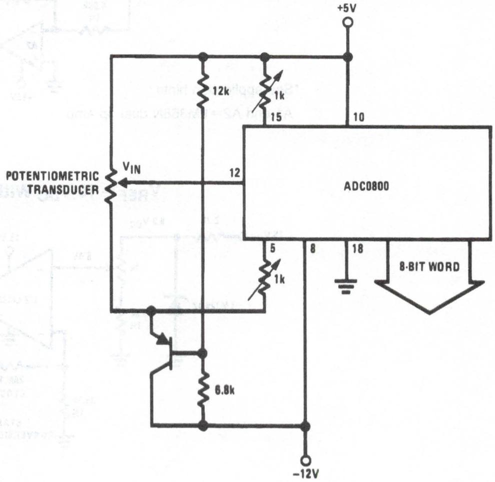
Typical Applications

General Connection


+5V
0V
−12V
CLOCK
15
10
18
8
11
7
OUTPUT ENABLE
6
SC
9
EOC
ADC0800
5
12
8-BIT WORD
−5V
V_{IN}

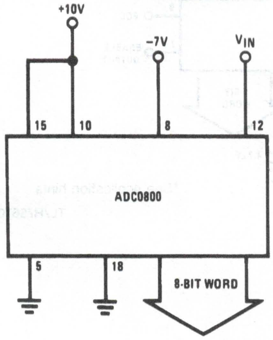
TL/H/5670–11

Ratiometric Input Signal with Tracking Reference


+5V
12k
1k
15
10
POTENTIOMETRIC TRANSDUCER
V_{IN}
12
ADC0800
5
8
18
1k
8-BIT WORD
6.8k
−12V

TL/H/5670–4

Hi-Voltage CMOS Output Levels


+10V
−7V
V_{IN}
15
10
8
12
ADC0800
5
18
8-BIT WORD

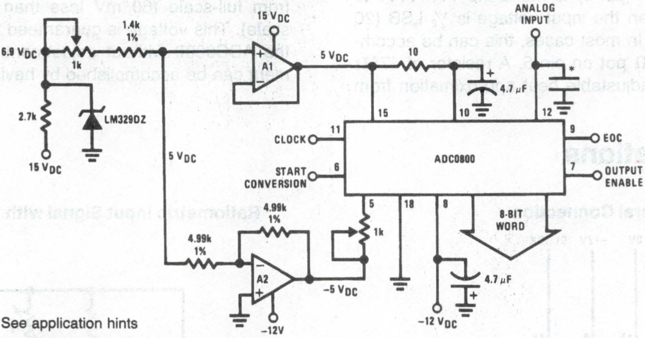
0V to 10V V_{IN} range

0V to 10V output levels

TL/H/5670–12

Typical Applications (Continued)

$V_{REF} = 10\ V_{DC}$ With TTL Logic Levels

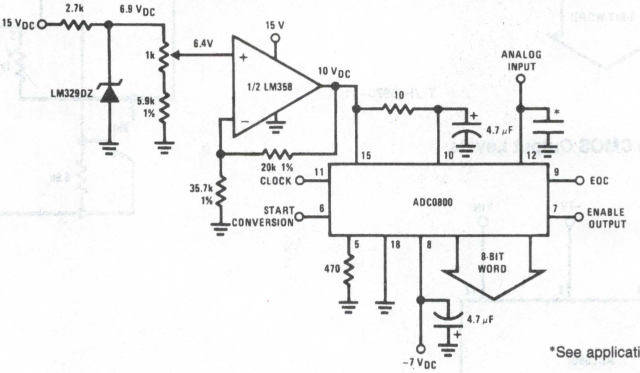

15 VDC
1.4k 1%
6.9 VDC
1k
A1
5 VDC
10
4.7 μF
ANALOG INPUT
*
2.7k
LM329DZ
15 VDC
15
10
12
11
9
CLOCK
EOC
5 VDC
ADC0800
START CONVERSION
6
7
OUTPUT ENABLE
5
18
8
8-BIT WORD
4.99k 1%
4.99k 1%
1k
A2
-5 VDC
4.7 μF
-12V
-12 VDC

*See application hints

A1 and A2 = LM358N dual op amp

TL/H/5670-13

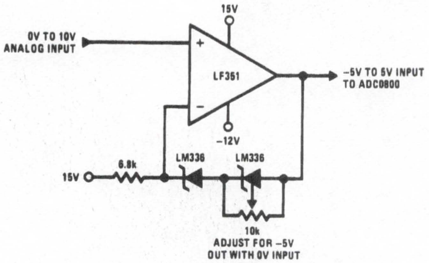
$V_{REF} = 10\ V_{DC}$ With 10V CMOS Logic Levels


15 VDC
2.7k
6.9 VDC
15 V
6.4V
1k
1/2 LM358
10 VDC
ANALOG INPUT
LM329DZ
5.9k 1%
10
4.7 μF
*
20k 1%
15
10
12
CLOCK
11
9
EOC
35.7k 1%
START CONVERSION
6
ADC0800
7
ENABLE OUTPUT
5
18
8
470
8-BIT WORD
4.7 μF
-7 VDC

*See application hints

TL/H/5670-14

Input Level Shifting


15V
0V TO 10V ANALOG INPUT
LF351
-5V TO 5V INPUT TO ADC0800
-12V
6.8k
LM336
LM336
15V
10k
ADJUST FOR -5V OUT WITH 0V INPUT

- Permits TTL compatible outputs with 0V to 10V input range (0V to −10V input range achieved by reversing polarity of zener diodes and returning the 6.8k resistor to V−).

TL/H/5670-5

Typical Applications (Continued)

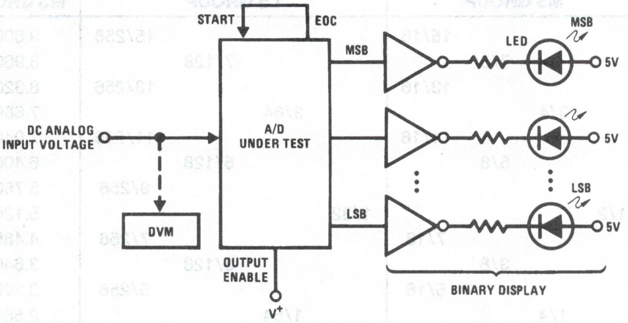
TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 3.* Note that the LED drivers invert the digital output of the A/D converter to provide a binary display. A lab DVM can be used if a precision voltage source is not available. After adjusting the zero and full-scale, any number of points can be checked, as desired.

For ease of testing, a 10.24 V_{DC} reference is recommended for the A/D converter. This provides an LSB of 40 mV (10.240/256). To adjust the zero of the A/D, an analog input voltage of ½ LSB or 20 mV should be applied and the zero adjust potentiometer should be set to provide a flicker on the LSB LED readout with all the other display LEDs OFF.

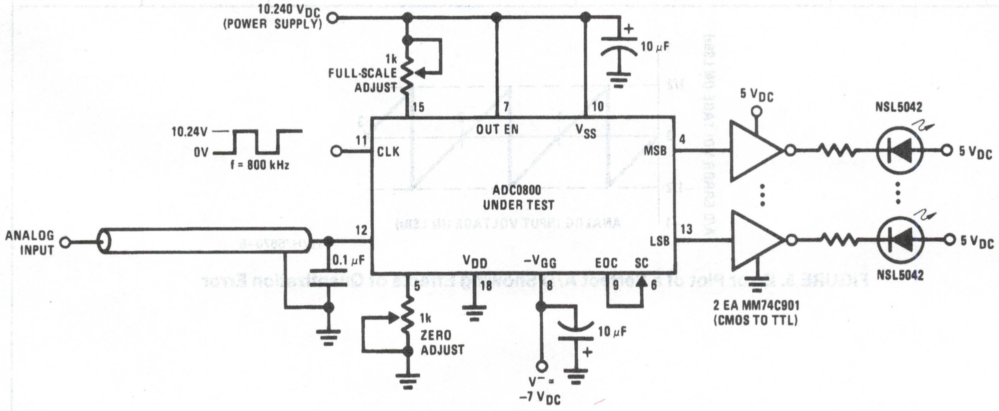
To adjust the full-scale adjust potentiometer, an analog input that is 1½ LSB less than the reference (10.240–0.060 or 10.180 V_{DC}) should be applied to the analog input and the full-scale adjusted for a flicker on the LSB LED, but this time with all the other LEDs ON.

A complete circuit for a simple A/D tester is shown in *Figure 4.* Note that the clock input voltage swing and the digital output voltage swings are from 0V to 10.24V. The MM74C901 provides a voltage translation to 5V operation and also the logic inversion so the readout LEDs are in binary.


START
EOC
MSB
LED
MSB
5V
DC ANALOG INPUT VOLTAGE
A/D UNDER TEST
5V
LSB
LSB
5V
DVM
OUTPUT ENABLE
V+
BINARY DISPLAY

TL/H/5670–15

FIGURE 3. Basic A/D Tester


10.240 VDC (POWER SUPPLY)
1k
FULL-SCALE ADJUST
10 µF
15
7
10
5 VDC
NSL5042
10.24V
0V
f = 800 kHz
11
CLK
OUT EN
VSS
MSB
4
5 VDC
ADC0800 UNDER TEST
ANALOG INPUT
12
0.1 µF
VDD
−VGG
EOC
SC
LSB
13
5 VDC
NSL5042
5
18
8
9
6
1k
ZERO ADJUST
10 µF
V− = −7 VDC
2 EA MM74C901 (CMOS TO TTL)

TL/H/5670–7

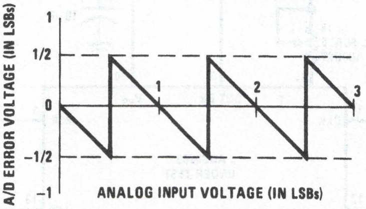
FIGURE 4. Complete Basic Tester Circuit

Typical Applications (Continued)

The digital output LED display can be decoded by dividing the 8 bits into the 4 most significant bits and 4 least significant bits. Table I shows the fractional binary equivalent of these two 8-bit groups. By adding the decoded voltages which are obtained from the column: "Input Voltage Value with a 10.240 V_{REF}" of both the MS and LS groups, the value of the digital display can be determined. For example, for an output LED display of "1011 0110" or "B6" (in hex) the voltage values from the table are 7.04 + 0.24 or 7.280 V_{DC}. These voltage values represent the center values of a perfect A/D converter. The input voltage has to change by ±½ LSB (±20 mV), the "quantization uncertainty" of an A/D, to obtain an output digital code change. The effects of this quantization error have to be accounted for in the interpretation of the test results. A plot of this natural error source is shown in *Figure 5* where, for clarity, both the analog input voltage and the error voltage are normalized to LSBs.

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		INPUT VOLTAGE VALUE WITH 10.24 V_{REF}	
					MS GROUP	LS GROUP	MS GROUP	LS GROUP
F	1	1	1	1	15/16	15/256	9.600	0.600
E	1	1	1	0	7/8	7/128	8.960	0.560
D	1	1	0	1	13/16	13/256	8.320	0.520
C	1	1	0	0	3/4	3/64	7.680	0.480
B	1	0	1	1	11/16	11/256	7.040	0.440
A	1	0	1	0	5/8	5/128	6.400	0.400
9	1	0	0	[illegible]	9/16	9/256	5.760	0.360
8	1	0	0	0	1/2	1/32	5.120	0.320
7	0	1	1	1	7/16	7/256	4.480	0.280
6	0	1	1	0	3/8	3/128	3.840	0.240
5	0	1	0	1	5/16	5/256	3.200	0.200
4	0	1	0	0	1/4	1/64	2.560	0.160
3	0	0	1	1	3/16	3/256	1.920	0.120
2	0	0	1	0	1/8	1/128	1.280	0.080
1	0	0	0	1	1/16	1/256	0.640	0.040
0	0	0	0	0			0	0



TL/H/5670–8

FIGURE 5. Error Plot of a Perfect A/D Showing Effects of Quantization Error

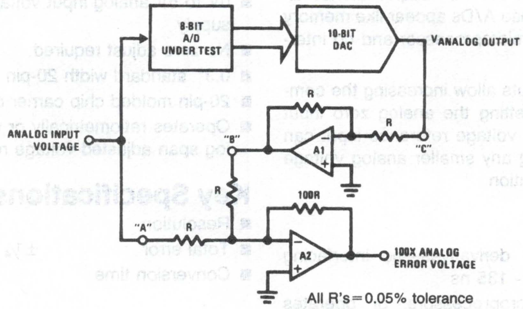
Typical Applications (Continued)

A low speed ramp generator can also be used to sweep the analog input voltage and the LED outputs will provide a binary counting sequence from zero to full-scale.

The techniques described so far are suitable for an engineering evaluation or a quick check on performance. For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in two digital words.

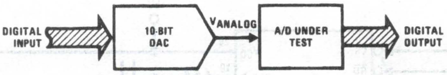
A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 6.* The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A–C".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 7* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.


8-BIT A/D UNDER TEST
10-BIT DAC
V_{ANALOG} OUTPUT
R
R
ANALOG INPUT VOLTAGE
"B"
A1
"C"
R
100R
"A"
R
A2
100X ANALOG ERROR VOLTAGE
All R's = 0.05% tolerance

TL/H/5670–16

FIGURE 6. A/D Tester with Analog Error Output

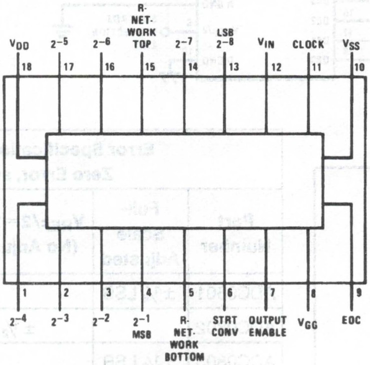

DIGITAL INPUT
10-BIT DAC
V_{ANALOG}
A/D UNDER TEST
DIGITAL OUTPUT

TL/H/5670–17

FIGURE 7. Basic "Digital" A/D Tester

Connection Diagram

Dual-In-Line Package


V_{DD} 18
2^{-5} 17
2^{-6} 16
R-NETWORK TOP 15
2^{-7} 14
LSB 2^{-8} 13
V_{IN} 12
CLOCK 11
V_{SS} 10
1 2^{-4}
2 2^{-3}
3 2^{-2}
4 2^{-1} MSB
5 R-NETWORK BOTTOM
6 STRT CONV
7 OUTPUT ENABLE
8 V_{GG}
9 EOC

TL/H/5670–9

Top View

Order Number ADC0800PD or ADC0800PCD
See NS Package Number D18A

National Semiconductor Corporation

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

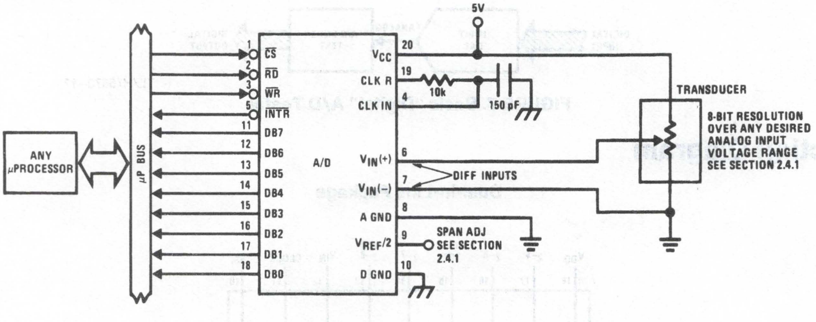
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3″ standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

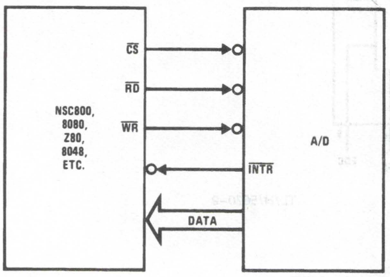
■ Resolution	8 bits
■ Total error	±1/4 LSB, ±1/2 LSB and ±1 LSB
■ Conversion time	100 μs

Typical Applications


5V
ANY µPROCESSOR
µP BUS
1
2
3
5
11
12
13
14
15
16
17
18
CS
RD
WR
INTR
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
A/D
VCC
CLK R
CLK IN
VIN(+)
VIN(−)
A GND
VREF/2
D GND
20
19
4
6
7
8
9
10
10k
150 pF
DIFF INPUTS
SPAN ADJ SEE SECTION 2.4.1
TRANSDUCER
8-BIT RESOLUTION OVER ANY DESIRED ANALOG INPUT VOLTAGE RANGE SEE SECTION 2.4.1

TL/H/5671-1

8080 Interface


NSC800, 8080, Z80, 8048, ETC.
CS
RD
WR
INTR
DATA
A/D

TL/H/5671-31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)

Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±1/4 LSB		
ADC0802		±1/2 LSB	
ADC0803	±1/2 LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0801/02LJ	$-55°C \leq T_A \leq +125°C$
ADC0801/02/03/04LCJ	$-40°C \leq T_A \leq +85°C$
ADC0801/02/03/05LCN	$-40°C \leq T_A \leq +85°C$
ADC0804LCN	$0°C \leq T_A \leq +70°C$
ADC0802/03/04LCV	$0°C \leq T_A \leq +70°C$
ADC0802/03/04LCWM	$0°C \leq T_A \leq +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \leq T_A \leq T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±1/4	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2=2.500\ V_{DC}$			±1/2	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±1/2	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2=2.500\ V_{DC}$			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	V_{REF}/2-No Connection			±1	LSB
V_{REF}/2 Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±1/8	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC}=5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{\text{INTR}}$ tied to $\overline{\text{WR}}$ with $\overline{\text{CS}}$=0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{\text{WR}}$ Input (Start Pulse Width)	$\overline{\text{CS}}$=0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{\text{RD}}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{\text{RD}}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{\text{WR}}$ or $\overline{\text{RD}}$ to Reset of $\overline{\text{INTR}}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC}=4.75\ V_{DC}$			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	$V_{IN}=5\ V_{DC}$		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	$V_{IN}=0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	$I_O=360\ \mu A$ $V_{CC}=4.75\ V_{DC}$			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	$I_O=-360\ \mu A$ $V_{CC}=4.75\ V_{DC}$	2.4			V_{DC}
DATA OUTPUTS AND $\overline{\text{INTR}}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{\text{INTR}}$ Output	 $I_{OUT}=1.6$ mA, $V_{CC}=4.75\ V_{DC}$ $I_{OUT}=1.0$ mA, $V_{CC}=4.75\ V_{DC}$			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O=-360\ \mu A$, $V_{CC}=4.75\ V_{DC}$	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O=-10\ \mu A$, $V_{CC}=4.75\ V_{DC}$	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT}=0\ V_{DC}$ $V_{OUT}=5\ V_{DC}$	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, $T_A=25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A=25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	$f_{CLK}=640$ kHz, $V_{REF}/2=NC$, $T_A=25°C$ and $\overline{\text{CS}}=5V$		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

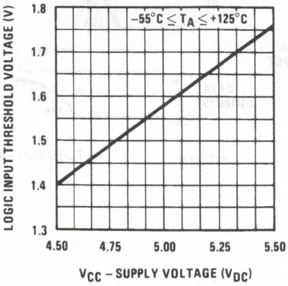
Note 7: The $\overline{\text{CS}}$ input is assumed to bracket the $\overline{\text{WR}}$ strobe input and therefore timing is dependent on the $\overline{\text{WR}}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{\text{WR}}$ pulse (see timing diagrams).

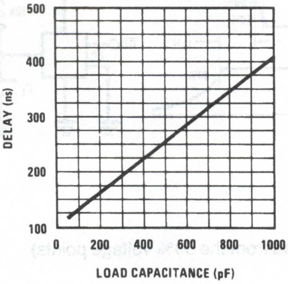
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

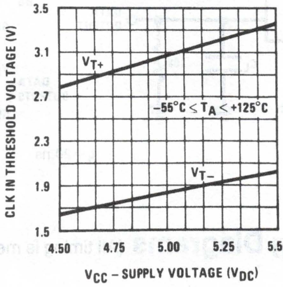
Note 9: The $V_{REF}/2$ pin is the center point of a two resistor divider connected from V_{CC} to ground. Each resistor is 2.2k, except for the ADC0804LCJ where each resistor is 16k. Total ladder input resistance is the sum of the two equal resistors.

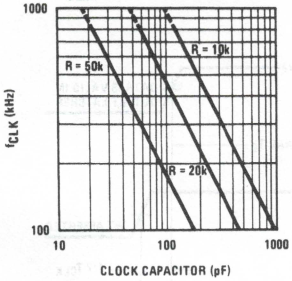
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

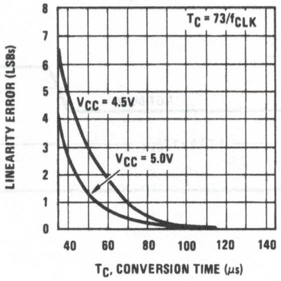
Typical Performance Characteristics

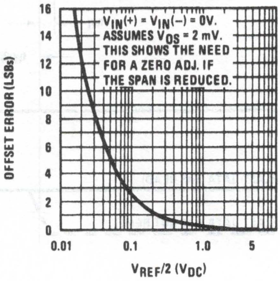

Logic Input Threshold Voltage vs. Supply Voltage

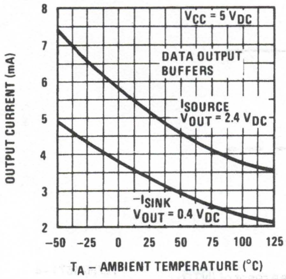

Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance

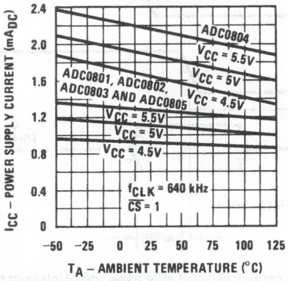

CLK IN Schmitt Trip Levels vs. Supply Voltage

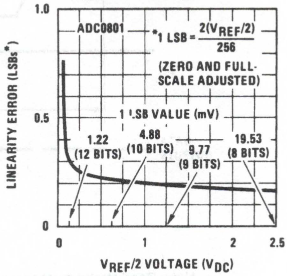

fCLK vs. Clock Capacitor


Full-Scale Error vs Conversion Time


Effect of Unadjusted Offset Error vs. VREF/2 Voltage

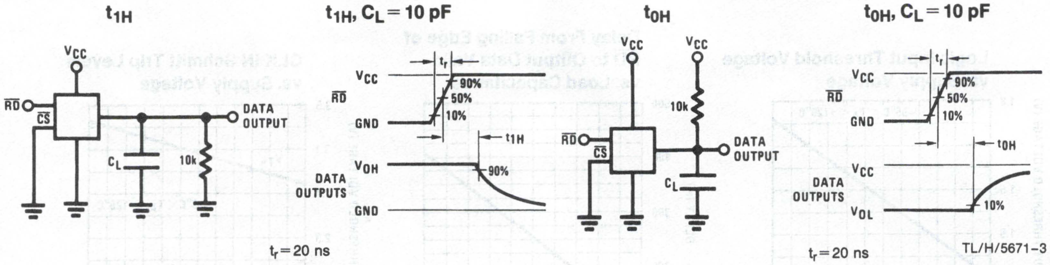

Output Current vs Temperature


Power Supply Current vs Temperature (Note 9)


Linearity Error at Low VREF/2 Voltages

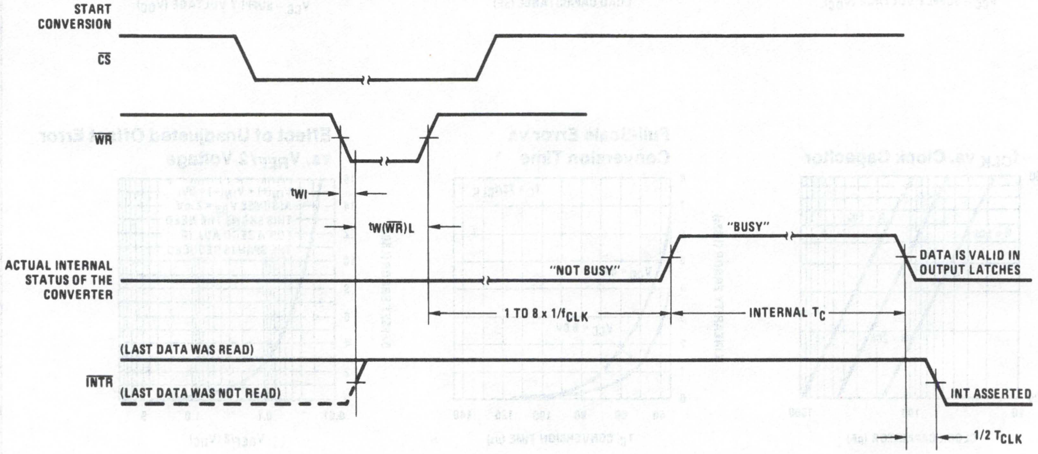
TL/H/5671–2

TRI-STATE Test Circuits and Waveforms

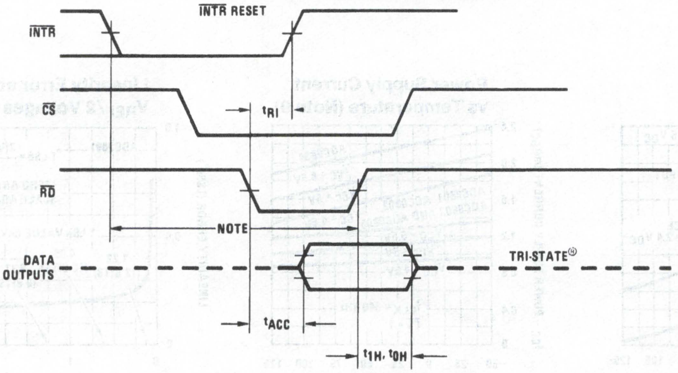

t_{1H}
V_{CC}
$\overline{RD}$
$\overline{CS}$
DATA OUTPUT
C_L
10k
t_{1H}, C_L = 10 pF
V_{CC}
$\overline{RD}$
GND
t_r
90%
50%
10%
t_{1H}
V_{OH}
DATA OUTPUTS
GND
90%
t_r = 20 ns
t_{0H}
V_{CC}
10k
DATA OUTPUT
C_L
t_{0H}, C_L = 10 pF
V_{CC}
$\overline{RD}$
GND
t_r
90%
50%
10%
t_{0H}
V_{CC}
DATA OUTPUTS
V_{OL}
10%
t_r = 20 ns

TL/H/5671-3

Timing Diagrams (All timing is measured from the 50% voltage points)


START CONVERSION
$\overline{CS}$
$\overline{WR}$
t_{WI}
$t_{W(\overline{WR})L}$
ACTUAL INTERNAL STATUS OF THE CONVERTER
"NOT BUSY"
"BUSY"
DATA IS VALID IN OUTPUT LATCHES
1 TO 8 x 1/f_{CLK}
INTERNAL T_C
(LAST DATA WAS READ)
$\overline{INTR}$
(LAST DATA WAS NOT READ)
INT ASSERTED
1/2 T_{CLK}

Output Enable and Reset $\overline{INTR}$

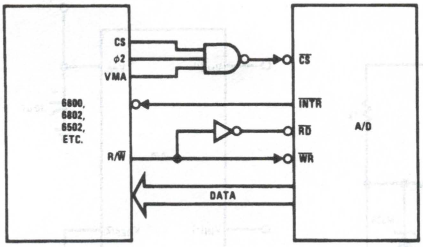

$\overline{INTR}$
$\overline{INTR}$ RESET
$\overline{CS}$
t_{RI}
$\overline{RD}$
NOTE
DATA OUTPUTS
TRI-STATE④
t_{ACC}
t_{1H}, t_{0H}

Note: Read strobe must occur 8 clock periods (8/f_{CLK}) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

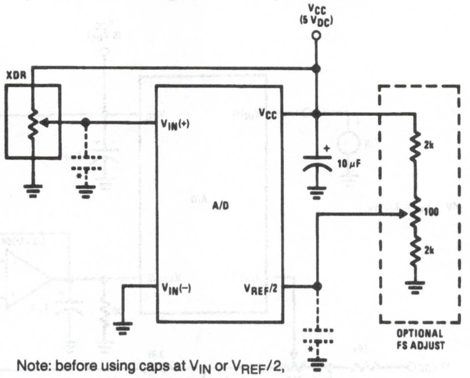
TL/H/5671-4

Typical Applications (Continued)

6800 Interface

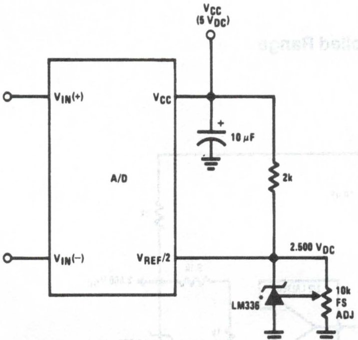

CS
φ2
VMA
6800,
6802,
6502,
ETC.
R/W̄
$\overline{CS}$
$\overline{INTR}$
$\overline{RD}$
$\overline{WR}$
A/D
DATA

Ratiometric with Full-Scale Adjust


V_{CC}
$(5\ V_{DC})$
XDR
$V_{IN}(+)$
V_{CC}
+
10 µF
*
A/D
$V_{IN}(-)$
$V_{REF}/2$
2k
100
2k
OPTIONAL
FS ADJUST

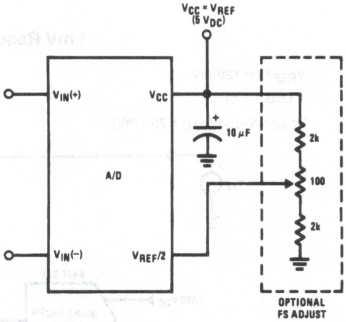
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

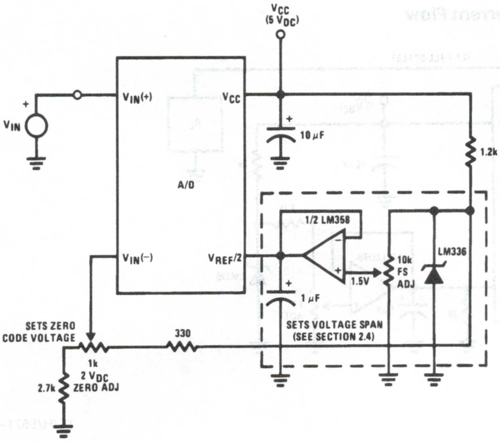

V_{CC}
$(5\ V_{DC})$
$V_{IN}(+)$
V_{CC}
+
10 µF
A/D
2k
$V_{IN}(-)$
$V_{REF}/2$
2.500 V_{DC}
LM336
*
10k
FS
ADJ

*For low power, see also LM385-2.5

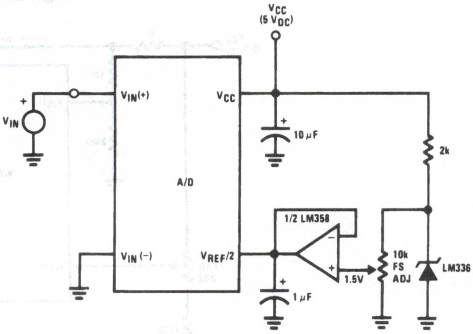
Absolute with a 5V Reference


$V_{CC} = V_{REF}$
$(5\ V_{DC})$
$V_{IN}(+)$
V_{CC}
+
10 µF
A/D
2k
100
2k
$V_{IN}(-)$
$V_{REF}/2$
OPTIONAL
FS ADJUST

Zero-Shift and Span Adjust: $2V \le V_{IN} \le 5V$


V_{CC}
$(5\ V_{DC})$
+
V_{IN}
$V_{IN}(+)$
V_{CC}
+
10 µF
1.2k
A/D
1/2 LM358
$V_{IN}(-)$
$V_{REF}/2$
−
+
10k
FS
ADJ
LM336
1.5V
+
1 µF
SETS VOLTAGE SPAN
(SEE SECTION 2.4)
SETS ZERO
CODE VOLTAGE
1k
2 V_{DC}
ZERO ADJ
330
2.7k

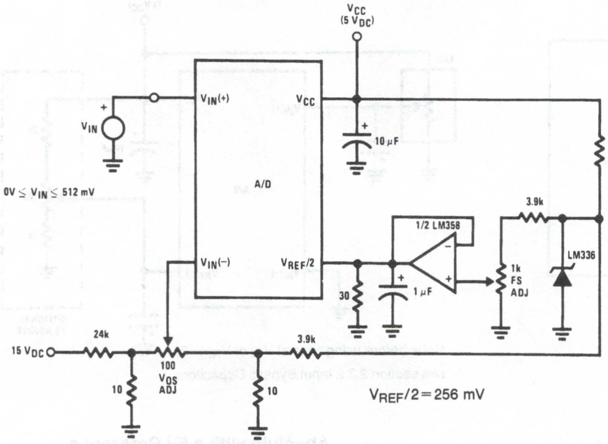
Span Adjust: $0V \le V_{IN} \le 3V$


V_{CC}
$(5\ V_{DC})$
+
V_{IN}
$V_{IN}(+)$
V_{CC}
+
10 µF
2k
A/D
1/2 LM358
−
+
$V_{IN}(-)$
$V_{REF}/2$
1.5V
10k
FS
ADJ
LM336
+
1 µF

TL/H/5671-5

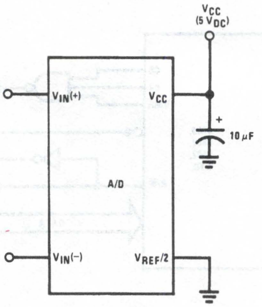
Typical Applications (Continued)

Directly Converting a Low-Level Signal


VCC (5 VDC)
VIN
0V ≤ VIN ≤ 512 mV
VIN(+)
VCC
A/D
10 µF
1k
3.9k
1/2 LM358
LM336
VIN(−)
VREF/2
30
1 µF
1k FS ADJ
15 VDC
24k
100 VOS ADJ
10
3.9k
10

$V_{REF}/2 = 256$ mV

A µP Interfaced Comparator


VCC (5 VDC)
VIN(+)
VCC
10 µF
A/D
VIN(−)
VREF/2

For: $V_{IN}(+) > V_{IN}(-)$

Output $= FF_{HEX}$

For: $V_{IN}(+) < V_{IN}(-)$

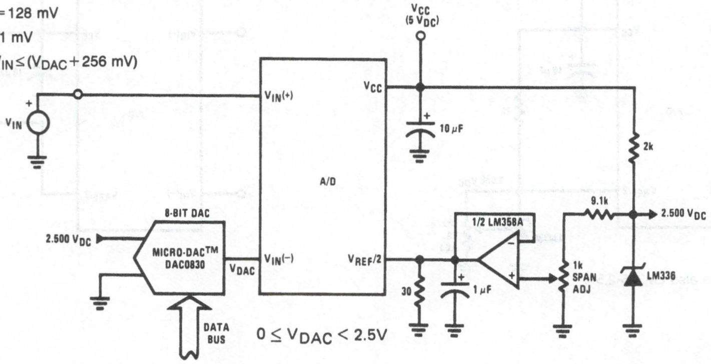
Output $= 00_{HEX}$

1 mV Resolution with µP Controlled Range

$V_{REF}/2 = 128$ mV

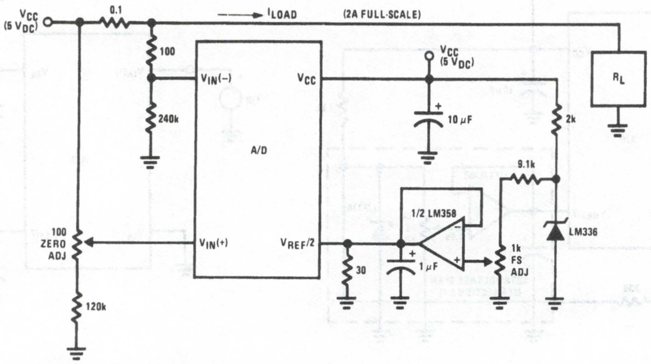
1 LSB = 1 mV

$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256\ \text{mV})$


VCC (5 VDC)
VIN
VIN(+)
VCC
10 µF
2k
A/D
8-BIT DAC
2.500 VDC
MICRO-DAC™ DAC0830
VDAC
DATA BUS
VIN(−)
VREF/2
30
1 µF
1/2 LM358A
9.1k
2.500 VDC
1k SPAN ADJ
LM336

$0 \leq V_{DAC} < 2.5V$

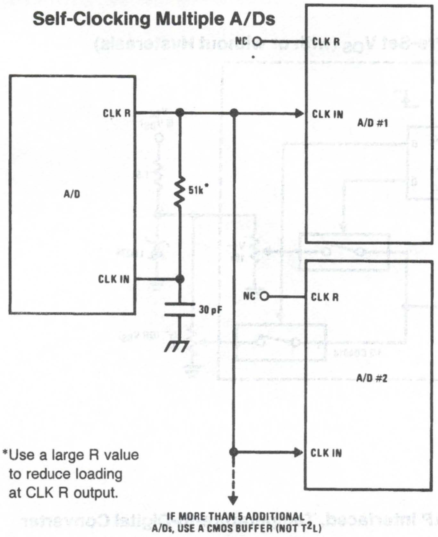
Digitizing a Current Flow


VCC (5 VDC)
0.1
ILOAD
(2A FULL-SCALE)
100
VIN(−)
VCC
VCC (5 VDC)
RL
240k
10 µF
2k
A/D
9.1k
1/2 LM358
LM336
100 ZERO ADJ
VIN(+)
VREF/2
30
1 µF
1k FS ADJ
120k

TL/H/5671-6

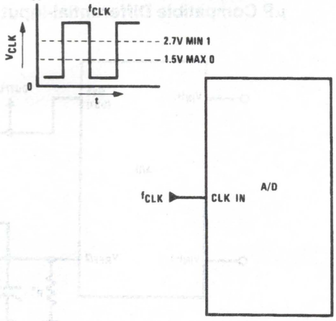
Typical Applications (Continued)

Self-Clocking Multiple A/Ds


A/D
CLK R
CLK IN
51k*
30 pF
NC
CLK R
CLK IN
A/D #1
NC
CLK R
A/D #2
CLK IN
IF MORE THAN 5 ADDITIONAL A/Ds, USE A CMOS BUFFER (NOT T²L)

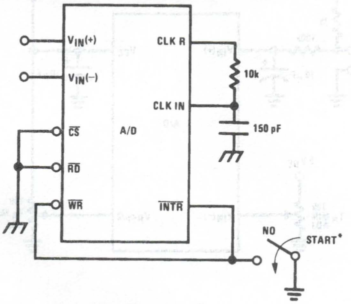
*Use a large R value to reduce loading at CLK R output.

External Clocking


5V
fCLK
VCLK
2.7V MIN 1
1.5V MAX 0
0
t
fCLK
CLK IN
A/D

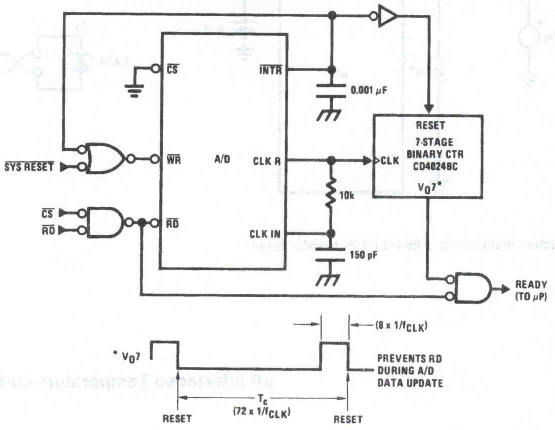
100 kHz ≤ f_{CLK} ≤ 1460 kHz

Self-Clocking in Free-Running Mode

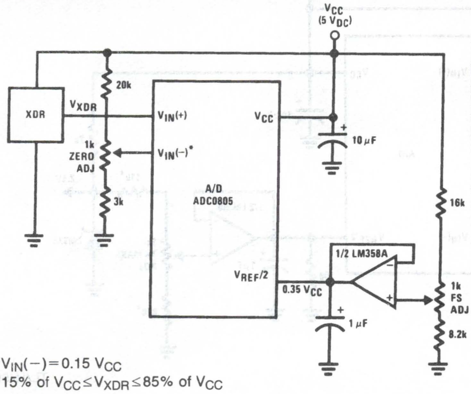

VIN(+)
VIN(−)
CS
RD
WR
A/D
CLK R
CLK IN
INTR
10k
150 pF
NO
START*

*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D


CS
INTR
0.001 µF
SYS RESET
WR
A/D
CLK R
CS
RD
RD
CLK IN
10k
150 pF
RESET
7-STAGE BINARY CTR CD4024BC
CLK
Vo7*
READY (TO µP)
(8 x 1/fCLK)
* Vo7
PREVENTS RD DURING A/D DATA UPDATE
RESET
Tc (72 x 1/fCLK)
RESET

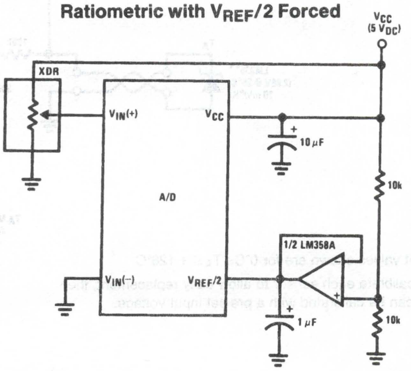
Operating with "Automotive" Ratiometric Transducers


VCC (5 VDC)
XDR
VXDR
20k
1k ZERO ADJ
3k
VIN(+)
VIN(−)*
VCC
A/D ADC0805
VREF/2
10 µF
16k
1/2 LM358A
0.35 VCC
1 µF
1k FS ADJ
8.2k

*$V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \le V_{XDR} \le 85\%$ of V_{CC}

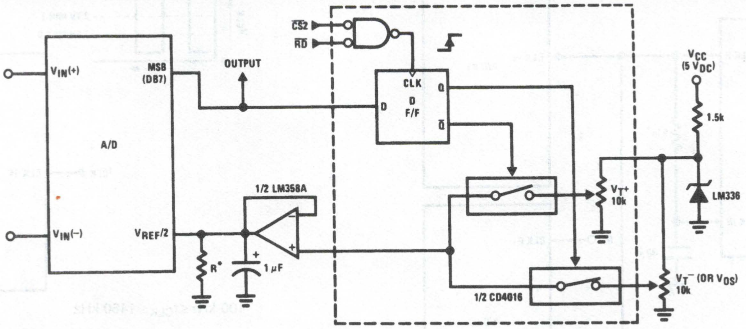
Ratiometric with $V_{REF}/2$ Forced


VCC (5 VDC)
XDR
VIN(+)
VCC
10 µF
A/D
10k
1/2 LM358A
VIN(−)
VREF/2
1 µF
10k

TL/H/5671–7

Typical Applications (Continued)

µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



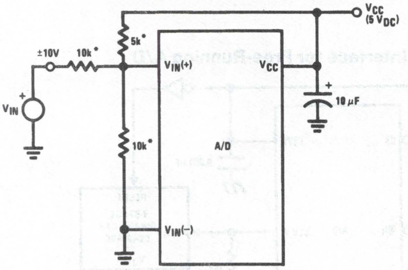
CS2
RD
CLK
D
F/F
Q
Q̄
D
V_IN(+)
MSB (DB7)
OUTPUT
A/D
V_IN(−)
V_REF/2
1/2 LM358A
R*
1 µF
1/2 CD4016
V_CC (5 V_DC)
1.5k
LM336
V_T+ 10k
V_T− (OR V_OS) 10k

*See *Figure 5* to select R value

DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$

Omit circuitry within the dotted area if hysteresis is not needed

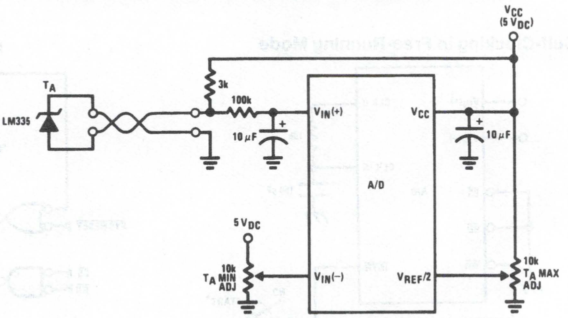
Handling ±10V Analog Inputs



V_CC (5 V_DC)
±10V
10k*
5k*
V_IN
V_IN(+)
V_CC
10 µF
10k*
A/D
V_IN(−)

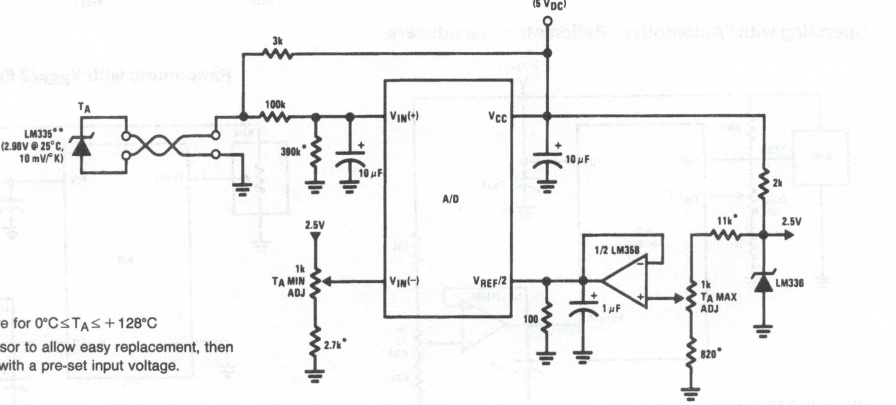
*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



V_CC (5 V_DC)
T_A
LM335
3k
100k
10 µF
V_IN(+)
V_CC
10 µF
A/D
5 V_DC
10k T_A MIN ADJ
V_IN(−)
V_REF/2
10k T_A MAX ADJ

µP Interfaced Temperature-to-Digital Converter



V_CC (5 V_DC)
3k
T_A
LM335** (2.98V @ 25°C, 10 mV/°K)
100k
390k*
10 µF
V_IN(+)
V_CC
10 µF
A/D
2k
2.5V
1k T_A MIN ADJ
2.7k*
V_IN(−)
V_REF/2
100
1 µF
1/2 LM358
11k*
2.5V
LM336
1k T_A MAX ADJ
820*

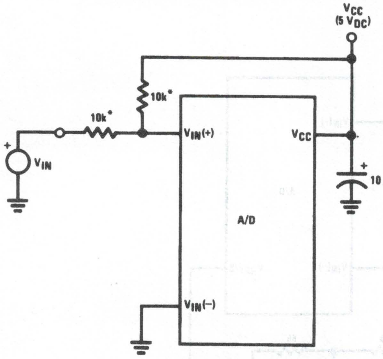
*Circuit values shown are for 0°C≤T_A≤+128°C

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

TL/H/5671-8

Typical Applications (Continued)

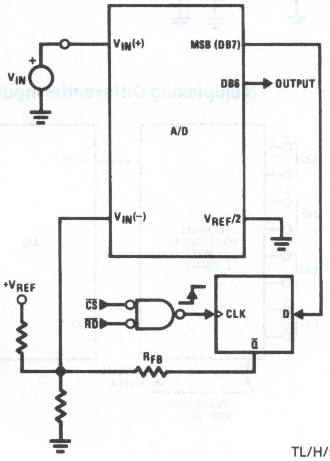
Handling ±5V Analog Inputs


VCC
(5 VDC)
10k*
10k*
VIN
VIN(+)
VCC
10 μF
A/D
VIN(−)

TL/H/5671-33

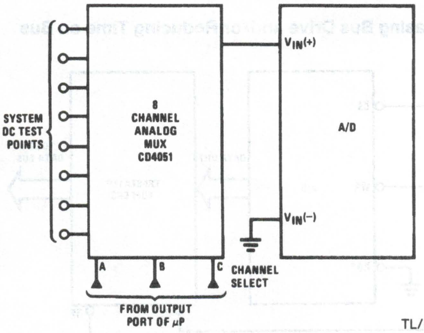
*Beckman Instruments #694-3-R10K resistor array

μP Interfaced Comparator with Hysteresis


VIN
VIN(+)
MSB (DB7)
DB6
OUTPUT
A/D
VIN(−)
VREF/2
+VREF
CS
RD
CLK
D
Q̄
RFB

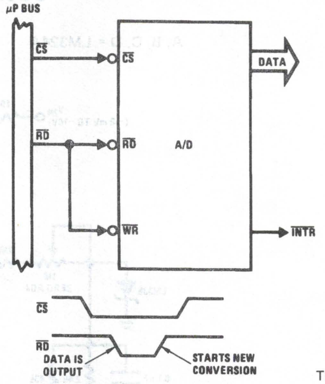
TL/H/5671-35

Analog Self-Test for a System


SYSTEM
DC TEST
POINTS
8
CHANNEL
ANALOG
MUX
CD4051
A
B
C
CHANNEL
SELECT
FROM OUTPUT
PORT OF μP
VIN(+)
A/D
VIN(−)

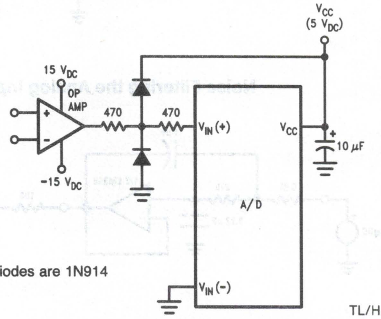
TL/H/5671-36

Read-Only Interface


μP BUS
CS
RD
DATA
A/D
WR
INTR
CS
RD
DATA IS
OUTPUT
STARTS NEW
CONVERSION

TL/H/5671-34

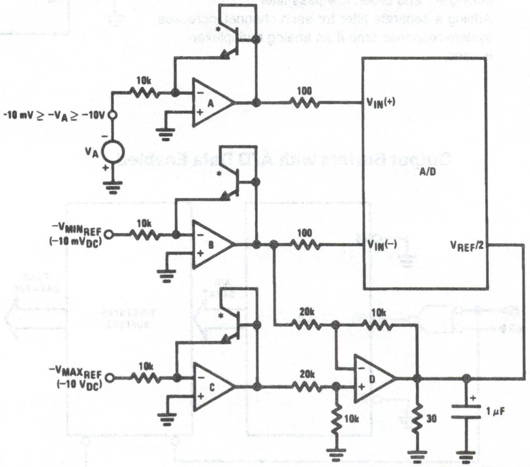
Protecting the Input


VCC
(5 VDC)
15 VDC
OP
AMP
470
470
VIN (+)
VCC
10 μF
−15 VDC
A/D
VIN (−)

Diodes are 1N914

TL/H/5671-9

A Low-Cost, 3-Decade Logarithmic Converter


*
10k
A
100
VIN(+)
−10 mV ≥ −VA ≥ −10V
VA
*
A/D
−VMINREF
(−10 mVDC)
10k
B
100
VIN(−)
VREF/2
*
20k
10k
−VMAXREF
(−10 VDC)
10k
C
20k
D
10k
30
1 μF

TL/H/5671-37

*LM389 transistors

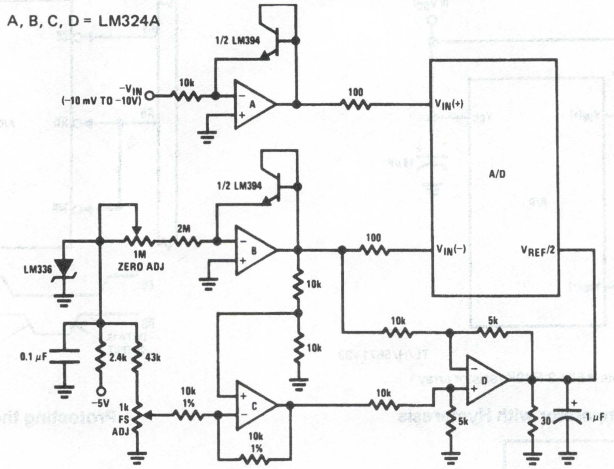
A, B, C, D = LM324A quad op amp

3

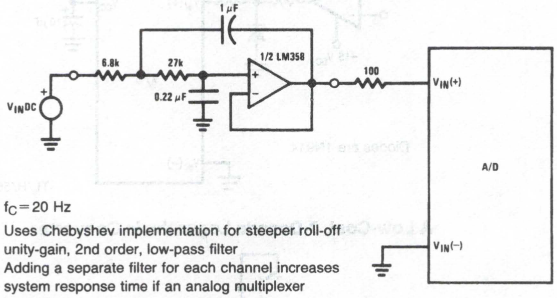
Typical Applications (Continued)

3-Decade Logarithmic A/D Converter

A, B, C, D = LM324A


1/2 LM394
$-V_{IN}$
(−10 mV TO −10V)
10k
A
100
$V_{IN}(+)$
A/D
1/2 LM394
2M
1M
ZERO ADJ
LM336
B
100
$V_{IN}(-)$
$V_{REF}/2$
10k
10k
10k
5k
0.1 µF
2.4k
43k
−5V
1k
FS
ADJ
10k
1%
C
10k
1%
10k
D
5k
30
1 µF

Noise Filtering the Analog Input

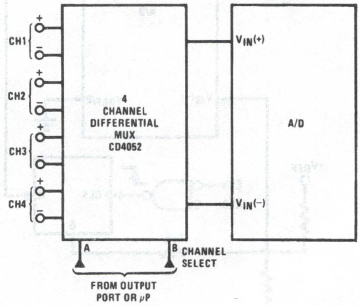

1 µF
6.8k
27k
1/2 LM358
100
$V_{IN}(+)$
$V_{IN}DC$
0.22 µF
A/D
$V_{IN}(-)$

$f_C = 20$ Hz

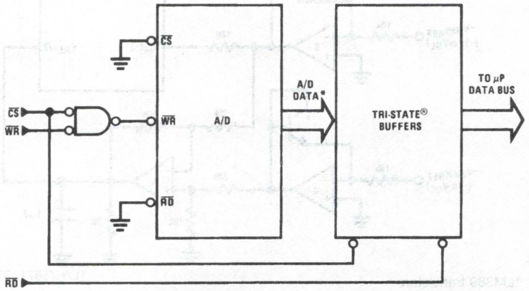
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

Adding a separate filter for each channel increases system response time if an analog multiplexer is used

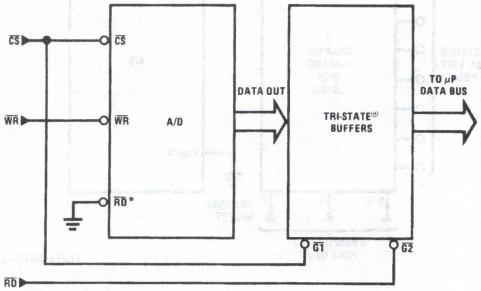
Multiplexing Differential Inputs


CH1
CH2
CH3
CH4
4 CHANNEL DIFFERENTIAL MUX CD4052
$V_{IN}(+)$
$V_{IN}(-)$
A/D
A
B
CHANNEL SELECT
FROM OUTPUT PORT OR µP

Output Buffers with A/D Data Enabled


CS
WR
RD
A/D
A/D DATA*
TRI-STATE® BUFFERS
TO µP DATA BUS
CS
WR
RD

Increasing Bus Drive and/or Reducing Time on Bus


CS
WR
RD*
A/D
DATA OUT
TRI-STATE® BUFFERS
TO µP DATA BUS
G1
G2
CS
WR
RD

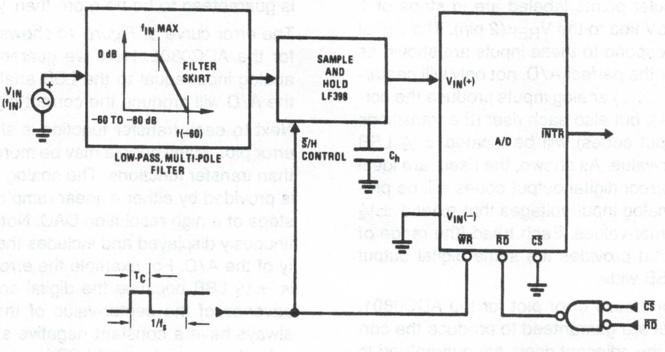
TL/H/5671–10

*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

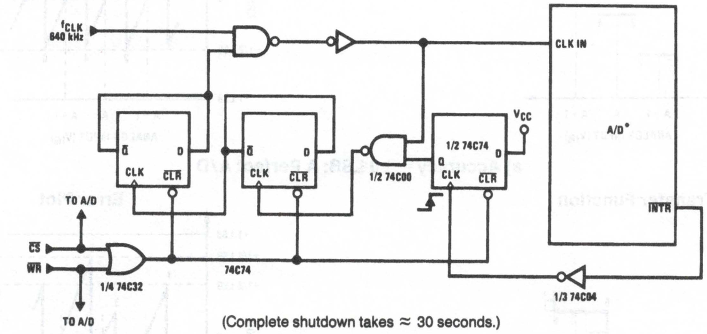
Sampling an AC Input Signal


f_IN MAX
0 dB
FILTER SKIRT
V_IN (f_IN)
−60 TO −80 dB
f(−60)
LOW-PASS, MULTI-POLE FILTER
SAMPLE AND HOLD LF398
S/H CONTROL
C_h
V_IN(+)
A/D
INTR
V_IN(−)
WR
RD
CS
CS
RD
T_C
1/f_s

Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

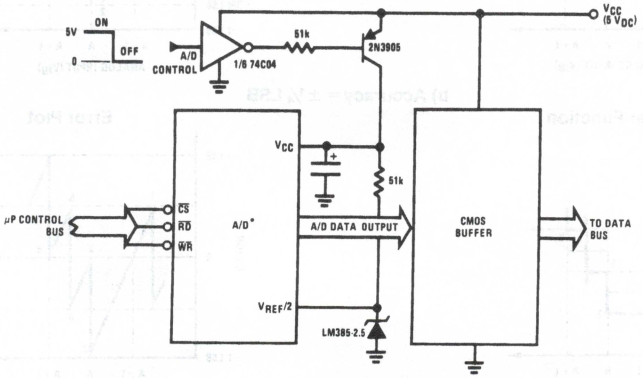
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating


f_CLK 640 kHz
CLK IN
A/D*
V_CC
1/2 74C74
D
Q
CLK
CLR
1/2 74C00
Q̄
D
CLK
CLR
74C74
INTR
1/3 74C04
TO A/D
CS
WR
1/4 74C32
TO A/D

(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown


5V
ON
OFF
0
A/D CONTROL
1/6 74C04
51k
2N3905
V_CC (5 V_DC)
V_CC
51k
µP CONTROL BUS
CS
RD
WR
A/D*
A/D DATA OUTPUT
CMOS BUFFER
TO DATA BUS
V_REF/2
LM385-2.5

TL/H/5671–11

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

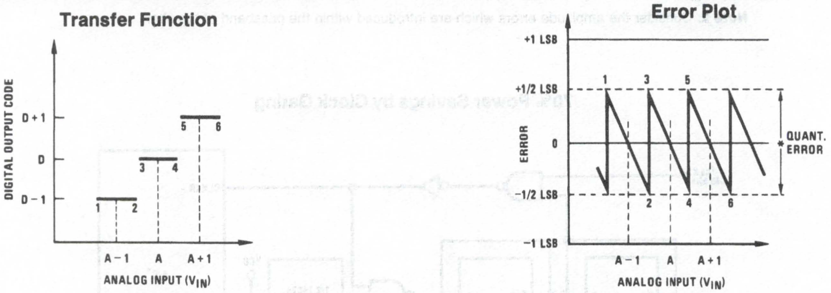
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output ditigal codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

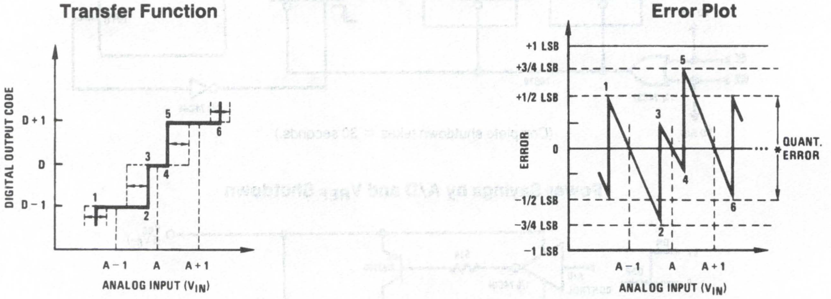
The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.


Transfer Function

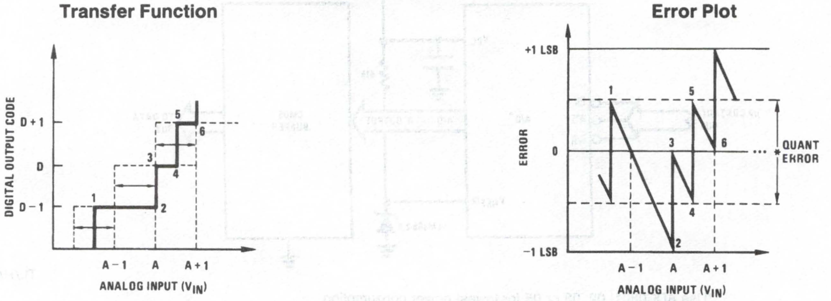
Error Plot

a) Accuracy = ±0 LSB: A Perfect A/D


Transfer Function

Error Plot

b) Accuracy = ±¼ LSB


Transfer Function

Error Plot

c) Accuracy = ±½ LSB

TL/H/5671-12

FIGURE 1. Clarifying the Error Specs of an A/D Converter

Functional Description (Continued)

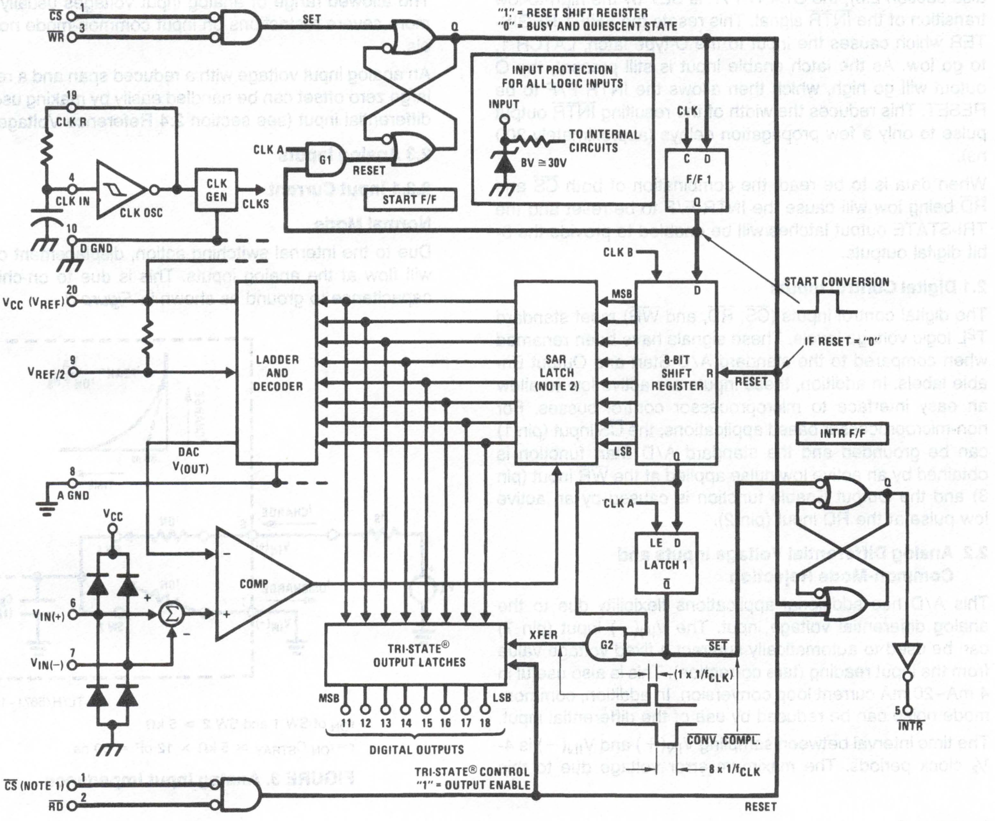
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}=0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.


CS
1
3
WR
SET
Q
"1" = RESET SHIFT REGISTER
"0" = BUSY AND QUIESCENT STATE
INPUT PROTECTION FOR ALL LOGIC INPUTS
INPUT
TO INTERNAL CIRCUITS
BV ≅ 30V
CLK
C D
F/F 1
Q
19
CLK R
CLK A
G1
RESET
START F/F
4
CLK IN
CLK OSC
CLK GEN
CLKS
10
D GND
CLK B
D
START CONVERSION
20
VCC (VREF)
LADDER AND DECODER
MSB
SAR LATCH (NOTE 2)
8-BIT SHIFT REGISTER
R
RESET
IF RESET = "0"
INTR F/F
LSB
Q
9
VREF/2
DAC V(OUT)
8
A GND
VCC
CLK A
LE D
LATCH 1
Q̄
COMP
6
VIN(+)
7
VIN(−)
XFER
G2
SET
(1 x 1/fCLK)
TRI-STATE® OUTPUT LATCHES
MSB
LSB
11 12 13 14 15 16 17 18
DIGITAL OUTPUTS
TRI-STATE® CONTROL
"1" = OUTPUT ENABLE
CONV. COMPL.
8 x 1/fCLK
5
INTR
RESET
CS (NOTE 1)
1
RD
2

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Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

Functional Description (Continued)

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{\text{INTR}}$ input signal.

Note that this $\overline{\text{SET}}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at ⅛ of the frequency of the external clock). If the data output is continuously enabled ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ both held low), the $\overline{\text{INTR}}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{\text{SET}}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{\text{INTR}}$ output will therefore stay low for the duration of the $\overline{\text{SET}}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{\text{INTR}}$ pin tied to $\overline{\text{WR}}$ and $\overline{\text{CS}}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{\text{INTR}}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{\text{Q}}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{\text{INTR}}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{\text{CS}}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{\text{WR}}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{\text{RD}}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(\text{MAX}) = (V_P)\,(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}\ (f_{CLK})]}{(2\pi f_{cm})\ (4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\ (640 \times 10^3)}{(6.28)\ (60)\ (4.5)}$$

which gives

$$V_P \cong 1.9\text{V}.$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

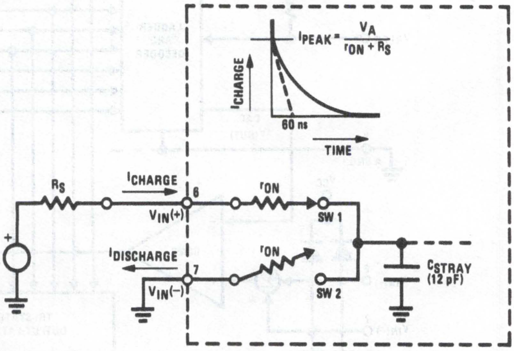
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



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r_{ON} of SW 1 and SW 2 ≅ 5 kΩ

$r = r_{ON}\ C_{STRAY} \cong 5\ \text{k}\Omega \times 12\ \text{pF} = 60\ \text{ns}$

FIGURE 3. Analog Input Impedance

Functional Description (Continued)

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of $V_{CC}+50$ mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($\leq$ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ($\leq$ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

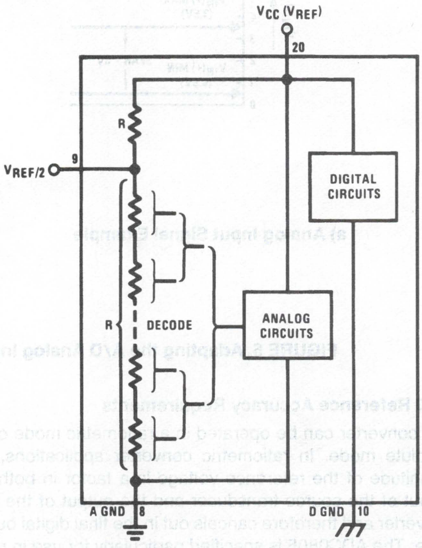

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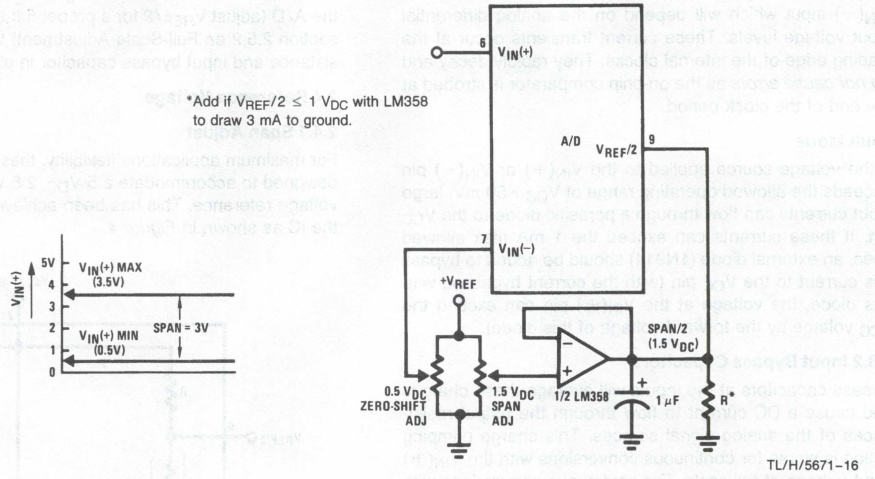
FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

Functional Description (Continued)



*Add if $V_{REF}/2 \leq 1$ V_{DC} with LM358 to draw 3 mA to ground.

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a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500$ V_{DC}).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

Functional Description (Continued)

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = The high end of the analog input range

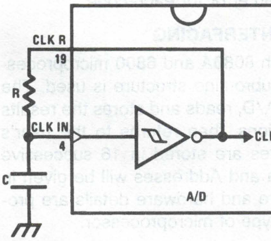
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} \cong \frac{1}{1.1\ RC}$$

$$R \cong 10\ k\Omega$$

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FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

Functional Description (Continued)

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7.*

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640· V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

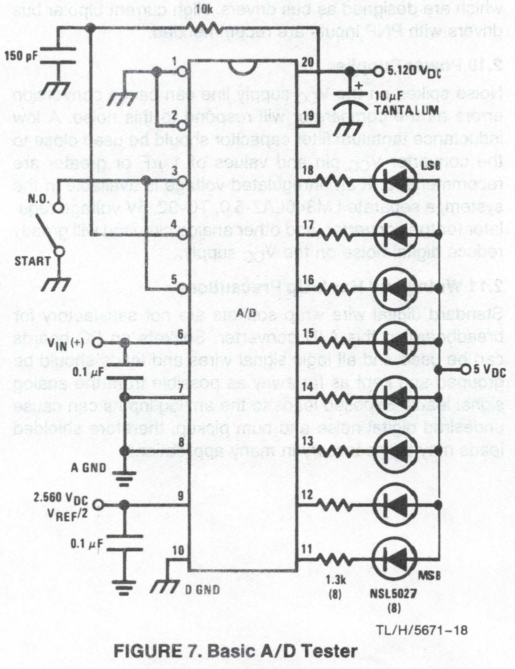

FIGURE 7. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8.* The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A−C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9,* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10.*

Functional Description (Continued)

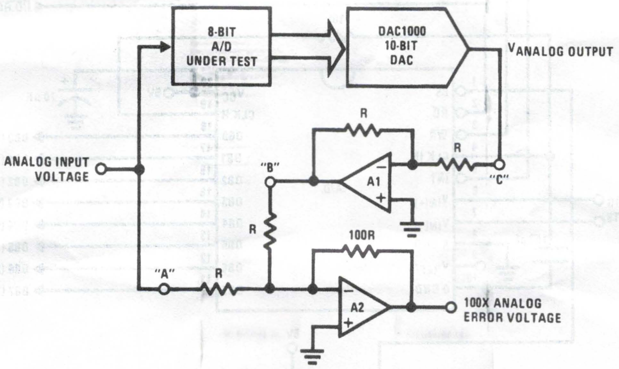
8-BIT
A/D
UNDER TEST
DAC1000
10-BIT
DAC
VANALOG OUTPUT
R
R
"B"
"C"
A1
ANALOG INPUT
VOLTAGE
R
100R
"A"
R
A2
100X ANALOG
ERROR VOLTAGE

FIGURE 8. A/D Tester with Analog Error Output

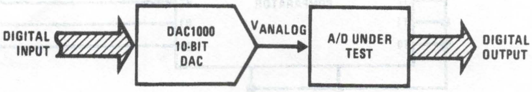
DIGITAL
INPUT
DAC1000
10-BIT
DAC
VANALOG
A/D UNDER
TEST
DIGITAL
OUTPUT

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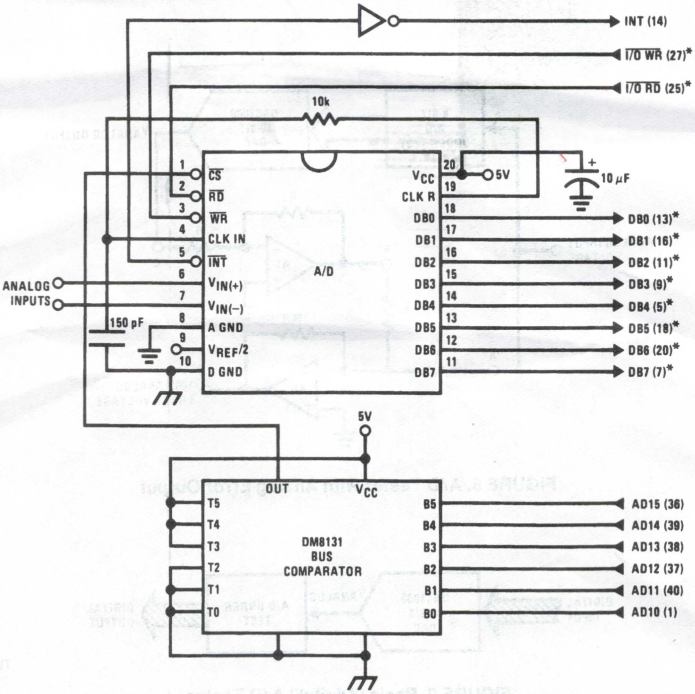
FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
					MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2/880	0.180
8	1	0	0	0	1/2	1/32	2/560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1/280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

*Display Output = VMS Group + VLS Group

Functional Description (Continued)


INT (14)
I/O WR (27)*
I/O RD (25)*
10k
1 CS
2 RD
3 WR
4 CLK IN
5 INT
6 VIN(+)
7 VIN(−)
8 A GND
9 VREF/2
10 D GND
A/D
20 VCC
19 CLK R
18 DB0
17 DB1
16 DB2
15 DB3
14 DB4
13 DB5
12 DB6
11 DB7
5V
10 µF
DB0 (13)*
DB1 (16)*
DB2 (11)*
DB3 (9)*
DB4 (5)*
DB5 (18)*
DB6 (20)*
DB7 (7)*
ANALOG INPUTS
150 pF
5V
OUT
VCC
T5
T4
T3
T2
T1
T0
DM8131 BUS COMPARATOR
B5
B4
B3
B2
B1
B0
AD15 (36)
AD14 (39)
AD13 (38)
AD12 (37)
AD11 (40)
AD10 (1)

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Note 1: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801-INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801-INS8080A CPU INTERFACE

```
0038   C3 00 03   RST 7:             JMP      LD DATA
 •      •          •
 •      •          •
0100   21 00 02   START:             LXI H 0200H     ; HL pair will point to
                                                     ; data storage locations
0103   31 00 04   RETURN:            LXI SP 0400H    ; Initialize stack pointer (Note 1)
0106   7D                            MOV A, L        ; Test # of bytes entered
0107   FE 0F                         CPI 0F H        ; If # = 16. JMP to
0109   CA 13 01                      JZ CONT         ; user program
010C   D3 E0                         OUT E0 H        ; Start A/D
010E   FB                            EI              ; Enable interrupt
010F   00         LOOP:              NOP             ; Loop until end of
0110   C3 0F 01                      JMP LOOP        ; conversion
0113    •         CONT:               •
 •      •          •                  •
 •      •         (User program to    •
 •      •         process data)       •
 •      •          •
 •      •          •                  •
0300   DB E0      LD DATA:           IN E0 H         ; Load data into accumulator
0302   77                            MOV M, A        ; Store data
0303   23                            INX H           ; Increment storage pointer
0304   C3 03 01                      JMP RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All address used were arbitrarily chosen.

Functional Description (Continued)

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

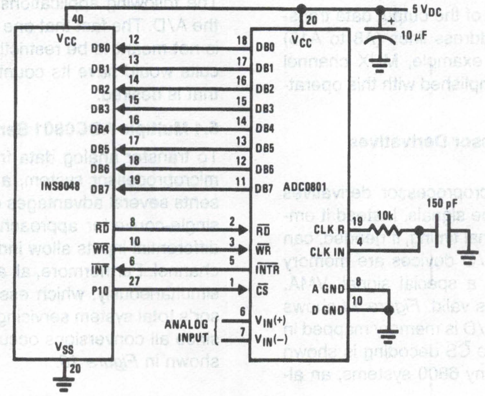

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FIGURE 11. INS8048 Interface

SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10                 JMP      10H        ; Program starts at addr 10
                      ORG      3H
04 50                 JMP      50H        ; Interrupt jump vector
                      ORG      10H        ; Main program
99 FE                 ANL      P1, #0FEH  ; Chip select
81                    MOVX     A, @R1     ; Read in the 1st data
                                          ; to reset the intr
89 01        START:   ORL      P1, #1     ; Set port pin high
B8 20                 MOV      R0, #20H   ; Data address
B9 FF                 MOV      R1, #0FFH  ; Dummy address
BA 10                 MOV      R2, #10H   ; Counter for 16 bytes
23 FF        AGAIN:   MOV      A, #0FFH   ; Set ACC for intr loop
99 FE                 ANL      P1, #0FEH  ; Send CS (bit 0 of P1)
91                    MOVX     @R1, A     ; Send WR out
05                    EN       I          ; Enable interrupt
96 21        LOOP:    JNZ      LOOP       ; Wait for interrupt
EA 1B                 DJNZ     R2, AGAIN  ; If 16 bytes are read
00                    NOP                 ; go to user's program
00                    NOP
                      ORG      50H
81           INDATA:  MOVX     A, @R1     ; Input data, CS still low
A0                    MOV      @R0, A     ; Store in memory
18                    INC      R0         ; Increment storage counter
89 01                 ORL      P1, #1     ; Reset CS signal
27                    CLR      A          ; Clear ACC to get out of
93                    RETR                ; the interrupt loop
```

Functional Description (Continued)

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 13*.

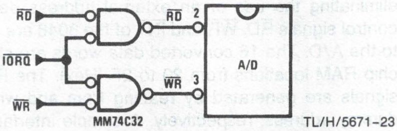


FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 14* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

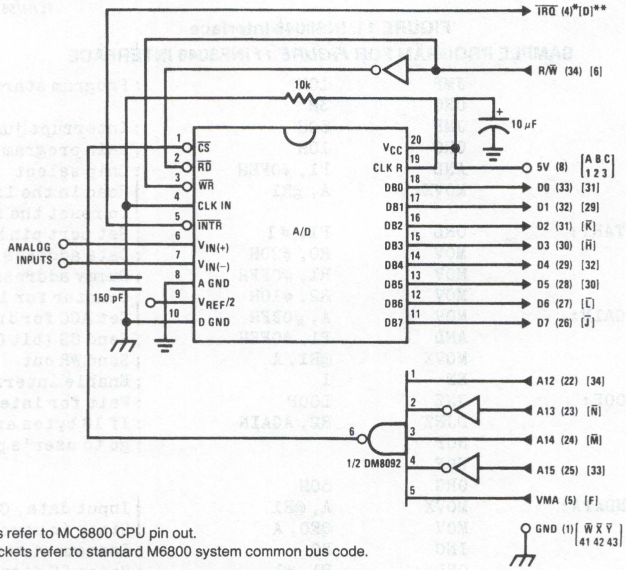
A sample interface program equivalent to the previous one is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 14. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE

```
0010    DF 36      DATAIN   STX    TEMP2      ; Save contents of X
0012    CE 00 2C            LDX    #$002C     ; Upon IRQ low CPU
0015    FF FF F8            STX    $FFF8      ; jumps to 002C
0018    B7 50 00            STAA   $5000      ; Start ADC0801
001B    0E                  CLI
001C    3E         CONVRT   WAI               ; Wait for interrupt
001D    DE 34               LDX    TEMP1
001F    8C 02 0F            CPX    #$020F     ; Is final data stored?
0022    27 14               BEQ    ENDP
0024    B7 50 00            STAA   $5000      ; Restarts ADC0801
0027    08                  INX
0028    DF 34               STX    TEMP1
002A    20 F0               BRA    CONVRT
002C    DE 34      INTRPT   LDX    TEMP1
002E    B6 50 00            LDAA   $5000      ; Read data
0031    A7 00               STAA   X          ; Store it at X
0033    3B                  RTI
0034    02 00      TEMP1    FDB    $0200      ; Starting address for
                                              ; data storage
0036    00 00      TEMP2    FDB    $0000
0038    CE 02 00   ENDP     LDX    #$0200     ; Reinitialize TEMP1
003B    DF 34               STX    TEMP1
003D    DE 36               LDX    TEMP2
003F    39                  RTS               ; Return from subroutine
                                              ; To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

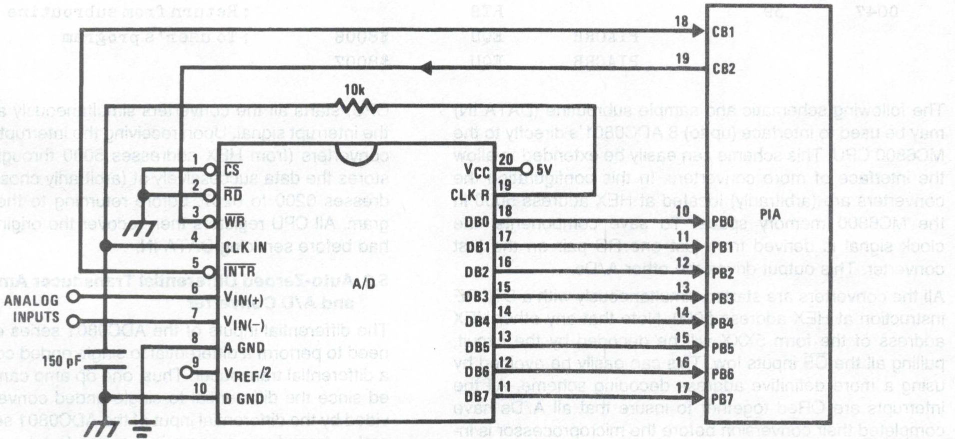

PIA
CB1
CB2
18
19
10k
A/D
CS
RD
WR
CLK IN
INTR
VIN(+)
VIN(−)
A GND
VREF/2
D GND
VCC
5V
CLK R
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
ANALOG INPUTS
150 pF
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
10
11
12
13
14
15
16
17

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FIGURE 15. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010   CE 00 38   DATAIN   LDX    #$0038   ; Upon IRQ low CPU
0013   FF FF F8            STX    $FFF8    ; jumps to 0038
0016   B6 80 06            LDAA   PIAORB   ; Clear possible IRQ flags
0019   4F                  CLRA
001A   B7 80 07            STAA   PIACRB
001D   B7 80 06            STAA   PIAORB   ; Set Port B as input
0020   0E                  CLI
0021   C6 34               LDAB   #$34
0023   86 3D               LDAA   #$3D
0025   F7 80 07   CONVRT   STAB   PIACRB   ; Starts ADC0801
0028   B7 80 07            STAA   PIACRB
002B   3E                  WAI             ; Wait for interrupt
002C   DE 40               LDX    TEMP1
002E   8C 02 0F            CPX    #$020F   ; Is final data stored?
0031   27 0F               BEQ    ENDP
0033   08                  INX
0034   DF 40               STX    TEMP1
0036   20 ED               BRA    CONVRT
0038   DE 40      INTRPT   LDX    TEMP1
003A   B6 80 06            LDAA   PIAORB   ; Read data in
003D   A7 00               STAA   X        ; Store it at X
003F   3B                  RTI
0040   02 00      TEMP1    FDB    $0200    ; Starting address for
                                           ; data storage
0042   CE 02 00   ENDP     LDX    #$0200   ; Reinitialize TEMP1
0045   DF 40               STX    TEMP1
0047   39                  RTS             ; Return from subroutine
                  PIAORB   EQU    $8006    ; To user's program
                  PIACRB   EQU    $8007
```

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

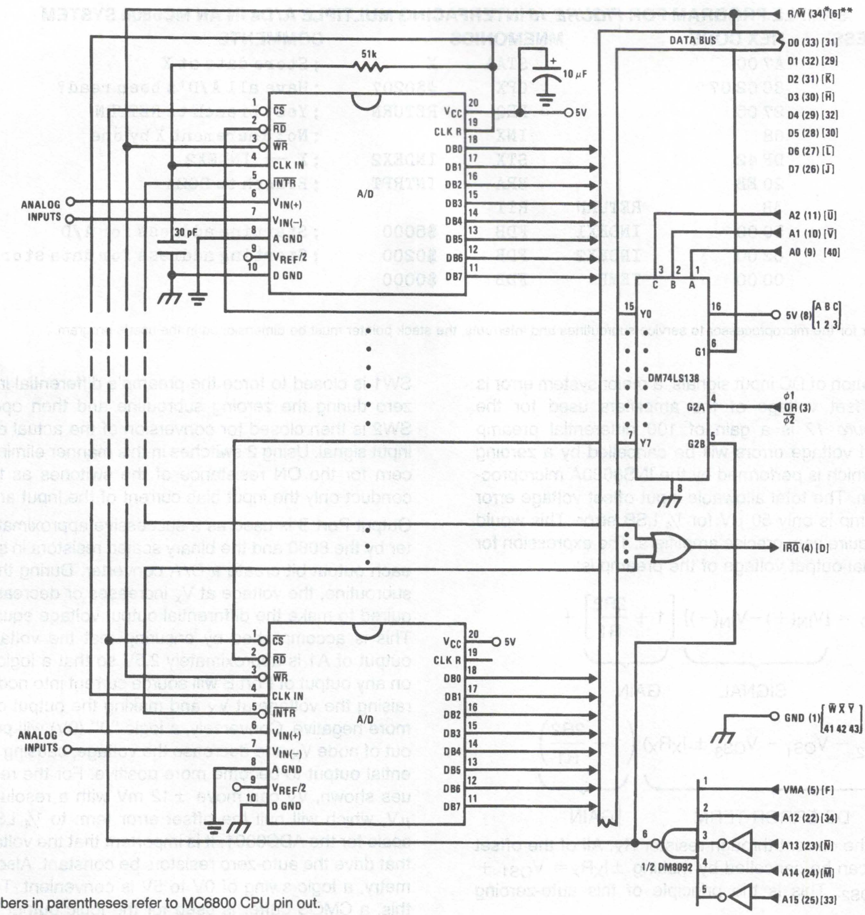
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)


R/W̄ (34)*[6]**
DATA BUS
D0 (33) [31]
D1 (32) [29]
D2 (31) [K̄]
D3 (30) [H̄]
D4 (29) [32]
D5 (28) [30]
D6 (27) [L̄]
D7 (26) [J̄]
A2 (11) [Ū]
A1 (10) [V̄]
A0 (9) [40]
5V (8) [A B C / 1 2 3]
ϕ1 OR (3) ϕ̄2
IRQ̄ (4) [D]
GND (1) [W̄ X̄ Ȳ / 41 42 43]
VMA (5) [F]
A12 (22) [34]
A13 (23) [N̄]
A14 (24) [M̄]
A15 (25) [33]
1/2 DM8092
DM74LS138
C B A
Y0
Y7
G1
G2A
G2B
51k
10 μF
5V
30 pF
ANALOG INPUTS
A/D
CS
RD
WR
CLK IN
INTR
VIN(+)
VIN(−)
A GND
VREF/2
D GND
VCC
CLK R
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7

Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers of letters in brackets refer to standard M6800 system common bus code.

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FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

```
ADDRESS  HEX CODE              MNEMONICS              COMMENTS
0010     DF 44      DATAIN     STX      TEMP          ; Save Contents of X
0012     CE 00 2A              LDX      #$002A        ; Upon IRQ LOW CPU
0015     FF FF F8              STX      $FFF8         ; Jumps to 002A
0018     B7 50 00              STAA     $5000         ; Starts all A/D's
001B     0E                    CLI
001C     3E                    WAI                    ; Wait for interrupt
001D     CE 50 00              LDX      #$5000
0020     DF 40                 STX      INDEX1        ; Reset both INDEX
0022     CE 02 00              LDX      #$0200        ; 1 and 2 to starting
0025     DF 42                 STX      INDEX2        ; addresses
0027     DE 44                 LDX      TEMP
0029     39                    RTS                    ; Return from subroutine
002A     DE 40      INTRPT     LDX      INDEX1        ; INDEX1 → X
002C     A6 00                 LDAA     X             ; Read data in from A/D at X
002E     08                    INX                    ; Increment X by one
002F     DF 40                 STX      INDEX1        ; X → INDEX1
0031     DE 42                 LDX      INDEX2        ; INDEX2 → X
```

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

```
ADDRESS   HEX CODE              MNEMONICS              COMMENTS
0033      A7 00                 STAA    X              ; Store data at X
0035      8C 02 07              CPX     #$0207         ; Have all A/D's been read?
0038      27 05                 BEQ     RETURN         ; Yes: branch to RETURN
003A      08                    INX                    ; No: increment X by one
003B      DF 42                 STX     INDEX2         ; X → INDEX2
003D      20 EB                 BRA     INTRPT         ; Branch to 002A
003F      3B        RETURN      RTI
0040      50 00     INDEX1      FDB     $5000          ; Starting address for A/D
0042      02 00     INDEX2      FDB     $0200          ; Starting address for data storage
0044      00 00     TEMP        FDB     $0000
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

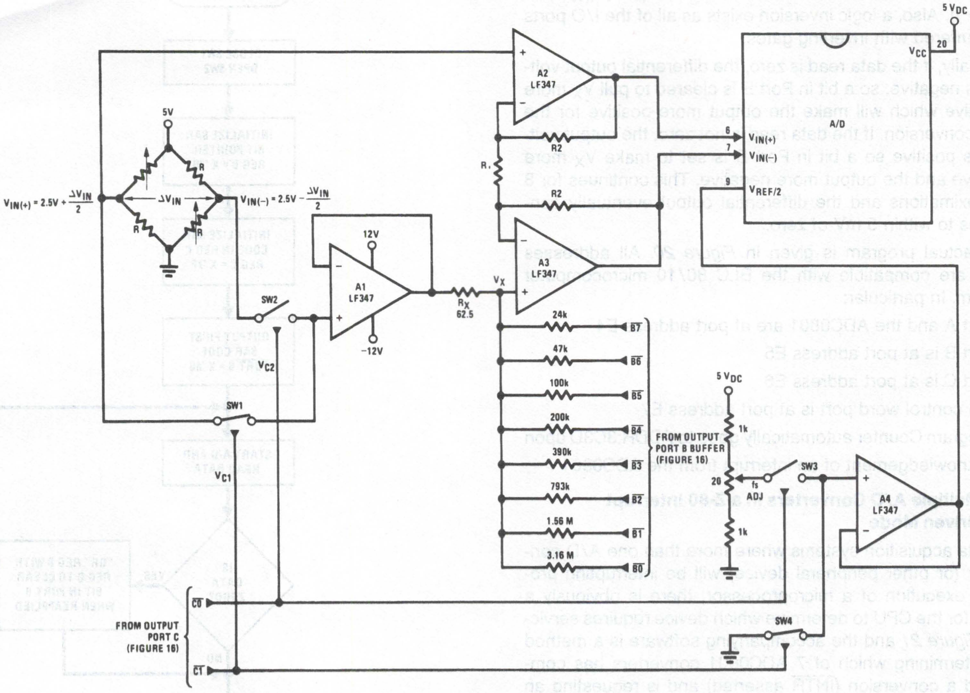
$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_X increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 μV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

Functional Description (Continued)


5 VDC
20
VCC
A/D
6
VIN(+)
7
VIN(−)
9
VREF/2
A2
LF347
R2
R1
R2
A3
LF347
VX
RX
62.5
5V
R
R
R
R
VIN(+) = 2.5V + ΔVIN/2
ΔVIN
VIN(−) = 2.5V − ΔVIN/2
12V
A1
LF347
−12V
SW2
VC2
SW1
VC1
24k
B7
47k
B6
100k
B5
200k
B4
390k
B3
793k
B2
1.56 M
B1
3.16 M
B0
FROM OUTPUT PORT B BUFFER (FIGURE 16)
5 VDC
1k
20
fs ADJ
1k
SW3
A4
LF347
SW4
C0
FROM OUTPUT PORT C (FIGURE 16)
C1

Note 1: R2 = 49.5 R1

Note 2: Switches are LMC13334 CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp

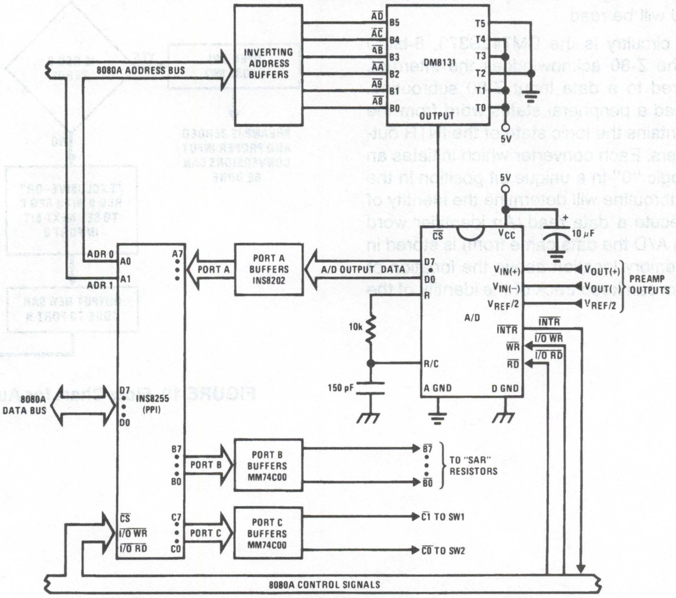

8080A ADDRESS BUS
INVERTING ADDRESS BUFFERS
A̅D̅
A̅C̅
A̅B̅
A̅A̅
A̅9̅
A̅8̅
B5
B4
B3
B2
B1
B0
DM8131
T5
T4
T3
T2
T1
T0
OUTPUT
5V
5V
10 μF
CS
VCC
ADR 0
ADR 1
A0
A1
A7
A0
PORT A
PORT A BUFFERS INS8202
A/D OUTPUT DATA
D7
D0
VIN(+)
VIN(−)
VREF/2
VOUT(+)
VOUT(−)
VREF/2
PREAMP OUTPUTS
A/D
10k
R
INTR
INTR
I/O WR
WR
I/O RD
RD
R/C
150 pF
A GND
D GND
8080A DATA BUS
D7
D0
INS8255 (PPI)
B7
B0
PORT B
PORT B BUFFERS MM74C00
B7
B0
TO "SAR" RESISTORS
CS
I/O WR
I/O RD
C7
C0
PORT C
PORT C BUFFERS MM74C00
C1 TO SW1
C0 TO SW2
8080A CONTROL SIGNALS

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FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 19*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{\text{INTR}}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{\text{INTR}}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

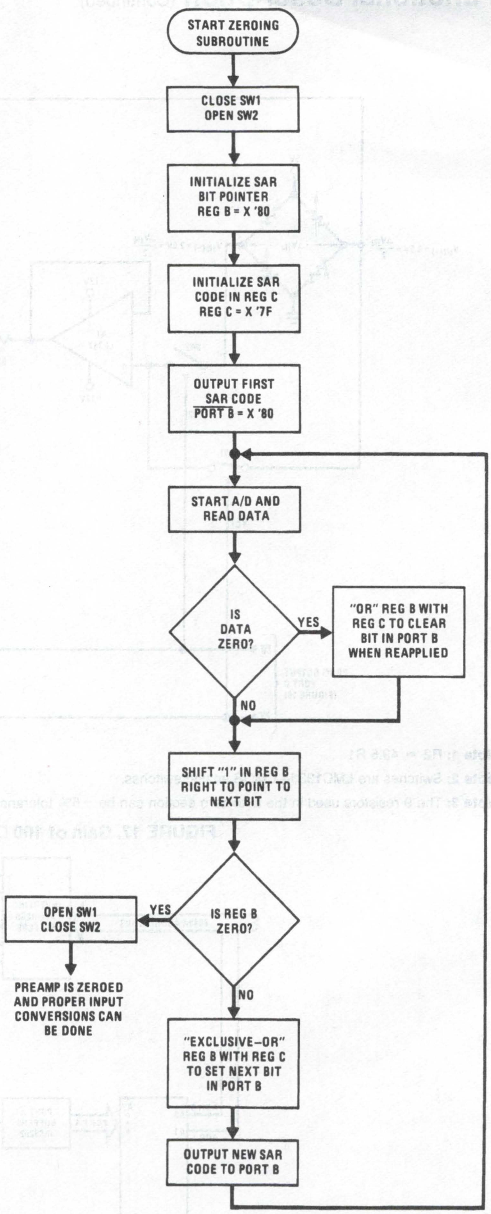
START ZEROING SUBROUTINE
CLOSE SW1 OPEN SW2
INITIALIZE SAR BIT POINTER REG B = X '80
INITIALIZE SAR CODE IN REG C REG C = X '7F
OUTPUT FIRST SAR CODE PORT B = X '80
START A/D AND READ DATA
IS DATA ZERO?
YES
"OR" REG B WITH REG C TO CLEAR BIT IN PORT B WHEN REAPPLIED
NO
SHIFT "1" IN REG B RIGHT TO POINT TO NEXT BIT
IS REG B ZERO?
YES
OPEN SW1 CLOSE SW2
PREAMP IS ZEROED AND PROPER INPUT CONVERSIONS CAN BE DONE
NO
"EXCLUSIVE-OR" REG B WITH REG C TO SET NEXT BIT IN PORT B
OUTPUT NEW SAR CODE TO PORT B

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FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D00  3E90    MVI 90
3D02  D3E7    Out Control Port                            ; Program PPI
3D04  2601    MVI H 01          Auto-Zero Subroutine
3D06  7C      MOV A,H
3D07  D3E6    OUT C                                       ; Close SW1 open SW2
3D09  0680    MVI B 80                                    ; Initialize SAR bit pointer
3D0B  3E7F    MVI A 7F                                    ; Initialize SAR code
3D0D  4F      MOV C,A           Return
3D0E  D3E5    OUT B                                       ; Port B = SAR code
3D10  31AA3D  LXI SP 3DAA       Start                     ; Dimension stack pointer
3D13  D3E4    OUT A                                       ; Start A/D
3D15  FB      IE
3D16  00      NOP               Loop                      ; Loop until INT asserted
3D17  C3163D  JMP Loop
3D1A  7A      MOV A,D           Auto-Zero
3D1B  C600    ADI 00
3D1D  CA2D3D  JZ Set C                                    ; Test A/D output data for zero
3D20  78      MOV A,B           Shift B
3D21  F600    ORI 00                                      ; Clear carry
3D23  1F      RAR                                         ; Shift "1" in B right one place
3D24  FE00    CPI 00                                      ; Is B zero? If yes last
3D26  CA373D  JZ Done                                     ; approximation has been made
3D29  47      MOV B,A
3D2A  C3333D  JMP New C
3D2D  79      MOV A,C           Set C
3D2E  B0      ORA B                                       ; Set bit in C that is in same
3D2F  4F      MOV C,A                                     ; position as "1" in B
3D30  C3203D  JMP Shift B
3D33  A9      XRA C             New C                     ; Clear bit in C that is in
3D34  C30D3D  JMP Return                                  ; same position as "1" in B
3D37  47      MOV B,A           Done                      ; then output new SAR code.
3D38  7C      MOV A,H                                     ; Open SW1, close SW2 then
3D39  EE03    XRI 03                                      ; proceed with program. Preamp
3D3B  D3E6    OUT C                                       ; is now zeroed.
3D3D          •                 Normal
              •
              •
              Program for processing
              proper data values
3C3D  DBE4    IN A              Read A/D Subroutine       ; Read A/D data
3C3F  EEFF    XRI FF                                      ; Invert data
3C41  57      MOV D,A
3C42  78      MOV A,B                                     ; Is B Reg = 0? If not stay
3C43  E6FF    ANI FF                                      ; in auto zero subroutine
3C45  C21A3D  JNZ Auto-Zero
3C48  C33D3D  JMP Normal
```

Note: All numerical values are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

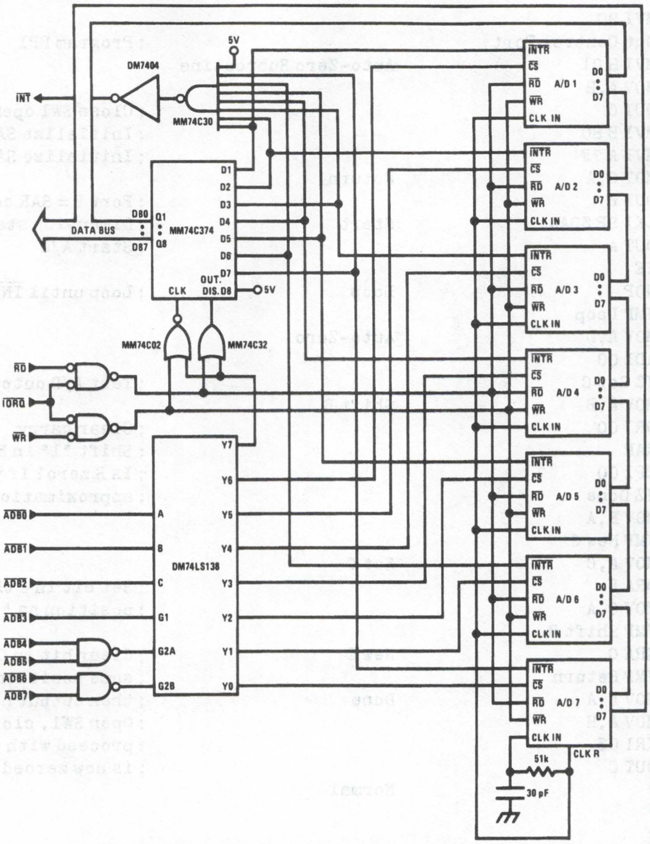
5V
DM7404
INT
MM74C30
INTR
CS
RD
WR
CLK IN
A/D 1
D0
D7
A/D 2
A/D 3
A/D 4
A/D 5
A/D 6
A/D 7
D1
D2
D3
D4
D5
D6
D7
D8
DB0
Q1
DATA BUS
DB7
Q8
MM74C374
CLK
OUT. DIS.
5V
MM74C02
MM74C32
RD
IORQ
WR
ADB0
ADB1
ADB2
ADB3
ADB4
ADB5
ADB6
ADB7
A
B
C
G1
G2A
G2B
DM74LS138
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
CLK R
51k
30 pF

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FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

```
                          SOURCE
LOC   OBJ CODE          STATEMENT                           COMMENT
0038  E5                PUSH HL           ; Save contents of all registers affected by
0039  C5                PUSH BC           ; this subroutine.
003A  F5                PUSH AF           ; Assumed INT mode 1 earlier set.
003B  21 00 3E          LD (HL),X3E00     ; Initialize memory pointer where data will be stored.
003E  0E 01             LD C, X01         ; C register will be port ADDR of A/D converters.
0040  D300              OUT X00, A        ; Load peripheral status word into 8-bit latch.
0042  DB00              IN A, X00         ; Load status word into accumulator.
0044  47                LD B,A            ; Save the status word.
0045  79         TEST   LD A,C            ; Test to see if the status of all A/D's have
0046  FE 08             CP, X08           ; been checked. If so, exit subroutine
0048  CA 60 00          JPZ, DONE
004B  78                LD A,B            ; Test a single bit in status word by looking for
004C  1F                RRA               ; a "1" to be rotated into the CARRY (an INT
004D  47                LD B,A            ; is loaded as a "1") If CARRY is set then load
004E  DA 5500           JPC, LOAD         ; contents of A/D at port ADDR in C register.
0051  0C         NEXT   INC C             ; If CARRY is not set, increment C register to point
0052  C3 4500           JP,TEST           ; to next A/D, then test next bit in status word.
0055  ED 78      LOAD   IN A, (C)         ; Read data from interrupting A/D and invert
0057  EE FF             XOR FF            ; the data.
0059  77                LD (HL),A         ; Store the data
005A  2C                INC L
005B  71                LD (HL),C         ; Store A/D identifier (A/D port ADDR).
005C  2C                INC L
005D  C3 51 00          JP,NEXT           ; Test next bit in status word.
0060  F1         DONE   POP AF            ; Re-establish all registers as they were
0061  C1                POP BC            ; before the interrupt.
0062  E1                POP HL
0063  C9                RET               ; Return to original program
```

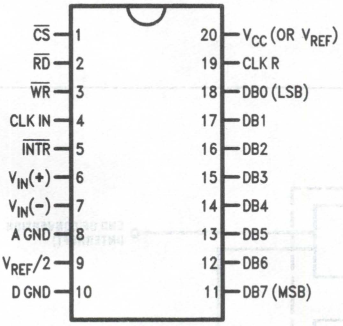
Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	$\pm\frac{1}{4}$ Bit Adjusted				ADC0801LCN
	$\pm\frac{1}{2}$ Bit Unadjusted	ADC0802LCWM	ADC0802LCV		ADC0802LCN
	$\pm\frac{1}{2}$ Bit Adjusted	ADC0803LCWM	ADC0803LCV		ADC0803LCN
	± 1 Bit Unadjusted	ADC0804LCWM	ADC0804LCV	ADC0804LCN	ADC0805LCN
PACKAGE OUTLINE		M20B—Small Outline	V20A—Chip Carrier	N20A—Molded DIP	

TEMP RANGE		−40°C TO +85°C	−55°C TO +125°C
ERROR	$\pm\frac{1}{4}$ Bit Adjusted	ADC0801LCJ	ADC0801LJ
	$\pm\frac{1}{2}$ Bit Unadjusted	ADC0802LCJ	ADC0802LJ
	$\pm\frac{1}{2}$ Bit Adjusted	ADC0803LCJ	
	± 1 Bit Unadjusted	ADC0804LCJ	
PACKAGE OUTLINE		J20A—Cavity DIP	J20A—Cavity DIP

Connection Diagrams

ADC080X
Dual-In-Line and Small Outline (SO) Packages



$\overline{CS}$ 1
$\overline{RD}$ 2
$\overline{WR}$ 3
CLK IN 4
$\overline{INTR}$ 5
$V_{IN}(+)$ 6
$V_{IN}(-)$ 7
A GND 8
$V_{REF}/2$ 9
D GND 10
20 V_{CC} (OR V_{REF})
19 CLK R
18 DB0 (LSB)
17 DB1
16 DB2
15 DB3
14 DB4
13 DB5
12 DB6
11 DB7 (MSB)

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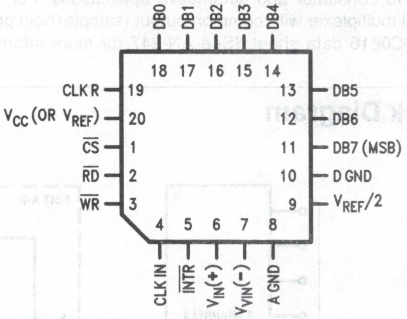
See Ordering Information

ADC080X
Molded Chip Carrier (PCC) Package



DB0
DB1
DB2
DB3
DB4
18 17 16 15 14
CLK R 19
V_{CC} (OR V_{REF}) 20
$\overline{CS}$ 1
$\overline{RD}$ 2
$\overline{WR}$ 3
13 DB5
12 DB6
11 DB7 (MSB)
10 D GND
9 $V_{REF}/2$
4 5 6 7 8
CLK IN
$\overline{INTR}$
$V_{IN}(+)$
$V_{IN}(-)$
A GND

TL/H/5671-32

National Semiconductor Corporation

ADC0808, ADC0809 8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

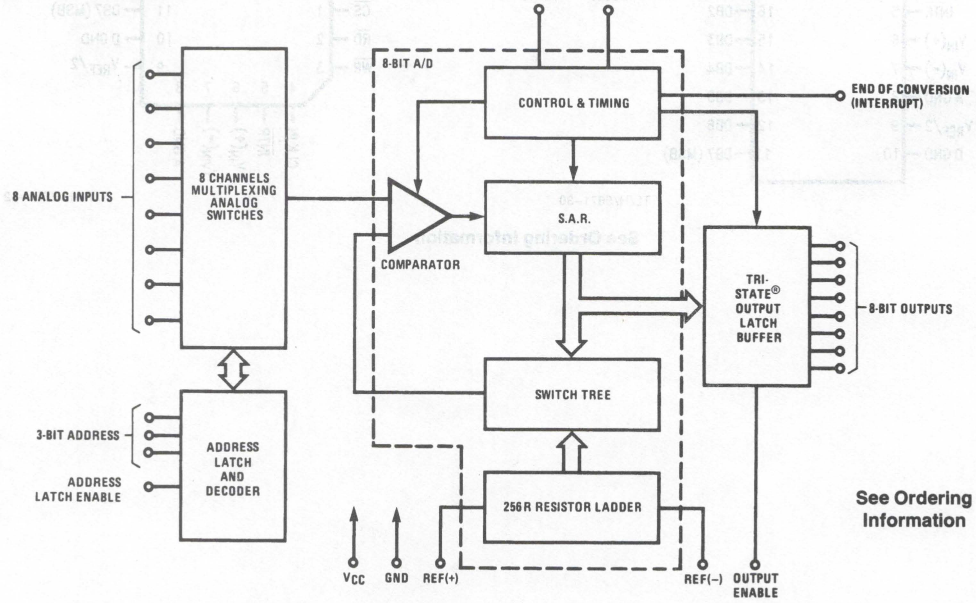
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 µs

Block Diagram


START
CLOCK
8-BIT A/D
CONTROL & TIMING
END OF CONVERSION (INTERRUPT)
8 ANALOG INPUTS
8 CHANNELS MULTIPLEXING ANALOG SWITCHES
S.A.R.
COMPARATOR
TRI-STATE® OUTPUT LATCH BUFFER
8-BIT OUTPUTS
SWITCH TREE
3-BIT ADDRESS
ADDRESS LATCH ENABLE
ADDRESS LATCH AND DECODER
256R RESISTOR LADDER
V_{CC}
GND
REF(+)
REF(−)
OUTPUT ENABLE

See Ordering Information

TL/H/5672–1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC}+0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	400V

Operating Conditions (Notes 1 & 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CJ	$-55°C \le T_A \le +125°C$
ADC0808CCJ, ADC0808CCN, ADC0809CCN	$-40°C \le T_A \le +85°C$
ADC0808CCV, ADC0809CCV	$-40°C \le T_A \le +85°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808 Total Unadjusted Error (Note 5)	25°C T_{MIN} to T_{MAX}			±½ ±¾	LSB LSB
	ADC0809 Total Unadjusted Error (Note 5)	0°C to 70°C T_{MIN} to T_{MAX}			±1 ±1¼	LSB LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ 4.5V≤V_{CC}≤5.5V, −55°C≤T_A≤+125°C unless otherwise noted ADC0808CCJ, ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V, T_A=25°C T_{MIN} to T_{MAX}		10	200 1.0	nA μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0, T_A=25°C T_{MIN} to T_{MAX}	−200 −1.0	−10		nA μA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ 4.5V $\leq V_{CC} \leq$ 5.5V, $-55°C \leq T_A \leq +125°C$ unless otherwise noted ADC0808CCJ, ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75 $\leq V_{CC} \leq$ 5.25V, $-40°C \leq T_A \leq +85°C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN}=15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN}=0$	-1.0			μA
I_{CC}	Supply Current	$f_{CLK}=640$ kHz		0.3	3.0	mA
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=-360$ μA	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O=1.2$ mA			0.45	V
I_{OUT}	TRI-STATE Output Current	$V_O=5V$ $V_O=0$	 -3		3 	μA μA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S=0\Omega$ *(Figure 5)*		1	2.5	μS
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L=50$ pF, $R_L=10k$ *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L=10$ pF, $R_L=10k$ *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c=640$ kHz, *(Figure 5)* (Note 7)	90	100	116	μS
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8+2 μS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs, (Note 12)		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless othewise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0V_{DC} to 5V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

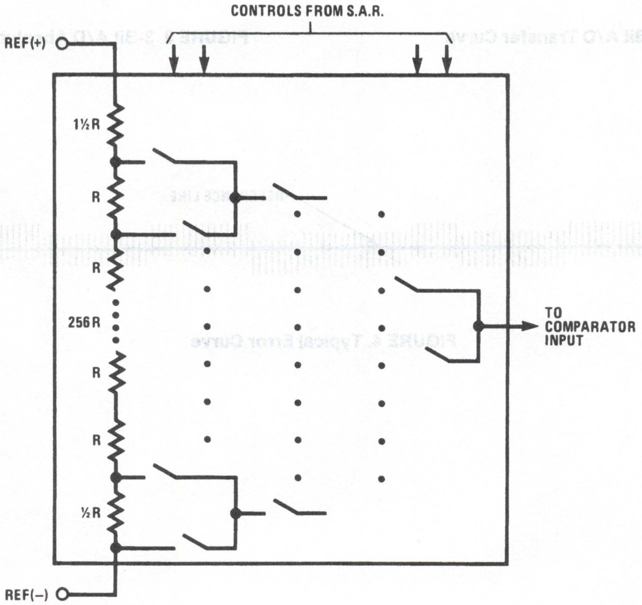


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed throught a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

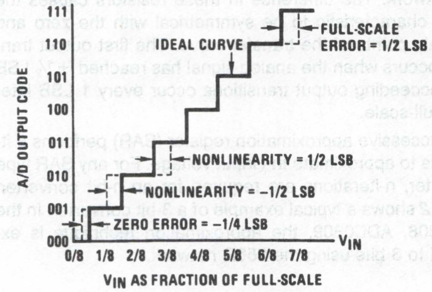


FIGURE 2. 3-Bit A/D Transfer Curve

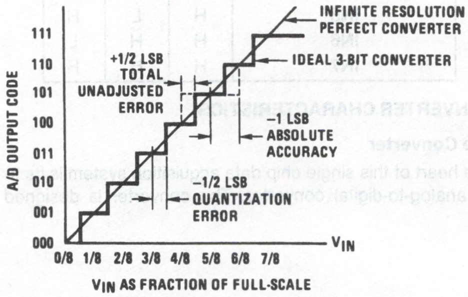
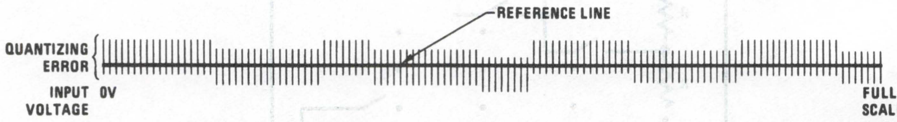


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

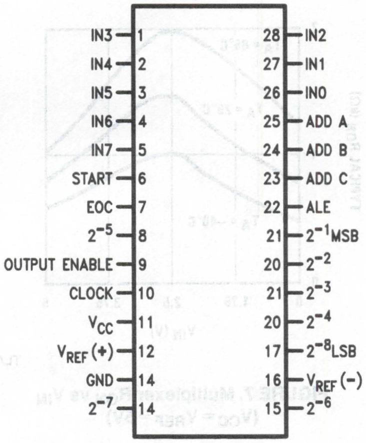


TL/H/5672-3

FIGURE 4. Typical Error Curve

Connection Diagrams

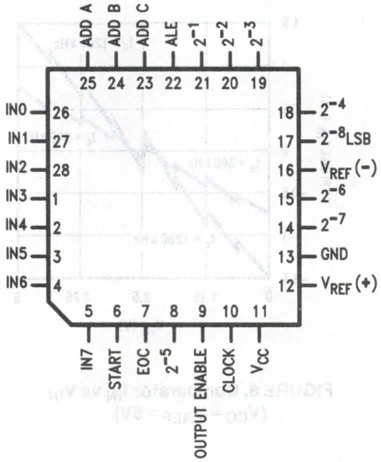
Dual-In-Line Package


IN3 1
IN4 2
IN5 3
IN6 4
IN7 5
START 6
EOC 7
2^{-5} 8
OUTPUT ENABLE 9
CLOCK 10
V_{CC} 11
$V_{REF}(+)$ 12
GND 14
2^{-7} 14
28 IN2
27 IN1
26 IN0
25 ADD A
24 ADD B
23 ADD C
22 ALE
21 2^{-1}MSB
20 2^{-2}
21 2^{-3}
20 2^{-4}
17 2^{-8}LSB
16 $V_{REF}(-)$
15 2^{-6}

TL/H/5672–11

Order Number ADC0808CCN, ADC0809CCN, ADC0808CCJ or ADC0808CJ
See NS Package J28A or N28A

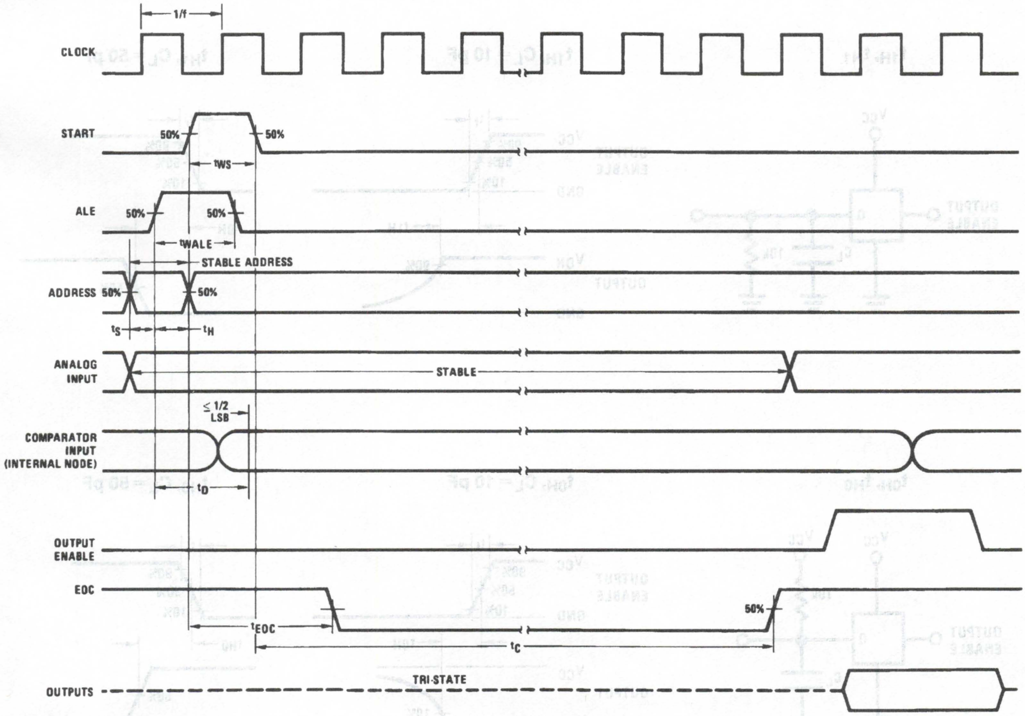
Molded Chip Carrier Package


ADD A 25
ADD B 24
ADD C 23
ALE 22
2^{-1} 21
2^{-2} 20
2^{-3} 19
IN0 26
IN1 27
IN2 28
IN3 1
IN4 2
IN5 3
IN6 4
18 2^{-4}
17 2^{-8}LSB
16 $V_{REF}(-)$
15 2^{-6}
14 2^{-7}
13 GND
12 $V_{REF}(+)$
5 IN7
6 START
7 EOC
8 2^{-5}
9 OUTPUT ENABLE
10 CLOCK
11 V_{CC}

TL/H/5672–12

Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Timing Diagram


1/f
CLOCK
START
50%
50%
t_{WS}
ALE
50%
50%
t_{WALE}
STABLE ADDRESS
ADDRESS
50%
50%
t_S
t_H
ANALOG INPUT
STABLE
≤ 1/2 LSB
COMPARATOR INPUT (INTERNAL NODE)
t_D
OUTPUT ENABLE
EOC
t_{EOC}
50%
t_C
OUTPUTS
TRI-STATE

TL/H/5672–4

FIGURE 5

Typical Performance Characteristics

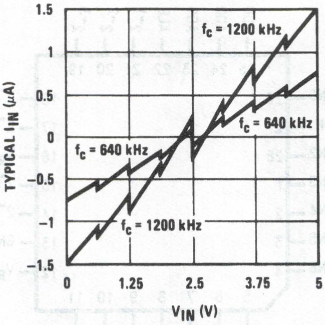
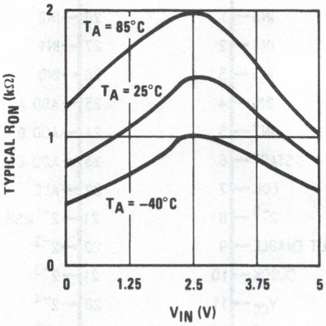


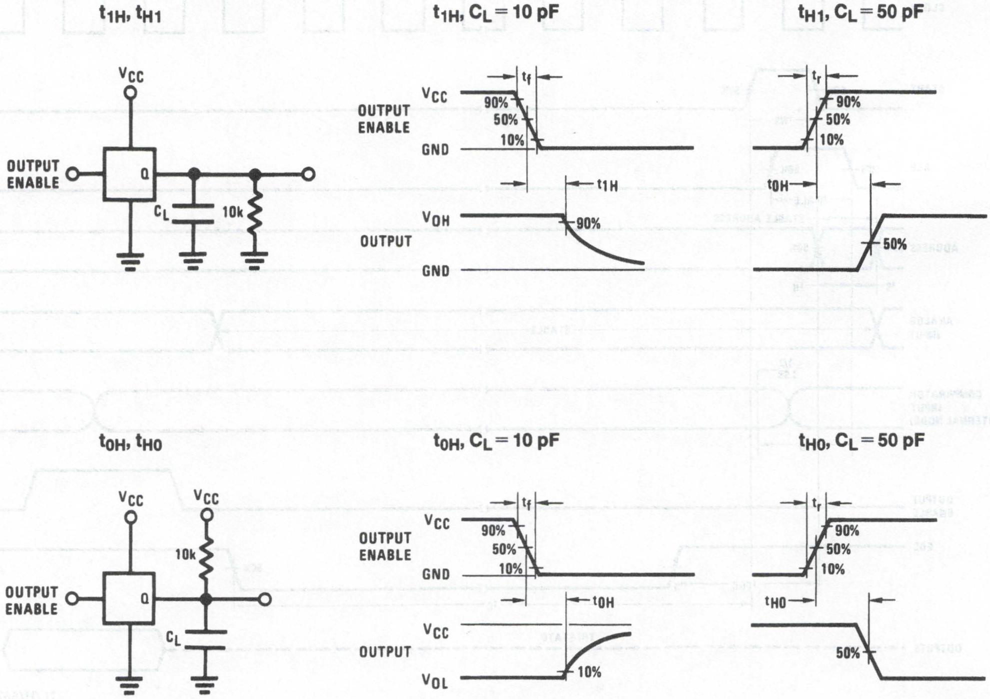
FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)



TL/H/5672–5

FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE Test Circuits and Timing Diagrams


t_{1H}, t_{H1}
V_{CC}
OUTPUT ENABLE
Q
C_L
10k
t_{1H}, C_L = 10 pF
t_f
V_{CC}
OUTPUT ENABLE
90%
50%
10%
GND
t_{1H}
V_{OH}
OUTPUT
90%
GND
t_{H1}, C_L = 50 pF
t_r
90%
50%
10%
t_{H1}
50%
t_{0H}, t_{H0}
V_{CC}
V_{CC}
10k
OUTPUT ENABLE
Q
C_L
t_{0H}, C_L = 10 pF
t_f
V_{CC}
OUTPUT ENABLE
90%
50%
10%
GND
t_{0H}
V_{CC}
OUTPUT
V_{OL}
10%
t_{H0}, C_L = 50 pF
t_r
90%
50%
10%
t_{H0}
50%

TL/H/5672–6

FIGURE 8

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \tag{1}$$

V_{IN} = Input voltage into the ADC0808

V_{fs} = Full-scale voltage

V_Z = Zero voltage

D_X = Data point being measured

D_{MAX} = Maximum data limit

D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 9)*.

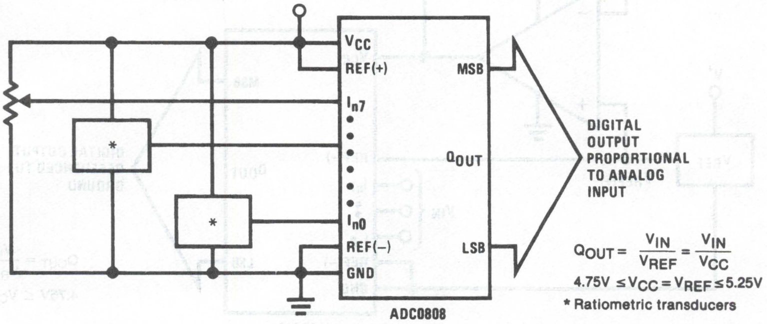
Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC}=V_{REF}=5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.


V_CC
REF(+)
I_n7
I_n0
REF(−)
GND
MSB
Q_OUT
LSB
ADC0808
*
*
DIGITAL OUTPUT PROPORTIONAL TO ANALOG INPUT
Q_OUT = V_IN/V_REF = V_IN/V_CC
4.75V ≤ V_CC = V_REF ≤ 5.25V
* Ratiometric transducers

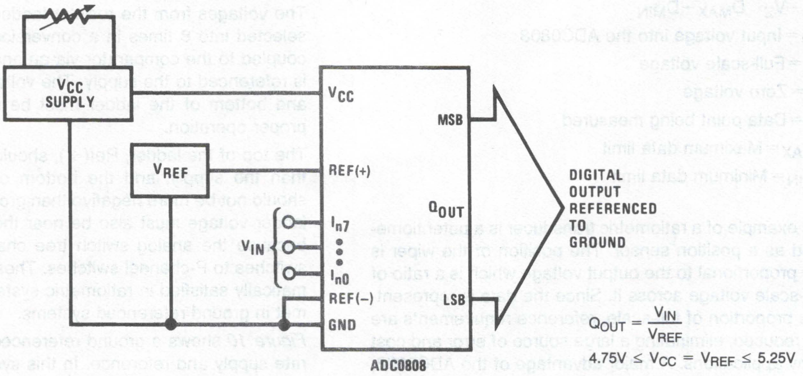
TL/H/5672–7

FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

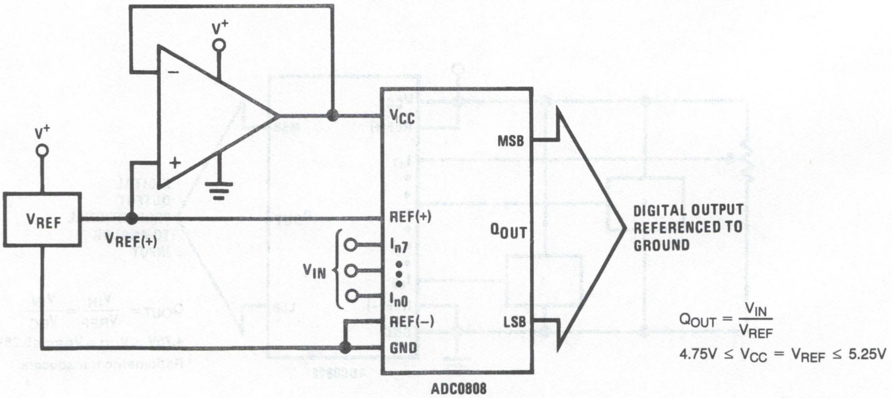
The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.


VCC SUPPLY
VREF
VCC
REF(+)
In7
VIN
In0
REF(−)
GND
MSB
QOUT
LSB
DIGITAL OUTPUT REFERENCED TO GROUND
ADC0808

$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$$4.75V \le V_{CC} = V_{REF} \le 5.25V$$

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply


V+
−
+
V+
VREF
VREF(+)
VCC
REF(+)
In7
VIN
In0
REF(−)
GND
MSB
QOUT
LSB
DIGITAL OUTPUT REFERENCED TO GROUND
ADC0808

$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$$4.75V \le V_{CC} = V_{REF} \le 5.25V$$

TL/H/5672-8

FIGURE 11: Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

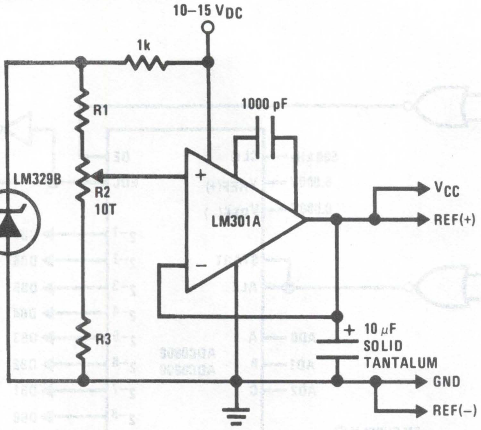
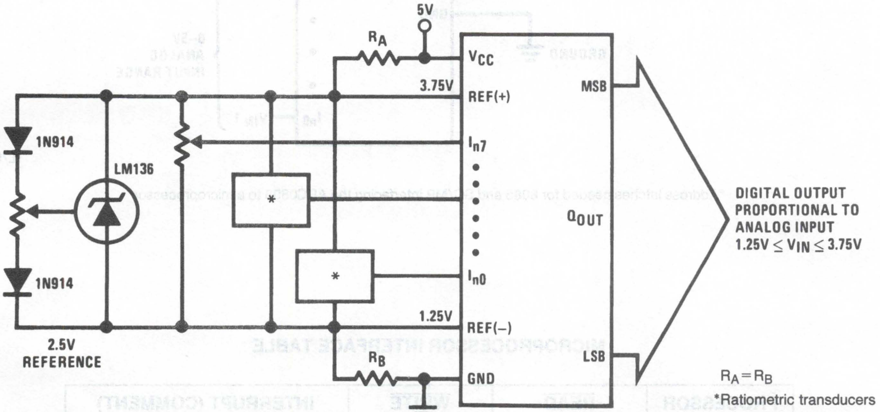

10–15 V_{DC}
1k
R1
1000 pF
LM329B
R2
10T
LM301A
V_{CC}
REF(+)
R3
+ 10 µF
SOLID
TANTALUM
GND
REF(−)

FIGURE 12. Typical Reference and Supply Circuit


5V
R_A
V_{CC}
3.75V
REF(+)
MSB
1N914
I_{n7}
LM136
*
Q_{OUT}
DIGITAL OUTPUT
PROPORTIONAL TO
ANALOG INPUT
1.25V ≤ V_{IN} ≤ 3.75V
1N914
*
I_{n0}
1.25V
REF(−)
2.5V
REFERENCE
LSB
R_B
GND
$R_A = R_B$
*Ratiometric transducers

TL/H/5672–9

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (2)$$

The center of an output code N is given by:

$$V_{IN} \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \qquad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(−)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

4.0 ANALOG COMPARATOR INPUTS

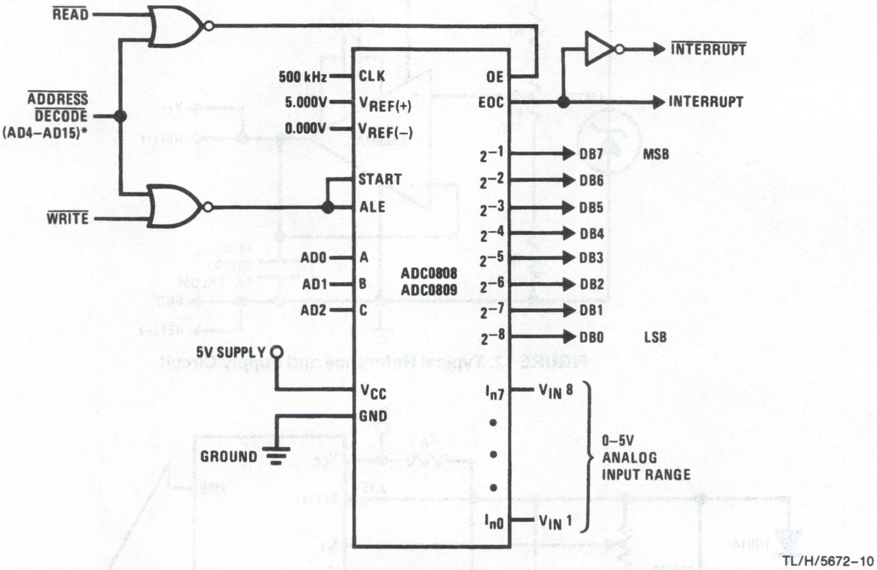
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application


$\overline{\text{READ}}$
$\overline{\text{ADDRESS DECODE}}$
(AD4–AD15)*
$\overline{\text{WRITE}}$
500 kHz
5.000V
0.000V
AD0
AD1
AD2
5V SUPPLY
GROUND
CLK
$V_{REF(+)}$
$V_{REF(-)}$
START
ALE
A
B
C
V_{CC}
GND
ADC0808
ADC0809
OE
EOC
2^{-1}
2^{-2}
2^{-3}
2^{-4}
2^{-5}
2^{-6}
2^{-7}
2^{-8}
I_{n7}
I_{n0}
$\overline{\text{INTERRUPT}}$
INTERRUPT
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
MSB
LSB
V_{IN} 8
V_{IN} 1
0–5V ANALOG INPUT RANGE
TL/H/5672-10

*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•ϕ2•R/W	VMA•ϕ•$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C			−55°C to +125°C
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP

National Semiconductor Corporation

ADC0811 8-Bit Serial I/O A/D Converter With 11-Channel Multiplexer

General Description

The ADC0811 is an 8-Bit successive approximation A/D converter with simultaneous serial I/O. The serial input controls an analog multiplexer which selects from 11 input channels or an internal half scale test voltage.

An input sample-and-hold is implemented by a capacitive reference ladder and sampled data comparator. This allows the input signal to vary during the conversion cycle.

Separate serial I/O and conversion clock inputs are provided to facilitate the interface to various microprocessors.

Features

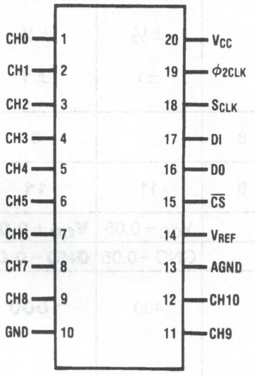
- Separate asynchronous converter clock and serial data I/O clock.
- 11-Channel multiplexer with 4-Bit serial address logic.
- Built-in sample and hold function.
- Ratiometric or absolute voltage referencing.
- No zero or full-scale adjust required.
- Internally addressable test voltage.
- 0V to 5V input range with single 5V power supply.
- TTL/MOS input/output compatible.
- 0.3″ standard width 20-pin dip or 20-pin molded chip carrier

Key Specifications

■ Resolution	8-Bits
■ Total unadjusted error	± ½LSB and ± 1LSB
■ Single supply	$5V_{DC}$
■ Low Power	15 mW
■ Conversion Time	32 μS

Connection Diagrams

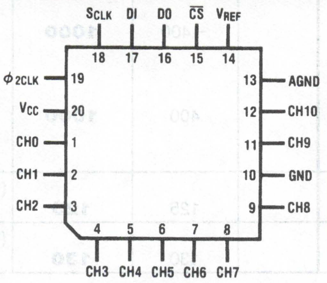
Dual-In-Line Package


CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
CH8 9
GND 10
20 VCC
19 φ2CLK
18 SCLK
17 DI
16 DO
15 CS
14 VREF
13 AGND
12 CH10
11 CH9

TL/H/5587–1

Top View

Molded Chip Carrier (PCC) Package

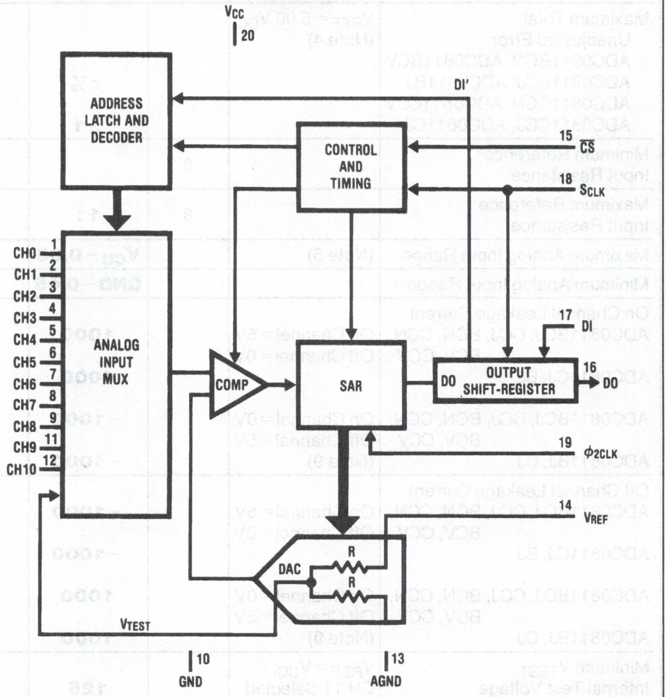

SCLK DI DO CS VREF
18 17 16 15 14
φ2CLK 19
VCC 20
CH0 1
CH1 2
CH2 3
13 AGND
12 CH10
11 CH9
10 GND
9 CH8
4 5 6 7 8
CH3 CH4 CH5 CH6 CH7

TL/H/5587–2

Top View

Order Number ADC0811J,N,V
See NS Packages J20A, N20A, V20A
Use Ordering Information

Functional Diagram


VCC
20
DI'
ADDRESS LATCH AND DECODER
CONTROL AND TIMING
15 CS
18 SCLK
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
CH8 9
CH9 11
CH10 12
ANALOG INPUT MUX
COMP
SAR
17 DI
DO
OUTPUT SHIFT-REGISTER
16 DO
19 φ2CLK
14 VREF
DAC
R
R
VTEST
10 GND
13 AGND

TL/H/5587–3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage	
Inputs and Outputs	$-0.3V$ to V_{CC} $+0.3V$
Input Current Per Pin (Note 3)	±5mA
Total Package Input Current (Note 3)	±20mA
Storage Temperature	$-65°C$ to $+150°C$
Package Dissipation at $T_A = 25°C$	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2000V

Operating Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0811BCN, ADC0811CCN	$0°C \le T_A \le 70°C$
ADC0811BCJ, ADC0811BCV	$-40°C \le T_A \le 85°C$
ADC0811CCJ, ADC0811CCV	$-40°C \le T_A \le 85°C$
ADC0811BJ, ADC0811CJ	$-55°C \le T_A \le 125°C$

Electrical Characteristics

The following specifications apply for V_{CC} = 4.75V to 5.25V, V_{REF} = +4.6V to (V_{CC} + 0.1V), $\phi_{2\ CLK}$ = 2.097 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	ADC0811BCJ, ADC0811BJ ADC0811CCJ, ADC0811CJ			ADC0811BCN, ADC0811BCV ADC0811CCN, ADC0811CCV			Units
		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Maximum Total Unadjusted Error	V_{REF} = 5.00 V_{DC} (Note 4)							
ADC0811BCN, ADC0811BCV						±½	**±½**	LSB
ADC0811BCJ, ADC0811BJ			**±½**					LSB
ADC0811CCN, ADC0811CCV						±1	**±1**	LSB
ADC0811CCJ, ADC0811CJ			**±1**					LSB
Minimum Reference Input Resistance		8		**5**	8		**5**	kΩ
Maximum Reference Input Resistance		8	**11**		8	11	**11**	kΩ
Maximum Analog Input Range	(Note 5)		**V_{CC}+0.05**			V_{CC}+0.05	**V_{CC}+0.05**	V
Minimum Analog Input Range			**GND−0.05**			GND−0.05	**GND−0.05**	V
On Channel Leakage Current								
ADC0811BCJ, CCJ, BCN, CCN, BCV, CCV	On Channel = 5V Off Channel = 0V		**1000**			400	**1000**	nA
ADC0811CJ, BJ			**1000**					nA
ADC0811BCJ, CCJ, BCN, CCN, BCV, CCV	On Channel = 0V Off Channel = 5V		**−1000**			−400	**−1000**	nA
ADC0811BJ, CJ	(Note 9)		**−1000**					nA
Off Channel Leakage Current								
ADC0811BCJ, CCJ, BCN, CCN, BCV, CCV	On Channel = 5V Off Channel = 0V		**−1000**			−400	**1000**	nA
ADC0811CJ, BJ			**−1000**					nA
ADC0811BCJ, CCJ, BCN, CCN, BCV, CCV	On Channel = 0V Off Channel = 5V		**1000**			400	**1000**	nA
ADC0811BJ, CJ	(Note 9)		**1000**					nA
Minimum V_{TEST} Internal Test Voltage	$V_{REF} = V_{CC}$, CH 11 Selected		**125**			125	**125**	(Note 10) Counts
Maximum V_{TEST} Internal Test Voltage	$V_{REF} = V_{CC}$, CH 11 Selected		**130**			130	**130**	(Note 10) Counts

Electrical Characteristics

The following specifications apply for $V_{CC} = 4.75V$ to $5.25V$, $V_{REF} = +4.6V$ to $(V_{CC} + 0.1V)$, $\phi_{2\ CLK} = 2.097$ MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Continued)

Parameter	Conditions	ADC0811BCJ, ADC0811BJ ADC0811CCJ, ADC0811CJ Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	ADC0811BCN, ADC0811BCV ADC0811CCN, ADC0811CCV Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	$V_{CC} = 5.25V$		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	$V_{CC} = 4.75V$		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	$V_{IN} = 5.0V$	0.005	**2.5**		0.005	2.5	**2.5**	µA
$I_{IN(0)}$, Logical "0" Input Current (Max)	$V_{IN} = 0V$	−0.005	**−2.5**		−0.005	2.5	**−2.5**	µA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	$V_{CC} = 4.75V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **4.5**			2.4 4.5	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	$V_{CC} = 5.25V$ $I_{OUT} = 1.6$ mA		**0.4**			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−0.01 0.01	**−3** **3**		−0.01 0.01	−3 3	**−3** **3**	µA µA
I_{SOURCE}, Output Source Current (Min)	$V_{OUT} = 0V$	−12	**−6.5**		−14	−6.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)	$V_{OUT} = V_{CC}$	18	**8.0**		16	8.0	**8.0**	mA
I_{CC}, Supply Current (Max)	$\overline{CS} = 1$, V_{REF} Open	1	**2.5**		1	2.5	**2.5**	mA
I_{REF} (Max)	$V_{REF} = 5V$	**0.7**	**1**		**0.7**	1	**1**	mA

AC CHARACTERISTICS

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
$\phi_{2\ CLK}$, ϕ_2 Clock Frequency	MIN		0.70		**1.0**	MHz
	MAX		3.0	2.0	**2.1**	
S_{CLK}, Serial Data Clock Frequency	MIN				**5.0**	KHz
	MAX		700	525	**525**	
T_C, Conversion Process Time	MIN	Not Including MUX Addressing and Analog Input Sampling Times	48		**48**	ϕ_2 cycles
	MAX		64		**64**	
t_{ACC}, Access Time Delay From $\overline{CS}$ Falling Edge to DO Data Valid	MIN				**1**	ϕ_2 cycles
	MAX				**3**	
$t_{SET\text{-}UP}$, Minimum Set-up Time of $\overline{CS}$ Falling Edge to S_{CLK} Rising Edge					$\mathbf{4/\phi_{2CLK} + \frac{1}{2\ S_{CLK}}}$	sec
$t_{H\overline{CS}}$, $\overline{CS}$ Hold Time After the Falling Edge of S_{CLK}					**0**	ns
$t_{\overline{CS}}$, Total $\overline{CS}$ Low Time	MIN				$\mathbf{t_{set\text{-}up} + 8/S_{CLK}}$	sec
	MAX				$\mathbf{t_{\overline{CS}}(min) + 48/\phi_{2CLK}}$	sec
t_{HDI}, Minimum DI Hold Time from S_{CLK} Rising Edge			0		**0**	ns
t_{HDO}, Minimum DO Hold Time from S_{CLK} Falling Edge		$R_L = 30k$, $C_L = 100$ pF			**10**	ns

Electrical Characteristics

The following specifications apply for V_{CC} = 4.75V to 5.25V, V_{REF} = +4.6V to (V_{CC} + 0.1V), $\phi_{2\ CLK}$ = 2.097 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J$ = 25°C. (Continued)

Parameter	Conditions		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
AC CHARACTERISTICS (Continued)						
t_{SDI}, Minimum DI Set-up Time to S_{CLK} Rising Edge			200		**400**	ns
t_{DDO}, Maximum Delay From S_{CLK} Falling Edge to DO Data Valid	R_L = 30k, C_L = 100 pF		180	400	**400**	ns
t_{TRI}, Maximum DO Hold Time, ($\overline{CS}$ Rising edge to DO TRI-STATE)	R_L = 3k, C_L = 100 pF		90	150	**150**	ns
t_{CA}, Analog Sampling Time	After Address Is Latched $\overline{CS}$ = Low				**4/S_{CLK} + 1 µs**	sec
t_{RDO}, Maximum DO Rise Time	R_L = 30 kΩ, C_L = 100 pf	"TRI-STATE" to "HIGH" State	75	150	**150**	ns
		"LOW" to "HIGH" State	150	300	**300**	
t_{FDO}, Maximum DO Fall Time	R_L = 30 kΩ, C_L = 100 pf	"TRI-STATE" to "LOW" State	75	150	**150**	ns
		"HIGH" to "LOW" State	150	300	**300**	
C_{IN}, Maximum Input Capacitance	Analog Inputs, ANO–AN10 and V_{REF}		11		**55**	pF
	All Others		5		**15**	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Under over voltage conditions (V_{IN}<0V and V_{IN}>V_{CC}) the maximum input current at any one pin is ±5 mA. If the voltage at more than one pin exceeds V_{CC} + .3V the total package current must be limited to 20 mA. For example the maximum number of pins that can be over driven at the maximum current level of ±5 mA is four.

Note 4: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 5: Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Guaranteed and 100% production tested under worst case condition.

Note 8: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

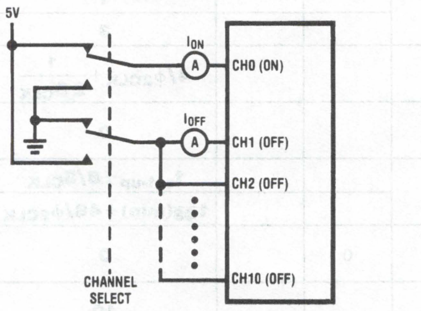
Note 9: Channel leakage current is measured after the channel selection.

Note 10: 1 count = V_{REF}/256.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Test Circuits

Leakage Current



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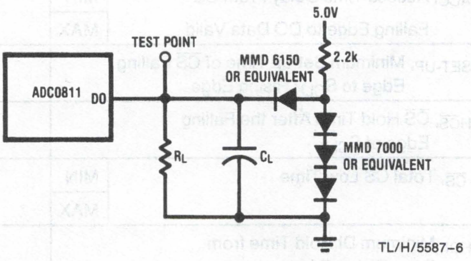
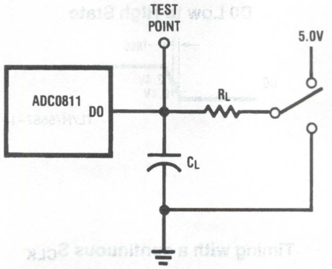
D0 Except "TRI-STATE"



TL/H/5587-6

Test Circuits (Continued)

t_{TRI} "TRI-STATE"



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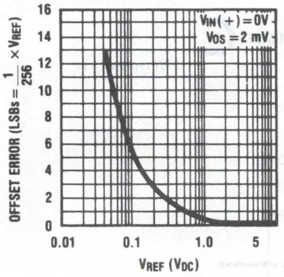
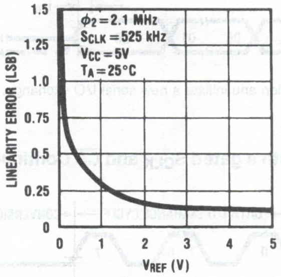
Typical Performance Characteristics

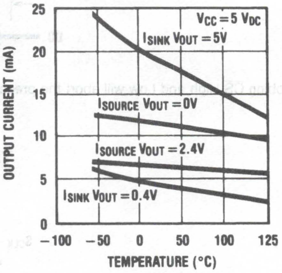
Unadjusted Offset Error vs V_{REF} Voltage



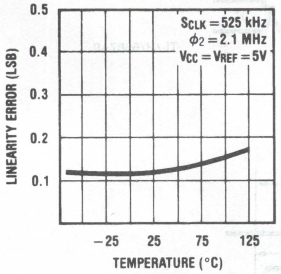
Linearity Error vs V_{REF} Voltage



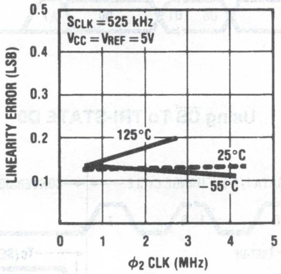
Output Current vs Temperature



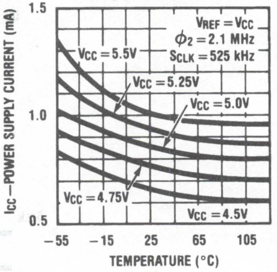
Linearity vs Temperature



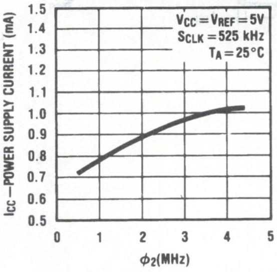
Linearity vs ϕ_2 Clock Frequency



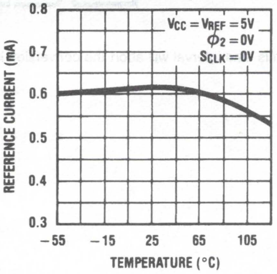
Power Supply Current vs Temperature



Power Supply Current vs ϕ_2 Clock Frequency



Resistive Ladder Reference Current vs Temperature



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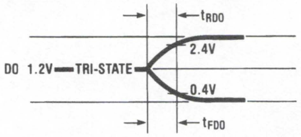
Timing Diagrams

D0 "TRI-STATE" Rise & Fall Times


t_{RDO}
2.4V
D0 1.2V — TRI-STATE
0.4V
t_{FDO}

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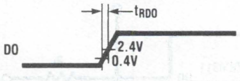
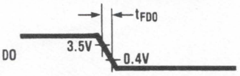
D0 Low to High State


t_{RDO}
D0
2.4V
0.4V

TL/H/5587-14

D0 High to Low State


t_{FDO}
D0
3.5V
0.4V

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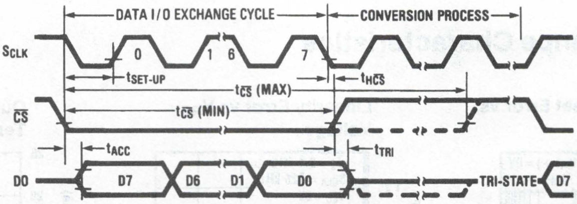
Timing with a continuous S_{CLK}


DATA I/O EXCHANGE CYCLE
CONVERSION PROCESS
S_{CLK}
0
1
6
7
t_{SET-UP}
$t_{H\overline{CS}}$
$t_{\overline{CS}}$ (MAX)
$\overline{CS}$
$t_{\overline{CS}}$ (MIN)
t_{ACC}
t_{TRI}
D0
D7
D6
D1
D0
TRI-STATE
D7

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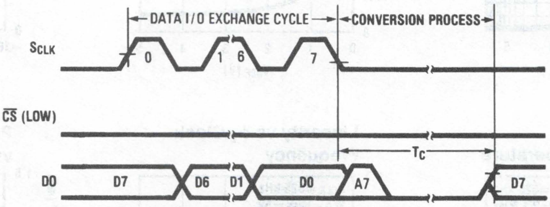
*Strobing $\overline{CS}$ High and Low will abort the present conversion and initiate a new serial I/O exchange.

Timing with a gated S_{CLK} and $\overline{CS}$ Continuously Low


DATA I/O EXCHANGE CYCLE
CONVERSION PROCESS
S_{CLK}
0
1
6
7
$\overline{CS}$ (LOW)
T_C
D0
D7
D6
D1
D0
A7
D7

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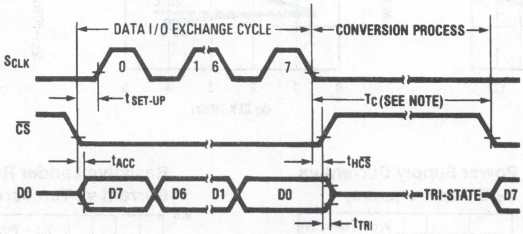
Using $\overline{CS}$ To TRI-STATE D0


DATA I/O EXCHANGE CYCLE
CONVERSION PROCESS
S_{CLK}
0
1
6
7
t_{SET-UP}
T_C (SEE NOTE)
$\overline{CS}$
t_{ACC}
$t_{H\overline{CS}}$
D0
D7
D6
D1
D0
TRI-STATE
D7
t_{TRI}

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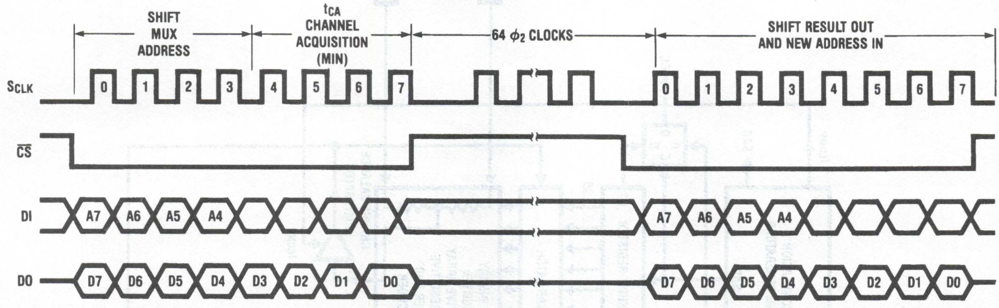
Note: Strobing $\overline{CS}$ Low during this time interval will abort the conversion in process.

Timing Diagrams (Continued)

$\overline{CS}$ High During Conversion


SHIFT MUX ADDRESS
t_{CA} CHANNEL ACQUISITION (MIN)
64 ϕ_2 CLOCKS
SHIFT RESULT OUT AND NEW ADDRESS IN
S_{CLK}
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7
$\overline{CS}$
DI
A7 A6 A5 A4
A7 A6 A5 A4
DO
D7 D6 D5 D4 D3 D2 D1 D0
D7 D6 D5 D4 D3 D2 D1 D0

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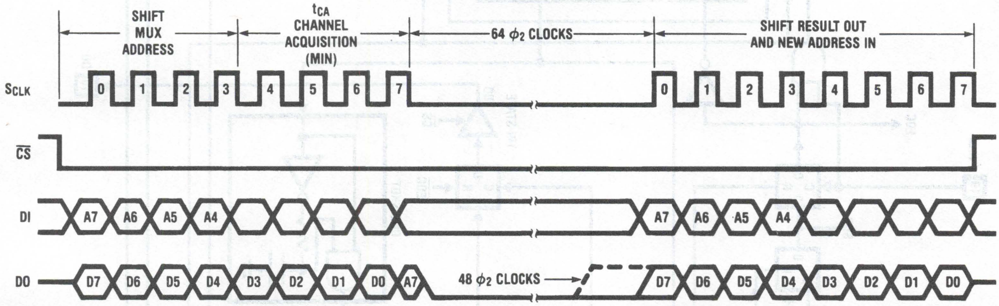
$\overline{CS}$ Low During Conversion


SHIFT MUX ADDRESS
t_{CA} CHANNEL ACQUISITION (MIN)
64 ϕ_2 CLOCKS
SHIFT RESULT OUT AND NEW ADDRESS IN
S_{CLK}
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7
$\overline{CS}$
DI
A7 A6 A5 A4
A7 A6 A5 A4
DO
D7 D6 D5 D4 D3 D2 D1 D0 A7
48 ϕ_2 CLOCKS
D7 D6 D5 D4 D3 D2 D1 D0

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Note: DO and DI lines share the 8-bit I/O shift register(see Functional Block Diagram). Since the MUX address bits are shifted in on S_{CLK} rising edges while S_{CLK} falling edges shift out conversion data on DO, the eighth falling edge of S_{CLK} will shift out the MSB MUX address bit (A7) on DO. Thus, if addressing channels CH8–CH10, a high DO will occur momentarily (one ϕ_2 clock period) until the 8-bit I/O shift register is cleared by the internal EOC signal.

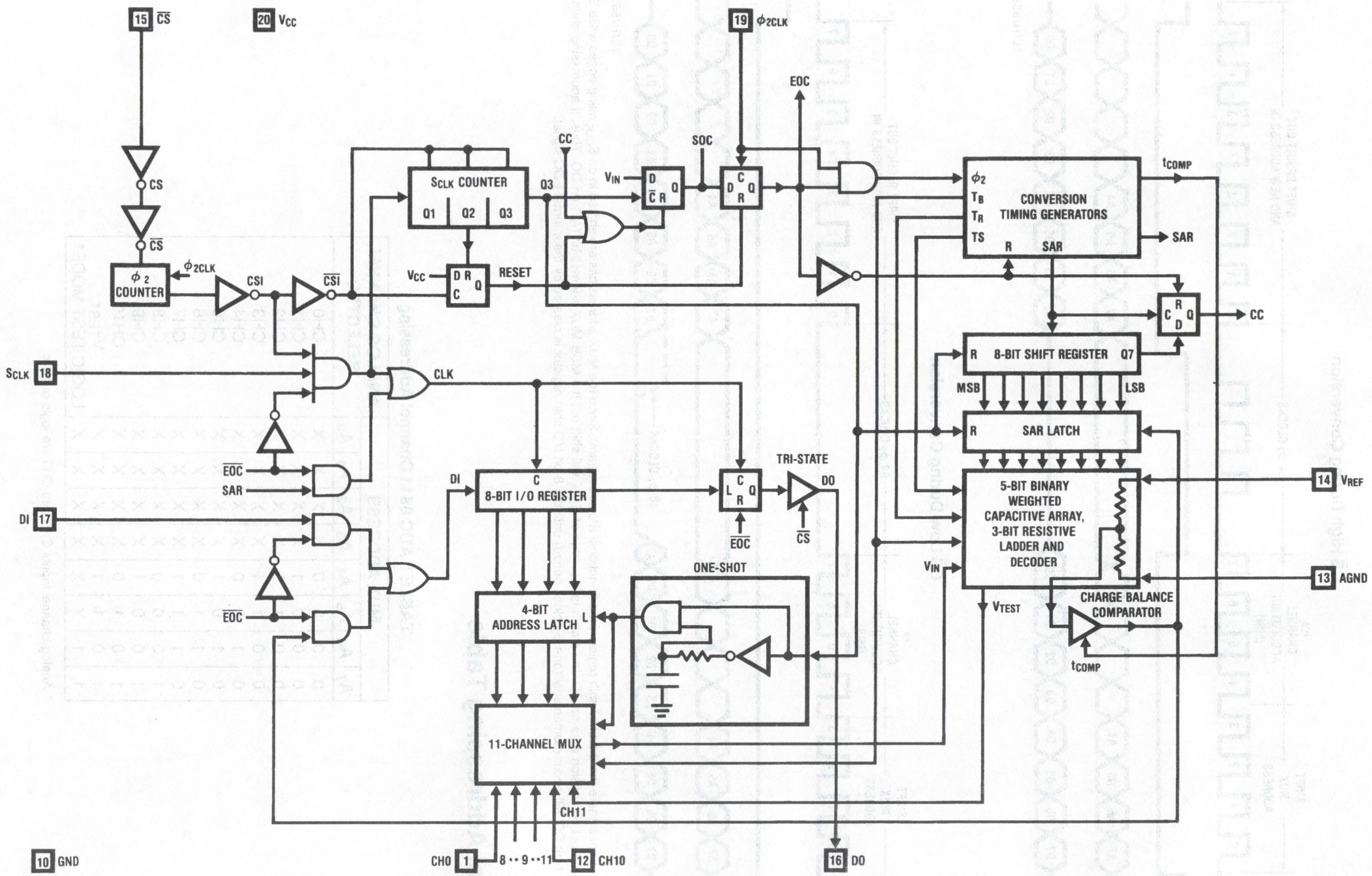
Channel Addressing Table

TABLE I. ADC 0811 Channel Addressing

MUX ADDRESS								ANALOG CHANNEL SELECTED
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	0	0	0	X	X	X	X	CH0
0	0	0	1	X	X	X	X	CH1
0	0	1	0	X	X	X	X	CH2
0	0	1	1	X	X	X	X	CH3
0	1	0	0	X	X	X	X	CH4
0	1	0	1	X	X	X	X	CH5
0	1	1	0	X	X	X	X	CH6
0	1	1	1	X	X	X	X	CH7
1	0	0	0	X	X	X	X	CH8
1	0	0	1	X	X	X	X	CH9
1	0	1	0	X	X	X	X	CH10
1	0	1	1	X	X	X	X	V_{TEST}
1	1	X	X	X	X	X	X	LOGIC TEST MODE*

* Analog channel inputs CH0 thru CH3 are logic outputs

Functional Block Diagram


15 CS
20 VCC
19 φ2CLK
CS
CS
φ2 COUNTER
φ2CLK
CSI
CSI
SCLK COUNTER
Q1 Q2 Q3
Q3
CC
VIN
D
C R
Q
SOC
C
D Q
R
EOC
VCC
D R
C Q
RESET
φ2
TB
TR
TS
CONVERSION TIMING GENERATORS
R SAR
tCOMP
SAR
R
C Q
D
CC
R 8-BIT SHIFT REGISTER Q7
MSB
LSB
R SAR LATCH
SCLK 18
CLK
EOC
SAR
DI 17
EOC
DI
C
8-BIT I/O REGISTER
C
L Q
R
EOC
TRI-STATE
DO
CS
4-BIT ADDRESS LATCH
L
ONE-SHOT
5-BIT BINARY WEIGHTED CAPACITIVE ARRAY, 3-BIT RESISTIVE LADDER AND DECODER
VIN
VTEST
CHARGE BALANCE COMPARATOR
tCOMP
14 VREF
13 AGND
11-CHANNEL MUX
CH11
10 GND
CH0 1
8 ·· 9 ·· 11
12 CH10
16 DO

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Functional Description

1.0 DIGITAL INTERFACE

The ADC0811 uses five input/output pins to implement the serial interface. Taking chip select ($\overline{CS}$) low enables the I/O data lines (DO and DI) and the serial clock input (S_{CLK}). The result of the last conversion is transmitted by the A/D on the DO line, while simultaneously the DI line receives the address data that selects the mux channel for the next conversion. The mux address is shifted in on the rising edge of S_{CLK} and the conversion data is shifted out on the falling edge. It takes eight S_{CLK} cycles to complete the serial I/O. A second clock (ϕ_2) controls the SAR during the conversion process and must be continuously enabled.

1.1 CONTINUOUS S_{CLK}

With a continuous S_{CLK} input $\overline{CS}$ must be used to synchronize the serial data exchange (see *Figure 1*). The ADC0811 recognizes a valid $\overline{CS}$ one to three ϕ_2 clock periods after the actual falling edge of $\overline{CS}$. This is implemented to ensure noise immunity of the $\overline{CS}$ signal. Any spikes on $\overline{CS}$ less than one ϕ_2 clock period will be ignored. $\overline{CS}$ must remain low during the complete I/O exchange which takes eight S_{CLK} cycles. Although $\overline{CS}$ is not immediately acknowledged for the purpose of starting a new conversion, the falling edge of $\overline{CS}$ immediately enables DO to output the MSB (D7) of the previous conversion.

The first S_{CLK} rising edge will be acknowledged after a setup time (t_{set-up}) has elapsed from the falling edge of $\overline{CS}$. This and the following seven S_{CLK} rising edges will shift in the channel address for the analog multiplexer. Since there are 12 channels only four address bits are utilized. The first four S_{CLK} cycles clock in the mux address, during the next four S_{CLK} cycles the analog input is selected and sampled. During this mux address/sample cycle, data from the last conversion is also clocked out on DO. Since D7 was clocked out on the falling edge of $\overline{CS}$ only data bits D6–D0 remain to be received. The following seven falling edges of S_{CLK} shift out this data on DO.

The 8th S_{CLK} falling edge initiates the beginning of the A/D's actual conversion process which takes between 48 to 64 ϕ_2 cycles (T_C). During this time $\overline{CS}$ can go high to TRI-STATE DO and disable the S_{CLK} input or it can remain low. If $\overline{CS}$ is held low a new I/O exchange will not start until the conversion sequence has been completed, however once the conversion ends serial I/O will immediately begin. Since there is an ambiguity in the conversion time (T_C) synchronizing the data exchange is impossible. Therefore $\overline{CS}$ should go high before the 48th ϕ_2 clock has elasped and return low after the 64th ϕ_2 to synchronize serial communication.

A conversion or I/O operation can be aborted at any time by strobing $\overline{CS}$. If $\overline{CS}$ is high or low less than one ϕ_2 clock it will be ignored by the A/D. If the $\overline{CS}$ is strobed high or low between 1 to 3 ϕ_2 clocks the A/D may or may not respond. Therefore $\overline{CS}$ must be strobed high or low greater than 3 ϕ_2 clocks to ensure recognition. If a conversion or I/O exchange is aborted while in process the consequent data output will be erroneous until a complete conversion sequence has been implemented.

1.2 DISCONTINUOUS S_{CLK}

Another way to accomplish synchronous serial communication is to tie $\overline{CS}$ low continuously and disable S_{CLK} after its 8th falling edge (see *Figure 2*). S_{CLK} must remain low for

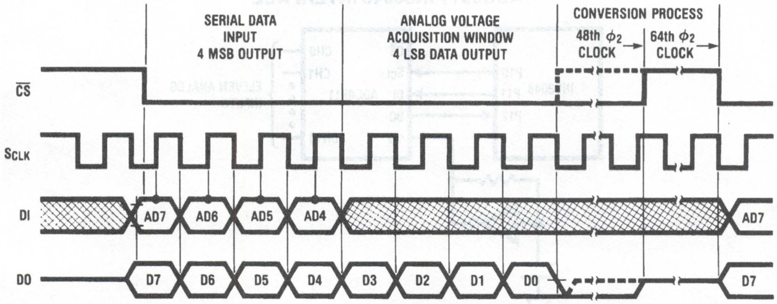
SERIAL DATA INPUT 4 MSB OUTPUT
ANALOG VOLTAGE ACQUISITION WINDOW 4 LSB DATA OUTPUT
CONVERSION PROCESS
48th ϕ_2 CLOCK
64th ϕ_2 CLOCK
$\overline{CS}$
S_{CLK}
DI
AD7
AD6
AD5
AD4
AD7
DO
D7
D6
D5
D4
D3
D2
D1
D0
D7

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FIGURE 1

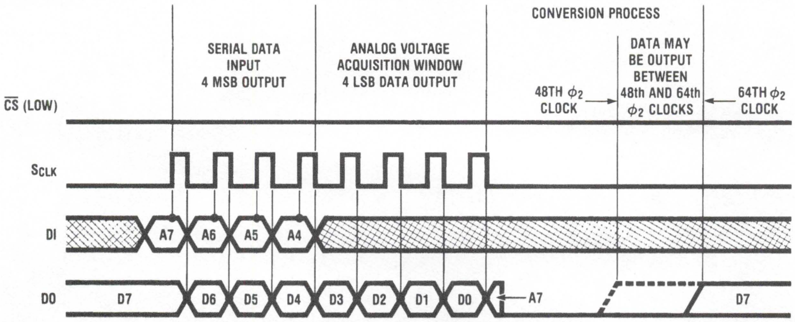
SERIAL DATA INPUT 4 MSB OUTPUT
ANALOG VOLTAGE ACQUISITION WINDOW 4 LSB DATA OUTPUT
CONVERSION PROCESS
DATA MAY BE OUTPUT BETWEEN 48th AND 64th ϕ_2 CLOCKS
48TH ϕ_2 CLOCK
64TH ϕ_2 CLOCK
$\overline{CS}$ (LOW)
S_{CLK}
DI
A7
A6
A5
A4
DO
D7
D6
D5
D4
D3
D2
D1
D0
A7
D7

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FIGURE 2

Functional Description (Continued)

at least 64 ϕ_2 clocks to insure that the A/D has completed its conversion. If S_{CLK} is enabled sooner, synchronizing to the data output on DO is not possible since an end of conversion signal from the A/D is not available and the actual conversion time is not known. With $\overline{CS}$ low during the conversion time (64 ϕ_2 max) DO will go low after the eighth falling edge of S_{CLK} and remain low until the conversion is completed. Once the conversion is through DO will transmit the MSB. The rest of the data will be shifted out once S_{CLK} is enabled as discussed previously.

If $\overline{CS}$ goes high during the conversion sequence DO is tri-stated, and the result is not affected so long as $\overline{CS}$ remains high until the end of the conversion.

1.2 MULTIPLEXER ADDRESSING

The four bit mux address is shifted, MSB first, into DI. Input data corresponds to the channel selected as shown in table 1. Care should be taken not to send an address greater than or equal to twelve (11XX) as this puts the A/D in a digital testing mode. In this mode the analog inputs CH0 thru CH3 become digital outputs, for our use in production testing.

2.0 ANALOG INPUT

2.1 THE INPUT SAMPLE AND HOLD

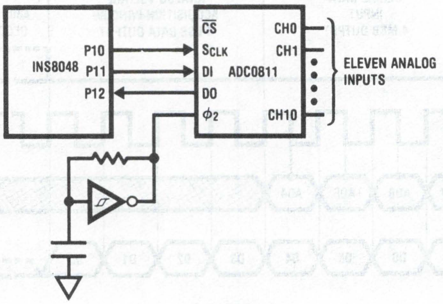
The ADC0811's sample/hold capacitor is implemented in its capacitive ladder structure. After the channel address is received, the ladder is switched to sample the proper analog input. This sampling mode is maintained for 1 μsec after the eighth S_{CLK} falling edge. The hold mode is initiated with the start of the conversion process. An acquisition window of $4t_{S_{CLK}} + 1$ μsec is therefore available to allow the ladder capacitance to settle to the analog input voltage. Any change in the analog voltage before or after the acquisition window will not effect the A/D conversion result.

In the most simple case, the ladder's acquisition time is determined by the R_{on} (3K) of the multiplexer switches and the total ladder capacitance (90pf). These values yield an acquisition time of about 2 μsec for a full scale reading. Therefore the analog input must be stable for at least 2 μsec before and 1 μsec after the eighth S_{CLK} falling edge to ensure a proper conversion. External input source resistance and capacitance will lengthen the acquisition time and should be accounted for.

Other conventional sample and hold error specifications are included in the error and timing specs of the A/D. The hold step and gain error sample/hold specs are taken into account in the ADC0811's total unadjusted error, while the hold settling time is included in the A/D's max conversion time of 64 ϕ_2 clock periods. The hold droop rate can be thought of as being zero since an unlimited amount of time can pass between a conversion and the reading of data. However, once the data is read it is lost and another conversion is started.

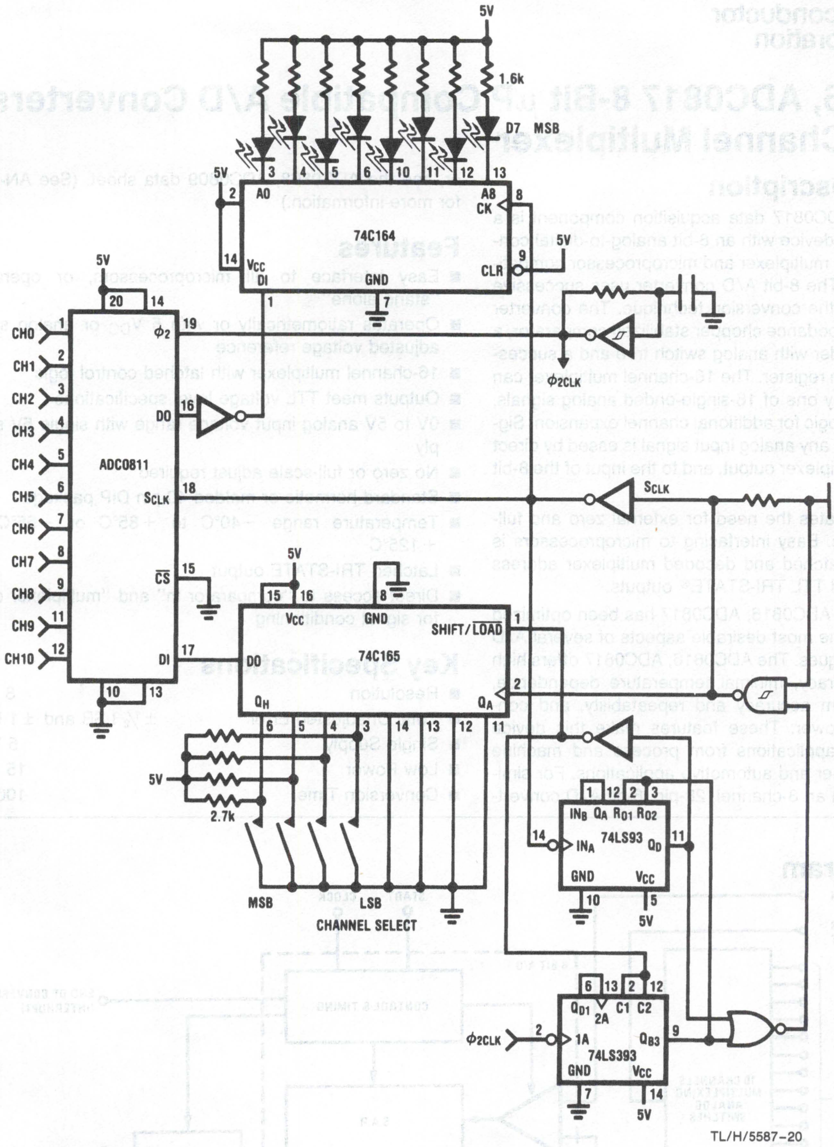
Typical Applications

ADC0811-INS8048 INTERFACE



TL/H/5587-21

ADC0811 FUNCTIONAL CIRCUIT


5V
1.6k
D7
MSB
3
4
5
6
10
11
12
13
5V
2
A0
A8
CK
8
74C164
14
VCC
DI
GND
7
1
5V
9
CLR
5V
20
14
19
φ2
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
CH9
CH10
ADC0811
DO
16
SCLK
18
CS
15
DI
17
10
13
φ2CLK
SCLK
5V
15
16
VCC
GND
SHIFT/LOAD
DO
74C165
QH
QA
6
5
4
3
14
13
12
11
5V
2.7k
MSB
LSB
START
CLOCK
CHANNEL SELECT
INB
QA
R01
R02
74LS93
INA
QD
GND
VCC
10
5
5V
QD1
2A
C1
C2
φ2CLK
1A
QB3
74LS393
GND
VCC
7
14
5V
9

TL/H/5587-20

Ordering Information

Temperature Range		0°C to 70°C	−40°C to +85°C	−55°C to +125°C
Total Unadjusted Error	±½ LSB	ADC0811BCN	ADC0811BCJ ADC0811BCV	ADC0811BJ
	±1 LSB	ADC0811CCN	ADC0811CCJ ADC0811CCV	ADC0811CJ
Package Outline		N20A	J20A, V20A	J20A

National
Semiconductor
Corporation

ADC0816, ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet. (See AN-258 for more information.)

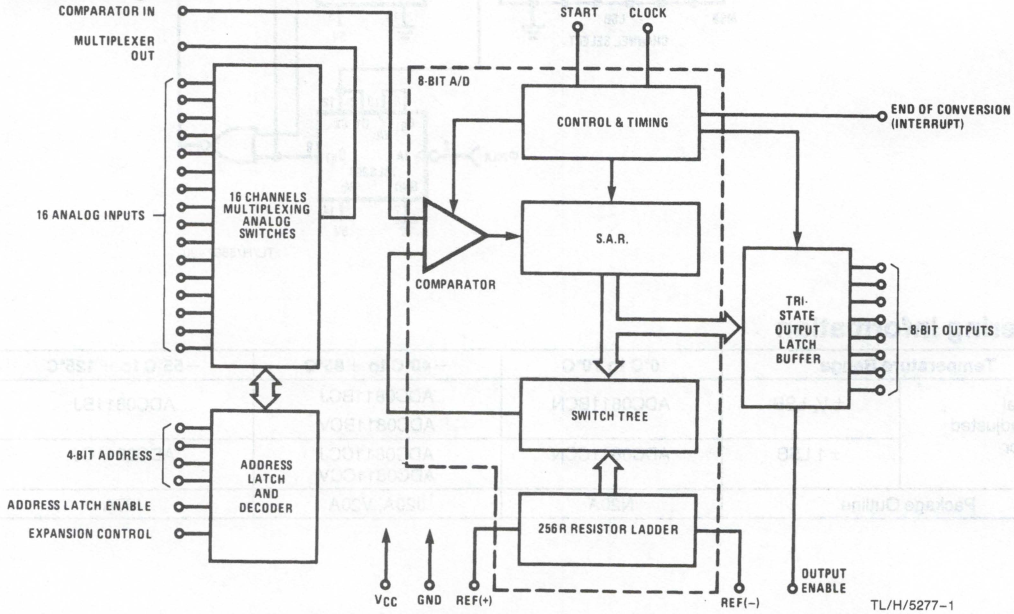
Features

- Easy interface to all microprocessors, or operates "stand alone"
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Outputs meet TTL voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Latched TRI-STATE output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 μs

Block Diagram


COMPARATOR IN
MULTIPLEXER OUT
16 ANALOG INPUTS
16 CHANNELS MULTIPLEXING ANALOG SWITCHES
4-BIT ADDRESS
ADDRESS LATCH ENABLE
EXPANSION CONTROL
ADDRESS LATCH AND DECODER
8-BIT A/D
START
CLOCK
CONTROL & TIMING
END OF CONVERSION (INTERRUPT)
S.A.R.
COMPARATOR
TRI-STATE OUTPUT LATCH BUFFER
8-BIT OUTPUTS
SWITCH TREE
256R RESISTOR LADDER
V_{CC}
GND
REF(+)
REF(−)
OUTPUT ENABLE

TL/H/5277-1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC}+0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	−0.3V to 15V
Storage Temperature Range	−65°C to + 150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
ESD Susceptibility (Note 9)	400V

Operating Conditions (Notes 1 & 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0816CJ	$-55°C \le T_A \le +125°C$
ADC0816CCJ, ADC0816CCN, ADC0817CCN	$-40°C \le T_A \le +85°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}
Voltage at Any Pin Except Control Inputs	0V to V_{CC}
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	0V to 15V

Electrical Characteristics

Converter Specifications: V_{CC} = 5 V_{DC} = $V_{REF(+)}$, $V_{REF(-)}$ = GND, V_{IN} = $V_{COMPARATOR\ IN}$, $T_{MIN} \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0816 Total Unadjusted Error (Note 5)	25°C T_{MIN} to T_{MAX}			±½ ±¾	LSB LSB
	ADC0817 Total Unadjusted Error (Note 5)	0°C to 70°C T_{MIN} to T_{MAX}			±1 ±1¼	LSB LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	4.5		kΩ
	Analog Input Voltage Range	(Note 4)V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2−0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	µA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0816CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN $4.75V \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel) T_A=25°C, R_L=10k T_A=85°C T_A=125°C		1.5	3 6 9	kΩ kΩ kΩ
ΔR_{ON}	ΔON Resistance Between Any 2 Channels	(Any Selected Channel) R_L=10k		75		Ω
I_{OFF+}	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V, T_A=25°C T_{MIN} to T_{MAX}		10	200 1.0	nA µA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0, T_A=25°C T_{MIN} to T_{Max}	−200 −1.0			nA µA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0816CJ—4.5V≤V_{CC}≤5.5V, −55°C≤T_A≤+125°C unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN—4.75V≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS (Continued)						
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN}=15V$			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN}=0$	−1.0			µA
I_{CC}	Supply Current	$f_{CLK}=640$ kHz		0.3	3.0	mA
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O-360 µA, $T_A=85°C$ $I_O=-300$ µA, $T_A=125°C$	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O=1.2$ mA			0.45	V
I_{OUT}	TRI-STATE Output Current	$V_O=V_{CC}$			3.0	µA
		$V_O=0$	−3.0			µA

Electrical Characteristics

Timing Specifications: $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)* (Note 7)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
T_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time from ALE	$R_S=0\Omega$ *(Figure 5)*		1	2.5	µS
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L=50$ pF, $R_L=10k$ *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L=10$ pF, $R_L=10k$ *(Figure 8)*		125	250	ns
t_C	Conversion Time	$f_c=640$ kHz, *(Figure 5)* (Note 8)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8+2µs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs (Note 8)		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, and linearity errors. See *Figure 3.* None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13.*

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6).* See paragraph 4.0.

Note 7: If start pulse is asynchronous with converter clock the minimum start pulse width is 8 clock periods plus 2 µS.

Note 8: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 9: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer: The device contains a 16-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table 1 shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1

Selected Analog Channel	Address Line D	C	B	A	Expansion Control
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

Additional single-ended analog signals can be multiplexed to the A/D converter by disabling all the multiplexer inputs using the expansion control. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

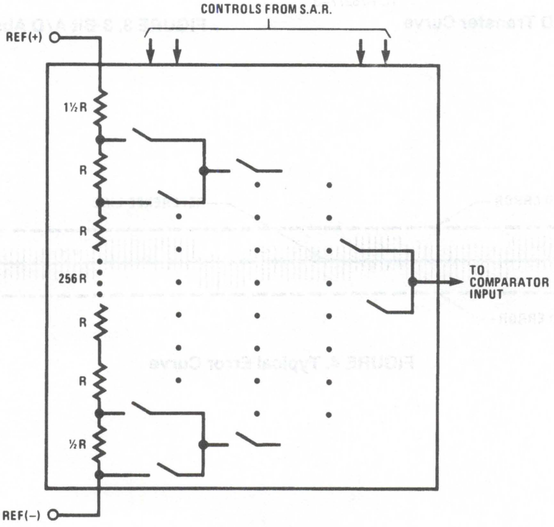
CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + ½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.



TL/H/5277-2

FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

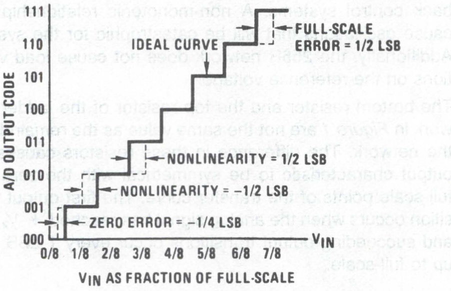
The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ulimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

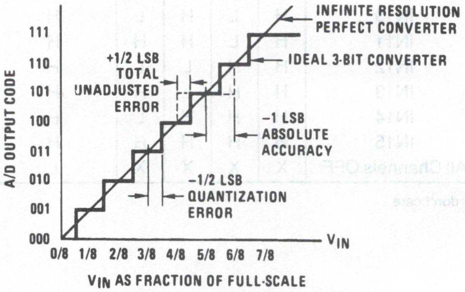
The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179.



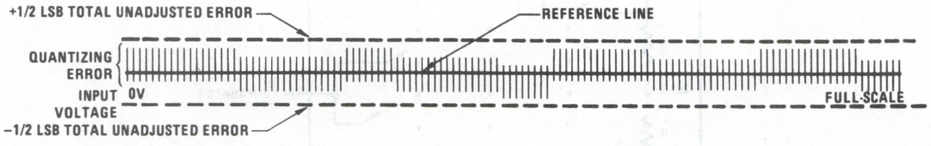
TL/H/5277-3

FIGURE 2. 3-Bit A/D Transfer Curve



TL/H/5277-4

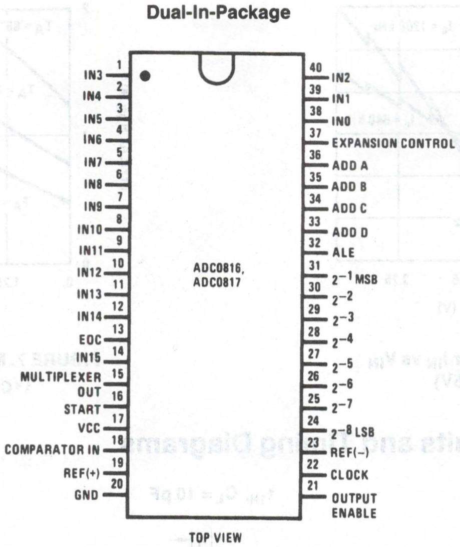
FIGURE 3. 3-Bit A/D Absolute Accuracy Curve



TL/H/5277-5

FIGURE 4. Typical Error Curve

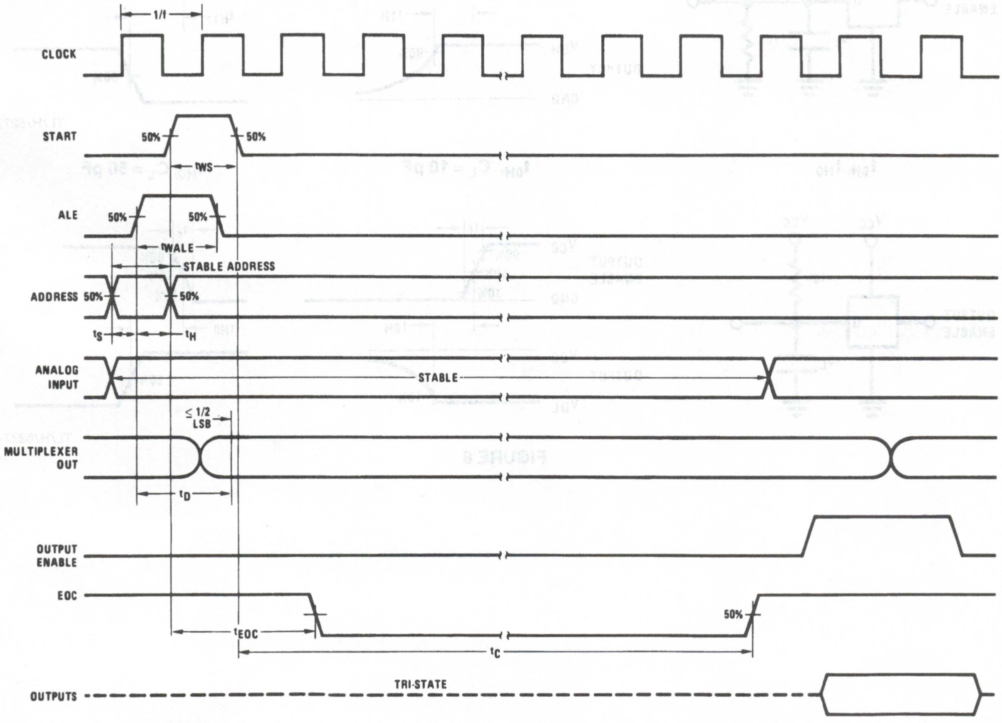
Connection Diagram


Dual-In-Package
1 IN3
2 IN4
3 IN5
4 IN6
5 IN7
6 IN8
7 IN9
8 IN10
9 IN11
10 IN12
11 IN13
12 IN14
13 EOC
14 IN15
15 MULTIPLEXER
16 OUT
17 START
VCC
18 COMPARATOR IN
19 REF(+)
20 GND
40 IN2
39 IN1
38 IN0
37 EXPANSION CONTROL
36 ADD A
35 ADD B
34 ADD C
33 ADD D
32 ALE
31 2^{-1} MSB
30 2^{-2}
29 2^{-3}
28 2^{-4}
27 2^{-5}
26 2^{-6}
25 2^{-7}
24 2^{-8} LSB
23 REF(−)
22 CLOCK
21 OUTPUT ENABLE
ADC0816,
ADC0817
TOP VIEW

Order Number
ADC0816CCN,
ADC0817CCN,
ADC0816CCJ or
ADC0816CJ
See NS Package Number
J40A or N40A

TL/H/5277-6

Timing Diagram


1/f
CLOCK
START
50%
50%
tWS
ALE
50%
50%
tWALE
STABLE ADDRESS
ADDRESS
50%
50%
t_S
t_H
ANALOG INPUT
STABLE
≤ 1/2 LSB
MULTIPLEXER OUT
t_D
OUTPUT ENABLE
EOC
50%
t_{EOC}
t_C
OUTPUTS
TRI-STATE

TL/H/5277-7

FIGURE 5

Typical Performance Characteristics

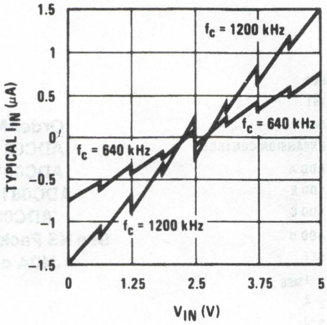
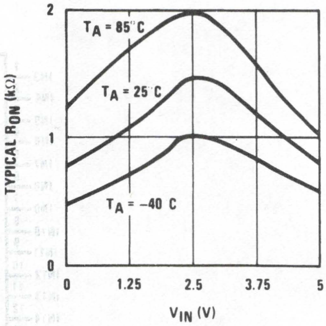


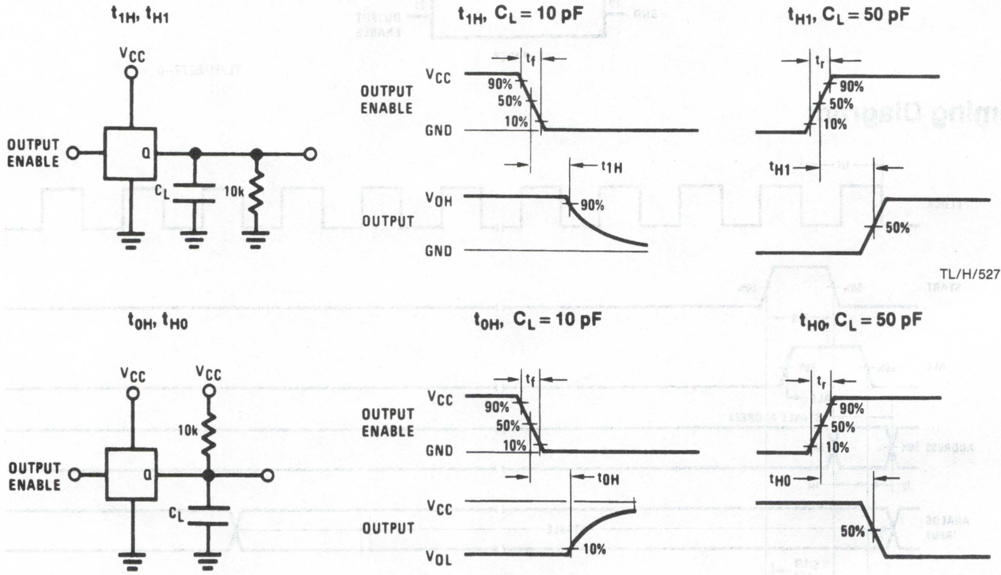
FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC}=V_{REF}=5V$)



TL/H/5277-8

FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC}=V_{REF}=5V$)

TRI-STATE Test Circuits and Timing Diagrams


t_{1H}, t_{H1}
V_{CC}
OUTPUT ENABLE
Q
C_L
10k
t_{1H}, C_L = 10 pF
V_{CC}
GND
OUTPUT ENABLE
t_f
90%
50%
10%
t_{1H}
V_{OH}
GND
OUTPUT
90%
t_{H1}, C_L = 50 pF
t_r
90%
50%
10%
t_{H1}
50%
t_{OH}, t_{HO}
V_{CC}
V_{CC}
10k
OUTPUT ENABLE
Q
C_L
t_{OH}, C_L = 10 pF
V_{CC}
GND
OUTPUT ENABLE
t_f
90%
50%
10%
t_{OH}
V_{CC}
OUTPUT
V_{OL}
10%
t_{HO}, C_L = 50 pF
t_r
90%
50%
10%
t_{HO}
50%

TL/H/5277-9

TL/H/5277-10

FIGURE 8

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0816, ADC0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0816 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \qquad (1)$$

V_{IN} = Input voltage into the ADC0816

V_{fs} = Full-scale voltage

V_Z = Zero voltage

D_X = Data point being measured

D_{MAX} = Maximum data limit

D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0816, ADC0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

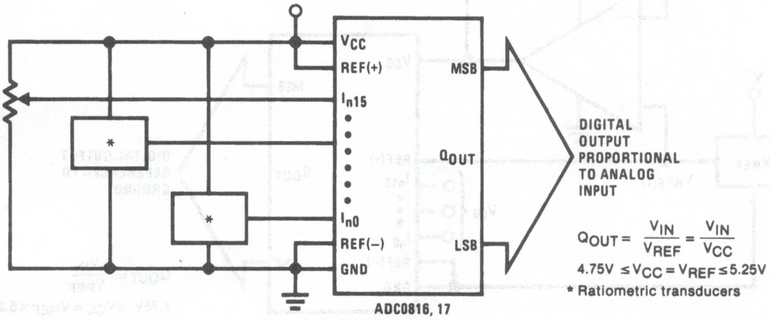
Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches These limitations are automaticaly satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.


*
*
VCC
REF(+)
In15
In0
REF(−)
GND
MSB
QOUT
LSB
ADC0816, 17
DIGITAL OUTPUT PROPORTIONAL TO ANALOG INPUT
$Q_{OUT} = \frac{V_{IN}}{V_{REF}} = \frac{V_{IN}}{V_{CC}}$
$4.75V \le V_{CC} = V_{REF} \le 5.25V$
* Ratiometric transducers

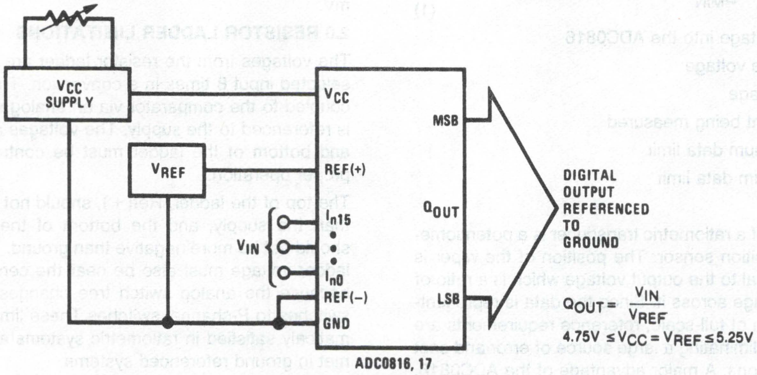
TL/H/5277–11

FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

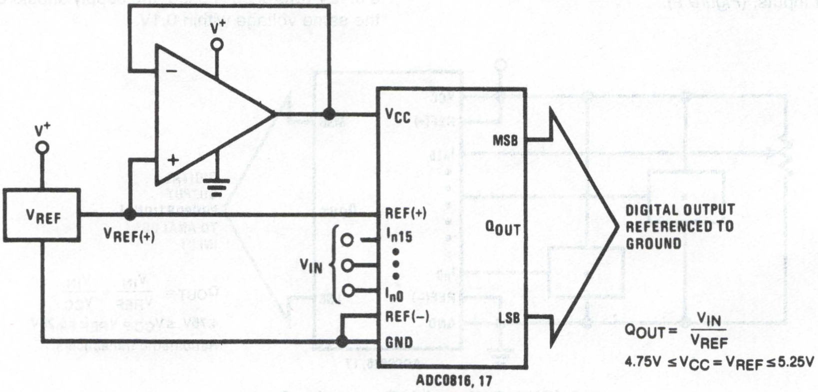
The ADC0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground references system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB to be half the size of the LSB in a 5V reference system.


V_CC SUPPLY
V_REF
V_CC
MSB
REF(+)
I_n15
V_IN
I_n0
REF(−)
GND
Q_OUT
LSB
DIGITAL OUTPUT REFERENCED TO GROUND
Q_OUT = V_IN / V_REF
4.75V ≤ V_CC = V_REF ≤ 5.25V
ADC0816, 17

TL/H/5277–12

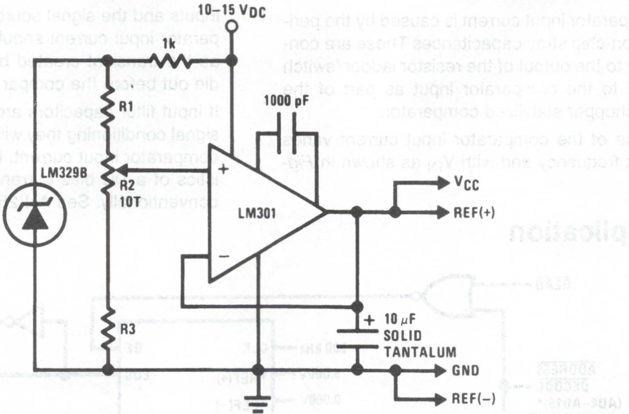
FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply


V+
−
+
V+
V_REF
V_REF(+)
V_CC
MSB
REF(+)
I_n15
V_IN
I_n0
REF(−)
GND
Q_OUT
LSB
DIGITAL OUTPUT REFERENCED TO GROUND
Q_OUT = V_IN / V_REF
4.75V ≤ V_CC = V_REF ≤ 5.25V
ADC0816, 17

TL/H/5277–13

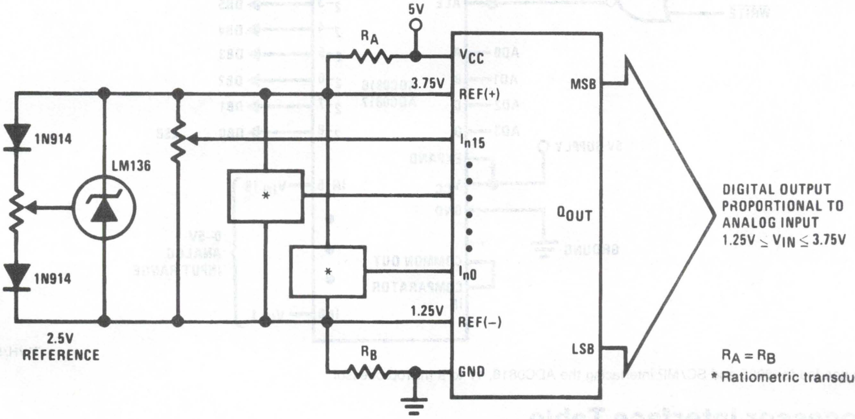
FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)


10–15 VDC
1k
R1
1000 pF
LM329B
R2
10T
+
LM301
−
VCC
REF(+)
R3
+ 10 µF
SOLID
TANTALUM
GND
REF(−)

TL/H/5277–14

FIGURE 12. Typical Reference and Supply Circuit


5V
RA
VCC
3.75V
REF(+)
MSB
1N914
LM136
In15
*
*
QOUT
DIGITAL OUTPUT
PROPORTIONAL TO
ANALOG INPUT
1.25V ≤ VIN ≤ 3.75V
1N914
In0
1.25V
REF(−)
2.5V
REFERENCE
RB
LSB
GND

RA = RB

* Ratiometric transducers

TL/H/5277–15

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \qquad (4)$$

where: V_{IN} = Voltage at comparator input

V_{REF} = Voltage at Ref(+)

V_{REF} = Voltage at Ref(−)

V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

Applications Information (Continued)

4.0 ANALOG COMPARATOR INPUTS

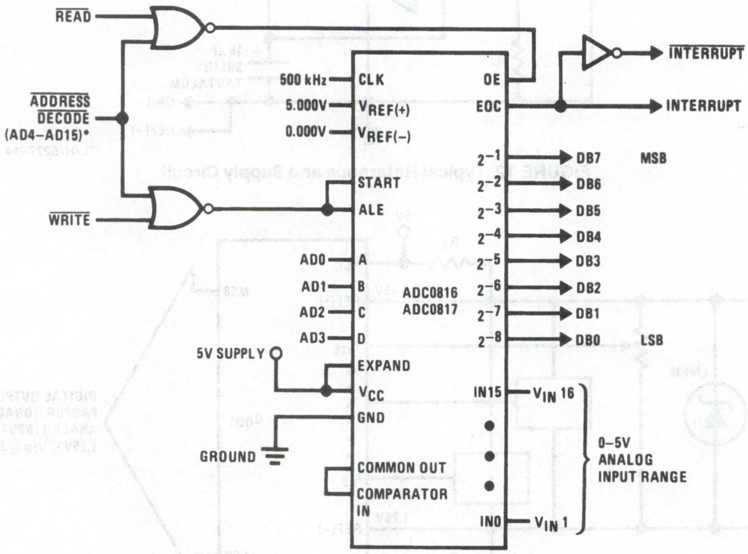
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6.*

If no filter capacitors are used at the analog or comparator inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally. See AN-258 for further discussion.

Typical Application


$\overline{READ}$
$\overline{ADDRESS}$
$\overline{DECODE}$
(AD4–AD15)*
$\overline{WRITE}$
500 kHz
5.000V
0.000V
CLK
$V_{REF(+)}$
$V_{REF(-)}$
START
ALE
AD0
AD1
AD2
AD3
A
B
C
D
5V SUPPLY
EXPAND
V_{CC}
GND
GROUND
COMMON OUT
COMPARATOR IN
ADC0816
ADC0817
OE
EOC
$\overline{INTERRUPT}$
INTERRUPT
2^{-1}
2^{-2}
2^{-3}
2^{-4}
2^{-5}
2^{-6}
2^{-7}
2^{-8}
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
MSB
LSB
IN15
V_{IN} 16
IN0
V_{IN} 1
0–5V ANALOG INPUT RANGE

TL/H/5277-16

*Address latches needed for 8085 and SC/MP interfacing the ADC0816, 17 to a microprocessor

Microprocessor Interface Table

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	$\overline{MEMR}$	$\overline{MEMW}$	INTR (Thru RST Circuit)
8085	$\overline{RD}$	$\overline{WR}$	INTR (Thru RST Circuit)
Z-80	$\overline{RD}$	$\overline{WR}$	$\overline{INT}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•ϕ 2•R/W	VMA•Q_2•$\overline{R/W}$	$\overline{IRQA}$ or $\overline{IRQB}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	±½ Bit Unadjusted	ADC0816CCN	ADC0816CCJ	ADC0816CJ
	±1 Bit Unadjusted	ADC0817CCN		
Package Outline		N40A Molded DIP	J40A Hermetic DIP	J40A Hermetic DIP

National Semiconductor Corporation

PRELIMINARY

ADC0819 8-Bit Serial I/O A/D Converter with 19-Channel Multiplexer

General Description

The ADC0819 is an 8-Bit successive approximation A/D converter with simultaneous serial I/O. The serial input controls an analog multiplexer which selects from 19 input channels or an internal half scale test voltage.

An input sample-and-hold is implemented by a capacitive reference ladder and sampled data comparator. This allows the input signal to vary during the conversion cycle.

Separate serial I/O and conversion clock inputs are provided to facilitate the interface to various microprocessors.

Features

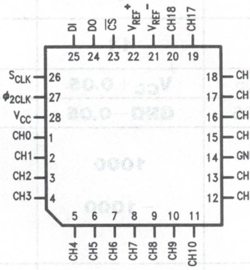
- Separate asynchronous converter clock and serial data I/O clock.
- 19-Channel multiplexer with 5-Bit serial address logic.
- Built-in sample and hold function.
- Ratiometric or absolute voltage referencing.
- No zero or full-scale adjust required.
- Internally addressable test voltage.
- 0V to 5V input range with single 5V power supply.
- TTL/MOS input/output compatible.
- 28-pin molded chip carrier or 28-pin molded DIP

Key Specifications

Resolution	8-Bits
Total unadjusted error	± ½LSB and ± 1LSB
Single supply	$5V_{DC}$
Low Power	15 mW
Conversion Time	16 μs

Connection Diagrams

Molded Chip Carrier (PCC) Package

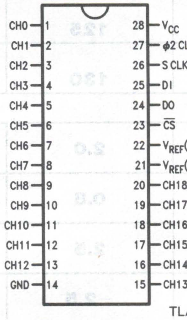

DI
DO
CS
VREF+
VREF−
CH18
CH17
25 24 23 22 21 20 19
SCLK 26
φ2CLK 27
VCC 28
CH0 1
CH1 2
CH2 3
CH3 4
18 CH16
17 CH15
16 CH14
15 CH13
14 GND
13 CH12
12 CH11
5 6 7 8 9 10 11
CH4
CH5
CH6
CH7
CH8
CH9
CH10

TL/H/9287–1

Top View

Order Number ADC0819BCV, CCV
See NS Package Number V28A

Dual-In-Line Package


CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
CH8 9
CH9 10
CH10 11
CH11 12
CH12 13
GND 14
28 VCC
27 φ2 CLK
26 S CLK
25 DI
24 DO
23 CS
22 VREF(+)
21 VREF(−)
20 CH18
19 CH17
18 CH16
17 CH15
16 CH14
15 CH13

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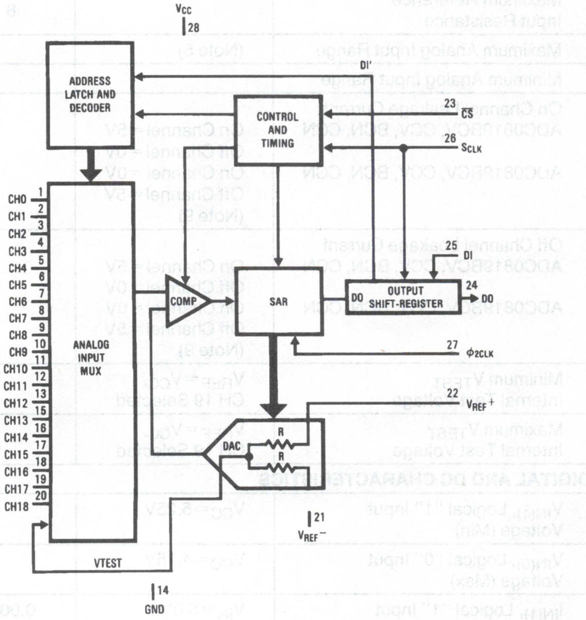
Top View

Order Number ADC0819BCN, CCN
See NS Package Number N28B

Functional Diagram


VCC
28
DI'
ADDRESS LATCH AND DECODER
CONTROL AND TIMING
23 CS
26 SCLK
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
CH8 9
CH9 10
CH10 11
CH11 12
CH12 13
CH13 15
CH14 16
CH15 17
CH16 18
CH17 19
CH18 20
ANALOG INPUT MUX
COMP
SAR
25 DI
DO
OUTPUT SHIFT-REGISTER
24 DO
27 φ2CLK
22 VREF+
DAC
R
R
21 VREF−
VTEST
14 GND

TL/H/9287–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage	
Inputs and Outputs	−0.3V to V_{CC} +0.3V
Input Current Per Pin (Note 3)	±5mA
Total Package Input Current (Note 3)	±20mA
Storage Temperature	−65°C to +150°C
Package Dissipation at $T_A = 25°C$	875 mW
Lead Temperature (Soldering, 10 sec.)	
Dual-In-Line Package (Plastic)	260°C
Surface Mount Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Susceptibility (Note 11)	2000V

Operating Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0819BCV, ADC0819CCV	$-40°C \le T_A \le +85°C$
ADC0819BCN, ADC0819CCN	$0°C \le T_A \le +70°C$

Electrical Characteristics

The following specifications apply for V_{CC} = 4.75V to 5.25V, V_{REF} = +4.6V to (V_{CC} + .1V), $\phi_{2\ CLK}$ = 2.097 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	ADC0819BCV, ADC0819BCN ADC0819CCV, ADC0819CCN Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Maximum Total Unadjusted Error	V_{REF} = 5.00 V_{DC} (Note 4)				
ADC0819BCV, BCN			±½	**±½**	LSB
ADC0819CCV, CCN			±1	**±1**	LSB
Minimum Reference Input Resistance		8		**5**	kΩ
Maximum Reference Input Resistance		8	11	**11**	kΩ
Maximum Analog Input Range	(Note 5)		V_{CC}+0.05	**V_{CC}+0.05**	V
Minimum Analog Input Range			GND−0.05	**GND−0.05**	V
On Channel Leakage Current ADC0819BCV, CCV, BCN, CCN	On Channel=5V Off Channel=0V		400	**1000**	nA
ADC0819BCV, CCV, BCN, CCN	On Channel=0V Off Channel=5V (Note 9)		−400	**−1000**	nA
Off Channel Leakage Current ADC0819BCV, CCV, BCN, CCN	On Channel=5V Off Channel=0V		−400	**−1000**	nA
ADC0819BCV, CCV, BCN, CCN	On Channel=0V Off Channel=5V (Note 9)		400	**1000**	nA
Minimum V_{TEST} Internal Test Voltage	$V_{REF}=V_{CC}$, CH 19 Selected		125	**125**	(Note 10) Counts
Maximum V_{TEST} Internal Test Voltage	$V_{REF}=V_{CC}$, CH 19 Selected		130	**130**	(Note 10) Counts
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC}=5.25V		2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC}=4.75V		0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN}=5.0V	0.005	2.5	**2.5**	μA
$I_{IN(0)}$, Logical "0" Input Current (Max)	V_{IN}=0V	−0.005	−2.5	**−2.5**	μA

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = 4.75V to 5.25V, V_{REF} = +4.6V to (V_{CC} + .1V), $\phi_{2\ CLK}$ = 2.097 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Parameter	Conditions	ADC0819BCV, ADC0819BCN ADC0819CCV, ADC0819CCN			Units
		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
DIGITAL AND DC CHARACTERISTICS (Continued)					
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC} = 4.75V I_{OUT} = −360 µA I_{OUT} = −10 µA		2.4 4.5	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC} = 5.25V I_{OUT} = 1.6 mA		0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT} = 0V V_{OUT} = 5V	−0.01 0.01	−3 3	**−3** **3**	µA µA
I_{SOURCE}, Output Source Current (Min)	V_{OUT} = 0V	−14	−6.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)	V_{OUT} = V_{CC}	16	8.0	**8.0**	mA
I_{CC}, Supply Current (Max)	$\overline{CS}$ = 1, V_{REF} Open	1	2.5	**2.5**	mA
I_{REF} (Max)	V_{REF} = 5V	**0.7**	1	**1**	mA

AC CHARACTERISTICS

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
$\phi_{2\ CLK}$, ϕ_2 Clock Frequency	MIN		0.70		**1.0**	MHz
	MAX		4.0	2.0	**2.1**	
S_{CLK}, Serial Data Clock Frequency	MIN				**5.0**	KHz
	MAX		1000	525	**525**	
T_C, Conversion Process Time	MIN	Not Including MUX Addressing and Analog Input Sampling Times	26		**26**	ϕ_2 cycles
	MAX		32		**32**	
t_{ACC}, Access Time Delay From $\overline{CS}$ Falling Edge to DO Data Valid	MIN				**1**	ϕ_2 cycles
	MAX				**3**	
$t_{SET\text{-}UP}$, Minimum Set-up Time of $\overline{CS}$ Falling Edge to S_{CLK} Rising Edge					$\mathbf{4/\phi_{2CLK} + \frac{1}{2\,S_{CLK}}}$	sec
$t_{H\overline{CS}}$, $\overline{CS}$ Hold Time After the Falling Edge of S_{CLK}					**0**	ns
$t_{\overline{CS}}$, Total $\overline{CS}$ Low Time	MIN				$\mathbf{t_{set\text{-}up} + 8/S_{CLK}}$	sec
	MAX				$\mathbf{t_{\overline{CS}}(min) + 26/\phi_{2CLK}}$	sec
t_{HDI}, Minimum DI Hold Time from S_{CLK} Rising Edge			0		**0**	ns
t_{HDO}, Minimum DO Hold Time from S_{CLK} Falling Edge		R_L = 30k, C_L = 100 pF			**10**	ns
t_{SDI}, Minimum DI Set-up Time to S_{CLK} Rising Edge			200		**400**	ns
t_{DDO}, Maximum Delay From S_{CLK} Falling Edge to DO Data Valid		R_L = 30k, C_L = 100 pF	180	200	**250**	ns
t_{TRI}, Maximum DO Hold Time, ($\overline{CS}$ Rising edge to DO TRI-STATE)		R_L = 3k, C_L = 100 pF	90	150	**150**	ns

Electrical Characteristics

The following specifications apply for $V_{CC}=4.75V$ to $5.25V$, $t_r=t_f=20$ ns, $V_{REF}=4.6V$ to $(V_{CC}+0.1V)$, unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A=T_J=25°C$.

Parameter	Conditions		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
AC CHARACTERISTICS (Continued)						
t_{CA}, Analog Sampling Time	After Address Is Latched $\overline{CS}$ = Low				**3/S_{CLK}+1 µs**	sec
t_{RDO}, Maximum DO Rise Time	$R_L=30$ kΩ, $C_L=100$ pf	"TRI-STATE" to "HIGH" State	75	150	**150**	ns
		"LOW" to "HIGH" State	150	300	**300**	
t_{FDO}, Maximum DO Fall Time	$R_L=30$ kΩ, $C_L=100$ pf	"TRI-STATE" to "LOW" State	75	150	**150**	ns
		"HIGH" to "LOW" State	150	300	**300**	
C_{IN}, Maximum Input Capacitance	Analog Inputs, AN0–AN10 and V_{REF}		11		**55**	pF
	All Others		5		**15**	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Under over voltage conditions ($V_{IN}<0V$ and $V_{IN}>V_{CC}$) the maximum input current at any one pin is ±5 mA. If the voltage at more than one pin exceeds V_{CC} + .3V the total package current must be limited to 20 mA. For example the maximum number of pins that can be over driven at the maximum current level of ±5 mA is four.

Note 4: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 5: Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Tested Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design Limits are guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

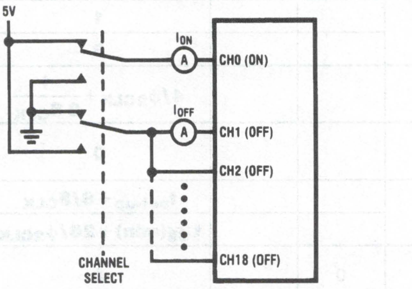
Note 9: Channel leakage current is measured after the channel selection.

Note 10: 1 count = $V_{REF}/256$.

Note 11: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

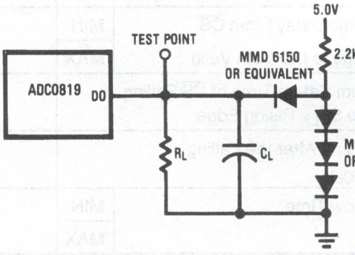
Test Circuits

Leakage Current



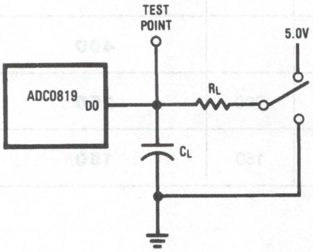
TL/H/9287-3

D0 Except "TRI-STATE"



TL/H/9287-4

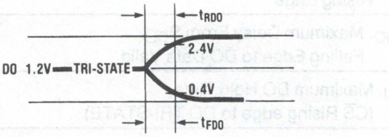
t_{TRI} "TRI-STATE"



TL/H/9287-5

Timing Diagrams

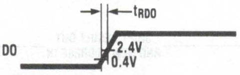
D0 "TRI-STATE" Rise & Fall Times



TL/H/9287-6

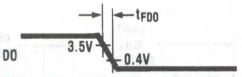
Timing Diagrams (Continued)

D0 Low to High State


tRDO
D0
2.4V
0.4V

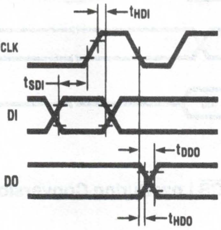
TL/H/9287-7

D0 High to Low State


tFDO
D0
3.5V
0.4V

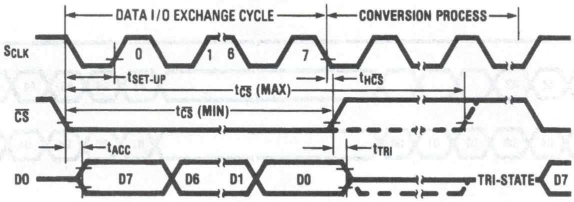
TL/H/9287-8

Data Input and Output Timing


tHDI
SCLK
tSDI
DI
tDDO
DO
tHDO

TL/H/9287-9

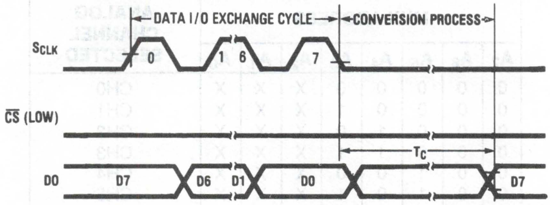
Timing with a continuous S_{CLK}


DATA I/O EXCHANGE CYCLE
CONVERSION PROCESS
SCLK
0
1
6
7
tSET-UP
tHCS
tCS (MAX)
tCS (MIN)
CS
tACC
tTRI
DO
D7
D6
D1
D0
TRI-STATE
D7

TL/H/9287-10

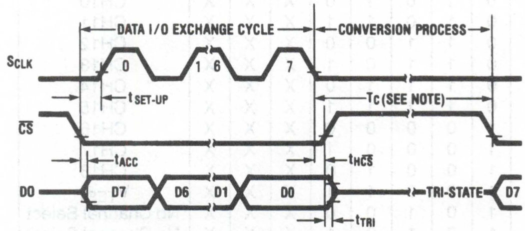
*Strobing $\overline{CS}$ High and Low will abort the present conversion and initiate a new serial I/O exchange.

Timing with a gated S_{CLK} and $\overline{CS}$ Continuously Low


DATA I/O EXCHANGE CYCLE
CONVERSION PROCESS
SCLK
0
1
6
7
CS (LOW)
TC
DO
D7
D6
D1
D0
D7

TL/H/9287-11

Using $\overline{CS}$ To TRI-STATE D0

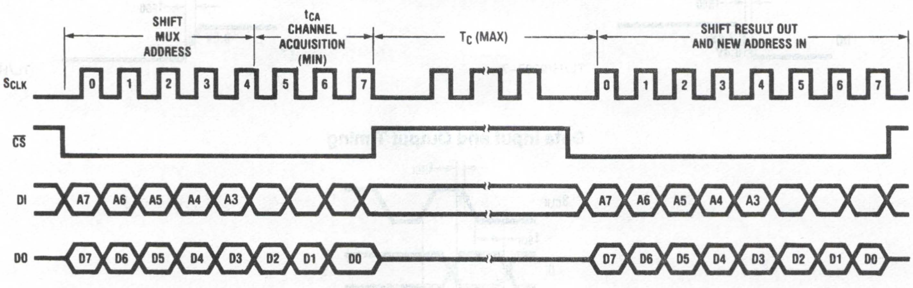

DATA I/O EXCHANGE CYCLE
CONVERSION PROCESS
SCLK
0
1
6
7
tSET-UP
TC (SEE NOTE)
CS
tACC
tHCS
DO
D7
D6
D1
D0
TRI-STATE
D7
tTRI

TL/H/9287-12

Note: Strobing $\overline{CS}$ Low during this time interval will abort the conversion in process.

Timing Diagrams (Continued)

$\overline{\text{CS}}$ High During Conversion


SHIFT MUX ADDRESS
t_{CA} CHANNEL ACQUISITION (MIN)
T_C (MAX)
SHIFT RESULT OUT AND NEW ADDRESS IN
SCLK
0
1
2
3
4
5
6
7
$\overline{\text{CS}}$
DI
A7
A6
A5
A4
A3
DO
D7
D6
D5
D4
D3
D2
D1
D0

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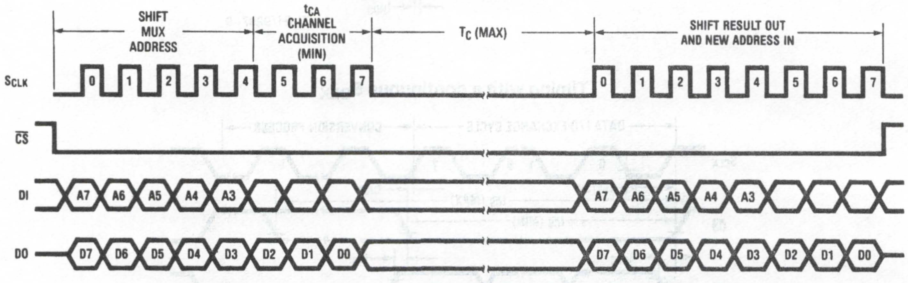
$\overline{\text{CS}}$ Low During Conversion


SHIFT MUX ADDRESS
t_{CA} CHANNEL ACQUISITION (MIN)
T_C (MAX)
SHIFT RESULT OUT AND NEW ADDRESS IN
SCLK
0
1
2
3
4
5
6
7
$\overline{\text{CS}}$
DI
A7
A6
A5
A4
A3
DO
D7
D6
D5
D4
D3
D2
D1
D0

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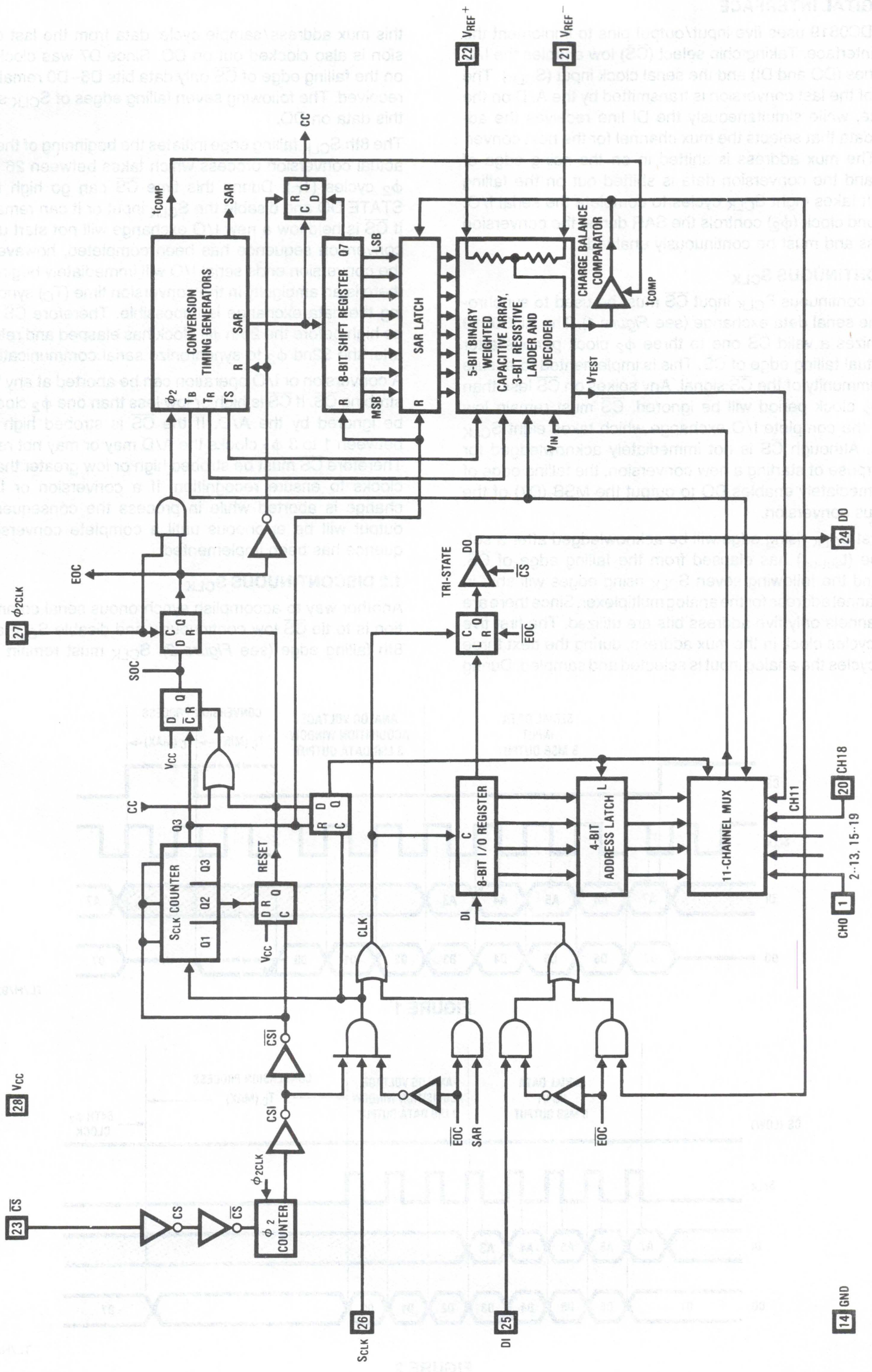
Channel Addressing Table

TABLE I. ADC 0819 Channel Addressing

MUX ADDRESS								ANALOG CHANNEL SELECTED
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	0	0	0	0	X	X	X	CH0
0	0	0	0	1	X	X	X	CH1
0	0	0	1	0	X	X	X	CH2
0	0	0	1	1	X	X	X	CH3
0	0	1	0	0	X	X	X	CH4
0	0	1	0	1	X	X	X	CH5
0	0	1	1	0	X	X	X	CH6
0	0	1	1	1	X	X	X	CH7
0	1	0	0	0	X	X	X	CH8
0	1	0	0	1	X	X	X	CH9
0	1	0	1	0	X	X	X	CH10
0	1	0	1	1	X	X	X	CH11
0	1	1	0	0	X	X	X	CH12
0	1	1	0	1	X	X	X	CH13
0	1	1	1	0	X	X	X	CH14
0	1	1	1	1	X	X	X	CH15
1	0	0	0	0	X	X	X	CH16
1	0	0	0	1	X	X	X	CH17
1	0	0	1	0	X	X	X	CH18
1	0	0	1	1	X	X	X	V_{TEST}
1	0	1	0	0	X	X	X	No Channel Select
1	0	1	0	1	X	X	X	No Channel Select
1	0	1	1	0	X	X	X	No Channel Select
1	0	1	1	1	X	X	X	No Channel Select
1	1	X	X	X	X	X	X	Logic Test Mode*

*Analog channel inputs CH0 thru CH4 are logic outputs

Functional Block Diagram


23 CS̄
28 VCC
27 φ2CLK
CS
CS̄
φ2 COUNTER
φ2CLK
CSI
CSI̅
SCLK 26
DI 25
EOC
SAR
EOC
SCLK COUNTER
Q1
Q2
Q3
Q3
VCC
D R Q C
RESET
R D C Q
CLK
CC
VCC
D C̄ R Q
SOC
D C R Q
EOC
DI
C
8-BIT I/O REGISTER
C L R Q
EOC
TRI-STATE
DO
CS
4-BIT ADDRESS LATCH
L
11-CHANNEL MUX
CH11
CH0 1
2‥13, 15‥19
20 CH18
24 DO
14 GND
φ2
TB
TR
TS
CONVERSION TIMING GENERATORS
R
SAR
tCOMP
SAR
R C D Q
CC
R
8-BIT SHIFT REGISTER
Q7
MSB
LSB
R
SAR LATCH
5-BIT BINARY WEIGHTED CAPACITIVE ARRAY, 3-BIT RESISTIVE LADDER AND DECODER
VIN
VTEST
CHARGE BALANCE COMPARATOR
tCOMP
22 VREF+
21 VREF−

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Functional Description

1.0 DIGITAL INTERFACE

The ADC0819 uses five input/output pins to implement the serial interface. Taking chip select ($\overline{CS}$) low enables the I/O data lines (DO and DI) and the serial clock input (S_{CLK}). The result of the last conversion is transmitted by the A/D on the DO line, while simultaneously the DI line receives the address data that selects the mux channel for the next conversion. The mux address is shifted in on the rising edge of S_{CLK} and the conversion data is shifted out on the falling edge. It takes eight S_{CLK} cycles to complete the serial I/O. A second clock (ϕ_2) controls the SAR during the conversion process and must be continuously enabled.

1.1 CONTINUOUS S_{CLK}

With a continuous S_{CLK} input $\overline{CS}$ must be used to synchronize the serial data exchange (see *Figure 1*). The ADC0819 recognizes a valid $\overline{CS}$ one to three ϕ_2 clock periods after the actual falling edge of $\overline{CS}$. This is implemented to ensure noise immunity of the $\overline{CS}$ signal. Any spikes on $\overline{CS}$ less than one ϕ_2 clock period will be ignored. $\overline{CS}$ must remain low during the complete I/O exchange which takes eight S_{CLK} cycles. Although $\overline{CS}$ is not immediately acknowledged for the purpose of starting a new conversion, the falling edge of $\overline{CS}$ immediately enables DO to output the MSB (D7) of the previous conversion.

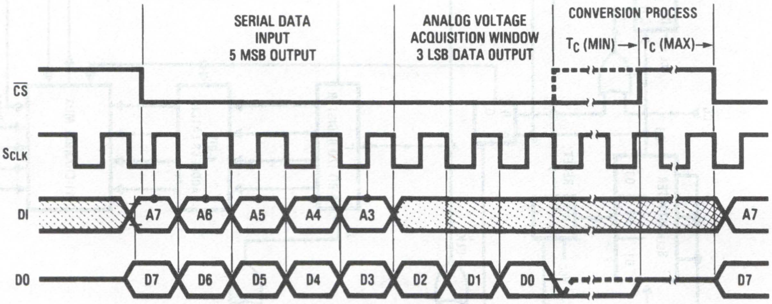
The first S_{CLK} rising edge will be acknowledged after a set-up time ($t_{set\text{-}up}$) has elapsed from the falling edge of $\overline{CS}$. This and the following seven S_{CLK} rising edges will shift in the channel address for the analog multiplexer. Since there are 19 channels only five address bits are utilized. The first five S_{CLK} cycles clock in the mux address, during the next three S_{CLK} cycles the analog input is selected and sampled. During this mux address/sample cycle, data from the last conversion is also clocked out on DO. Since D7 was clocked out on the falling edge of $\overline{CS}$ only data bits D6–D0 remain to be received. The following seven falling edges of S_{CLK} shift out this data on DO.

The 8th S_{CLK} falling edge initiates the beginning of the A/D's actual conversion process which takes between 26 and 32 ϕ_2 cycles (T_C). During this time $\overline{CS}$ can go high to TRI-STATE DO and disable the S_{CLK} input or it can remain low. If $\overline{CS}$ is held low a new I/O exchange will not start until the conversion sequence has been completed, however once the conversion ends serial I/O will immediately begin. Since there is an ambiguity in the conversion time (T_C) synchronizing the data exchange is impossible. Therefore $\overline{CS}$ should go high before the 26th ϕ_2 clock has elasped and return low after the 32nd ϕ_2 to synchronize serial communication.

A conversion or I/O operation can be aborted at any time by strobing $\overline{CS}$. If $\overline{CS}$ is high or low less than one ϕ_2 clock it will be ignored by the A/D. If the $\overline{CS}$ is strobed high or low between 1 to 3 ϕ_2 clocks the A/D may or may not respond. Therefore $\overline{CS}$ must be strobed high or low greater than 3 ϕ_2 clocks to ensure recognition. If a conversion or I/O exchange is aborted while in process the consequent data output will be erroneous until a complete conversion sequence has been implemented.

1.2 DISCONTINUOUS S_{CLK}

Another way to accomplish synchronous serial communication is to tie $\overline{CS}$ low continuously and disable S_{CLK} after its 8th falling edge (see *Figure 2*). S_{CLK} must remain low for



TL/H/9287-16

FIGURE 1

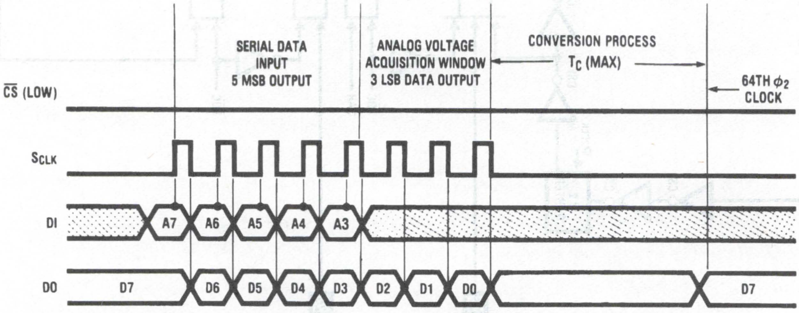


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FIGURE 2

Functional Description (Continued)

at least 32 ϕ_2 clocks to ensure that the A/D has completed its conversion. If S_{CLK} is enabled sooner, synchronizing to the data output on DO is not possible since an end of conversion signal from the A/D is not available and the actual conversion time is not known. With $\overline{CS}$ low during the conversion time (32 ϕ_2 max) DO will go high or low after the eighth falling edge of S_{CLK} until the conversion is completed. Once the conversion is through DO will transmit the MSB. The rest of the data will be shifted out once S_{CLK} is enabled as discussed previously.

If $\overline{CS}$ goes high during the conversion sequence DO is tri-stated, and the result is not affected so long as $\overline{CS}$ remains high until the end of the conversion.

1.2 MULTIPLEXER ADDRESSING

The five bit mux address is shifted, MSB first, into DI. Input data corresponds to the channel selected as shown in table 1. Care should be taken not to send an address greater than or equal to twenty four (11XXX) as this puts the A/D in a digital testing mode. In this mode the analog inputs CH0 thru CH4 become digital outputs, for our use in production testing.

2.0 ANALOG INPUT

2.1 THE INPUT SAMPLE AND HOLD

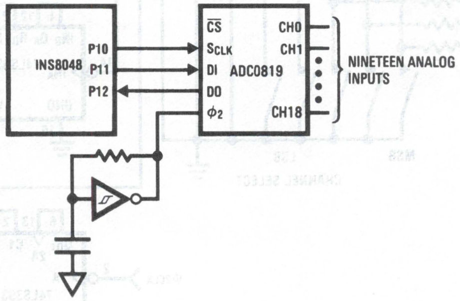
The ADC0819's sample/hold capacitor is implemented in its capacitive ladder structure. After the channel address is received, the ladder is switched to sample the proper analog input. This sampling mode is maintained for 1 µsec after the eighth S_{CLK} falling edge. The hold mode is initiated with the start of the conversion process. An acquisition window of $3t_{SCLK}+1$ µsec is therefore available to allow the ladder capacitance to settle to the analog input voltage. Any change in the analog voltage before or after the acquisition window will not effect the A/D conversion result.

In the most simple case, the ladder's acquisition time is determined by the R_{on} (3K) of the multiplexer switches and the total ladder capacitance (90pf). These values yield an acquisition time of about 2 µsec for a full scale reading. Therefore the analog input must be stable for at least 2 µsec before and 1 µsec after the eighth S_{CLK} falling edge to ensure a proper conversion. External input source resistance and capacitance will lengthen the acquisition time and should be accounted for.

Other conventional sample and hold error specifications are included in the error and timing specs of the A/D. The hold step and gain error sample/hold specs are taken into account in the ADC0819's total unadjusted error, while the hold settling time is included in the A/D's max conversion time of 32 ϕ_2 clock periods. The hold droop rate can be thought of as being zero since an unlimited amount of time can pass between a conversion and the reading of data. However, once the data is read it is lost and another conversion is started.

Typical Applications

ADC0819-INS8048 INTERFACE



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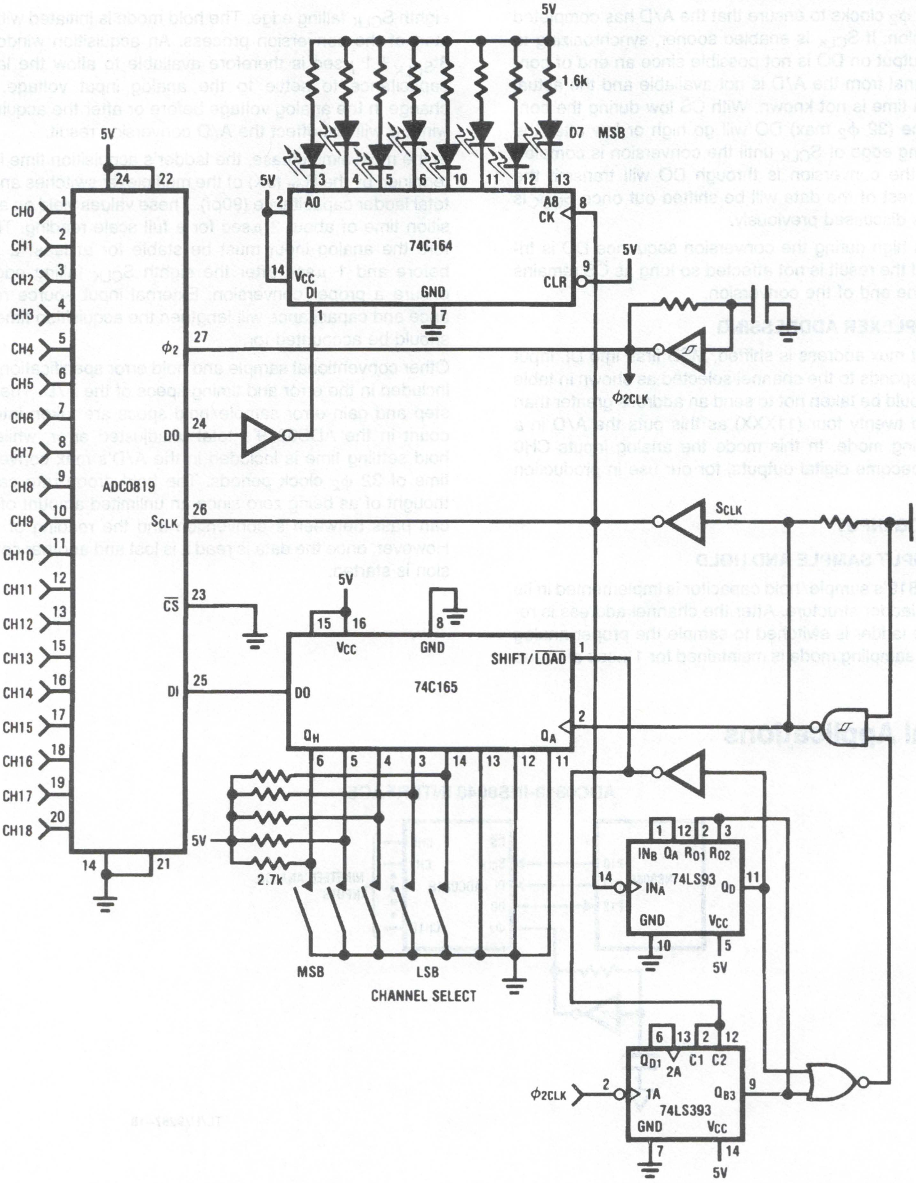
ADC0819 FUNCTIONAL CIRCUIT


5V
1.6k
D7
MSB
3
4
5
6
10
11
12
13
5V
2
A0
A8
8
CK
74C164
14
VCC
DI
GND
1
7
5V
9
CLR
5V
24
22
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
CH9
CH10
CH11
CH12
CH13
CH14
CH15
CH16
CH17
CH18
ADC0819
φ2
27
DO
24
SCLK
26
CS
23
DI
25
14
21
5V
φ2CLK
SCLK
5V
15
16
8
VCC
GND
SHIFT/LOAD
74C165
DO
QH
QA
2.7k
MSB
LSB
CHANNEL SELECT
INB
QA
R01
R02
INA
74LS93
QD
GND
VCC
10
5
5V
QD1
2A
C1
C2
φ2CLK
1A
QB3
74LS393
GND
VCC
7
14
5V

TL/H/9287-19

Ordering Information

Temperature Range		0°C to +70°C	−40°C to +85°C
Total Unadjusted Error	±½ LSB	ADC0819BCN	ADC0819BCV
	±1 LSB	ADC0819CCN	ADC0819CCV
Package Outline		N28B	V28A

National Semiconductor Corporation

microCMOS

ADC0820 8-Bit High Speed μP Compatible A/D Converter with Track/Hold Function

General Description

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5 μs conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/μs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

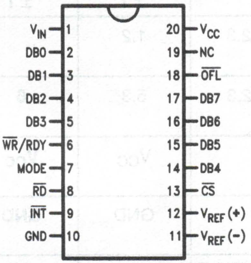
■ Resolution	8 Bits
■ Conversion Time	2.5 μs Max (RD Mode) 1.5 μs Max (WR-RD Mode)
■ Input signals with slew rate of 100 mV/μs converted without external sample-and-hold to 8 bits	
■ Low Power	75 mW Max
■ Total Unadjusted Error	± ½ LSB and ± 1 LSB

Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—5 V_{DC}
- Easy interface to all microprocessors, or operates stand-alone
- Latched TRI-STATE® output
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{CC}
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3" standard width 20-pin DIP
- 20-pin molded chip carrier package
- 20-pin small outline package

Connection and Functional Diagrams

Dual-In-Line and Small Outline Packages

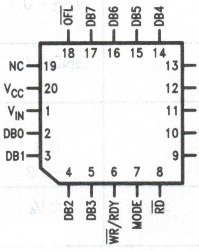


V_IN 1
DB0 2
DB1 3
DB2 4
DB3 5
WR/RDY 6
MODE 7
RD 8
INT 9
GND 10
20 V_CC
19 NC
18 OFL
17 DB7
16 DB6
15 DB5
14 DB4
13 CS
12 V_REF (+)
11 V_REF (−)

TL/H/5501-1

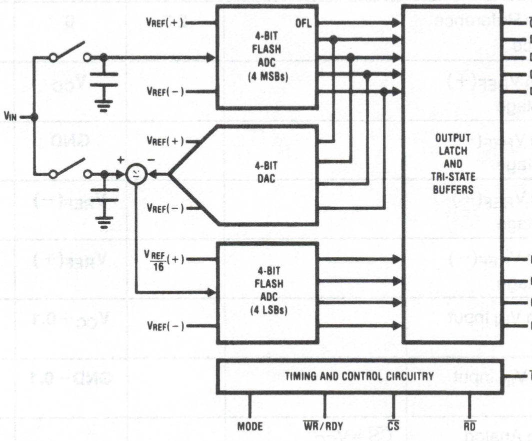
Top View

Molded Chip Carrier Package



OFL DB7 DB6 DB5 DB4
18 17 16 15 14
NC 19
V_CC 20
V_IN 1
DB0 2
DB1 3
13 CS
12 V_REF (+)
11 V_REF (−)
10 GND
9 INT
4 5 6 7 8
DB2 DB3 WR/RDY MODE RD

TL/H/5501-33



V_REF(+)
V_REF(−)
OFL
4-BIT FLASH ADC (4 MSBs)
V_IN
V_REF(+)
V_REF(−)
4-BIT DAC
V_REF/16(+)
V_REF(−)
4-BIT FLASH ADC (4 LSBs)
OUTPUT LATCH AND TRI-STATE BUFFERS
OFL
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
TIMING AND CONTROL CIRCUITRY
INT
MODE
WR/RDY
CS
RD

TL/H/5501-2

FIGURE 1

See Ordering Information

3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	10V
Logic Control Inputs	$-0.2V$ to $V_{CC}+0.2V$
Voltage at Other Inputs and Output	$-0.2V$ to $V_{CC}+0.2V$
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$	875 mW
Input Current at Any Pin (Note 5)	1 mA
Package Input Current (Note 5)	4 mA
ESD Susceptability (Note 9)	1200V
Lead Temp. (Soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0820BD, ADC0820CJ	$-55°C \le T_A \le +125°C$
ADC0820BCD, ADC0820CCJ	$-40°C \le T_A \le +85°C$
ADC0820BCN, ADC0820CCN	$0°C \le T_A \le 70°C$
ADC0820BCV, ADC0820CCV	$0°C \le T_A \le 70°C$
ADC0820BCWM, ADC0820CCWM	$0°C \le T_A \le 70°C$
V_{CC} Range	4.5V to 8V

Converter Characteristics

The following specifications apply for RD mode (pin 7=0), $V_{CC}=5V$, $V_{REF}(+)=5V$, and $V_{REF}(-)=GND$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A=T_j=25°C$.

Parameter	Conditions	ADC0820BD, ADC0820CJ ADC0820BCD, ADC0820CCJ			ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820CCV ADC0820BCWM, ADC0820CCWM			Limit Units
		Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
Resolution			**8**			8	**8**	Bits
Total Unadjusted Error (Note 3)	ADC0820BD, BCD		±½					LSB
	ADC0820BCN					±½	±½	LSB
	ADC0820CD, CCD		±1					LSB
	ADC0820CCN					±1	±1	LSB
Minimum Reference Resistance		2.3	**1.00**		2.3	1.2		kΩ
Maximum Reference Resistance		2.3	**6**		2.3	5.3	**6**	kΩ
Maximum $V_{REF}(+)$ Input Voltage			**V_{CC}**			V_{CC}	**V_{CC}**	V
Minimum $V_{REF}(-)$ Input Voltage			**GND**			GND	**GND**	V
Minimum $V_{REF}(+)$ Input Voltage			**$V_{REF}(-)$**			$V_{REF}(-)$	**$V_{REF}(-)$**	V
Maximum $V_{REF}(-)$ Input Voltage			**$V_{REF}(+)$**			$V_{REF}(+)$	**$V_{REF}(+)$**	V
Maximum V_{IN} Input Voltage			**$V_{CC}+0.1$**			$V_{CC}+0.1$	**$V_{CC}+0.1$**	V
Minimum V_{IN} Input Voltage			**GND−0.1**			GND−0.1	**GND−0.1**	V
Maximum Analog Input Leakage Current	$\overline{CS}=V_{CC}$							
	$V_{IN}=V_{CC}$		**3**			0.3	**3**	µA
	$V_{IN}=GND$		**−3**			−0.3	**−3**	µA
Power Supply Sensitivity	$V_{CC}=5V \pm 5\%$	±1/16	±¼		±1/16	±¼	±¼	LSB

DC Electrical Characteristics

The following specifications apply for $V_{CC} = 5V$, unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$.**

Parameter	Conditions		ADC0820BD, ADC0820CJ ADC0820BCD, ADC0820CCJ			ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820CCV ADC0820BCWM, ADC0820CCWM			Limit Units
			Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		**2.0**			2.0	**2.0**	V
		Mode		**3.5**			3.5	**3.5**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		**0.8**			0.8	**0.8**	V
		Mode		**1.5**			1.5	**1.5**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN(1)} = 5V$; $\overline{CS}$, $\overline{RD}$		0.005	**1**		0.005		**1**	μA
	$V_{IN(1)} = 5V$; $\overline{WR}$		0.1	**3**		0.1	0.3	**3**	μA
	$V_{IN(1)} = 5V$; Mode		50	**200**		50	170	**200**	μA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN(0)} = 0V$; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		−0.005	**−1**		−0.005		**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{OUT} = -360\ \mu A$; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			**2.4**			2.8	**2.4**	V
	$V_{CC} = 4.75V$, $I_{OUT} = -10\ \mu A$; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			**4.5**			4.6	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{OUT} = 1.6$ mA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY			**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current	$V_{OUT} = 5V$; DB0–DB7, RDY		0.1	**3**		0.1	0.3	**3**	μA
	$V_{OUT} = 0V$; DB0–DB7, RDY		−0.1	**−3**		−0.1	−0.3	**−3**	μA
I_{SOURCE}, Output Source Current	$V_{OUT} = 0V$; DB0–DB7, $\overline{OFL}$		−12	**−6**		−12	−7.2	**−6**	mA
	$\overline{INT}$		−9	**−4.0**		−9	−5.3	**−4.0**	mA
I_{SINK}, Output Sink Current	$V_{OUT} = 5V$; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		14	**7**		14	8.4	**7**	mA
I_{CC}, Supply Current	$\overline{CS} = \overline{WR} = \overline{RD} = 0$		7.5	**15**		7.5	13	**15**	mA

AC Electrical Characteristics

The following specifications apply for $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $V_{REF}(+) = 5V$, $V_{REF}(-) = 0V$ and $T_A = 25°C$ unless otherwise specified.

Parameter		Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_{CRD}, Conversion Time for RD Mode		Pin 7 = 0, *(Figure 2)*	1.6		2.5	μs
t_{ACC0}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = 0, *(Figure 2)*	$t_{CRD}+20$		$t_{CRD}+50$	ns
$t_{CWR\text{-}RD}$, Conversion Time for WR-RD Mode		Pin 7 = V_{CC}; $t_{WR} = 600$ ns, $t_{RD} = 600$ ns; *(Figures 3a and 3b)*			1.52	μs
t_{WR}, Write Time	Min	Pin 7 = V_{CC}; *(Figures 3a and 3b)*		600		ns
	Max	(Note 4) See Graph	50			μs
t_{RD}, Read Time	Min	Pin 7 = V_{CC}; *(Figures 3a and 3b)* (Note 4) See Graph		600		ns
t_{ACC1}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD} < t_I$; *(Figure 3a)* $C_L = 15$ pF	190		280	ns
		$C_L = 100$ pF	210		320	ns
t_{ACC2}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD} > t_I$; *(Figure 3b)* $C_L = 15$ pF	70		120	ns
		$C_L = 100$ pF	90		150	ns

AC Electrical Characteristics (Continued) The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20$ ns, $V_{REF}(+)=5V$, $V_{REF}(-)=0V$ and $T_A=25°C$ unless otherwise specified.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_I, Internal Comparison Time	Pin 7 = V_{CC}; *(Figures 3b* and *4)* $C_L=50$ pF	800		1300	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L=1k$, $C_L=10$ pF	100		200	ns
$t_{\overline{INT}L}$, Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	Pin 7 = V_{CC}, $C_L=50$ pF $t_{RD}>t_I$; *(Figure 3b)* $t_{RD}<t_I$; *(Figure 3a)*	 $t_{RD}+200$		 t_I $t_{RD}+290$	 ns ns
$t_{\overline{INT}H}$, Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	*(Figures 2, 3a* and *3b)* $C_L=50$ pF	125		225	ns
$t_{\overline{INT}HWR}$, Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	*(Figure 4)*, $C_L=50$ pF	175		270	ns
t_{RDY}, Delay from $\overline{CS}$ to RDY	*(Figure 2)*, $C_L=50$ pF, Pin 7 = 0	50		100	ns
t_{ID}, Delay from $\overline{INT}$ to Output Valid	*(Figure 4)*	20		50	ns
t_{RI}, Delay from $\overline{RD}$ to $\overline{INT}$	Pin 7 = V_{CC}, $t_{RD}<t_I$ *(Figure 3a)*	200		290	ns
t_P, Delay from End of Conversion to Next Conversion	*(Figures 2, 3a, 3b* and *4)* (Note 4) See Graph			500	ns
Slew Rate, Tracking		0.1			V/µs
C_{VIN}, Analog Input Capacitance		45			pF
C_{OUT}, Logic Output Capacitance		5			pF
C_{IN}, Logic Input Capacitance		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 3: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 4: Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified. See Accuracy vs t_{WR} and Accuracy vs t_{RD} graphs.

Note 5: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 1 mA or less. The 4 mA package input current limits the number of pins that can exceed the power supply boundaries with a 1 mA current limit to four.

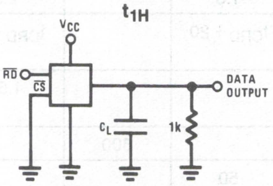
Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

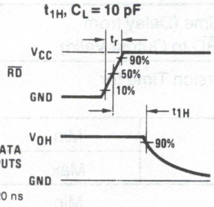
Note 9: Human body model, 100 pF discharaged through a 1.5 kΩ resistor.

TRI-STATE Test Circuits and Waveforms

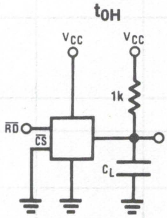


t_{0H}

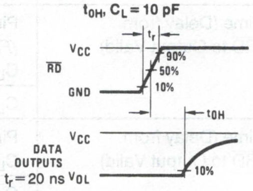
TL/H/5501-3



TL/H/5501-4

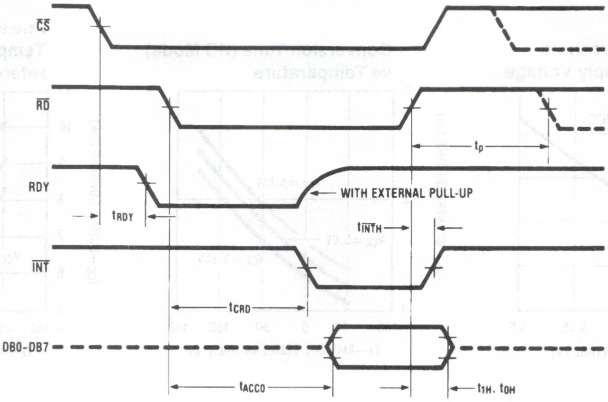


TL/H/5501-5



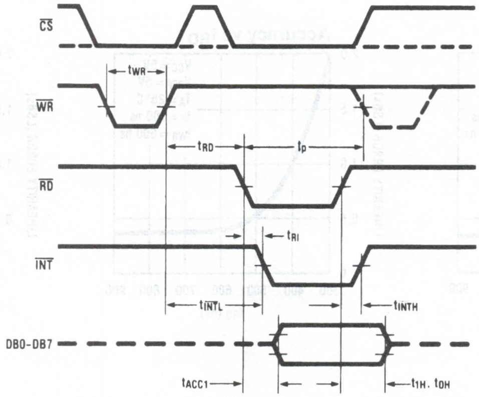
TL/H/5501-6

Timing Diagrams


CS
RD
RDY
INT
DB0-DB7
WITH EXTERNAL PULL-UP
t_P
t_{RDY}
$t_{\overline{INTH}}$
t_{CRD}
t_{ACC0}
t_{1H}, t_{0H}

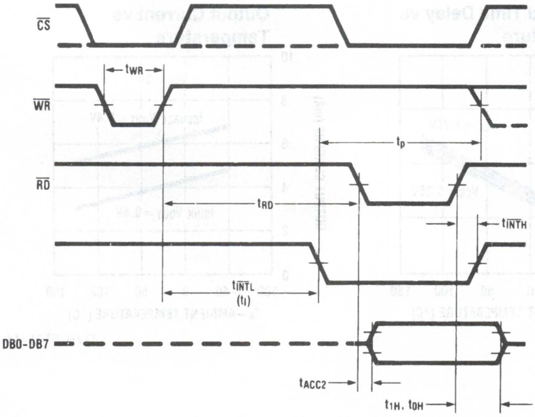
TL/H/5501-7

FIGURE 2. RD Mode (Pin 7 is Low)


CS
WR
RD
INT
DB0-DB7
t_{WR}
t_{RD}
t_P
t_{RI}
$t_{\overline{INTL}}$
$t_{\overline{INTH}}$
t_{ACC1}
t_{1H}, t_{0H}

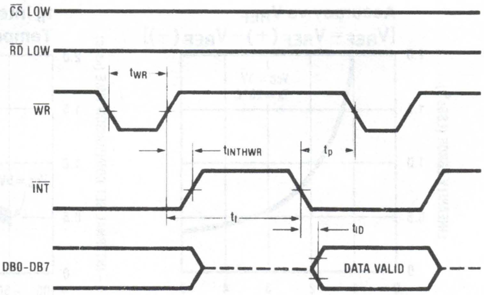
TL/H/5501-8

FIGURE 3a. WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)


CS
WR
RD
DB0-DB7
t_{WR}
t_P
t_{RD}
$t_{\overline{INTH}}$
$t_{\overline{INTL}}$
(t_I)
t_{ACC2}
t_{1H}, t_{0H}

TL/H/5501-9

FIGURE 3b. WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)

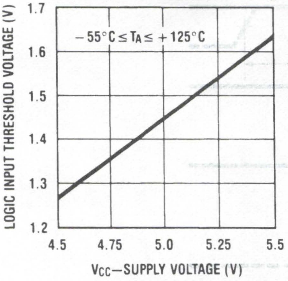

CS LOW
RD LOW
WR
INT
DB0-DB7
t_{WR}
t_{INTHWR}
t_P
t_I
t_{ID}
DATA VALID

TL/H/5501-10

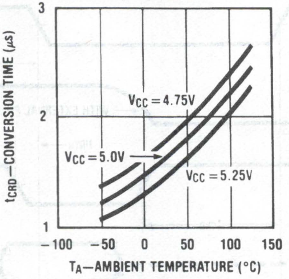
FIGURE 4. WR-RD Mode (Pin 7 is High)
Stand-Alone Operation

Typical Performance Characteristics

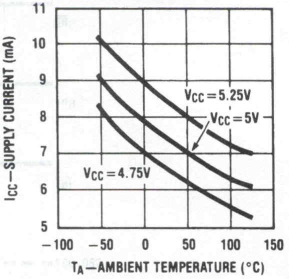
Logic Input Threshold Voltage vs Supply Voltage



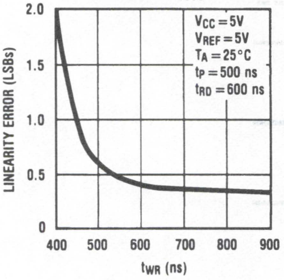
Conversion Time (RD Mode) vs Temperature



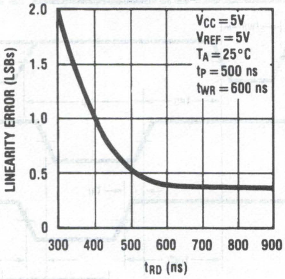
Power Supply Current vs Temperature (not including reference ladder)



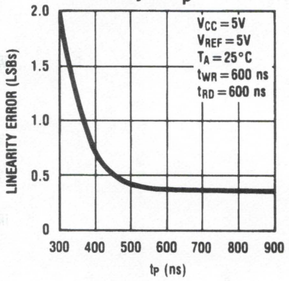
Accuracy vs t_{WR}



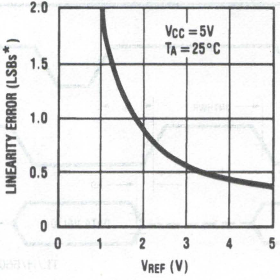
Accuracy vs t_{RD}



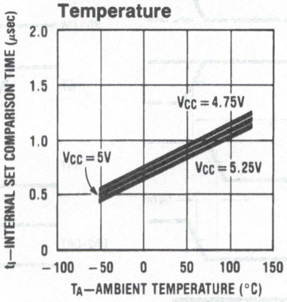
Accuracy vs t_P



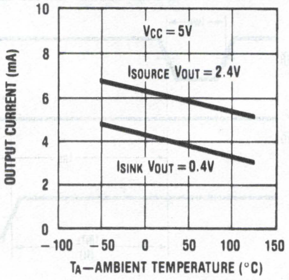
Accuracy vs V_{REF} [$V_{REF} = V_{REF}(+) - V_{REF}(-)$]



t_I, Internal Time Delay vs Temperature



Output Current vs Temperature



$*1\ \mathrm{LSB} = \frac{V_{REF}}{256}$

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Description of Pin Functions

Pin	Name	Function
1	V_{IN}	Analog input; range $= \text{GND} \le V_{IN} \le V_{CC}$
2	DB0	TRI-STATE data output—bit 0 (LSB)
3	DB1	TRI-STATE data output—bit 1
4	DB2	TRI-STATE data output—bit 2
5	DB3	TRI-STATE data output—bit 3
6	$\overline{\text{WR}}$/RDY	**WR-RD Mode** **$\overline{\text{WR}}$:** With $\overline{\text{CS}}$ low, the conversion is started on the falling edge of $\overline{\text{WR}}$. Approximately 800 ns (the preset internal time out, t_I) after the $\overline{\text{WR}}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{\text{RD}}$ does not occur prior to this time out (see *Figures 3a* and *3b*). **RD Mode** **RDY:** This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{\text{CS}}$; RDY will go TRI-STATE when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see *Figure 2*).
7	Mode	**Mode:** Mode selection input—it is internally tied to GND through a 50 μA current source. **RD Mode:** When mode is low **WR-RD Mode:** When mode is high
8	$\overline{\text{RD}}$	**WR-RD Mode** With $\overline{\text{CS}}$ low, the TRI-STATE data outputs (DB0-DB7) will be activated when $\overline{\text{RD}}$ goes low (see *Figure 4*). $\overline{\text{RD}}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (t_I, ~800 ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{\text{RD}}$ (see *Figures 3a* and *3b*). **RD Mode** With $\overline{\text{CS}}$ low, the conversion will start with $\overline{\text{RD}}$ going low, also $\overline{\text{RD}}$ will enable the TRI-STATE data outputs at the completion of the conversion. RDY going TRI-STATE and $\overline{\text{INT}}$ going low indicates the completion of the conversion (see *Figure 2*).
9	$\overline{\text{INT}}$	**WR-RD Mode** $\overline{\text{INT}}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{\text{INT}}$ will go low, ~ 800 ns (the preset internal time out, t_I) after the rising edge of $\overline{\text{WR}}$ (see *Figure 3b*); or $\overline{\text{INT}}$ will go low after the falling edge of $\overline{\text{RD}}$, if $\overline{\text{RD}}$ goes low prior to the 800 ns time out (see *Figure 3a*). $\overline{\text{INT}}$ is reset by the rising edge of $\overline{\text{RD}}$ or $\overline{\text{CS}}$ (see *Figures 3a* and *3b*). **RD Mode** $\overline{\text{INT}}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{\text{INT}}$ is reset by the rising edge of $\overline{\text{RD}}$ or $\overline{\text{CS}}$ (see *Figure 2*).
10	GND	Ground
11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: $\text{GND} \le V_{REF}(-) \le V_{REF}(+)$ (Note 5)
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-) \le V_{REF}(+) \le V_{CC}$ (Note 5)
13	$\overline{\text{CS}}$	$\overline{\text{CS}}$ must be low in order for the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to be recognized by the converter.
14	DB4	TRI-STATE data output—bit 4
15	DB5	TRI-STATE data output—bit 5
16	DB6	TRI-STATE data output—bit 6
17	DB7	TRI-STATE data output—bit 7 (MSB)
18	$\overline{\text{OFL}}$	Overflow output—If the analog input is higher than the $V_{REF}(+)$, $\overline{\text{OFL}}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit). This output is always active and does not go into TRI-STATE as DB0–DB7 do.
19	NC	No connection
20	V_{CC}	Power supply voltage

1.0 Functional Description

1.1 GENERAL OPERATION

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (*Figure 1*). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the "sampled-data" comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

3

1.0 Functional Description (Continued)

1.2 THE SAMPLED-DATA COMPARATOR

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively coupled input (*Figure 5*). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (*Figure 5a*) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_B, approximately 1.2V). In the second cycle (*Figure 5b*), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input (V_B') becomes

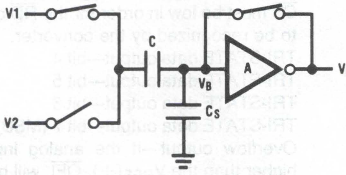
$$V_B - (V1 - V2)\frac{C}{C + C_S}$$

and the output will go high or low depending on the sign of $V_B' - V_B$.

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (*Figure 6*), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor and opening all of the other switches (S switches). The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

1.3 ARCHITECTURE

In the ADC0820, one bank of 15 comparators is used in each 4-bit flash A/D converter (*Figure 7*). The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.



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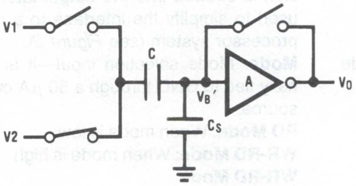
- $V_O = V_B$
- V on C = $V1 - V_B$
- C_S = stray input node capacitor
- V_B = inverter input bias voltage

FIGURE 5a. Zeroing Phase



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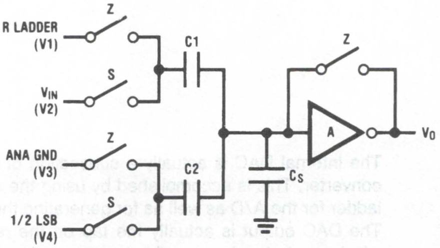
- $V_B' - V_B = (V2 - V1)\frac{C}{C + C_S}$
- $V_O' = \frac{-A}{C + C_S}[CV2 - CV1]$
- V_O' is dependent on $V2 - V1$

FIGURE 5b. Compare Phase

FIGURE 5. Sampled-Data Comparator



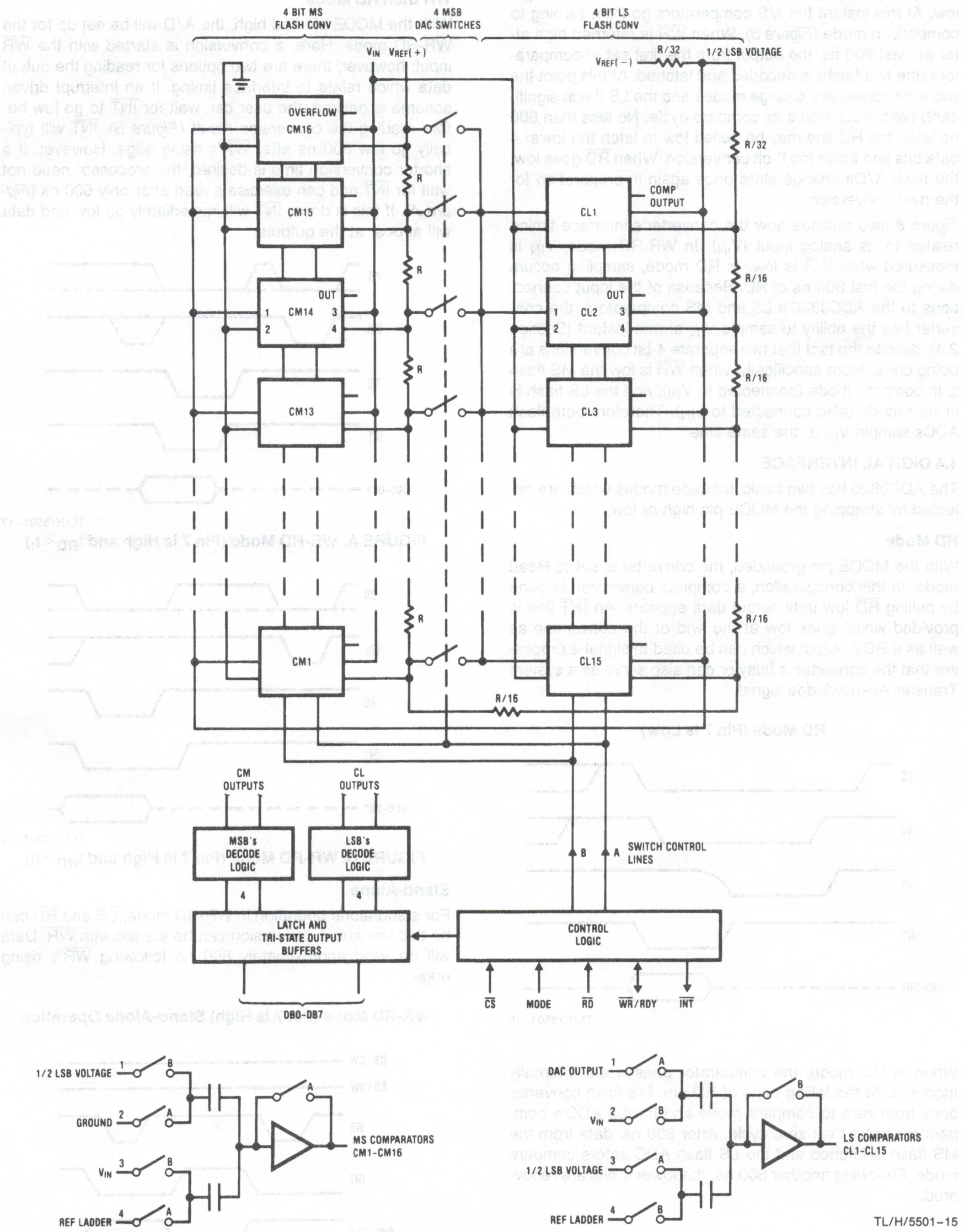
TL/H/5501-14

$$V_O = \frac{-A}{C1 + C2 + C_S}[C1(V2 - V1) + C2(V4 - V3)]$$

$$= \frac{-A}{C1 + C2 + C_S}[\Delta Q_{C1} + \Delta Q_{C2}]$$

FIGURE 6. ADC0820 Comparator (from MS Flash ADC)

Detailed Block Diagram


4 BIT MS FLASH CONV
4 MSB DAC SWITCHES
4 BIT LS FLASH CONV
V_IN
V_REF(+)
V_REF(−)
R/32
1/2 LSB VOLTAGE
OVERFLOW
CM16
R
CM15
OUT
1
CM14
3
2
4
CM13
CM1
R/32
COMP OUTPUT
CL1
R/16
CL2
CL3
CL15
R/16
CM OUTPUTS
CL OUTPUTS
MSB's DECODE LOGIC
LSB's DECODE LOGIC
LATCH AND TRI-STATE OUTPUT BUFFERS
DB0–DB7
B
A
SWITCH CONTROL LINES
CONTROL LOGIC
CS
MODE
RD
WR/RDY
INT
1/2 LSB VOLTAGE
GROUND
V_IN
REF LADDER
MS COMPARATORS CM1–CM16
DAC OUTPUT
1/2 LSB VOLTAGE
REF LADDER
LS COMPARATORS CL1–CL15

TL/H/5501–15

FIGURE 7

1.0 Functional Description (Continued)

When a typical conversion is started, the $\overline{\text{WR}}$ line is brought low. At this instant the MS comparators go from zeroing to comparison mode (*Figure 8*). When $\overline{\text{WR}}$ is returned high after at least 600 ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600 ns later, the $\overline{\text{RD}}$ line may be pulled low to latch the lower 4 data bits and finish the 8-bit conversion. When $\overline{\text{RD}}$ goes low, the flash A/Ds change state once again in preparation for the next conversion.

Figure 8 also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{\text{WR}}$ is low. In RD mode, sampling occurs during the first 800 ns of $\overline{\text{RD}}$. Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant (Section 2.4), despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{\text{WR}}$ is low the MS flash is in compare mode (connected to V_{IN}), and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

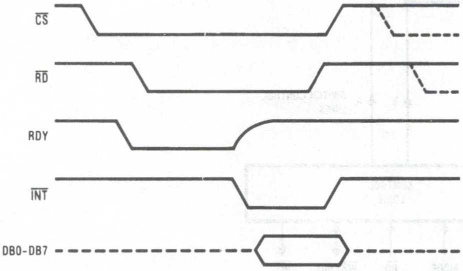
1.4 DIGITAL INTERFACE

The ADC0820 has two basic interface modes which are selected by strapping the MODE pin high or low.

RD Mode

With the MODE pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{\text{RD}}$ low until output data appears. An $\overline{\text{INT}}$ line is provided which goes low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

RD Mode (Pin 7 is Low)

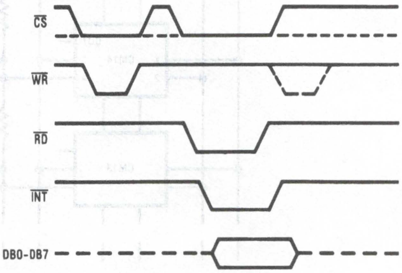


TL/H/5501-16

When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{\text{RD}}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800 ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800 ns, the lower 4 bits are recovered.

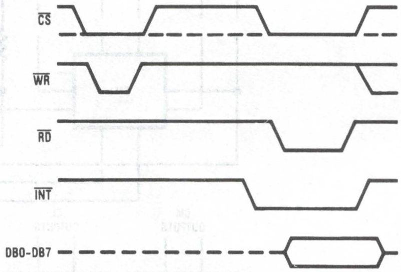
WR then RD Mode

With the MODE pin tied high, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{\text{WR}}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt driven scheme is desired, the user can wait for $\overline{\text{INT}}$ to go low before reading the conversion result (*Figure B*). $\overline{\text{INT}}$ will typically go low 800 ns after $\overline{\text{WR}}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{\text{INT}}$ and can exercise a read after only 600 ns (*Figure A*). If this is done, $\overline{\text{INT}}$ will immediately go low and data will appear at the outputs.



TL/H/5501-17

FIGURE A. WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)



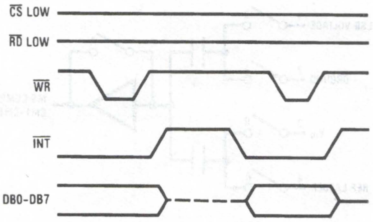
TL/H/5501-18

FIGURE B. WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)

Stand-Alone

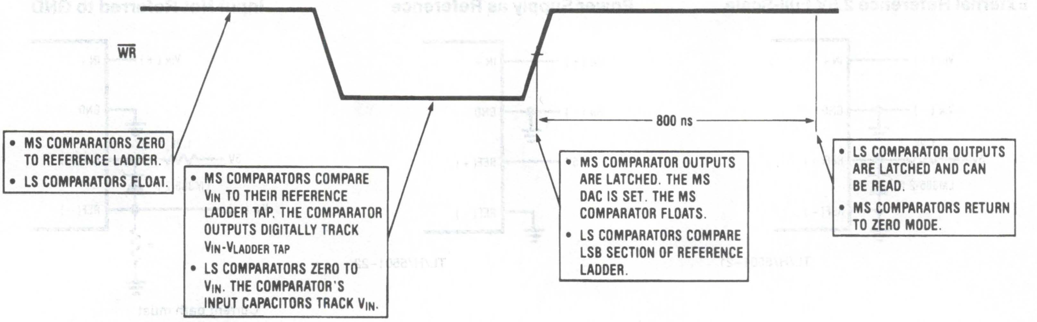
For stand-alone operation in WR-RD mode, $\overline{\text{CS}}$ and $\overline{\text{RD}}$ can be tied low and a conversion can be started with $\overline{\text{WR}}$. Data will be valid approximately 800 ns following $\overline{\text{WR}}$'s rising edge.

WR-RD Mode (Pin 7 is High) Stand-Alone Operation



TL/H/5501-19

1.0 Functional Description (Continued)


$\overline{WR}$
• MS COMPARATORS ZERO TO REFERENCE LADDER.
• LS COMPARATORS FLOAT.
• MS COMPARATORS COMPARE V_{IN} TO THEIR REFERENCE LADDER TAP. THE COMPARATOR OUTPUTS DIGITALLY TRACK V_{IN}-$V_{LADDER\ TAP}$
• LS COMPARATORS ZERO TO V_{IN}. THE COMPARATOR'S INPUT CAPACITORS TRACK V_{IN}.
800 ns
• MS COMPARATOR OUTPUTS ARE LATCHED. THE MS DAC IS SET. THE MS COMPARATOR FLOATS.
• LS COMPARATORS COMPARE LSB SECTION OF REFERENCE LADDER.
• LS COMPARATOR OUTPUTS ARE LATCHED AND CAN BE READ.
• MS COMPARATORS RETURN TO ZERO MODE.

TL/H/5501-20

Note: MS means most significant
LS means least significant

FIGURE 8. Operating Sequence (WR-RD Mode)

OTHER INTERFACE CONSIDERATIONS

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50 μs. When the MS flash ADC's sampled-data comparators (Section 1.2) are in comparison mode ($\overline{WR}$ is low), the input capacitors (C, *Figure 6*) must hold their charge. Switch leakage and inverter bias current can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion (Section 1.3), a new conversion cannot be started until this phase is complete. The minimum spec for this time (t_P, *Figures 2, 3a, 3b,* and *4*) is 500 ns.

2.0 Analog Considerations

2.1 REFERENCE AND INPUT

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing $V_{REF}(V_{REF}=V_{REF}(+)-V_{REF}(-))$ to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF}=2V$ then 1 LSB = 7.8 mV). The input/reference arrangement also facilitates ratiometric operation and in many cases the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. *Figure 9* shows some of the configurations that are possible.

2.2 INPUT CURRENT

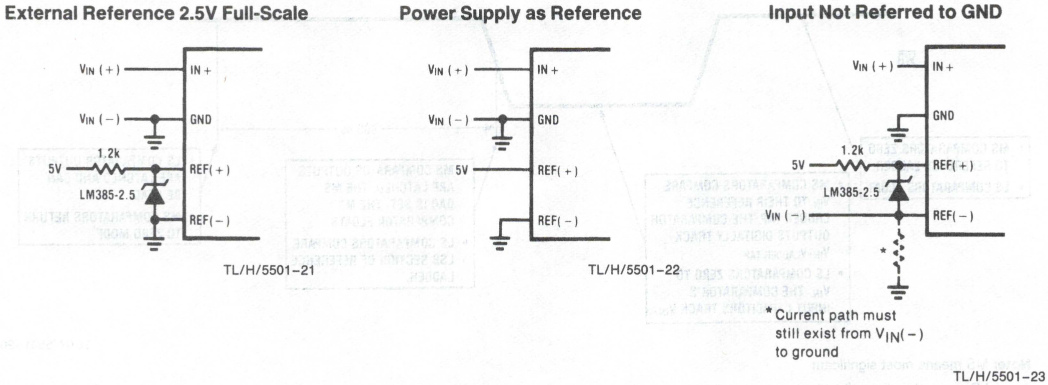
Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the ADC0820 is shown in *Figure 10a*. When a conversion starts ($\overline{WR}$ low, WR-RD mode), all input switches close, connecting V_{IN} to thirty-one 1 pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase (Section 1.3). In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5 kΩ to 10 kΩ). In addition, about 12 pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in *Figure 10b*. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800 ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is low. Since other factors force this time to be at least 600 ns, input time constants of 100 ns can be accommodated without special consideration. Typical total input capacitance values of 45 pF allow R_S to be 1.5 kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

2.0 Analog Considerations (Continued)


External Reference 2.5V Full-Scale

Power Supply as Reference

Input Not Referred to GND

VIN (+)
IN+
VIN (−)
GND
1.2k
5V
REF(+)
LM385-2.5
REF(−)
TL/H/5501-21
VIN (+)
IN+
VIN (−)
GND
5V
REF(+)
REF(−)
TL/H/5501-22
VIN (+)
IN+
GND
1.2k
5V
REF(+)
LM385-2.5
VIN (−)
REF(−)
*
TL/H/5501-23

* Current path must still exist from $V_{IN}(-)$ to ground

FIGURE 9. Analog Input Options

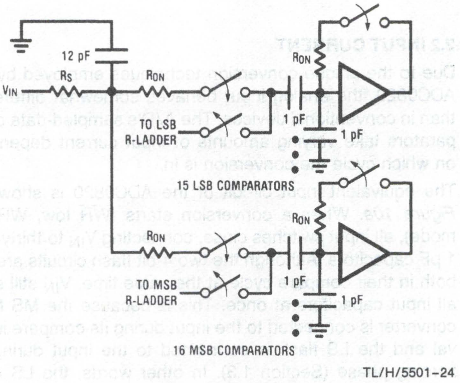

12 pF
RS
VIN
RON
RON
TO LSB
R-LADDER
1 pF
1 pF
15 LSB COMPARATORS
RON
RON
TO MSB
R-LADDER
1 pF
1 pF
16 MSB COMPARATORS
TL/H/5501-24

FIGURE 10a

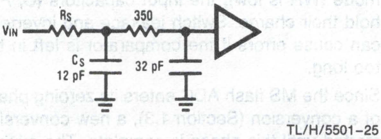

RS
350
VIN
CS
12 pF
32 pF
TL/H/5501-25

FIGURE 10b

2.3 INPUT FILTERING

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is low, so at least 600 ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients by putting an external cap on the V_{IN} terminal.

2.4 INHERENT SAMPLE-HOLD

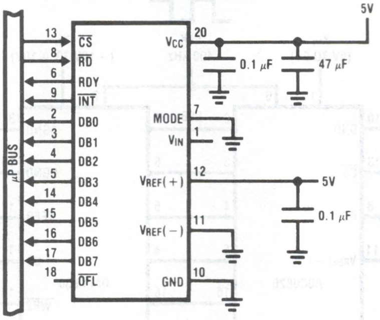
Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least ½ LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled-data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5 μs, the time through which V_{IN} must be 1/2 LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when $\overline{WR}$ is low (Sections 1.3 and 2.2). Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100 ns after the rising edge of $\overline{WR}$ (100 ns due to internal logic prop delay) will be the measured value.

Input signals with slew rates typically below 100 mV/μs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1 μs would still not be able to measure a 5V 1 kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7 kHz waveforms.

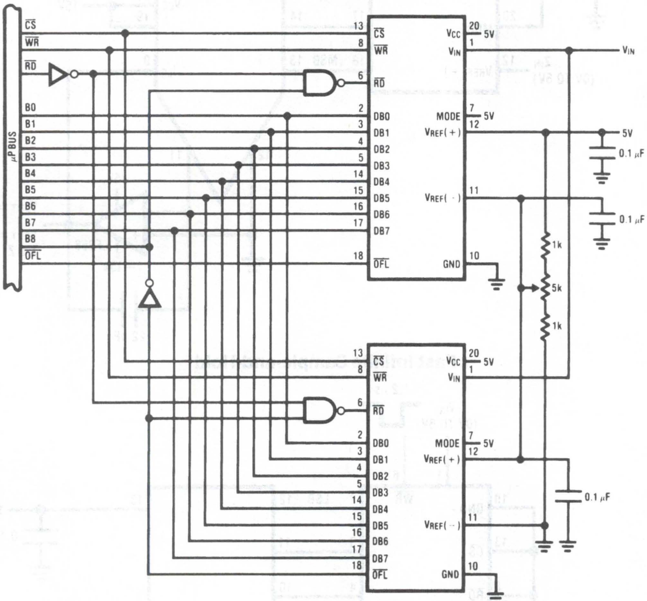
3.0 Typical Applications

8-Bit Resolution Configuration


μP BUS
13
8
6
9
2
3
4
5
14
15
16
17
18
CS
RD
RDY
INT
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
OFL
VCC
MODE
VIN
VREF(+)
VREF(−)
GND
20
7
1
12
11
10
5V
0.1 μF
47 μF
5V
0.1 μF

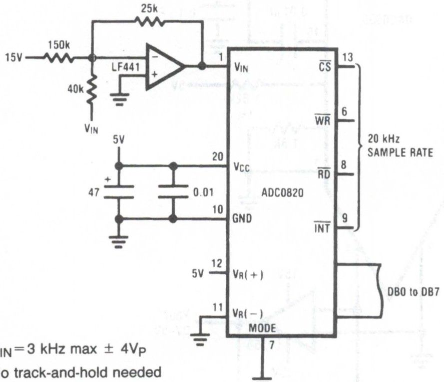
TL/H/5501-26

9-Bit Resolution Configuration


μP BUS
CS
WR
RD
B0
B1
B2
B3
B4
B5
B6
B7
B8
OFL
13
8
6
2
3
4
5
14
15
16
17
18
CS
WR
RD
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
OFL
VCC
VIN
MODE
VREF(+)
VREF(−)
GND
20
1
7
12
11
10
5V
VIN
5V
5V
0.1 μF
0.1 μF
1k
5k
1k
5V
5V
0.1 μF

TL/H/5501-27

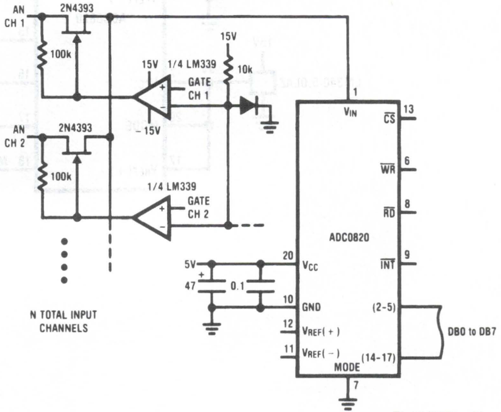
Telecom A/D Converter


25k
150k
15V
LF441
40k
VIN
1
VIN
CS
13
WR
6
RD
8
INT
9
20 kHz
SAMPLE RATE
5V
20
VCC
47
0.01
ADC0820
10
GND
5V
12
VR(+)
11
VR(−)
MODE
7
DB0 to DB7

- V_{IN} = 3 kHz max ± $4V_P$
- No track-and-hold needed
- Low power consumption

TL/H/5501-28

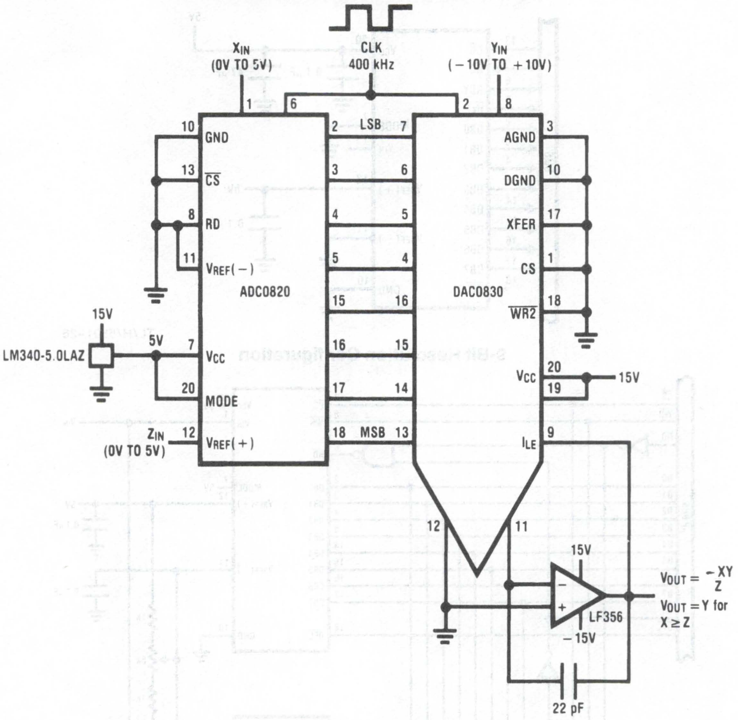
Multiple Input Channels


AN
CH 1
2N4393
100k
15V
15V
1/4 LM339
10k
GATE
CH 1
−15V
AN
CH 2
2N4393
100k
1/4 LM339
GATE
CH 2
N TOTAL INPUT
CHANNELS
1
VIN
CS
13
WR
6
RD
8
ADC0820
5V
47
0.1
20
VCC
INT
9
10
GND
(2-5)
12
VREF(+)
11
VREF(−)
MODE
(14-17)
7
DB0 to DB7

TL/H/5501-29

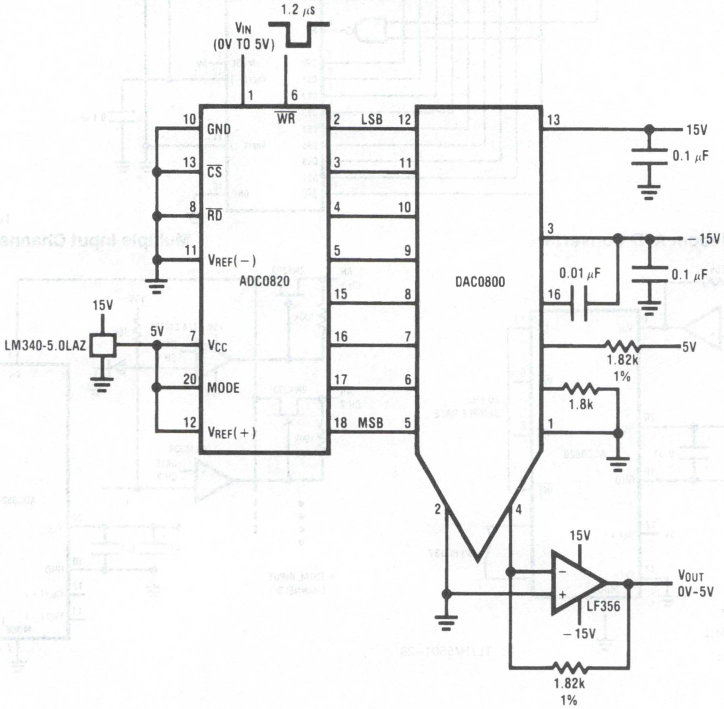
3.0 Typical Applications (Continued)

8-Bit 2-Quadrant Analog Multiplier


XIN
(0V TO 5V)
CLK
400 kHz
YIN
(−10V TO +10V)
1
6
2
8
10
GND
13
CS
8
RD
11
VREF(−)
ADC0820
15V
LM340-5.0LAZ
5V
7
VCC
20
MODE
ZIN
(0V TO 5V)
12
VREF(+)
2
LSB
7
3
6
4
5
5
4
15
16
16
15
17
14
18
MSB
13
AGND
3
DGND
10
XFER
17
CS
1
DAC0830
WR2
18
VCC
20
19
15V
ILE
9
12
11
15V
LF356
−15V
22 pF
VOUT = −XY/Z
VOUT = Y for X ≥ Z

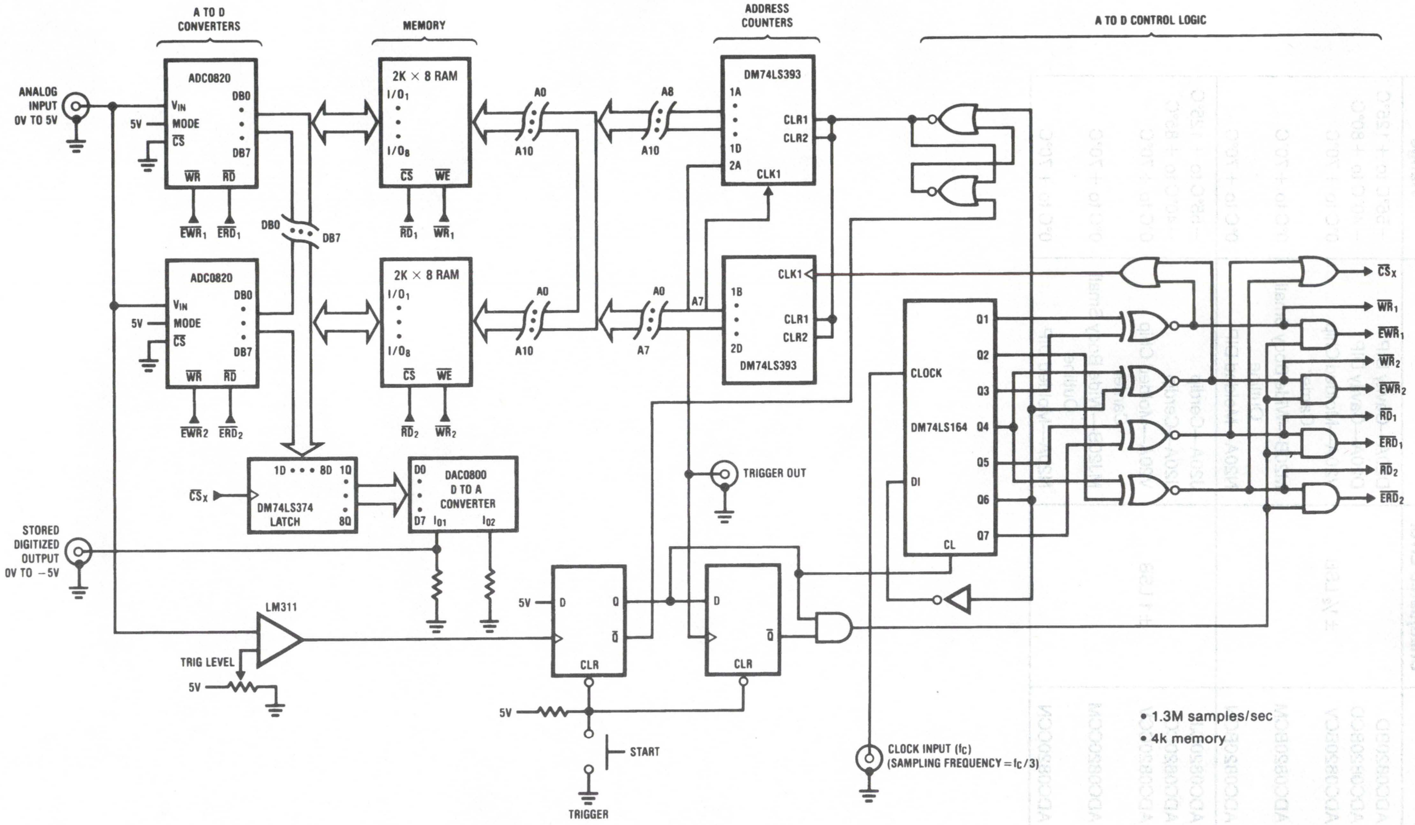
TL/H/5501-30

Fast Infinite Sample-and-Hold


VIN
(0V TO 5V)
1.2 μs
1
6
WR
10
GND
13
CS
8
RD
11
VREF(−)
ADC0820
15V
LM340-5.0LAZ
5V
7
VCC
20
MODE
12
VREF(+)
2
LSB
12
3
11
4
10
5
9
15
8
16
7
17
6
18
MSB
5
DAC0800
13
15V
0.1 μF
3
−15V
0.01 μF
16
0.1 μF
1.82k
1%
5V
1.8k
1
2
4
15V
LF356
−15V
VOUT
0V-5V
1.82k
1%

TL/H/5501-31

Digital Waveform Recorder


A TO D CONVERTERS
MEMORY
ADDRESS COUNTERS
A TO D CONTROL LOGIC
ANALOG INPUT 0V TO 5V
ADC0820
VIN
MODE
CS
WR
RD
DB0
DB7
5V
EWR1
ERD1
EWR2
ERD2
2K × 8 RAM
I/O1
I/O8
CS
WE
RD1
WR1
RD2
WR2
A0
A10
A8
A7
DM74LS393
1A
1D
2A
1B
2D
CLR1
CLR2
CLK1
DM74LS374 LATCH
1D
8D
1Q
8Q
CSX
DAC0800 D TO A CONVERTER
D0
D7
IO1
IO2
STORED DIGITIZED OUTPUT 0V TO −5V
LM311
TRIG LEVEL
D
Q
Q̄
CLR
START
TRIGGER
TRIGGER OUT
CLOCK
DM74LS164
DI
CL
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CLOCK INPUT (fC) (SAMPLING FREQUENCY = fC/3)
WR1
EWR1
WR2
EWR2
RD1
ERD1
RD2
ERD2

- 1.3M samples/sec
- 4k memory

TL/H/5501-32

Ordering Information

Part Number	Total Unadjusted Error	Package	Temperature Range
ADC0820BD	±½ LSB	D20A—Cavity DIP	−55°C to +125°C
ADC0820BCD		D20A—Cavity DIP	−40°C to +80°C
ADC0820BCV		V20A—Molded Chip Carrier	0°C to +70°C
ADC0820BCM		M20B—Wide Body Small Outline	0°C to +70°C
ADC0820BCN		N20A—Molded DIP	0°C to +70°C
ADC0820CJ	±1 LSB	J20A—Cerdip	−55°C to +125°C
ADC0820CCJ		J20A—Cerdip	−40°C to +85°C
ADC0820CCV		V20A—Molded Chip Carrier	0°C to +70°C
ADC0820CCM		MJ20B—Wide Body Small Outline	0°C to +70°C
ADC0820CCN		N20A—Molded DIP	0°C to +70°C

National Semiconductor Corporation

ADC0829 μP Compatible 8-Bit A/D with 11-Channel MUX/Digital Input

General Description

The ADC0829 is an 8-bit successive approximation A/D converter with an 11-channel multiplexer of which six can be used as digital inputs, as well as, analog inputs.

This A/D is designed to operate from the μP data bus using a single 5V supply.

Channel selection, conversion control, software configuration and bus interface logic are all contained on this monolithic CMOS device.

This device contains three 16-bit registers which are accessed via double byte instructions. The control register is a write only register which controls the start of a new conversion, selects the channel to be converted, configures the 8-bit I/O port as input or output, and provides information for the 8-bit output register.

The conversion results register is a read only register which contains the current status and most recent conversion results. The discrete input register is also a read only register which contains the four address bits of the selected channel, and the six discrete inputs which are connected to the analog multiplexer.

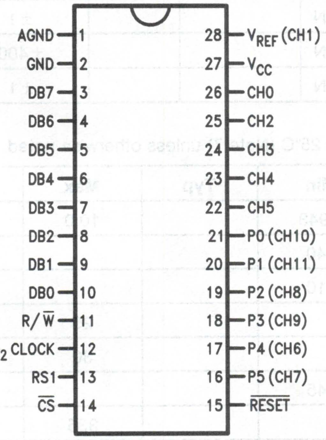
Features

- Easy interface to all microprocessors or operates "stand alone"
- Operates ratiometrically or with analog span adjusted voltage reference
- 11-Channel multiplexer with latched control logic of which six can be used as digital inputs
- 0 to 5V analog input range with single 5V supply
- TTL/MOS input/output compatible
- No zero or full scale adjusts required
- Standard 28-pin DIP
- Temperature range −40°C to +85°C

Key Specification

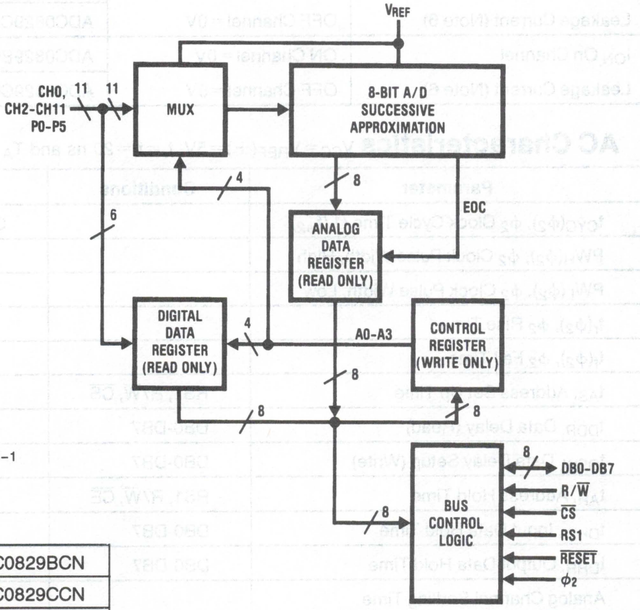
■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Conversion Time	256 μs
■ Single Supply	$5V_{DC}$
■ Low Power	50 mW

Connection and Block Diagrams


AGND 1
GND 2
DB7 3
DB6 4
DB5 5
DB4 6
DB3 7
DB2 8
DB1 9
DB0 10
R/W̄ 11
φ2 CLOCK 12
RS1 13
CS̄ 14
28 VREF (CH1)
27 VCC
26 CH0
25 CH2
24 CH3
23 CH4
22 CH5
21 P0 (CH10)
20 P1 (CH11)
19 P2 (CH8)
18 P3 (CH9)
17 P4 (CH6)
16 P5 (CH7)
15 RESET

TL/H/5508-1

Top View


VREF
CH0, CH2-CH11 P0-P5
11
11
MUX
8-BIT A/D SUCCESSIVE APPROXIMATION
4
8
6
EOC
ANALOG DATA REGISTER (READ ONLY)
DIGITAL DATA REGISTER (READ ONLY)
4
A0-A3
CONTROL REGISTER (WRITE ONLY)
8
8
8
8
8
DB0-DB7
R/W̄
CS̄
RS1
RESET
φ2
BUS CONTROL LOGIC

TL/H/5508-2

Ordering Information

Error	± 1/2 Bit Unadjusted	ADC0829BCN
	± 1 Bit Unadjusted	ADC0829CCN
Package Outline		N28B

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	$-0.3V$ to $V_{CC} + 0.3V$
Analog Inputs	$-0.3V$ to $V_{CC} + 0.3V$
Storage Temperature	$-65°C$ to $+150°C$
Package Dissipation at $T_A = 25°C$ (Board Mount)	875 mW
Lead Temp. (Soldering, 10 seconds)	260°C
ESD Susceptability (Note 8)	2000V
Input Current Per Pin	±5 mA
Package	+20 mA

Operating Conditions (Notes 1 and 2)

Supply Voltage, V_{CC}	$4.75\ V_{DC}$ to $5.5\ V_{DC}$
Temperature Range	$-40°C$ to $+85°C$

Converter and Multiplexer Electrical Characteristics

$V_{CC} = 5V_{DC} = V_{REF}(+)$, $V_{REF}(-) = GND$, SCLK $\phi_2 = 1.048$ MHz, $-40°C \le T_A \le +85°C$ unless otherwise noted.

Parameter	Conditions	Min	Typ (Notes)	Max	Units
Total Unadjusted Error; (Note 3)					
ADC0829BCN	V_{REF} Forced to 5.000 V_{DC}			±½	LSB
ADC0829CCN	V_{REF} Forced to 5.000 V_{DC}			±1	LSB
Reference Input Resistance		1.0	4.5		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND-0.10		$V_{CC}+0.10$	V
$V_{REF}(+)$ Voltage, Top of Ladder	Measured at REF(+)		V_{CC}	$V_{CC}+0.01$	V
$\frac{V_{REF}(+) + V_{REF}(-)}{2}$ Voltage, Center of Ladder		$V_{CC}/2-0.1$	$V_{CC}/2$	$V_{CC}/2+0.01$	V
$V_{REF}(-)$ Voltage, Bottom of Ladder	Measured at REF(−)	−0.1	0		V
I_{OFF}, Off Channel Leakage Current (Note 6)	ON Channel = 5V OFF Channel = 0V	ADC0829BCN		±400	nA
		ADC0829CCN		±1	μA
I_{ON}, On Channel Leakage Current (Note 6)	ON Channel = 0V OFF Channel = 5V	ADC0829BCN		±400	nA
		ADC0829CCN		±1	μA

AC Characteristics

$V_{CC} = V_{REF}(+) = 5V$, $t_r = t_f = 20$ ns and $T_A = 25°C$ (Note 7) unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
$t_{CYC}(\phi_2)$, ϕ_2 Clock Cycle Time ($1/f_{\phi 2}$)		0.943		10.0	μs
$PW_H(\phi_2)$, ϕ_2 Clock Pulse Width, High		440			ns
$PW_L(\phi_2)$, ϕ_2 Clock Pulse Width, Low		410			ns
$t_r(\phi_2)$, ϕ_2 Rise Time				25	ns
$t_f(\phi_2)$, ϕ_2 Fall Time				30	ns
t_{AS}, Address Set Up Time	RS1, $R/\overline{W}$, $\overline{CS}$	145			ns
t_{DDR}, Data Delay (Read)	DB0-DB7			335	ns
t_{DSW}, Data Delay Setup (Write)	DB0-DB7	185			ns
t_{AH}, Address Hold Time	RS1, $R/\overline{W}$, $\overline{CE}$	20			ns
t_{DHW}, Input Data Hold Time	DB0-DB7	20			ns
t_{DHR}, Output Data Hold Time	DB0-DB7	10			ns
Analog Channel Settling Time		32			Clocks
t_c, Conversion Time		256			Clocks

Digital and DC Characteristics $V_{CC} = 4.5V$ to $5.5V$ and $-40°C \leq T_A \leq 85°C$ unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Bus Control Inputs (R/$\overline{W}$, ENABLE $\overline{RESET}$, RS1, $\overline{CS}$) and Peripheral Inputs (P0-P5)					
$V_{IN}(1)$, Logical "1" Input Voltage		2.0			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.8	V
I_{IN}, Input Leakage Current				±1	μA
ϕ_2 CLOCK INPUT					
$V_{IN}(1)$, Logical "1" Input Voltage		$V_{CC}-0.8$			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.4	V
Data Bus (DB0-DB7)					
$V_{IN}(1)$, Logical "1" Input Voltage		2.0			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.8	V
I_{OUT}, TRI-STATE® Output Current	$V_{OUT}=0V$			−10	μA
	$V_{OUT}=5V$			10	μA
$V_{OUT}(1)$, Logical "1" Output Voltage	$I_{OUT}=-1.6$ mA	2.4			V
$V_{OUT}(0)$, Logical "0" Output Voltage	$I_{OUT}=1.6$ mA			0.4	V
Power Supply Requirements					
I_{CC}, Supply Current				10	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.90 V_{DC} over temperature variations, initial tolerance and loading.

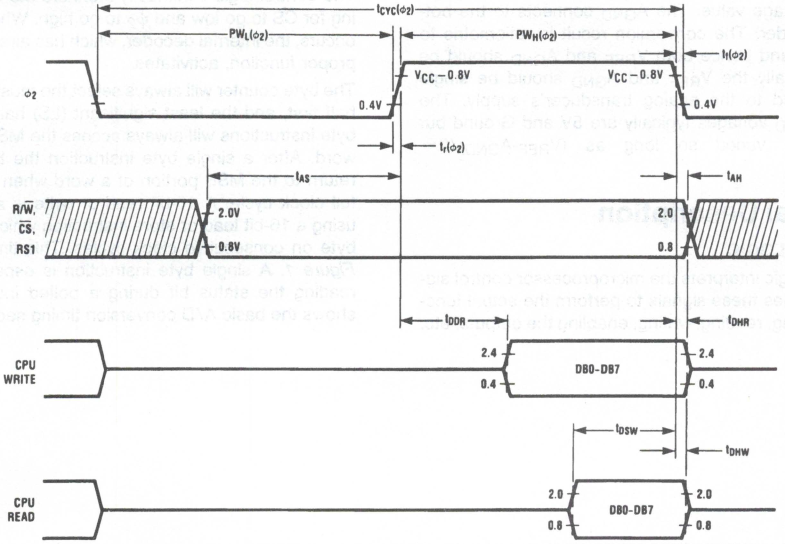
Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Off channel leakage current is measured after the channel selection.

Note 7: The temperature coefficient is 0.3%/°C.

Note 8: Human Body Model, 100 pF discharged through a 1.5 kΩ resistor.

Timing Diagram



TL/H/5508-3

Pin Descriptions

ANALOG AND DIGITAL INPUTS

CH0, CH2-CH5—These are dedicated analog inputs. They are fed directly to the internal 12 to 1 multiplexer which feeds the A/D converter.

P0-P5/CH6-CH11—These 6 pins are dual purpose and may be used as either TTL compatible digital inputs, or analog inputs. When used as digital inputs they may be read via the discrete input register. When they are used as analog inputs they function like CH-0, CH2-5.

MICROPROCESSOR INTERFACE SIGNALS

DB0-DB7—The bi-directional data lines for the data bus connect to the μP's main data bus to enable data transfer to and from the μP. DB0-DB7 remain in a high impedance state unless the ADC0829 is read.

ϕ_2 Clock—This signal is used for two purposes. First it synchronizes data transfer in and out of the ADC. Second, it is the master clock for the A/D converter logic and all other timing signals are derived from it.

R/$\overline{\text{W}}$—The read/write pin controls the direction of data transfer on D0-D7.

$\overline{\text{RESET}}$—A low on this pin forces the ADC0829 into a known state. The start bit is cleared, Channel CH0 is selected and the internal byte counter is reset to the MS Byte. The A/D data register is not reset. Reset must be held low for at least 3 clocks.

$\overline{\text{CS}}$—Chip Select must be low in order for data transfer between the ADC0829 and the μP to occur.

RS1—The Register Select pin is used to address the internal registers.

POWER SUPPLY PINS

V_{CC}—This is the positive 5V supply pin. It powers the digital load and the sample data comparator. Care should be exercised to ensure that supply noise on this pin is adequately filtered, by using a bypass capacitor from V_{CC} to D_{GND}.

D_{GND}—Digital ground should be connected to the systems digital ground.

V_{REF} and A_{GND}—The positive reference pin attaches to the top of the 256R resistor ladder and sets the full scale conversion voltage value. The A_{GND} connects to the bottom of the ladder. The conversion result is ratiometric to V_{REF} - A_{GND} and hence both V_{REF} and A_{GND} should be noise free. Ideally the V_{REF} and A_{GND} should be single point connected to the analog transducer's supply. The V_{REF} and A_{GND} voltages typically are 5V and Ground but they may be varied so long as $(V_{REF}\text{-}A_{GND})/2 = V_{CC}/2 \pm 0.1V$.

Functional Description

1.0 CONTROL LOGIC

The Control Logic interprets the microprocessor control signals and decodes these signals to perform the actual functions of selecting, reading, writing, enabling the outputs, etc.

2.0 STATE DESCRIPTIONS

There are three internal states within the A/D converter: the NO OP state; the sample state; and the converting state.

The NO OP state is a stable state since the external stimulus (e.g. start conversion signal) is needed for a state transition.

The first transient state is sampling the input. The first 32 clocks of the conversion are used for acquiring the channel; this settling time allows any transients to decay before conversion begins. The second transient state is the actual conversion. The conversion is completed in 256 clocks and the conversion results register is updated. The converter then returns to the stable NO OP state awaiting further instructions.

The device has no comparator bias current and draws minimal power during the NO OP state.

3.0 INITIALIZATION

The device is initialized by an active low on $\overline{\text{RESET}}$. All outputs are initialized to the inactive state and the converter placed in its NO OP state. The data register is not affected by $\overline{\text{RESET}}$. System TRI-STATE outputs are initialized to the high impedance state.

4.0 CONVERSION CONTROL

The program normally initiates a conversion cycle with a double write command. (See control word format.) The control word selects a channel, configures the peripheral I/O, and provides peripheral data information. The conversion is initiated by setting the SC bit in the control word high.

The converter then resets the start conversion bit and begins the conversion cycle.

When the conversion is complete and the new conversion results transferred to the data register, the status bit is set. The status bit is not reset when the conversion status is read. A full double byte write into the control word will reset the status bit, or a low level at master $\overline{\text{RESET}}$.

If a new conversion command occurs during a conversion, the conversion is aborted and a new channel acquisition phase will immediately begin.

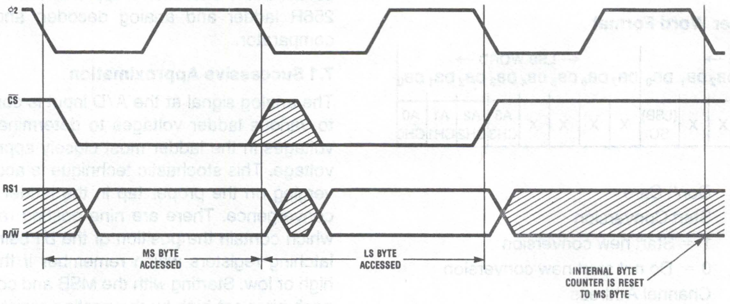
5.0 CONTROL STRUCTURE

The control logic continually monitors the control bus waiting for $\overline{\text{CS}}$ to go low and ϕ_2 to go high. When this condition occurs, the internal decoder, which has already selected the proper function, activitates.

The byte counter will always select the most significant (MS) half first, and the least significant (LS) half second. Single byte instructions will always access the MSB portion of any word. After a single byte instruction the byte counter will return to the MSB portion of a word when $\overline{\text{CS}}$ is high for a full clock cycle. A 16-bit read or write is accomplished by using a 16-bit load or store instruction which transfers each byte on consecutive clock cycles. This timing is shown in *Figure 1*. A single byte instruction is especially useful for reading the status bit during a polled interrupt. *Figure 2* shows the basic A/D conversion timing sequence and flow.

Functional Description (Continued)

Timing for a Typical µP 16 Byte Access


φ2
CS
RS1
R/W
MS BYTE ACCESSED
LS BYTE ACCESSED
INTERNAL BYTE COUNTER IS RESET TO MS BYTE

Timing for a Typical µP 8 Byte Access

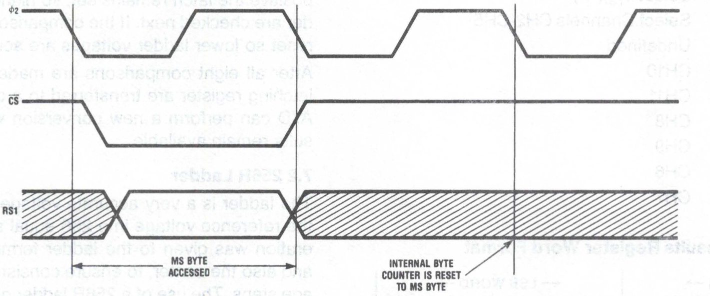

φ2
CS
RS1
MS BYTE ACCESSED
INTERNAL BYTE COUNTER IS RESET TO MS BYTE

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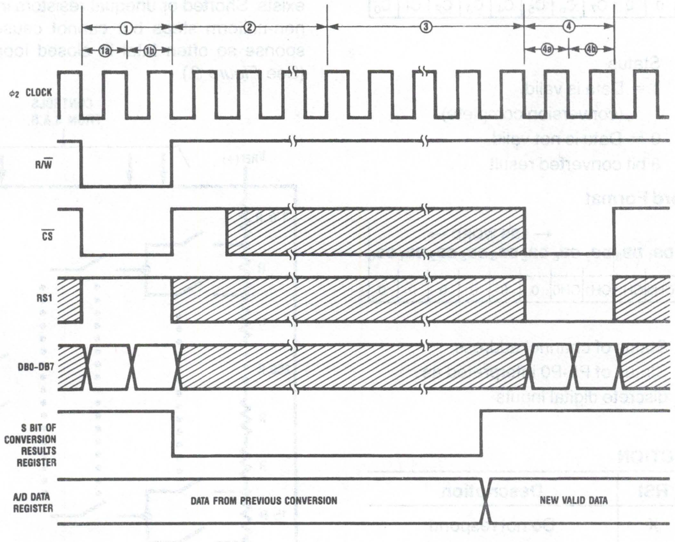
FIGURE 1


①
②
③
④
ⓐ
ⓑ
ⓐ
ⓑ
φ2 CLOCK
R/W
CS
RS1
DB0-DB7
S BIT OF CONVERSION RESULTS REGISTER
A/D DATA REGISTER
DATA FROM PREVIOUS CONVERSION
NEW VALID DATA

① START CONVERSION
  ⓐ SET SC BIT TO A 1
  ⓑ LOAD ADDRESS
② ANALOG INPUT SETTLING TIME ALLOWS INTERNAL MULTIPLEXER TO SELECT A CHANNEL AND STABILIZE (~32 CLOCKS).
③ A/D CONVERSION TIME (~256 CLOCKS)
④ READ END OF CONVERSION DATA
  ⓐ EOC BIT READ IF A 1 CONVERSION COMPLETE.
  ⓑ A/D DATA REGISTER READ. IF EOC = 1, THEN NEW VALID DATA.

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FIGURE 2. A/D Conversion Timing Sequence

Functional Description (Continued)

6.0 WORD FORMAT

6.1 Control Register Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
X	X	X	X	X	X	X	(LSB) SC	X	X	X	X	A3 CH3	A2 CH2	A1 CH1	A0 CH0

X:	Don't Care
SC:	Start Conversion
	1 = Start new conversion
	0 = Do not start new conversion
CH3-CH0:	Channel Address
Hex Value	Definition
0	Select CH0
1	Select $V_{ref}(+)$
2-5	Select Channels CH2-CH5
6-9	Undefined
A	CH10
B	CH11
C	CH8
D	CH9
E	CH6
F	CH7

6.2 Conversion Results Register Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
S	0	0	0	0	0	0	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

S:	Status
	1 = Data is valid (conversion complete)
	0 = Data is not valid
C_7-C_0:	8 bit converted result

6.3 Discrete Input Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
P5	P4	P3	P2	P1	P0	CH3	CH2	CH1	CH0	0	0	0	0	0	0

CH3-CH0:	Status of channel address
P5-P0:	Status of P5-P0 interpreted as discrete digital inputs

ADU ADDRESS SELECTION

CSO*	R/W	RSI	Description
1	X	X	Do not respond
0	0	0	Write NO OP
0	0	1	Write Control Word
0	1	0	Read Conversion Results
0	1	1	Read Discrete Inputs

Note: All words are transferred as two 8-bit bytes, MSB transferred first LSB transferred second.

7.0 ANALOG TO DIGITAL CONVERTER

The ADC0829 A/D Converter is composed of three major sections: the successive approximation register (SAR); the 256R ladder and analog decoder; and the sample-data comparator.

7.1 Successive Approximation

The analog signal at the A/D input is compared eight times to various ladder voltages to determine which of the 256 voltages in the ladder most closely approximates the input voltage. This stochastic technique is accomplished by converging on the proper tap in the ladder by simple iterative convergence. There are nine posting registers in the SAR which contain the position of the bit being tested and eight latching registers which remember if the comparison was high or low. Starting with the MSB and continuing downward each bit is set high by the posting register. The analog tree decoder selects the corresponding tap in the ladder and the A/D input is compared to that voltage. If the comparison is positive the latch remains set, so higher voltages in the ladder are checked next. If the comparison is negative the bit is reset so lower ladder voltages are sought.

After all eight comparisons are made, the contents of the latching register are transferred to a data register, thus the A/D can perform a new conversion while the previous results remain available.

7.2 256R Ladder

The ladder is a very accurate voltage divider which divides the reference voltage into 256 equal steps. Special consideration was given to the ladder terminations at each end, and also the center, to ensure consistent and accurate voltage steps. The use of a 256R ladder guarantees monotonicity since only a single voltage gradient across the ladder exists. Shorted or unequal resistors in the ladder may cause non-uniform steps but cannot cause a nonmonotonic response so often fatal in closed loop system applications. (See *Figure 3.*)

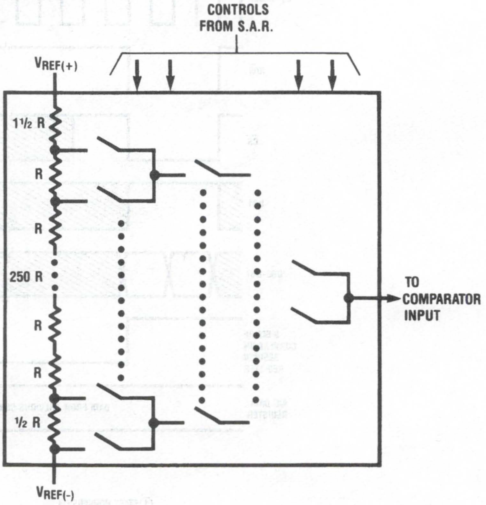

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FIGURE 3. Resistor Ladder and Switch Tree

Functional Description (Continued)

Actually of the 256 resistors in the ladder, 254 have the same value while the end point resistors are equal to 1-1/2R and 1/2R. This ensures the system output characteristic is symmetrical with the zero and full scale points of its input to output, or transfer curve.

The tree decoder routes the 256 voltages from the ladder to a single point at the comparator input. This allows comparisons between the A/D input and any voltage the SAR directs the decoder to route to the comparator.

Since the ladder is dependent upon only the matching of resistors, the voltages it generates are very stable with temperature and have excellent repeatability and long term drift.

8.0 MULTIPLEXER

8.1 Analog Inputs

The analog multiplexer selects one of 11 channels and directs them to the input of the A/D converter. The multiplexer was designed to minimize the effects of leakage currents and multiplexer output capacitance.

Special input protection is used to prevent damage from static voltages or voltages exceeding the specified range from −0.3V to $V_{CC}+0.3V$. However, normal precautions are recommended to avoid such situations whenever possible.

8.2 Digital Inputs

Six of the analog inputs can also be used as digital inputs to sense TTL voltage levels. Care must be taken when these inputs are interpreted since TTL levels may not always be present.

8.3 A/D Comparator

Probably the most important section of the A/D converter is the comparator since the comparator's offset voltage and stability determine the converter's ultimate accuracy. The low voltage offset of the chopper-stabilized comparator of this converter optimizes performance by minimizing temperature dependent input offset errors as well as drift.

The dc signal appearing at the amplifier input is converted to an ac signal, amplified by an ac amplifier and restored to a dc signal. The drift of the comparator is minimized since the drift signal is a dc component blocked by the ac amplifier.

The comparator has very high input impedance to dc voltages since it looks like a capacitor. Because the comparator is chopping the dc voltages at the input, the difference between the A/D input voltage and ladder voltage appears on the comparator's input capacitor. The input voltage difference, chopping frequency, and comparator input capacitor causes a CVF current. The CVF current is a small bias current which will not produce any error when the A/D input is connected to a low impedance voltage source. If the voltage source has an output impedance of less than 10k, the error is still insignificant since the bias current exponentially decays.

Adding a capacitor to the input of the comparator integrates the exponential charging current converting it into dc bias current. (See Figure 1.) Two main considerations on the integration capacitor are charge sharing with a filter capacitor and settling time.

9.0 BUS INTERFACE

The ADC0829 communicates to the microprocessor through an 8-bit I/O port. The I/O port is composed of a TTL to CMOS buffer and a TRI-STATE® output driver.

The TTL to CMOS Buffer translates the TTL voltage levels into CMOS levels very rapidly and is quite stable with supply and temperature. The buffer has a small amount of hysteresis (about 100 mV) to improve both noise immunity and internal rise and fall times.

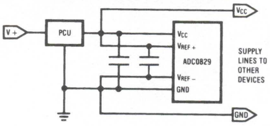
The TRI-STATE bus driver is a bipolar and N-channel pair that easily drive the bus capacitance. Since the bus drivers collectively can sink or source a quarter of an amp total, a non-overlap circuit is used which guarantees that only one of the two drive transistors is on at a time.

Since this output drives the bus capacitance, even the non-overlapping circuit cannot prevent noise on V_{CC}. The amount of noise depends on the V_{CC} current used to charge the bus capacitance.

The external filter capacitor on V_{CC} provides some of the transient current while the bus is being driven. A capacitor with good ac characteristics and low series resistance is a good choice to prevent V_{CC} transients from affecting accuracy.

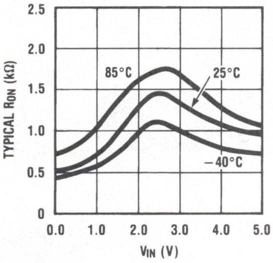
Application Information

Recommended Supply



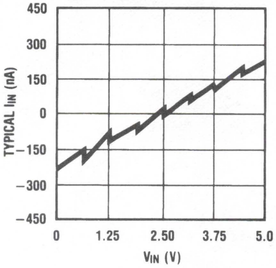
TL/H/5508-7

Multiplexer R_{ON} vs V_{IN} ($V_{CC}=V_{REF}=5V$)



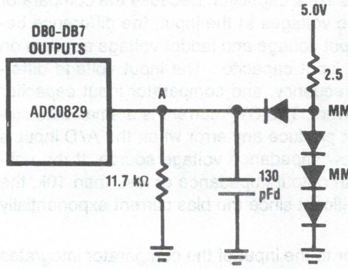
TL/H/5508-8

Comparator I_{IN} vs V_{IN} ($V_{CC}=V_{REF}=5V$, $f_c=1.048$ MHz)



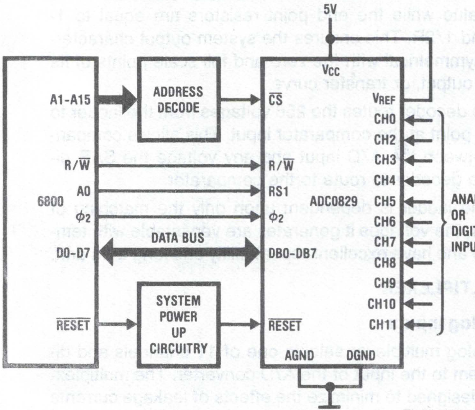
TL/H/5508-9

Data Bus Test Circuit


5.0V
DB0-DB7 OUTPUTS
ADC0829
A
2.5 kΩ
MMD6150 OR EQUIV.
MMD7000 OR EQUIV.
11.7 kΩ
130 pFd

TL/H/5508-10

Typical Application


5V
VCC
A1-A15
ADDRESS DECODE
CS
VREF
CH0
CH2
CH3
R/W
CH4
6800
A0
RS1
ADC0829
CH5
ϕ2
ϕ2
CH6
DATA BUS
CH7
D0-D7
DB0-DB7
CH8
CH9
ANALOG OR DIGITAL INPUTS
SYSTEM POWER UP CIRCUITRY
CH10
RESET
RESET
CH11
AGND
DGND

TL/H/5508-11

National
Semiconductor
Corporation

ADC0831/ADC0832/ADC0834 and ADC0838 8-Bit Serial I/O A/D Converters with Multiplexer Options

General Description

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or μPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

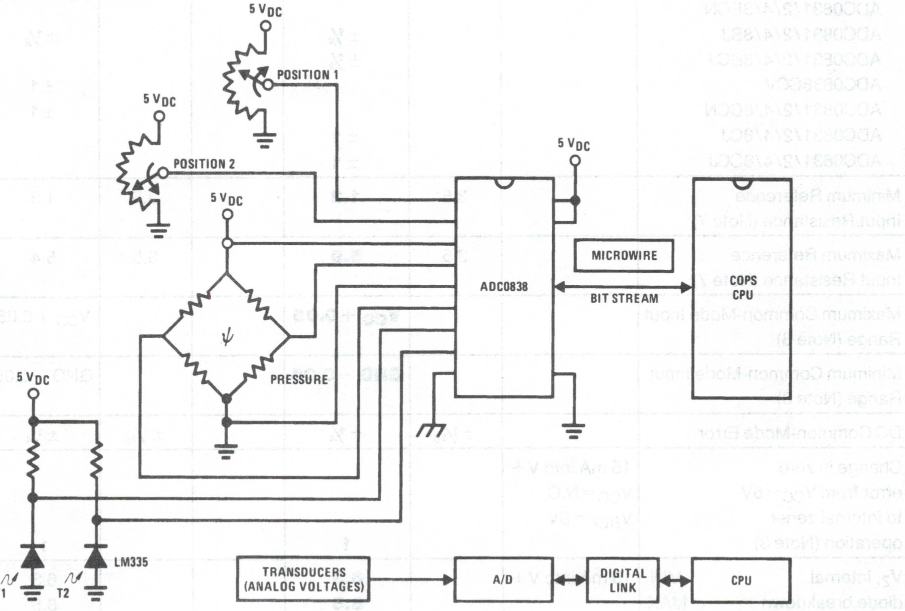
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand-alone"
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 2-, 4- or 8-channel multiplexer options with address logic
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- TTL/MOS input/output compatible
- 0.3″ standard width, 8-, 14- or 20-pin DIP package
- 20 Pin Molded Chip Carrier Package (ADC0838 only)

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	32 μs

Typical Application



TL/H/5583–1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to V_{CC} + 0.3V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 4)	±5 mA
Package	±20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at $T_A = 25°C$ (Board Mount)	0.8W
Lead Temperature (Soldering 10 sec.)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Susceptibility (Note 5)	2000V

Operating Ratings (Notes 1 & 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0831/2/4/8BJ ADC0831/2/4/8CJ	−55°C to +125°C
ADC0831/2/4/8BCJ ADC0831/2/4/8CCJ	−40°C to +85°C
ADC0831/2/4/8BCN ADC0838BCV ADC0831/2/4/8CCN ADC0838CCV	−0°C to +70°C

Converter and Multiplexer Electrical Characteristics

The following specifications apply for $V_{CC} = V+ = V_{REF} = 5V$, $V_{REF} \leq V_{CC} + 0.1V$, $T_A = T_j = 25°C$, and $f_{CLK} = 250$ kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	BJ, CJ, BCJ and CCJ Devices			BCV, CCV, BCN and CCN Devices			Units
		Typ (Note 12)	**Tested Limit (Note 13)**	**Design Limit (Note 14)**	**Typ (Note 12)**	**Tested Limit (Note 13)**	**Design Limit (Note 14)**	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Total Unadjusted Error	$V_{REF} = 5.00$ V (Note 6)							LSB
ADC0838BCV						±½	±½	
ADC0831/2/4/8BCN							**±½**	
ADC0831/2/4/8BJ			**±½**			±½		
ADC0831/2/4/8BCJ			**±½**					
ADC0838CCV						±1	±1	
ADC0831/2/4/8CCN						±1	**±1**	
ADC0831/2/4/8CJ			**±1**					
ADC0831/2/4/8CCJ			**±1**					
Minimum Reference Input Resistance (Note 7)		3.5	**1.3**		3.5	1.3	**1.3**	kΩ
Maximum Reference Input Resistance (Note 7)		3.5	**5.9**		3.5	5.4	**5.9**	kΩ
Maximum Common-Mode Input Range (Note 8)			**V_{CC} + 0.05**			V_{CC} + 0.05	**V_{CC} + 0.05**	V
Minimum Common-Mode Input Range (Note 8)			**GND − 0.05**			GND − 0.05	**GND − 0.05**	V
DC Common-Mode Error		±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
Change in zero error from $V_{CC} = 5V$ to internal zener operation (Note 3)	15 mA into V+ V_{CC} = N.C. $V_{REF} = 5V$		**1**			1	**1**	LSB
V_Z, internal diode breakdown (at V_+) (Note 3) MIN MAX	15 mA into V+		**6.3** **8.5**			6.3 8.5	**6.3** **8.5**	V
Power Supply Sensitivity	$V_{CC} = 5V \pm 5\%$	±1/16	**±¼**	±¼	±1/16	±¼	**±¼**	LSB

Converter and Multiplexer Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = V+ = 5V$, $T_A = T_j = 25°C$, and $f_{CLK} = 250$ kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	BJ, CJ, BCJ and CCJ Devices			BCV, CCV, BCN and CCN Devices			Units
		Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)								
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel = 5V Off Channel = 0V		**−0.1**	**−1**		−0.2	**−1**	μA
	On Channel = 0V Off Channel = 5V		**+0.1**	**+1**		+0.2	**+1**	μA
I_{ON}, On Channel Leakage Current (Note 9)	On Channel = 0V Off Channel = 5V		**−0.1**	**−1**		−0.2	**−1**	μA
	On Channel = 5V Off Channel = 0V		**+0.1**	**+1**		+0.2	**+1**	μA
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	$V_{CC} = 5.25V$		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	$V_{CC} = 4.75V$		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	$V_{IN} = 5.0V$	0.005	**1**		0.005	1	**1**	μA
$I_{IN(0)}$, Logical "0" Input Current (Max)	$V_{IN} = 0V$	−0.005	**−1**		−0.005	−1	**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	$V_{CC} = 4.75V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **4.5**			2.4 4.5	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	$V_{CC} = 4.75V$ $I_{OUT} = 1.6$ mA		**0.4**			0.4	**4.0**	V
I_{OUT}, TRI-STATE Output Current (Max)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−0.1 0.1	**−3** **3**		−0.1 0.1	−3 +3	**−3** **+3**	μA μA
I_{SOURCE}, Output Source Current (Min)	$V_{OUT} = 0V$	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)	$V_{OUT} = V_{CC}$	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max) ADC0831, ADC0834, ADC0838		0.9	**2.5**		0.9	2.5	**2.5**	mA
ADC0832	Includes Ladder Current	2.3	**6.5**		2.3	6.5	**6.5**	mA

AC Characteristics

The following specifications apply for $V_{CC} = 5V$, $t_r = t_f = 20$ ns and 25°C unless otherwise specified.

Parameter		Conditions	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Limit Units
f_{CLK}, Clock Frequency	Min			10		kHz
	Max				400	kHz
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle (Note 10)	Min				40	%
	Max				60	%
t_{SET-UP}, $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge					250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge					90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 11)		$C_L = 100$ pF				
		Data MSB First	650		1500	ns
		Data LSB First	250		600	ns
t_{1H}, t_{0H},—Rising Edge of CS to Data Output and SARS Hi-Z		$C_L = 10$ pF, $R_L = 10k$ (see TRI-STATE® Test Circuits)	125		250	ns
		$C_L = 100$ pf, $R_L = 2k$		500		ns
C_{IN}, Capacitance of Logic Input			5			pF
C_{OUT}, Capacitance of Logic Outputs			5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground plugs.

Note 3: Internal zener diodes (6.3 to 8.5V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore guaranteed for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+. (See *Figure 3* in Functional Description Section 6.0)

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V-$ or $V_{IN} > V+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

Note 7: Cannot be tested for ADC0832.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater then the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 1 µs. The maximum time the clock can be high is 60 µs. The clock can be stopped when low so long as the analog input voltage remains stable.

Note 11: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

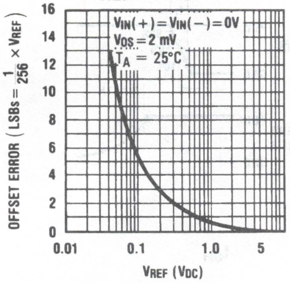
Note 12: Typicals are at 25°C and represent most likely parametric norm.

Note 13: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

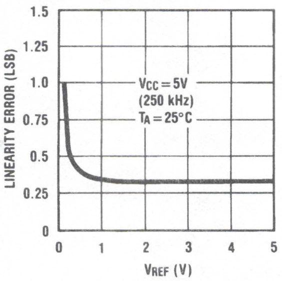
Note 14: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Performance Characteristics

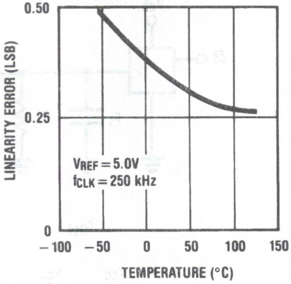
Unadjusted Offset Error vs V_{REF} Voltage



Linearity Error vs V_{REF} Voltage



Linearity Error vs Temperature



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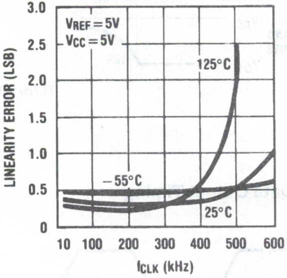
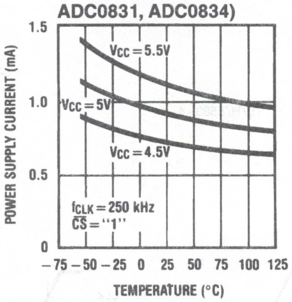
Linearity Error vs f_{CLK}

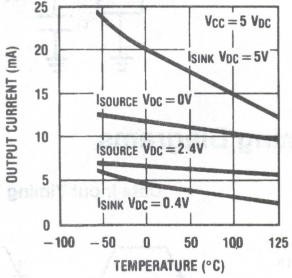


Power Supply Current vs Temperature (ADC0838, ADC0831, ADC0834)



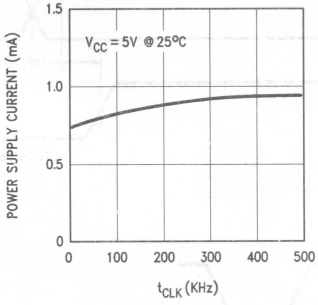
Note: For ADC0832 add I_{REF}.

Output Current vs Temperature



TL/H/5583-40

Power Supply Current vs f_{CLK}



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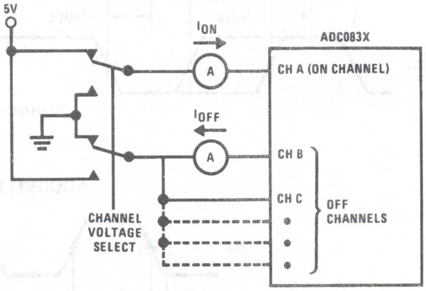
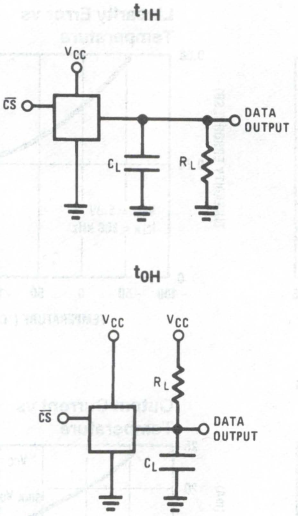
Leakage Current Test Circuit


5V
I_{ON}
ADC083X
A
CH A (ON CHANNEL)
I_{OFF}
A
CH B
CH C
OFF CHANNELS
CHANNEL VOLTAGE SELECT

TL/H/5583-3

TRI-STATE Test Circuits and Waveforms


t_{1H}
V_{CC}
$\overline{CS}$
DATA OUTPUT
C_L
R_L
t_{0H}
V_{CC}
V_{CC}
R_L
$\overline{CS}$
DATA OUTPUT
C_L

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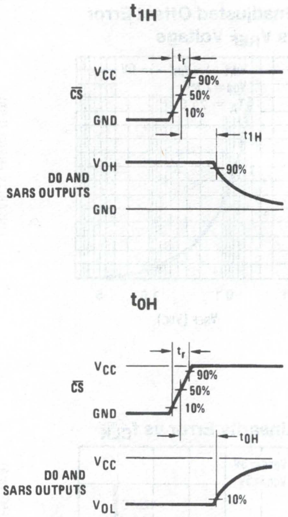
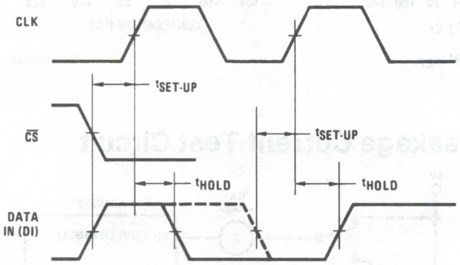

t_{1H}
t_r
V_{CC}
$\overline{CS}$
90%
50%
10%
GND
t_{1H}
V_{OH}
90%
D0 AND SARS OUTPUTS
GND
t_{0H}
t_r
V_{CC}
$\overline{CS}$
90%
50%
10%
GND
t_{0H}
V_{CC}
D0 AND SARS OUTPUTS
10%
V_{OL}

TL/H/5583-23

Timing Diagrams

Data Input Timing


CLK
t_{SET-UP}
$\overline{CS}$
t_{SET-UP}
t_{HOLD}
t_{HOLD}
DATA IN (DI)

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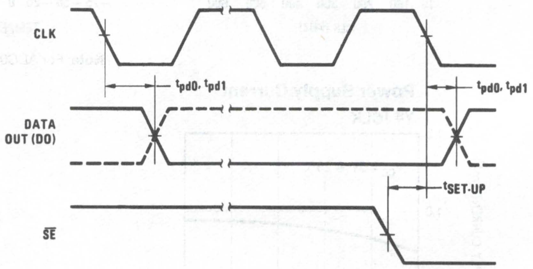
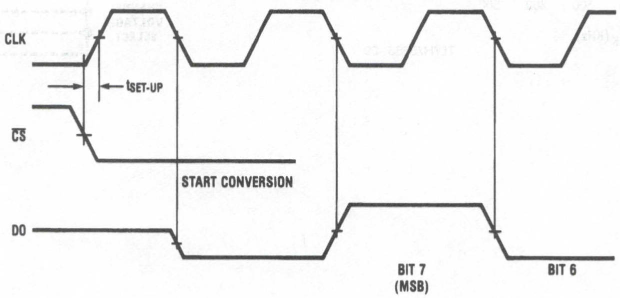
Data Output Timing


CLK
t_{pd0}, t_{pd1}
t_{pd0}, t_{pd1}
DATA OUT (DO)
t_{SET-UP}
$\overline{SE}$

TL/H/5583-25

ADC0831 Start Conversion Timing


CLK
t_{SET-UP}
$\overline{CS}$
START CONVERSION
DO
BIT 7 (MSB)
BIT 6

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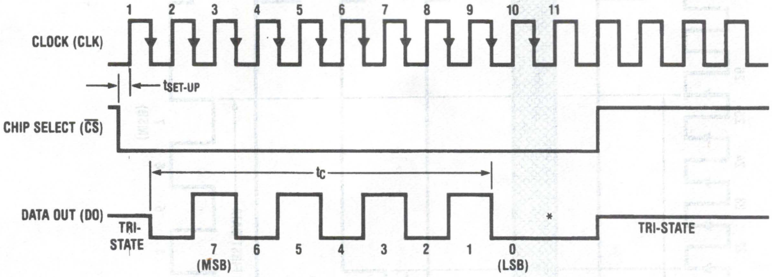
Timing Diagrams (Continued)

ADC0831 Timing


1
2
3
4
5
6
7
8
9
10
11
CLOCK (CLK)
tSET-UP
CHIP SELECT (CS)
tC
DATA OUT (DO)
TRI-STATE
7 (MSB)
6
5
4
3
2
1
0 (LSB)
*
TRI-STATE

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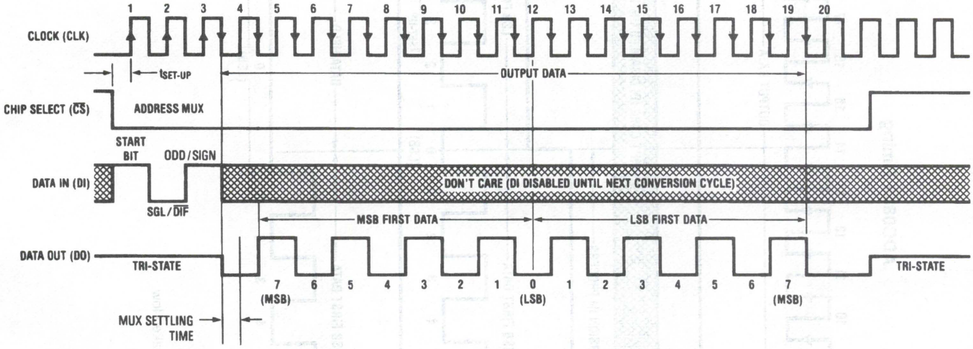
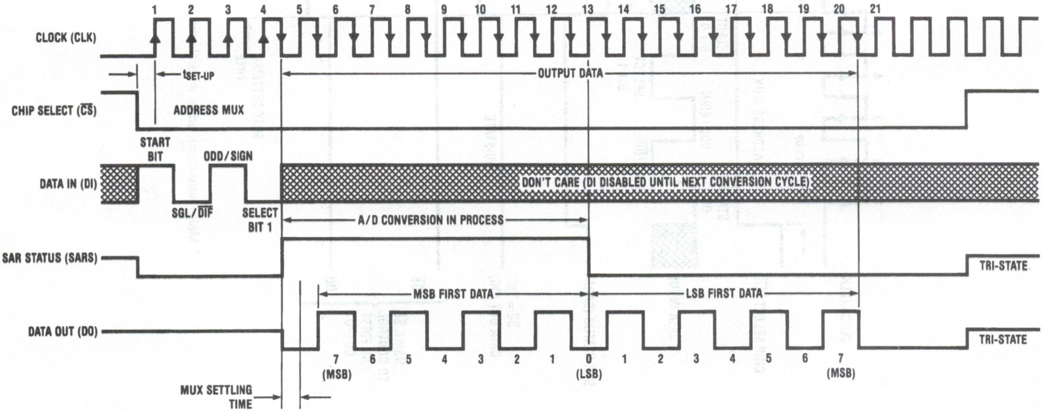
*LSB first output not available on ADC0831.

ADC0832 Timing


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
CLOCK (CLK)
tSET-UP
OUTPUT DATA
CHIP SELECT (CS)
ADDRESS MUX
START BIT
ODD/SIGN
DATA IN (DI)
DON'T CARE (DI DISABLED UNTIL NEXT CONVERSION CYCLE)
SGL/DIF
MSB FIRST DATA
LSB FIRST DATA
DATA OUT (DO)
TRI-STATE
7 (MSB)
6
5
4
3
2
1
0 (LSB)
1
2
3
4
5
6
7 (MSB)
TRI-STATE
MUX SETTLING TIME

TL/H/5583–28

ADC0834 Timing


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
CLOCK (CLK)
tSET-UP
OUTPUT DATA
CHIP SELECT (CS)
ADDRESS MUX
START BIT
ODD/SIGN
DATA IN (DI)
DON'T CARE (DI DISABLED UNTIL NEXT CONVERSION CYCLE)
SGL/DIF
SELECT BIT 1
A/D CONVERSION IN PROCESS
SAR STATUS (SARS)
TRI-STATE
MSB FIRST DATA
LSB FIRST DATA
DATA OUT (DO)
TRI-STATE
7 (MSB)
6
5
4
3
2
1
0 (LSB)
1
2
3
4
5
6
7 (MSB)
MUX SETTLING TIME

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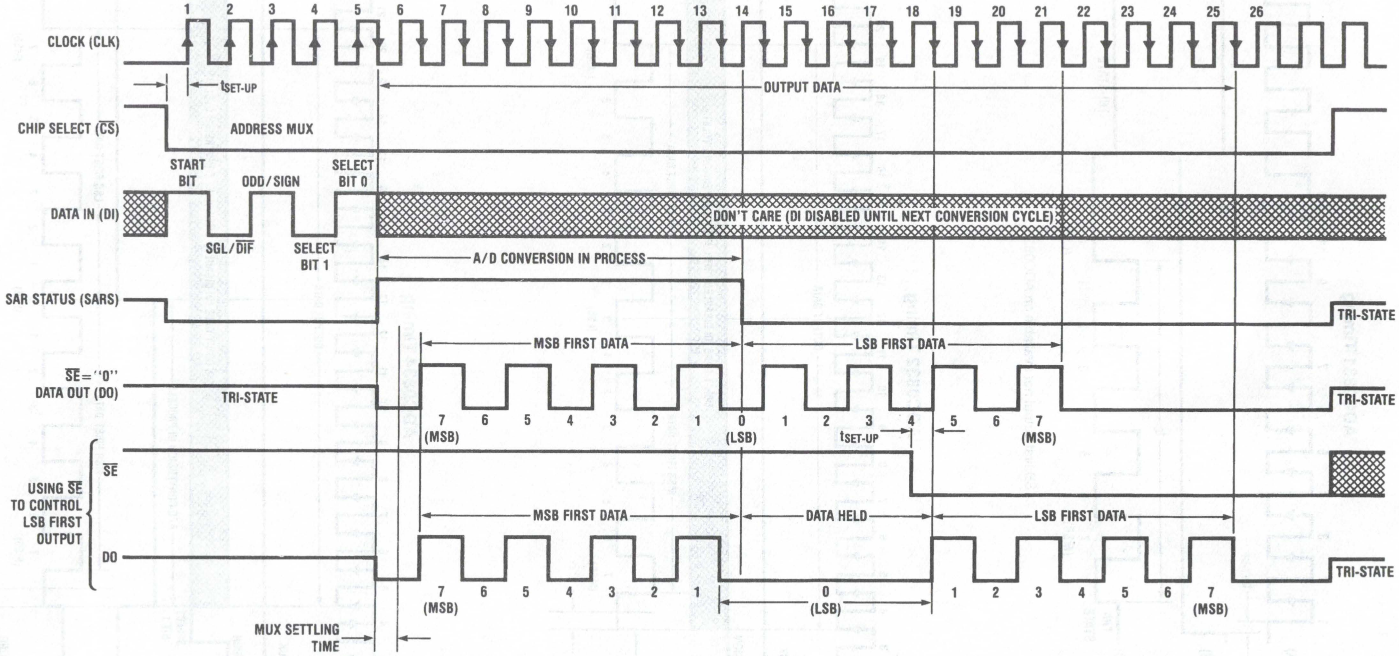
Timing Diagrams (Continued)

ADC0838 Timing


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
CLOCK (CLK)
t_{SET-UP}
OUTPUT DATA
CHIP SELECT ($\overline{CS}$)
ADDRESS MUX
START BIT
ODD/SIGN
SELECT BIT 0
DATA IN (DI)
DON'T CARE (DI DISABLED UNTIL NEXT CONVERSION CYCLE)
SGL/$\overline{DIF}$
SELECT BIT 1
A/D CONVERSION IN PROCESS
SAR STATUS (SARS)
TRI-STATE
MSB FIRST DATA
LSB FIRST DATA
$\overline{SE}$="0" DATA OUT (DO)
TRI-STATE
7 (MSB) 6 5 4 3 2 1 0 (LSB) 1 2 3 4 5 6 7 (MSB)
t_{SET-UP}
TRI-STATE
$\overline{SE}$
USING $\overline{SE}$ TO CONTROL LSB FIRST OUTPUT
MSB FIRST DATA
DATA HELD
LSB FIRST DATA
DO
7 (MSB) 6 5 4 3 2 1 0 (LSB) 1 2 3 4 5 6 7 (MSB)
TRI-STATE
MUX SETTLING TIME

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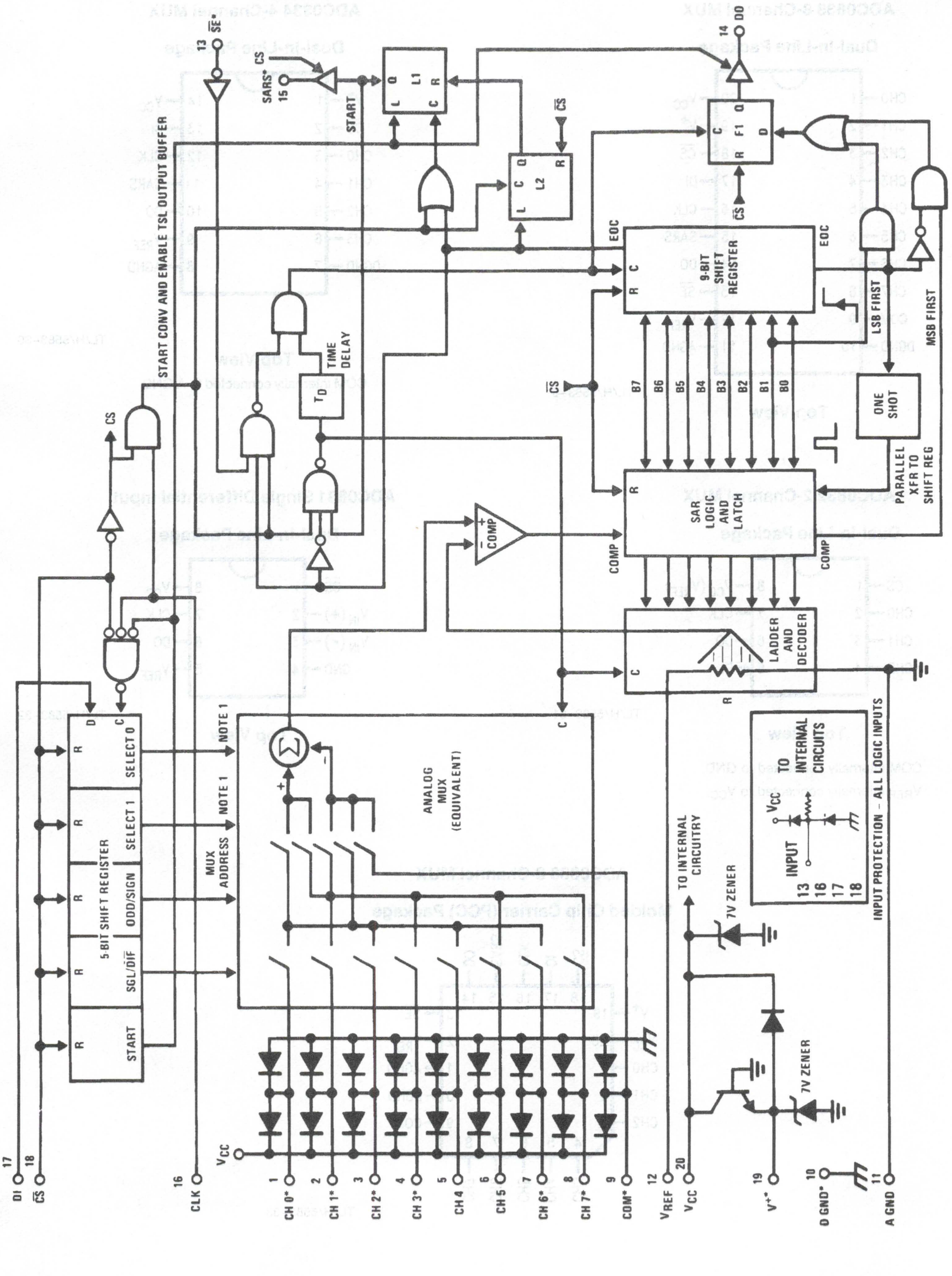
* Make sure clock edge #18 clocks in the LSB before $\overline{SE}$ is taken low

ADC0838 Functional Block Diagram


DI 17
CS 18
R
5-BIT SHIFT REGISTER
START
SGL/DIF
ODD/SIGN
SELECT 1
SELECT 0
D
C
CS
START CONV AND ENABLE TSL OUTPUT BUFFER
CLK 16
MUX ADDRESS
NOTE 1
NOTE 1
13 SE*
SARS* 15
CS
START
L Q
L1
C R
T_D
TIME DELAY
L C Q
L2
R
CS
V_CC
1 CH 0*
2 CH 1*
3 CH 2*
4 CH 3*
5 CH 4
6 CH 5
7 CH 6*
8 CH 7*
9 COM*
+
−
Σ
ANALOG MUX (EQUIVALENT)
C
COMP
− +
COMP
R
SAR LOGIC AND LATCH
B7
B6
B5
B4
B3
B2
B1
B0
R C
9-BIT SHIFT REGISTER
EOC
EOC
C
R F1 Q
D
14 DO
CS
LSB FIRST
MSB FIRST
ONE SHOT
PARALLEL XFR TO SHIFT REG
C
R
LADDER AND DECODER
12 V_REF
20 V_CC
TO INTERNAL CIRCUITRY
7V ZENER
19 V+*
7V ZENER
10 D GND*
11 A GND
INPUT
13
16
17
18
V_CC
TO INTERNAL CIRCUITS
INPUT PROTECTION – ALL LOGIC INPUTS

TL/H/5583-7

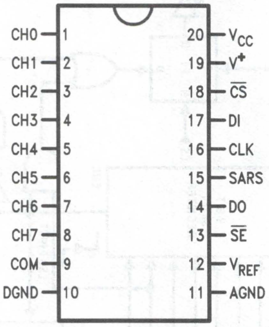
*Some of these functions/pins are not available with other options.

Note 1: For the ADC0834, D1 is input directly to the D input of SELECT 1. SELECT 0 is forced to a "1". For the ADC0832, DI is input directly to the DI input of ODD/SIGN. SELECT 0 is forced to a "0" and SELECT 1 is forced to a "1".

Connection Diagrams

ADC0838 8-Channel MUX

Dual-In-Line Package


CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
COM 9
DGND 10
20 V_{CC}
19 V^{+}
18 $\overline{CS}$
17 DI
16 CLK
15 SARS
14 DO
13 $\overline{SE}$
12 V_{REF}
11 AGND

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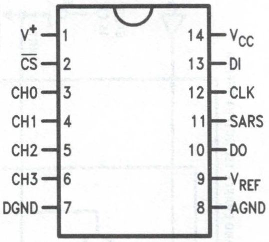
Top View

ADC0834 4-Channel MUX

Dual-In-Line Package


V^{+} 1
$\overline{CS}$ 2
CH0 3
CH1 4
CH2 5
CH3 6
DGND 7
14 V_{CC}
13 DI
12 CLK
11 SARS
10 DO
9 V_{REF}
8 AGND

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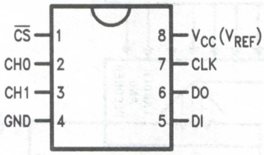
Top View

COM internally connected to A GND

ADC0832 2-Channel MUX

Dual-In-Line Package


$\overline{CS}$ 1
CH0 2
CH1 3
GND 4
8 V_{CC} (V_{REF})
7 CLK
6 DO
5 DI

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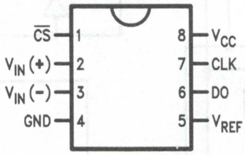
Top View

COM internally connected to GND.

V_{REF} internally connected to V_{CC}.

ADC0831 Single Differential Input

Dual-In-Line Package


$\overline{CS}$ 1
V_{IN} (+) 2
V_{IN} (−) 3
GND 4
8 V_{CC}
7 CLK
6 DO
5 V_{REF}

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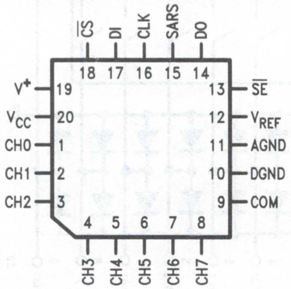
Top View

ADC0838 8-Channel MUX

Molded Chip Carrier (PCC) Package


$\overline{CS}$ 18
DI 17
CLK 16
SARS 15
DO 14
V^{+} 19
V_{CC} 20
CH0 1
CH1 2
CH2 3
13 $\overline{SE}$
12 V_{REF}
11 AGND
10 DGND
9 COM
4 CH3
5 CH4
6 CH5
7 CH6
8 CH7

TL/H/5583-33

Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of these converters utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or a new pseudo-differential option which will convert the difference between the voltage at any analog input and a common terminal. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a different pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC0831 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line on the ADC0838 can be used as a pseudo-differential input. In this mode, the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply application where the analog circuitry may be biased up to a potential other than ground and the output signals are all referred to this potential.

TABLE I. Multiplexer/Package Options

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	**Differential**	
ADC0831	1	1	8
ADC0832	2	1	8
ADC0834	4	2	14
ADC0838	8	4	20

Functional Description (Continued)

TABLE II. MUX Addressing: ADC0838

Single-Ended MUX Mode

MUX Address				Analog Single-Ended Channel #								
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								−
1	0	0	1			+						−
1	0	1	0					+				−
1	0	1	1							+		−
1	1	0	0		+							−
1	1	0	1				+					−
1	1	1	0						+			−
1	1	1	1								+	−

Differential MUX Mode

MUX Address				Analog Differential Channel-Pair #							
				0		1		2		3	
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7
0	0	0	0	+	−						
0	0	0	1			+	−				
0	0	1	0					+	−		
0	0	1	1							+	−
0	1	0	0	−	+						
0	1	0	1			−	+				
0	1	1	0					−	+		
0	1	1	1							−	+

TABLE III. MUX Addressing: ADC0834

Single-Ended MUX Mode

MUX Address			Channel #			
SGL/ DIF	ODD/ SIGN	SELECT 1	0	1	2	3
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

COM is internally tied to A GND

Differential MUX Mode

MUX Address			Channel #			
SGL/ DIF	ODD/ SIGN	SELECT 1	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

TABLE IV. MUX Addressing: ADC0832

Single-Ended MUX Mode

MUX Address		Channel #	
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to A GND

Differential MUX Mode

MUX Address		Channel #	
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	0	1
0	0	+	−
0	1	−	+

Functional Description (Continued)

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

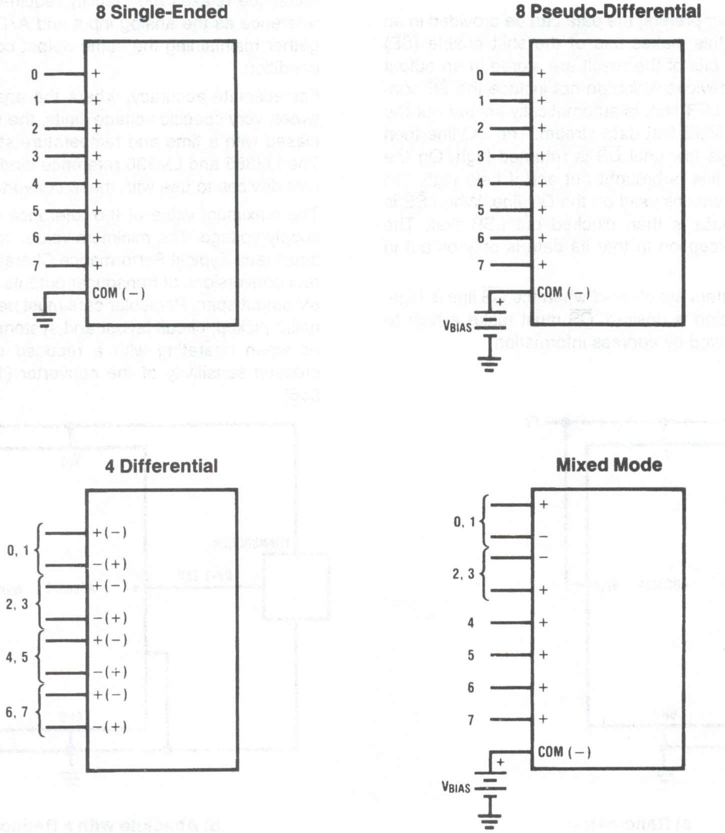
A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate diagram is shown of each device.

1. A conversion is initiated by first pulling the $\overline{\text{CS}}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.



TL/H/5583-9

FIGURE 1. Analog Input Multiplexer Options for the ADC0838

Functional Description (Continued)

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

7. After 8 clock periods the conversion is completed. The SAR status line returns low to indicate this ½ clock cycle later.

8. If the programmer prefers, the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{SE}$) control line]. All 8 bits of the result are stored in an output shift register. On devices which do not include the $\overline{SE}$ control line, the data, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. On the ADC0838 the $\overline{SE}$ line is brought out and if held high, the value of the LSB remains valid on the DO line. When $\overline{SE}$ is forced low, the data is then clocked out LSB first. The ADC0831 is an exception in that its data is only output in MSB first format.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

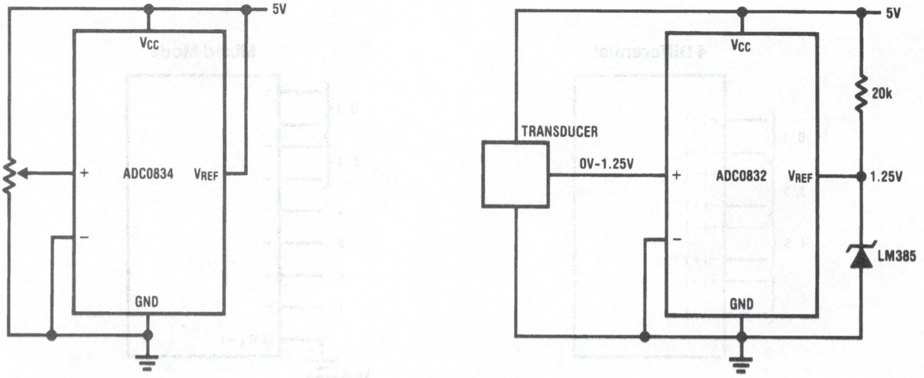
3.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input to these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 3.5 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC} (done internally on the ADC0832). This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).



TL/H/5583-10

a) Ratiometric

b) Absolute with a Reduced Span

FIGURE 2. Reference Examples

Functional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(\max) = V_{PEAK}(2\pi f_{CM})\left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK}, is the A/D clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error ($\approx$5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ±1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for V_{REF} = 5.000 V_{DC}).

5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input (or V_{CC} for the ADC0832) for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

and

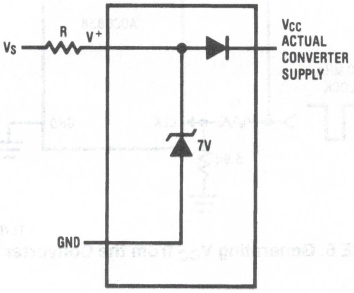
V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

6.0 POWER SUPPLY

A unique feature of the ADC0838 and ADC0834 is the inclusion of a zener diode connected from the V+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in *Figure 3*. (See Note 3)



TL/H/5583-11

FIGURE 3. An On-Chip Shunt Regulator Diode

Functional Description (Continued)

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. *Figures 4 and 5* illustrate two useful applications of this on-board zener when an external transistor can be afforded.

An important use of the interconnecting diode between V+ and V_{CC} is shown in *Figures 6 and 7*. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The low current requirements of the A/D and the relatively high clock frequencies used (typically in the range of 10k–400 kHz) allows using the small value filter capacitor shown to keep the ripple on the V_{CC} line to well under ¼ of an LSB. The shunt zener regulator can also be used in this mode. This requires a clock voltage swing which is in excess of V_Z. A current limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V+ pin.

Applications

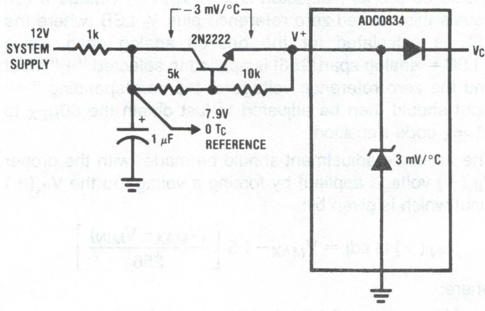

−3 mV/°C
ADC0834
12V
SYSTEM
SUPPLY
1k
2N2222
V+
VCC
5k
10k
7.9V
0 TC
REFERENCE
1 µF
3 mV/°C
TL/H/5583–12

FIGURE 4. Operating with a Temperature Compensated Reference

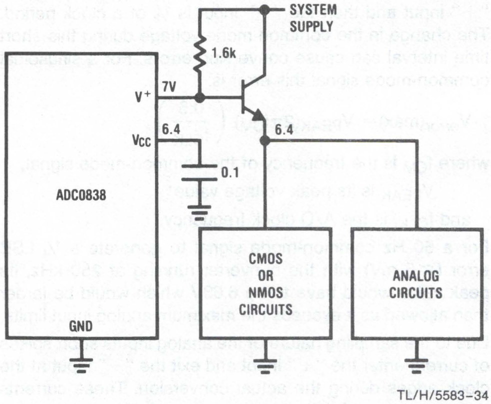

12V
SYSTEM
SUPPLY
1.6k
7V
V+
6.4
6.4
VCC
0.1
ADC0838
CMOS
OR
NMOS
CIRCUITS
ANALOG
CIRCUITS
GND
TL/H/5583–34

FIGURE 5. Using the A/D as the System Supply Regulator

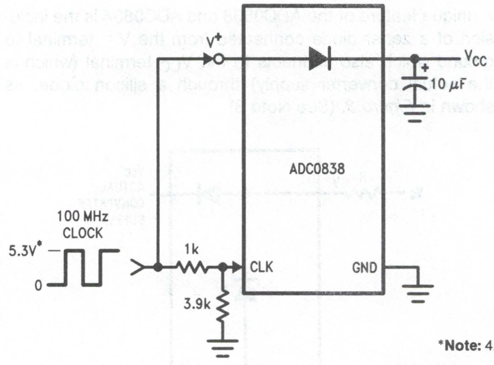

V+
VCC
10 µF
ADC0838
100 MHz
CLOCK
5.3V*
0
1k
CLK
GND
3.9k
TL/H/5583–35

FIGURE 6. Generating V_{CC} from the Converter Clock

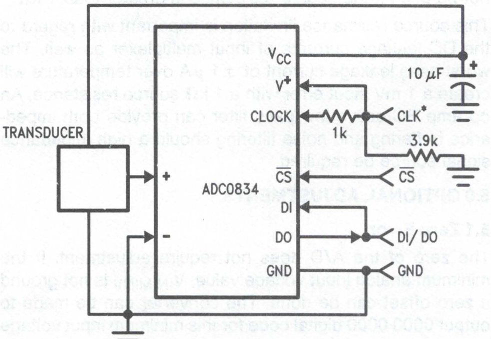
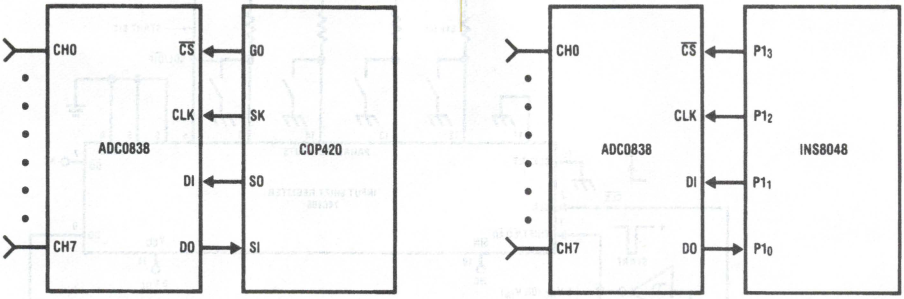

VCC
10 µF
V+
CLOCK
CLK*
1k
3.9k
TRANSDUCER
CS
CS
+
ADC0834
DI
−
DO
DI/DO
GND
GND
TL/H/5583–36

FIGURE 7. Remote Sensing— Clock and Power on 1 Wire

***Note:** $4.5V \le V_{CC} \le 6.3V$

Applications (Continued)

Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048



TL/H/5583-13

COP CODING EXAMPLE

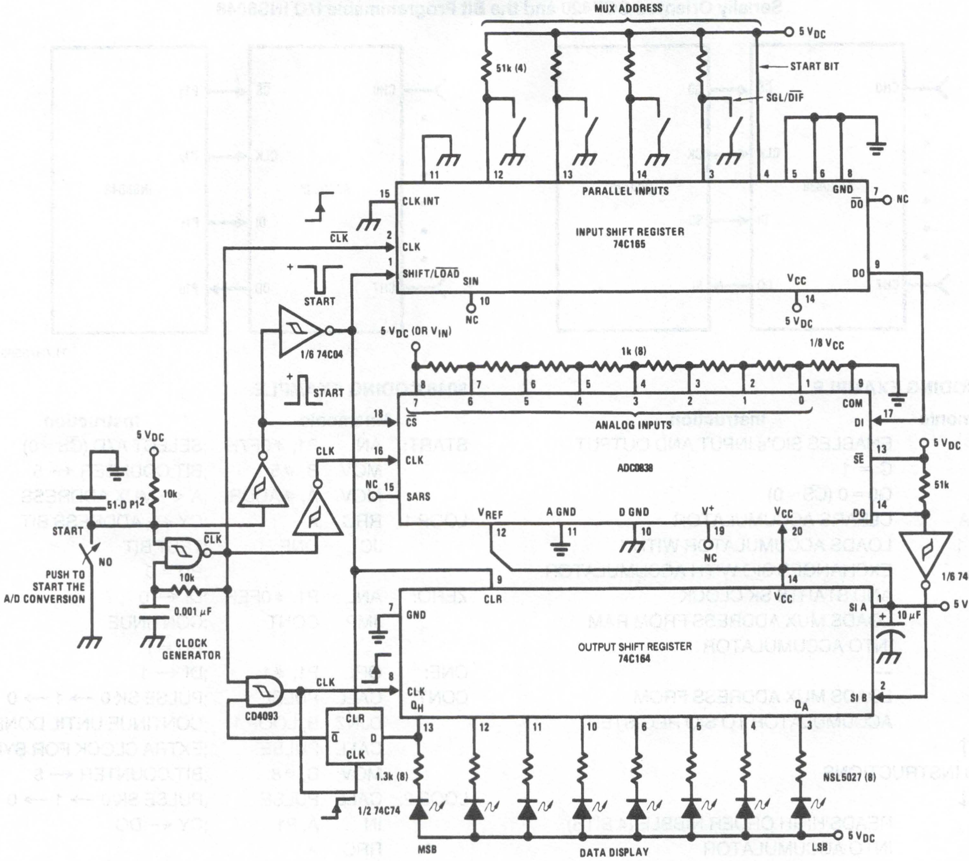
```
Mnemonic        Instruction
LEI             ENABLES SIO's INPUT AND OUTPUT
SC              C = 1
OGI             G0 = 0 (CS = 0)
CLR A           CLEARS ACCUMULATOR
AISC 1          LOADS ACCUMULATOR WITH 1
XAS             EXCHANGES SIO WITH ACCUMULATOR
                AND STARTS SK CLOCK
LDD             LOADS MUX ADDRESS FROM RAM
                INTO ACCUMULATOR
NOP             —
XAS             LOADS MUX ADDRESS FROM
                ACCUMULATOR TO SIO REGISTER
   ↑
 8 INSTRUCTIONS
   ↓
XAS             READS HIGH ORDER NIBBLE (4 BITS)
                INTO ACCUMULATOR
XIS             PUTS HIGH ORDER NIBBLE INTO RAM
CLR A           CLEARS ACCUMULATOR
RC              C = 0
XAS             READS LOW ORDER NIBBLE INTO
                ACCUMULATOR AND STOPS SK
XIS             PUTS LOW ORDER NIBBLE INTO RAM
OGI             G0 = 1 (CS = 1)
LEI             DISABLES SIO's INPUT AND OUTPUT
```

8048 CODING EXAMPLE

```
         Mnemonic                  Instruction
START:   ANL    P1, #0F7H     ;SELECT A/D (CS = 0)
         MOV    B, #5         ;BIT COUNTER ← 5
         MOV    A, #ADDR      ;A ← MUX ADDRESS
LOOP 1:  RRC    A             ;CY ← ADDRESS BIT
         JC     ONE           ;TEST BIT
                              ;BIT = 0
ZERO:    ANL    P1, #0FEH     ;DI ← 0
         JMP    CONT          ;CONTINUE
                              ;BIT = 1
ONE:     ORL    P1, #1        ;DI ← 1
CONT:    CALL   PULSE         ;PULSE SK 0 → 1 → 0
         DJNZ   B, LOOP 1     ;CONTINUE UNTIL DONE
         CALL   PULSE         ;EXTRA CLOCK FOR SYNC
         MOV    B, #8         ;BIT COUNTER ← 8
LOOP 2:  CALL   PULSE         ;PULSE SK 0 → 1 → 0
         IN     A, P1         ;CY ← DO
         RRC    A
         RRC    A
         MOV    A, C          ;A ← RESULT
         RLC    A             ;A(0) ← BIT AND SHIFT
         MOV    C, A          ;C ← RESULT
         DJNZ   B, LOOP 2     ;CONTINUE UNTIL DONE
RETR
                              ;PULSE SUBROUTINE
PULSE:   ORL    P1, #04       ;SK ← 1
         NOP                  ;DELAY
         ANL    P1, #0FBH     ;SK ← 0
         RET
```

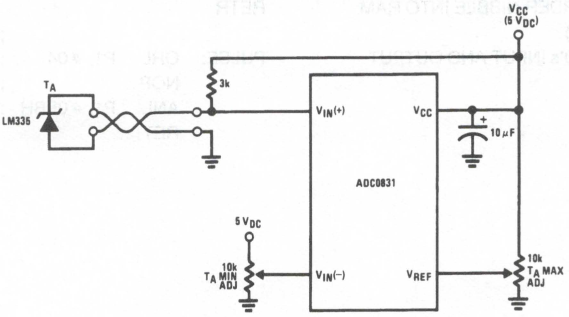
Applications (Continued)

A "Stand-Alone" Hook-Up for ADC0838 Evaluation


MUX ADDRESS
5 VDC
START BIT
SGL/DIF
51k (4)
11
12
13
14
3
4
5
6
8
PARALLEL INPUTS
GND
DO
7
NC
15
CLK INT
CLK
2
CLK
1
SHIFT/LOAD
SIN
INPUT SHIFT REGISTER
74C165
VCC
DO
9
14
5 VDC
10
NC
START
1/6 74C04
5 VDC (OR VIN)
1k (8)
1/8 VCC
8
7
6
5
4
3
2
1
9
START
7
6
5
4
3
2
1
0
COM
18
CS
ANALOG INPUTS
DI
17
CLK
16
CLK
SE
13
5 VDC
NC
15
SARS
ADC0838
51k
5 VDC
14
DO
VREF
A GND
D GND
V+
VCC
12
11
10
19
20
NC
1/6 74C14
51-D P1*
10k
START
CLK
PUSH TO START THE A/D CONVERSION
NO
10k
0.001 µF
CLOCK GENERATOR
9
CLR
14
VCC
1
SI A
10 µF
5 VDC
7
GND
OUTPUT SHIFT REGISTER
74C164
8
CLK
QH
SI B
2
QA
CD4093
CLK
CLR
Q
D
CLK
13
12
11
10
6
5
4
3
1.3k (8)
NSL5027 (8)
1/2 74C74
MSB
DATA DISPLAY
LSB
5 VDC

*Pinouts shown for ADC0838.
For all other products tie to
pin functions as shown.

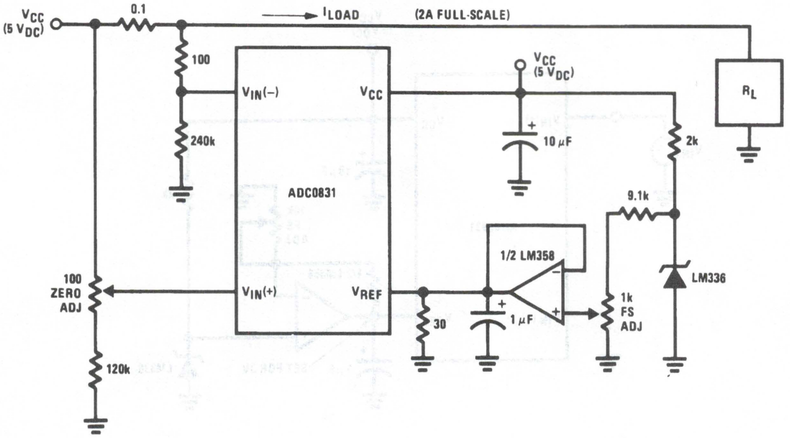
Low-Cost Remote Temperature Sensor


VCC (5 VDC)
TA
LM335
3k
VIN(+)
VCC
10 µF
ADC0831
5 VDC
10k
TA MIN ADJ
VIN(−)
VREF
10k
TA MAX ADJ

TL/H/5583–14

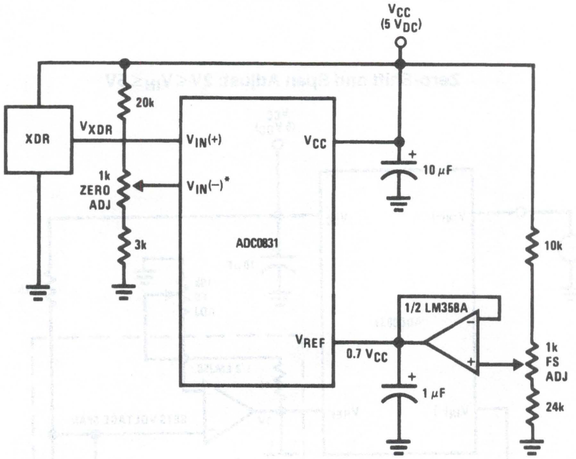
Applications (Continued)

Digitizing a Current Flow


VCC (5 VDC)
0.1
ILOAD
(2A FULL-SCALE)
100
240k
VIN(−)
VCC
VCC (5 VDC)
10 μF
RL
2k
ADC0831
9.1k
1/2 LM358
LM336
100 ZERO ADJ
VIN(+)
VREF
30
1 μF
1k FS ADJ
120k

TL/H/5583–15

Operating with Ratiometric Transducers


VCC (5 VDC)
20k
XDR
VXDR
VIN(+)
VCC
10 μF
1k ZERO ADJ
VIN(−)*
3k
ADC0831
10k
1/2 LM358A
VREF
0.7 VCC
1k FS ADJ
1 μF
24k

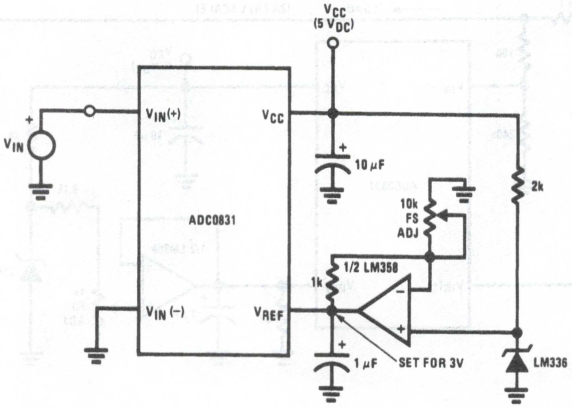
TL/H/5583–37

*$V_{IN}(-) = 0.15\ V_{CC}$

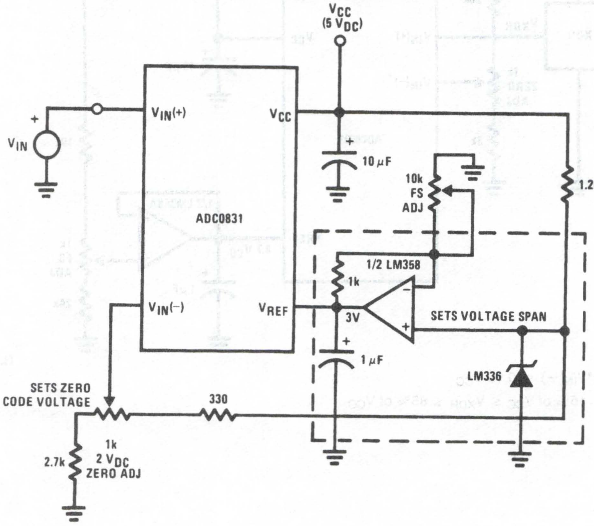
15% of $V_{CC} \le V_{XDR} \le 85\%$ of V_{CC}

Applications (Continued)

Span Adjust: $0V \leq V_{IN} \leq 3V$


V_CC
(5 V_DC)
V_IN(+)
V_CC
+
V_IN
10 µF
2k
10k
FS
ADJ
ADC0831
1/2 LM358
1k
V_IN(−)
V_REF
−
+
1 µF
SET FOR 3V
LM336

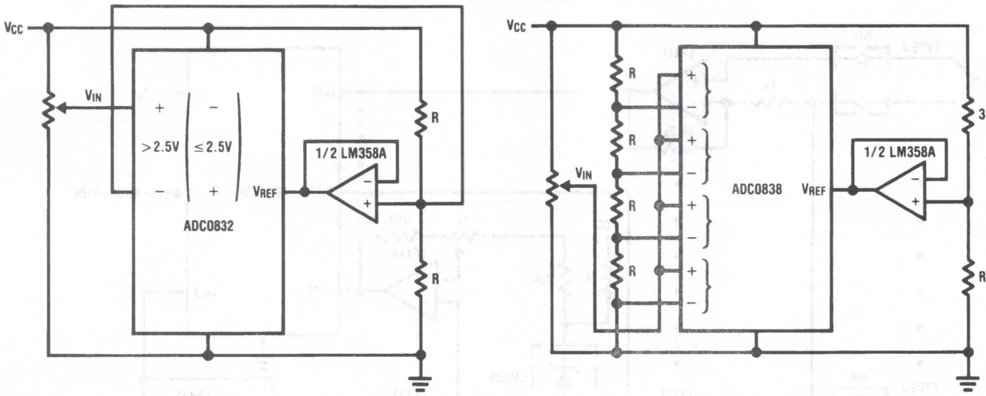
Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$


V_CC
(5 V_DC)
V_IN(+)
V_CC
+
V_IN
10 µF
10k
FS
ADJ
1.2k
ADC0831
1/2 LM358
1k
V_IN(−)
V_REF
3V
SETS VOLTAGE SPAN
1 µF
LM336
SETS ZERO
CODE VOLTAGE
330
1k
2.7k
2 V_DC
ZERO ADJ

TL/H/5583-16

Applications (Continued)

Obtaining Higher Resolution


VCC
VIN
+
−
>2.5V
≤2.5V
−
+
VREF
ADC0832
R
1/2 LM358A
R
VCC
R
R
R
R
VIN
ADC0838
VREF
1/2 LM358A
3R
R

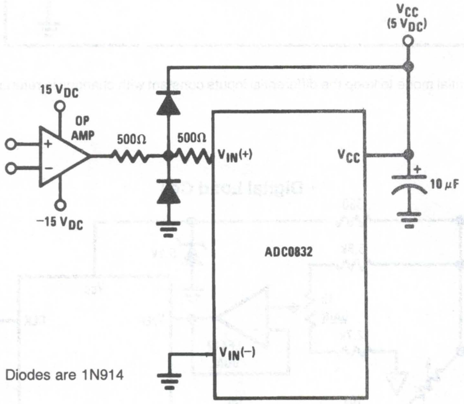
TL/H/5583-17

Controller performs a routine to determine which input polarity (9-bit example) or which channel pair (10-bit example) provides a non-zero output code. This information provides the extra bits.

a) 9-Bit A/D

b)10-Bit A/D

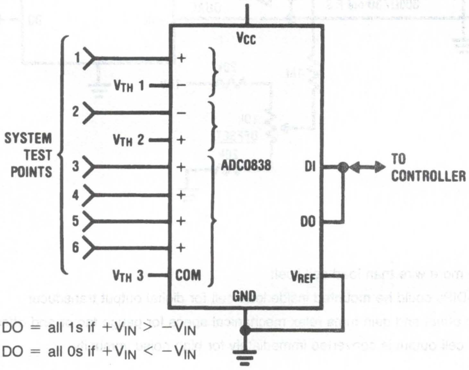
Protecting the Input


VCC
(5 VDC)
15 VDC
OP AMP
500Ω
500Ω
VIN(+)
VCC
10 µF
−15 VDC
ADC0832
VIN(−)

Diodes are 1N914

TL/H/5583-18

High Accuracy Comparators


5V
VCC
1
VTH 1
2
VTH 2
SYSTEM TEST POINTS
3
4
5
6
VTH 3
COM
ADC0838
DI
TO CONTROLLER
DO
VREF
GND

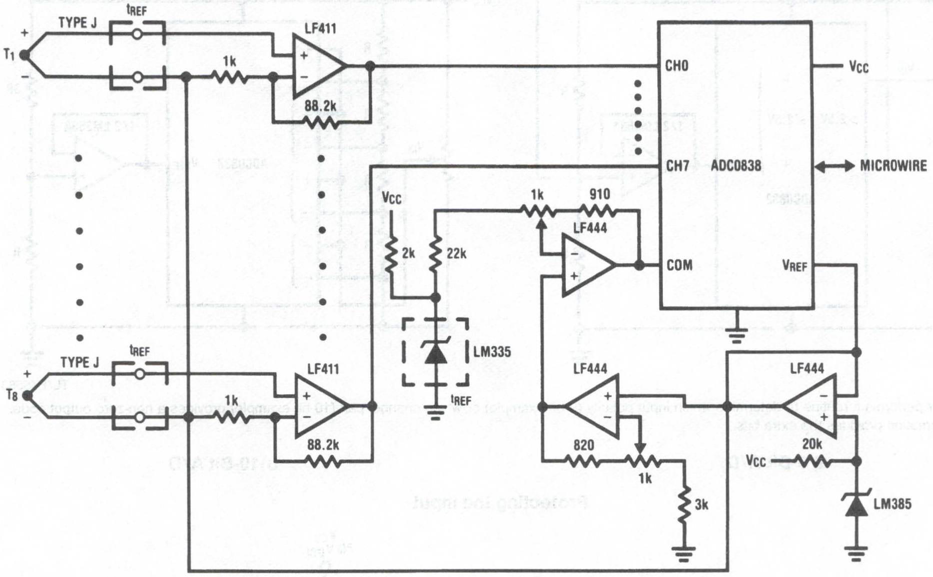
DO = all 1s if $+V_{IN} > -V_{IN}$

DO = all 0s if $+V_{IN} < -V_{IN}$

TL/H/5583-38

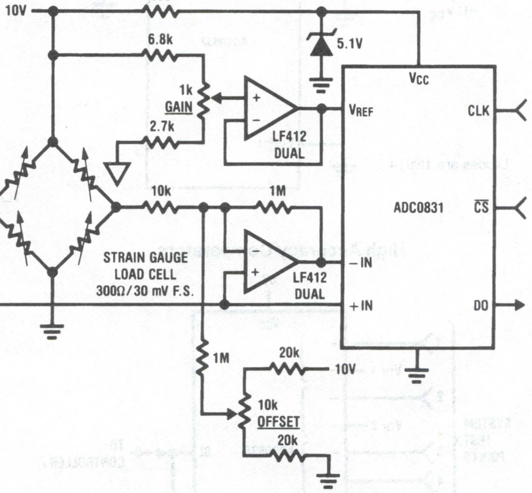
Applications (Continued)

Convert 8 Thermocouples with only One Cold-Junction Compensator


TYPE J
tREF
+
T1
−
1k
LF411
+
−
88.2k
CH0
CH7
ADC0838
Vcc
MICROWIRE
Vcc
2k
22k
1k
910
LF444
−
+
COM
VREF
LM335
tREF
LF444
+
−
820
1k
3k
LF444
−
+
20k
Vcc
LM385
TYPE J
tREF
+
T8
−
1k
LF411
+
−
88.2k

Uses the pseudo-differential mode to keep the differential inputs constant with changes in reference temperature (T_{REF}).

Digital Load Cell

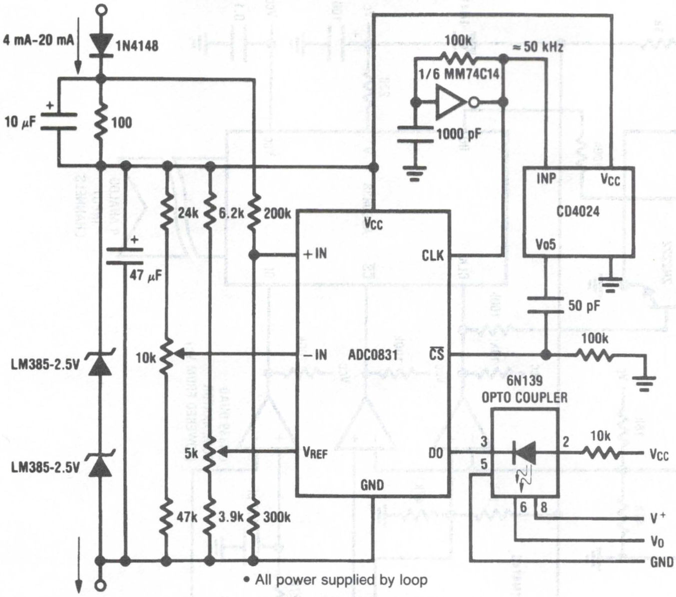

10V
330
5.1V
6.8k
1k
GAIN
2.7k
+
−
LF412
DUAL
Vcc
VREF
CLK
ADC0831
CS
10k
1M
−IN
+IN
DO
+
LF412
DUAL
STRAIN GAUGE
LOAD CELL
300Ω/30 mV F.S.
1M
20k
10V
10k
OFFSET
20k

TL/H/5583–19

- Uses one more wire than load cell itself
- Two mini-DIPs could be mounted inside load cell for digital output transducer
- Electronic offset and gain trims relax mechanical specs for gauge factor and offset
- Low level cell output is converted immediately for high noise immunity

Applications (Continued)

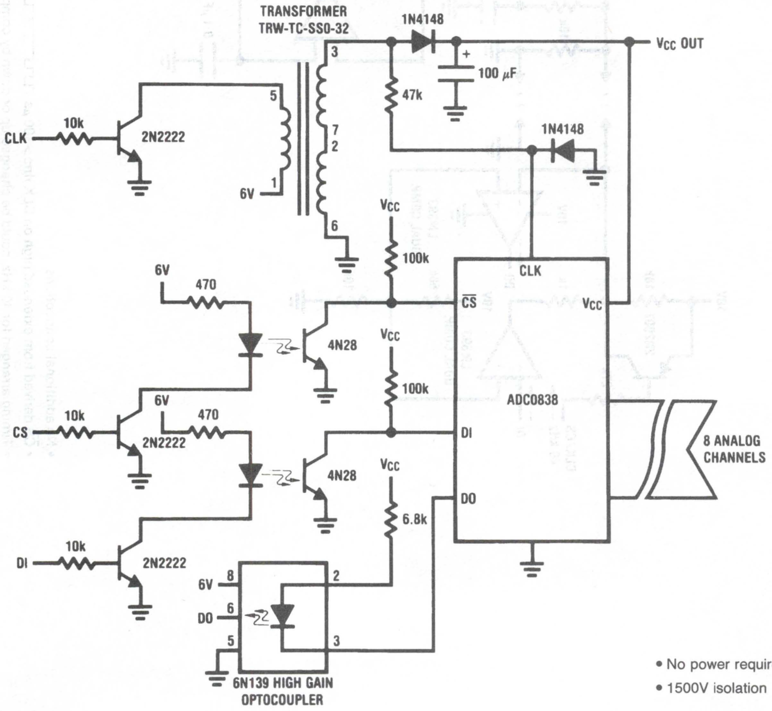
4 mA–20 mA Current Loop Converter


4 mA-20 mA
1N4148
10 µF
100
100k
≈50 kHz
1/6 MM74C14
1000 pF
INP
Vcc
CD4024
Vo5
50 pF
100k
24k
6.2k
200k
47 µF
Vcc
+IN
CLK
LM385-2.5V
10k
−IN
ADC0831
CS
6N139
OPTO COUPLER
LM385-2.5V
5k
VREF
DO
3
5
2
10k
Vcc
GND
6
8
47k
3.9k
300k
V+
Vo
GND

- All power supplied by loop
- 1500V isolation at output

TL/H/5583–20

Isolated Data Converter

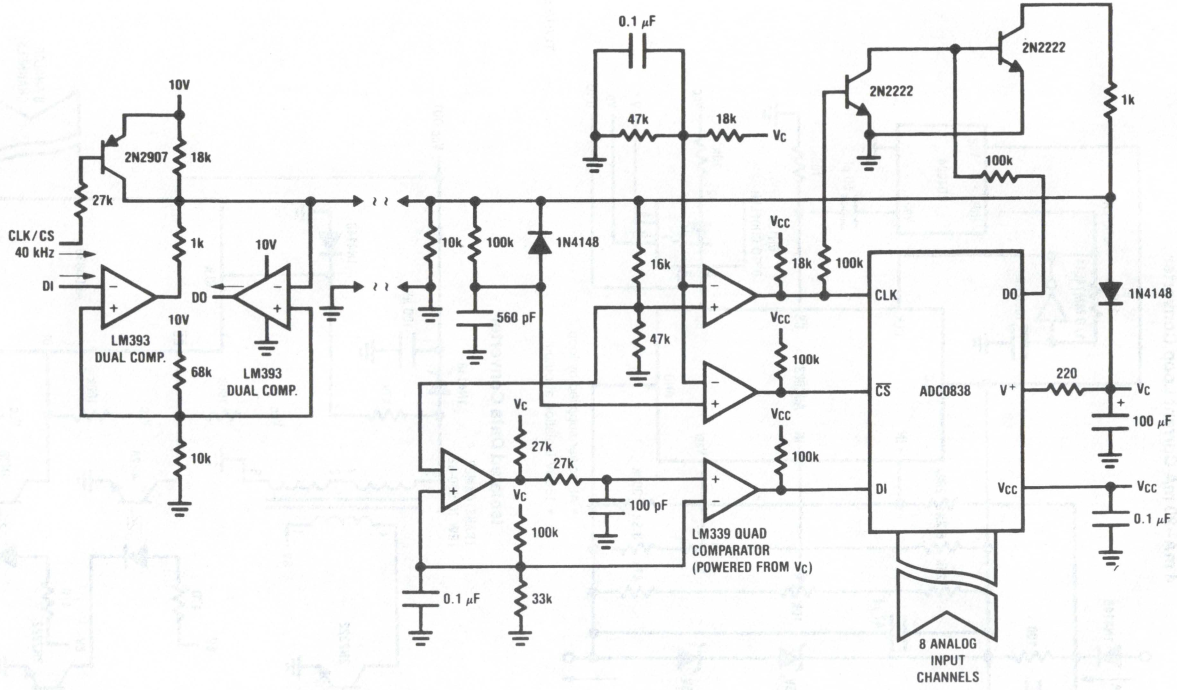

TRANSFORMER
TRW-TC-SS0-32
1N4148
Vcc OUT
3
100 µF
5
47k
10k
CLK
2N2222
7
2
1N4148
6V
1
6
Vcc
100k
6V
470
CLK
CS
Vcc
4N28
Vcc
100k
ADC0838
6V
10k
CS
2N2222
470
DI
8 ANALOG CHANNELS
4N28
Vcc
6.8k
DO
10k
DI
2N2222
6V
8
2
DO
6
5
3
6N139 HIGH GAIN OPTOCOUPLER

- No power required remotely
- 1500V isolation

TL/H/5583–39

Applications (Continued)

Two Wire Interface for 8 Channels

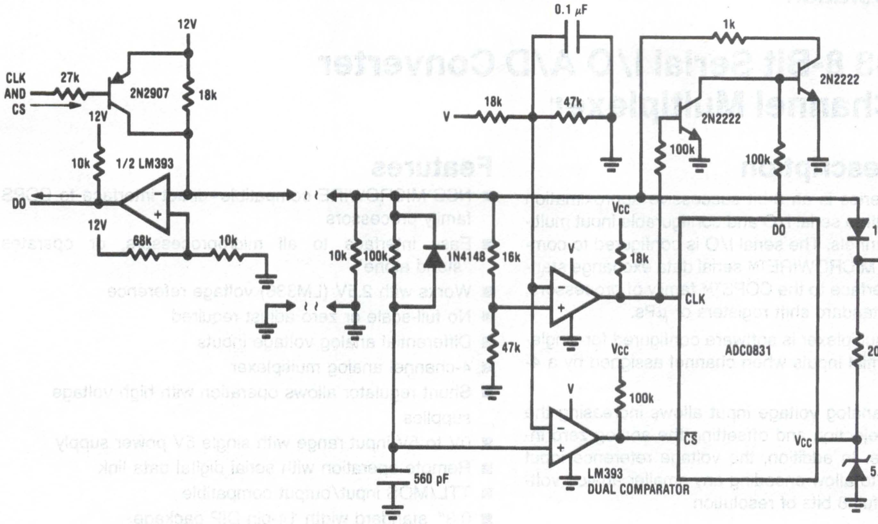

10V
2N2907
18k
27k
CLK/CS
40 kHz
DI
1k
10V
DO
LM393
DUAL COMP.
10V
68k
LM393
DUAL COMP.
10k
0.1 µF
47k
18k
VC
10k
100k
1N4148
560 pF
16k
47k
VCC
18k
100k
VCC
100k
VCC
100k
VC
27k
27k
100 pF
VC
100k
0.1 µF
33k
LM339 QUAD
COMPARATOR
(POWERED FROM VC)
2N2222
2N2222
1k
100k
CLK
DO
1N4148
CS
ADC0838
V+
220
VC
100 µF
DI
VCC
VCC
0.1 µF
8 ANALOG
INPUT
CHANNELS

- No additional connections
- $\overline{\text{CS}}$ derived from extended high on CLK line > 100 µs
- Timing arranged for 40 kHz, could be changed up or down by component change
- 10% CLK frequency change without component change OK

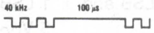
TL/H/5583–21

Applications (Continued)

Two Wire 1-Channel Interface


12V
CLK AND CS
27k
2N2907
18k
12V
10k
1/2 LM393
DO
12V
68k
10k
10k
100k
1N4148
18k
16k
47k
560 pF
0.1 µF
V
18k
47k
1k
2N2222
2N2222
100k
100k
V
VCC
18k
DO
CLK
ADC0831
VCC
100k
V
CS
VCC
LM393 DUAL COMPARATOR
1N4148
V
100 µF
200
5.1V

- Simpler version of 8-channel
- $\overline{CS}$ derived from long CLK pulse


40 kHz
100 µs

TL/H/5583–22

Ordering Information

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0831BJ ADC0831BCJ ADC0831BCN	1	±½	Hermetic (J) Hermetic (J) Molded (N)	−55°C to +125°C −40°C to +85°C 0°C to +70°C
ADC0831CCJ ADC0831CCN		±1	Hermetic (J) Molded (N)	−40°C to +85°C 0°C to +70°C
ADC0832BJ ADC0832BCJ ADC0832BCN	2	±½	Hermetic (J) Hermetic (J) Molded (N)	−55°C to +125°C −40°C to +85°C 0°C to +70°C
ADC0832CCJ ADC0832CCN		±1	Hermetic (J) Molded (N)	−40°C to +85°C 0°C to +70°C
ADC0834BJ ADC0834BCJ ADC0834BCN	4	±½	Hermetic (J) Hermetic (J) Molded (N)	−55°C to +125°C −40°C to +85°C 0°C to +70°C
ADC0834CCJ ADC0834CCN		±1	Hermetic (J) Molded (N)	−40°C to +85°C 0°C to +70°C
ADC0838BJ ADC0838BCJ ADC0838BCV ADC0838BCN	8	±½	Hermetic (J) Hermetic (J) PCC (V) Molded (N)	−55°C to +125°C −40°C to +85°C 0°C to +70°C 0°C to +70°C
ADC0838CCJ ADC0838CCV ADC0838CCN		±1	Hermetic (J) PCC (V) Molded (N)	−40°C to +85°C 0°C to +70°C 0°C to +70°C

See NS Package Number J08A, J14A, J20A, N08E, N14A, N20A or V20A

National Semiconductor Corporation

ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer

General Description

The ADC0833 series is an 8-bit successive approximation A/D converter with a serial I/O and configurable input multiplexer with 4 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, as well as with standard shift registers or μPs.

The 4-channel multiplexer is software configured for single-ended or differential inputs when channel assigned by a 4-bit serial word.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Key Specifications

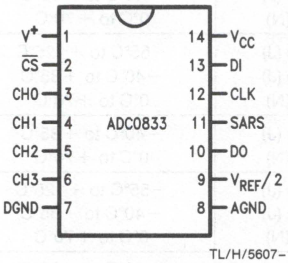
■ Resolution	8 Bits
■ Total Unadjusted Error	± ½ LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	23 mW
■ Conversion Time	32 μs

Features

- NSC MICROWIRE compatible-direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand alone"
- Works with 2.5V (LM336) voltage reference
- No full-scale or zero adjust required
- Differential analog voltage inputs
- 4-channel analog multiplexer
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- TTL/MOS input/output compatible
- 0.3″ standard width 14-pin DIP package

Connection and Functional Diagrams

Dual-In-Line Package

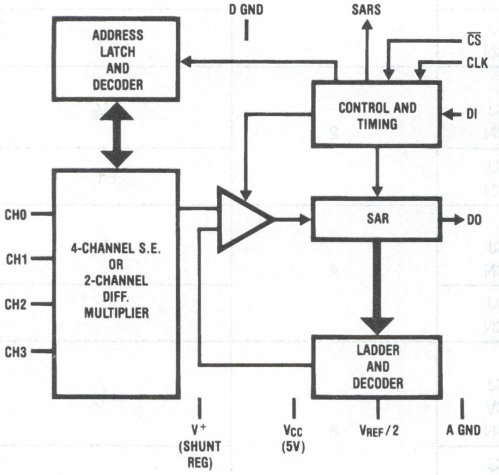

V+ 1
CS 2
CH0 3
CH1 4
CH2 5
CH3 6
DGND 7
ADC0833
14 VCC
13 DI
12 CLK
11 SARS
10 DO
9 VREF/2
8 AGND

TL/H/5607-14

Top View

Order Number ADC0833BCJ, ADC0833BJ, ADC0833CJ, ADC0833CCJ, ADC0833BCN or ADC0833CCN

See NS Package Number J14A or N14A


D GND
SARS
CS
CLK
ADDRESS LATCH AND DECODER
CONTROL AND TIMING
DI
CH0
CH1
CH2
CH3
4-CHANNEL S.E. OR 2-CHANNEL DIFF. MULTIPLIER
SAR
DO
LADDER AND DECODER
V+ (SHUNT REG)
Vcc (5V)
VREF/2
A GND

TL/H/5607-1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to V_{CC} + 0.3V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Storage Temperature	−65°C to + 150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temperature (Soldering, 10 sec.)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
ESD Susceptibility (Note 5)	2000V

Operating Conditions (Notes 1 & 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0833BJ, ADC0833CJ	$-55°C \le T_A \le 125°C$
ADC0833BCJ, ADC0833CCJ	$-40°C \le T_A \le 85°C$
ADC0833BCN, ADC0833CCN	$0°C \le T_A \le 70°C$

Electrical Characteristics

The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz and $V_{REF}/2 \le (V_{CC} + 0.1V)$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Total Unadjusted Error	$V_{REF}/2$ Forced to 2.500 V_{DC}				
ADC0833BCN			±½	**±½**	LSB
ADC0883BJ, BCJ			**±½**		LSB
ADC0833CCN			±1	**±1**	LSB
ADC0833CJ, CCJ			**±1**		LSB
Minimum Total Ladder Resistance (Note 9)					
ADC0833BCJ/CCJ/BJ/CJ		7.0	**2.6**		kΩ
ADC0833BCN/CCN		7.0	2.6	**2.6**	kΩ
Maximum Total Ladder Resistance (Note 9)					
ADC0833BCJ/CCJ/BJ/CJ		7.0	**11.8**		kΩ
ADC0833BCN/CCN		7.0	10.8	**11.8**	kΩ
Minimum Common-Mode Input Range (Note 10)	All MUX Inputs and COM Input				
ADC0833BCJ/CCJ/BJ/CJ			**GND−0.05**		V
ADC0833BCN/CCN			GND−0.05	**GND−0.05**	V
Maximum Common-Mode Input Range (Note 10)	All MUX Inputs and COM Input				
ADC0833BCJ/CCJ/BJ/CJ			**V_{CC}+0.05**		V
ADC0833BCN/CCN			V_{CC}+0.05	**V_{CC}+0.05**	V
DC Common-Mode Error					
ADC0833BCJ/CCJ/BJ/CJ		±1/16	**±¼**		LSB
ADC0833BCN/CCN		±1/16	±1/4	**±¼**	LSB
Change In Zero Error From V_{CC}=5V To Internal Zener Operation (Note 3)	15mA Into V+ V_{CC}=N.C. $V_{REF}/2$ = 2.500V				
ADC0833BCJ/CCJ/BJ/CJ			**1**		LSB
ADC0833BCN/CCN			1	**1**	LSB

Electrical Characteristics

The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz and $V_{REF}/2 \leq (V_{CC} + 0.1V)$ unless otherwise specified. **Boldface limits apply from t_{MIN} to t_{MAX};** all other limits $T_A = T_j = 25°C$. (Continued)

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)					
V_Z, Minimum Internal Diode Breakdown (At V+) (Note 3)	15mA Into V+				
ADC0833BCJ/CCJ/BJ/CJ			**6.3**		V
ADC0833BCN/CCN			6.3	**6.3**	V
V_Z, Maximum Internal Diode Breakdown (At V+) (Note 3)	15mA Into V+				
ADC0833BCJ/CCJ/BJ/CJ			**8.5**		V
ADC0833BCN/CCN			8.5	**8.5**	V
Power Supply Sensitivity	$V_{CC} = 5V \pm 5\%$				
ADC0833BCJ/CCJ/BJ/CJ		±1/16	±1/4		LSB
ADC0833BCN/CCN		±1/16	±1/4	**±1/4**	LSB
I_{OFF}, Off Channel Leakage Current (Note 11)	On Channel = 5V, Off Channel = 0V				
ADC0833BCJ/CCJ/BJ/CJ			**−1** −200		µA nA
ADC0833BCN/CCN			−200	**−1**	µA nA
	On Channel = 0V, Off Channel = 5V				
ADC0833BCJ/CCJ/BJ/CJ			**1** 200		µA nA
ADC0833BCN/CCN			200	**1**	µA nA
I_{ON}, On Channel Leakage Current (Note 11)	On Channel = 5V, Off Channel = 0V				
ADC083BCJ/CCJ/BJ/CJ			**1** 200		µA nA
ADC0833BCN/CCN			200	**1**	µA nA
	On Channel = 0V, Off Channel = 5V				
ADC083BCJ/CCJ/BJ/CJ			**−1** −200		µA nA
ADC0833BCN/CCN			−200	**−1**	µA nA
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$				
ADC0833BCJ/CCJ/BJ/CJ			**2.0**		V
ADC0833BCN/CCN			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$				
ADC0833BCJ/CCJ/BJ/CJ			**0.8**		V
ADC0833BCN/CCN			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$				
ADC0833BCJ/CCJ/BJ/CJ		0.005	**1**		µA
ADC0833BCN/CCN		0.005	1	**1**	µA

Electrical Characteristics

The following specifications apply for $V_{CC} = V^{+} = 5V$, $f_{CLK} = 250$ kHz and $V_{REF}/2 \leq (V_{CC} + 0.1V)$ unless otherwise specified. **Boldface limits apply from t_{MIN} to t_{MAX};** all other limits $T_A = T_j = 25°C$. (Continued)

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
DIGITAL AND DC CHARACTERISTICS (Continued)					
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN} = 0V$				
ADC0833BCJ/CCJ/BJ/CJ		−0.005	**−1**		μA
ADC0833BCN/CCN		−0.005	−1	**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC} = 4.75V$				
ADC0833BCJ/CCJ/BJ/CJ	$I_{OUT} = -360\mu A$		**2.4**		V
ADC0833BCN/CCN			2.4	**2.4**	V
ADC0833BCJ/CCJ/BJ/CJ	$I_{OUT} = -10\mu A$		**4.5**		V
ADC0833BCN/CCN			4.5	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage	$I_{OUT} = 1.6mA$, $V_{CC} = 4.75V$				
ADC0833BCJ/CCJ/BJ/CJ			**0.4**		V
ADC0833BCN/CCN			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (DO, SARS)					
ADC0833BCJ/CCJ/BJ/CJ	$V_{OUT} = 0.4V$	−0.1	**−3**		μA
ADC0833BCN/CCN		−0.1	−3	**−3**	μA
ADC0833BCJ/CCJ/BJ/CJ	$V_{OUT} = 5V$	0.1	**3**		μA
ADC0833BCN/CCN		0.1	3	**3**	μA
I_{SOURCE}	V_{OUT} Short to GND				
ADC0833BCJ/CCJ/BJ/CJ		−14	**−6.5**		mA
ADC0833BCN/CCN		−14	−7.5	**−6.5**	mA
I_{SINK}	V_{OUT} Short to V_{CC}				
ADC0833BCJ/CCJ/BJ/CJ		16	**8.0**		mA
ADC0833BCN/CCN		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Note 3)	$V_{REF}/2$ Open Circuit				
ADC0833BCJ/CCJ/BJ/CJ		0.9	**4.5**		mA
ADC0833BCN/CCN		0.9	4.5	**4.5**	mA

AC Electrical Characteristics

The following specifications apply for $V_{CC} = V^+ = 5V$ and $t_r = t_f = 20$ ns unless otherwise specified. These limits apply for $T_A = T_j = 25°C$.

Parameter		Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
f_{CLK}, Clock Frequency	Min			10		kHz
	Max				400	kHz
T_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle (Note 12)	Min				40	%
	Max				60	%
t_{SET-UP}, $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge					250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge					90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 13)		$C_L = 100$ pF				
		Data MSB First	650		1500	ns
		Data LSB First	250		600	ns
t_{1H}, t_{0H}—Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z		$C_L = 10$ pF, $R_L = 10k$	125		250	ns
		$C_L = 100$ pF, $R_L = 2k$ (see TRI-STATE Test Circuits)		500	500	ns
C_{IN}, Capacitance of Logic Input			5			pF
C_{OUT}, Capacitance of Logic Outputs			5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground pins.

Note 3: Internal zener diodes (approx. 7V) are connected from V^+ to GND and V_{CC} to GND. The zener at V^+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V^+. Functionality is therefore guaranteed for V^+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max. of 6.5V. It is recommended that a resistor be used to limit the max. current into V^+.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 9: See Applications, section 3.0.

Note 10: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

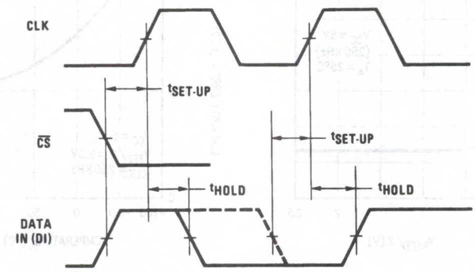
Note 11: Leakage current is measured with the clock not switching.

Note 12: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 1 μs. The maximum time the clock can be high is 60 μs. The clocked can be stopped when low so long as the analog input voltage remains stable.

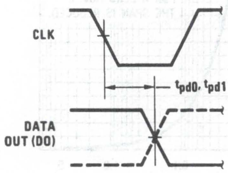
Note 13: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Timing Diagrams

Data Input Timing

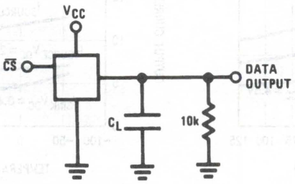

CLK
tSET-UP
CS
tSET-UP
tHOLD
tHOLD
DATA IN (DI)

Data Output Timing

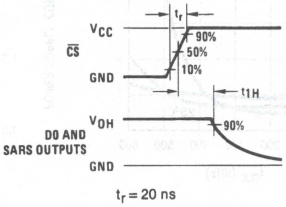

CLK
tpd0, tpd1
DATA OUT (DO)

TRI-STATE Test Circuits and Waveforms

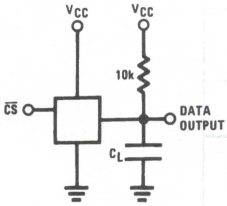
t_{1H}


VCC
CS
DATA OUTPUT
CL
10k

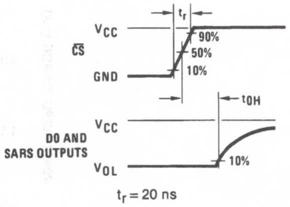
t_{1H}, $C_L = 10$ pF


tr
VCC
CS
90%
50%
10%
GND
t1H
VOH
90%
DO AND SARS OUTPUTS
GND
tr = 20 ns

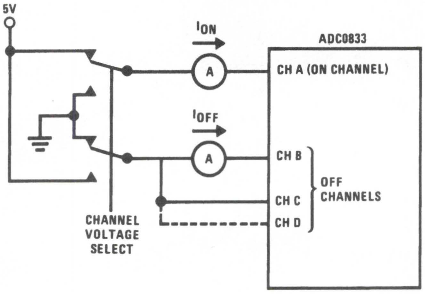
t_{0H}


VCC
VCC
10k
CS
DATA OUTPUT
CL

t_{0H}, $C_L = 10$ pF

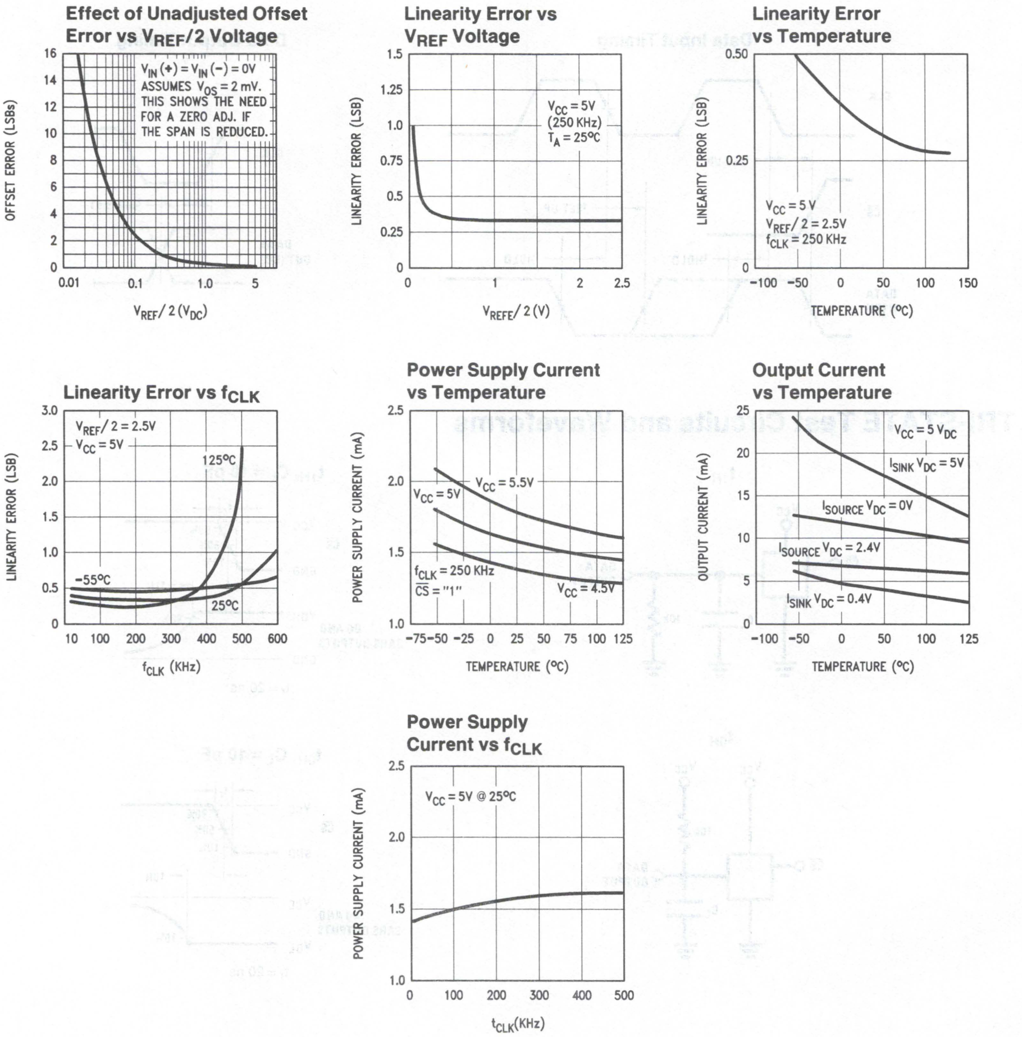

tr
VCC
CS
90%
50%
10%
GND
t0H
VCC
DO AND SARS OUTPUTS
VOL
10%
tr = 20 ns

Leakage Current Test Circuit


5V
ION
A
ADC0833
CH A (ON CHANNEL)
IOFF
A
CH B
CH C
CH D
OFF CHANNELS
CHANNEL VOLTAGE SELECT

TL/H/5607–2

Typical Performance Characteristics



Effect of Unadjusted Offset Error vs $V_{REF}/2$ Voltage

Linearity Error vs V_{REF} Voltage

Linearity Error vs Temperature

Linearity Error vs f_{CLK}

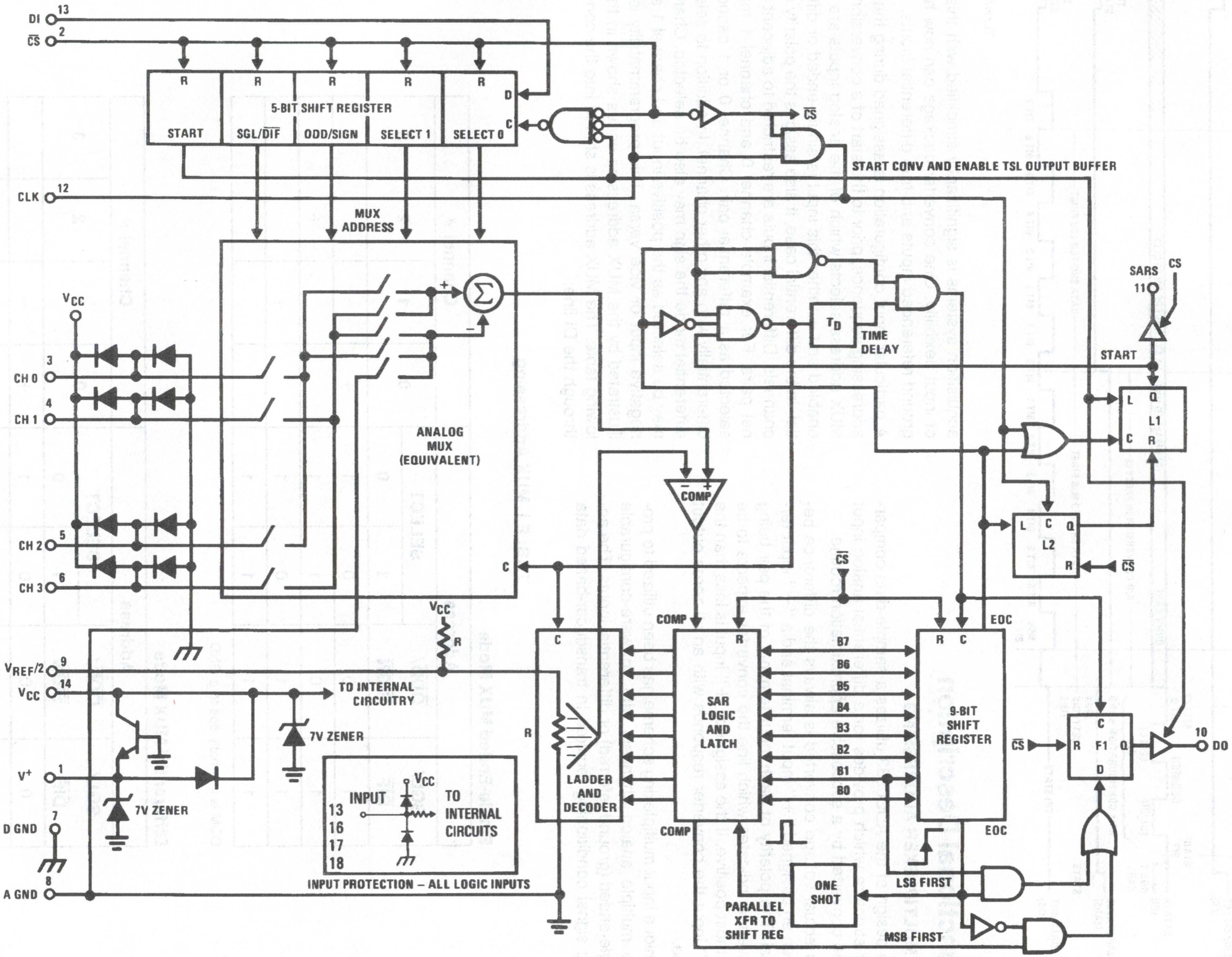
Power Supply Current vs Temperature

Output Current vs Temperature

Power Supply Current vs f_{CLK}

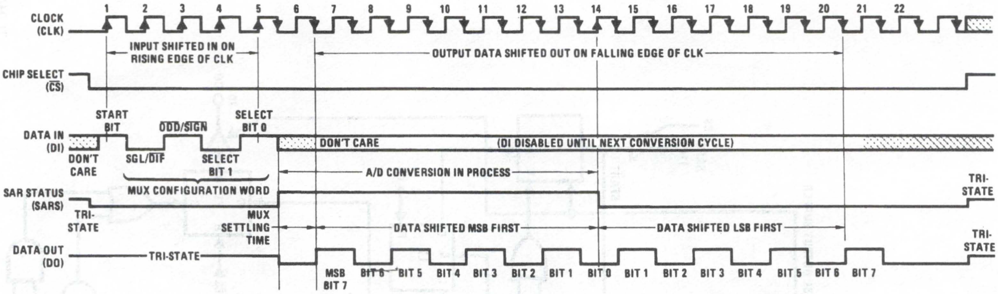
TL/H/5607–3

ADC0833 Functional Block Diagram


DI 13
CS 2
CLK 12
5-BIT SHIFT REGISTER
R
D
C
START
SGL/DIF
ODD/SIGN
SELECT 1
SELECT 0
CS
START CONV AND ENABLE TSL OUTPUT BUFFER
MUX ADDRESS
VCC
CH 0 3
CH 1 4
CH 2 5
CH 3 6
ANALOG MUX (EQUIVALENT)
Σ
+
−
C
TD
TIME DELAY
SARS 11
CS
START
L
Q
L1
C
R
L2
COMP
VCC
R
VREF/2 9
VCC 14
TO INTERNAL CIRCUITRY
7V ZENER
V+ 1
7V ZENER
D GND 7
A GND 8
INPUT
VCC
TO INTERNAL CIRCUITS
13
16
17
18
INPUT PROTECTION – ALL LOGIC INPUTS
LADDER AND DECODER
SAR LOGIC AND LATCH
COMP
B7
B6
B5
B4
B3
B2
B1
B0
9-BIT SHIFT REGISTER
EOC
F1
DO 10
ONE SHOT
PARALLEL XFR TO SHIFT REG
LSB FIRST
MSB FIRST

TL/H/5607–4

Timing Diagram


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
CLOCK (CLK)
INPUT SHIFTED IN ON RISING EDGE OF CLK
OUTPUT DATA SHIFTED OUT ON FALLING EDGE OF CLK
CHIP SELECT ($\overline{\text{CS}}$)
START BIT
$\overline{\text{ODD}}$/SIGN
SELECT BIT 0
DATA IN (DI)
DON'T CARE
SGL/$\overline{\text{DIF}}$
SELECT BIT 1
MUX CONFIGURATION WORD
DON'T CARE
(DI DISABLED UNTIL NEXT CONVERSION CYCLE)
A/D CONVERSION IN PROCESS
SAR STATUS (SARS)
TRI-STATE
TRI-STATE
MUX SETTLING TIME
DATA SHIFTED MSB FIRST
DATA SHIFTED LSB FIRST
DATA OUT (DO)
TRI-STATE
TRI-STATE
MSB BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7

TL/H/5607–5

Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of the ADC0833 utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended (ground referred) or differential inputs. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a differential pair. Channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following table. The MUX address is shifted into the converter through the DI line.

TABLE I. MUX Addressing

Single-Ended MUX Mode

Address				Channel #			
SGL/$\overline{\text{DIF}}$	$\overline{\text{ODD}}$/SIGN	SELECT		0	1	2	3
		1	0				
1	0	0	1	+			
1	0	1	1			+	
1	1	0	1		+		
1	1	1	1				+

COM is internally ties to a GND

Differential MUX Mode

Address				Channel #			
SGL/$\overline{\text{DIF}}$	$\overline{\text{ODD}}$/SIGN	SELECT		0	1	2	3
		1	0				
0	0	0	1	+	−		
0	0	1	1			+	−
0	1	0	1	−	+		
0	1	1	1			−	+

Functional Description (Continued)

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50mV above V_{CC}(typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

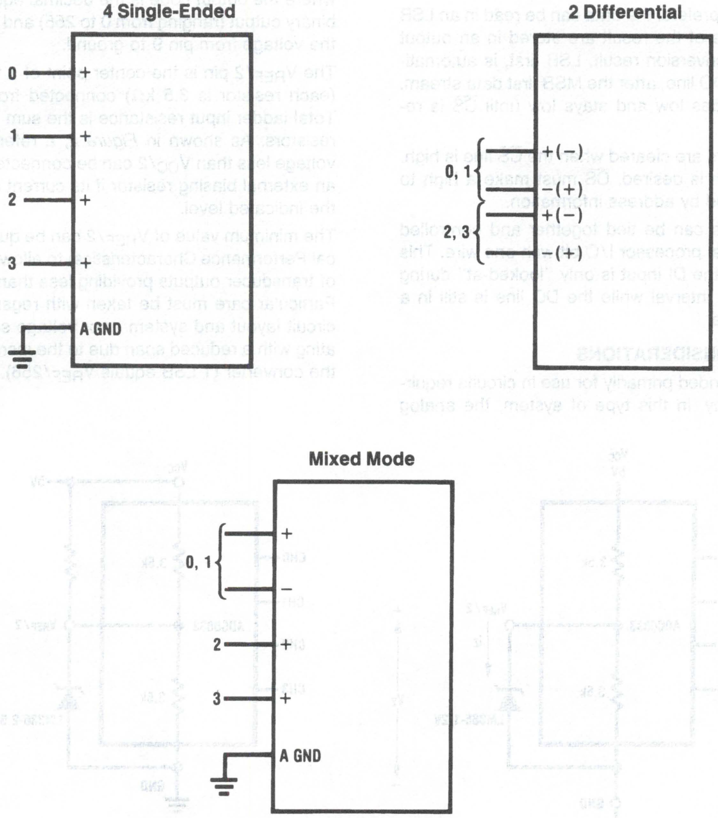
A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagram and Functional Block Diagram and to follow a complete conversion sequence.

1. A conversion is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 4 bits to be the MUX assignment word.



TL/H/5607–6

FIGURE 1. Analog Input Multiplexer Options for the ADC0833

Functional Description (Continued)

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

7. After 8 clock periods the conversion is completed. The SAR status line returns low to indicate this ½ clock cycle later.

8. If the programmer prefers, the data can be read in an LSB first format. All 8 bits of the result are stored in an output shift register. The conversion result, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

3.0 REFERENCE CONSIDERATIONS

The ADC0833 is intended primarily for use in circuits requiring absolute accuracy. In this type of system, the analog inputs vary between very specific voltage limits and the reference voltage for the A/D converter must remain stable with time and temperature. For ratiometric applications, an ADC0834 is a pin-for-pin compatible alternative since it has a V_{REF} input (note the ADC0834 needs one less bit of mux addressing information).

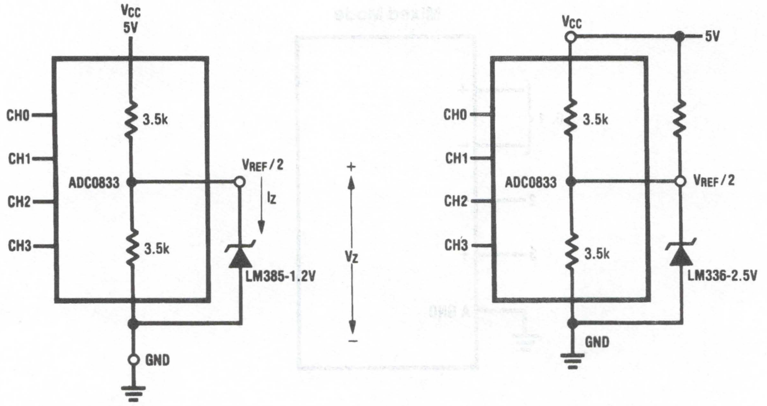
The voltage applied to the $V_{REF}/2$ pin defines the voltage span of the analog input [the difference between $V_{IN}(+)$ and $V_{IN}(-)$] over which the 256 possible output codes apply. A full-scale conversion (an all 1s output code) will result when the voltage difference between a selected "+" input and "−" input is approximately *twice* the voltage at the $V_{REF}/2$ pin. This internal gain of 2 from the applied reference to the full-scale input voltage allows biasing a low voltage reference diode from the $5V_{DC}$ converter supply. To accommodate a 5V input span, only a 2.5V reference is required. The LM385 and LM336 reference diodes are good low current devices to use with these converters. The output code changes in accordance with the following equation:

$$\text{Output Code} = 256 \left(\frac{V_{IN}(+) - V_{IN}(-)}{2(V_{REF}/2)} \right)$$

where the output code is the decimal equivalent of the 8-bit binary output (ranging from 0 to 255) and the term $V_{REF}/2$ is the voltage from pin 9 to ground.

The $V_{REF}/2$ pin is the center point of a two resistor divider (each resistor is 3.5 kΩ) connected from V_{CC} to ground. Total ladder input resistance is the sum of these two equal resistors. As shown in *Figure 2,* a reference diode with a voltage less than $V_{CC}/2$ can be connected without requiring an external biasing resistor if its current requirements meet the indicated level.

The minimum value of $V_{REF}/2$ can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).



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$V_{FULL\text{-}SCALE} \cong 2.4V$ $\qquad$ $V_{FULL\text{-}SCALE} \cong 5.0V$

Note: No external biasing resistor needed if $V_Z < \frac{V_{CC}}{2}$ and $I_Z \text{ min} < \frac{V_{CC}/2 - V_Z}{1.75\ k\Omega}$

FIGURE 2. Reference Biasing Examples

Functional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the inputs be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(\max) = V_{PEAK}(2\pi f_{CM})\left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK} is the A/D clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ± 1 μA over temperature will create a 1 mV inut error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input or V_{CC} for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper $V_{In}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

and

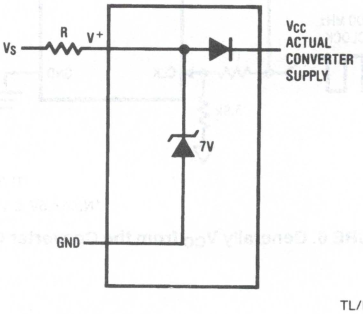
V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The $V_{REF}/2$ voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

6.0 POWER SUPPLY

A unique feature of the ADC0833 is the inclusion of a 7V zener diode connected from the V+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in *Figure 3.*



TL/H/5607–8

FIGURE 3. An On-Chip Shunt Regulator Diode

Functional Description (Continued)

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. *Figures 4* and *5* illustrate two useful applications of this on-board zener when an external transistor can be afforded.

An important use of the interconnecting diode between V+ and V_{CC} is shown in *Figures 6* and *7*. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The low current requirements of the A/D (~3 mA) and the relatively high clock frequencies used (typically in the range of 10k-400 kHz) allows using the small value filter capacitor shown to keep the ripple on the V_{CC} line to well under ¼ of an LSB. The shunt zener regulator can also be used in this mode. This requires a clock voltage swing which is in excess of V_Z. A current limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V+ pin.

Applications

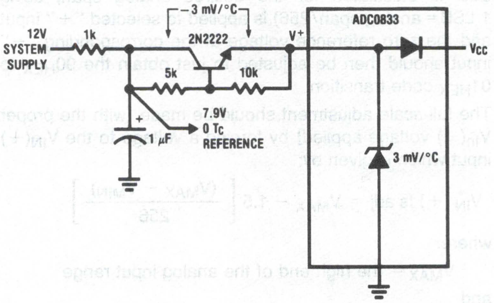

12V
SYSTEM
SUPPLY
1k
−3 mV/°C
2N2222
5k
10k
+
1 µF
7.9V
0 Tc
REFERENCE
ADC0833
V+
Vcc
3 mV/°C
TL/H/5607–15

FIGURE 4. Operating with a Temperature Compensated Reference

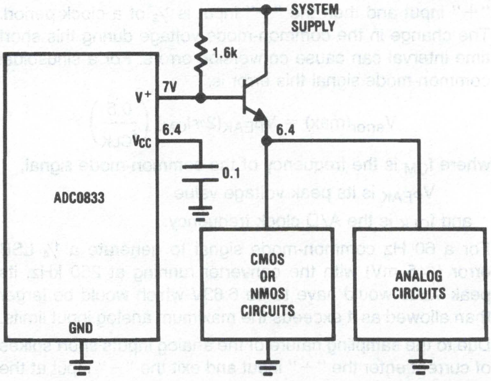
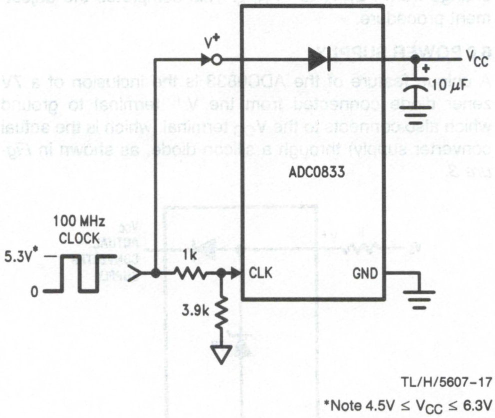

12V
SYSTEM
SUPPLY
1.6k
7V
V+
6.4
6.4
Vcc
0.1
ADC0833
GND
CMOS
OR
NMOS
CIRCUITS
ANALOG
CIRCUITS
TL/H/5607–16

FIGURE 5. Using the A/D as the System Supply Regulator


V+
Vcc
+
10 µF
ADC0833
100 MHz
CLOCK
5.3V*
0
1k
CLK
GND
3.9k
TL/H/5607–17

*Note 4.5V ≤ V_{CC} ≤ 6.3V

FIGURE 6. Generally V_{CC} from the Converter Clock

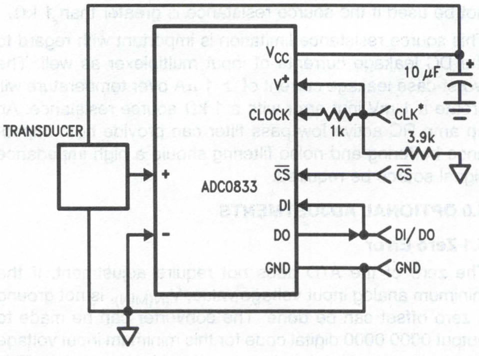
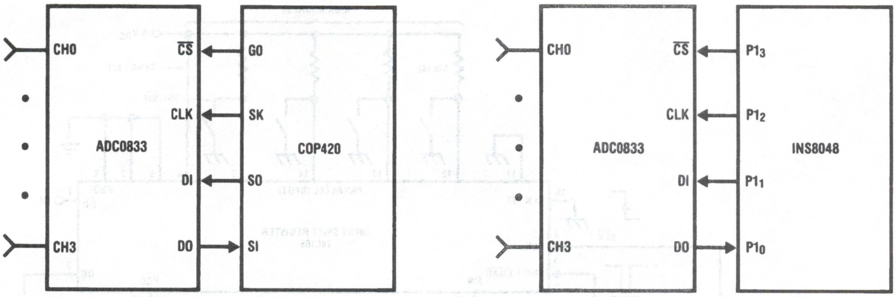

Vcc
V+
10 µF
CLOCK
1k
CLK*
3.9k
TRANSDUCER
+
−
CS
CS
ADC0833
DI
DO
DI/DO
GND
GND
TL/H/5607–9

FIGURE 7. Remote Sensing—Clock and Power on 1 Wire

Applications (Continued)

Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048



TL/H/5607-10

COP CODING EXAMPLE

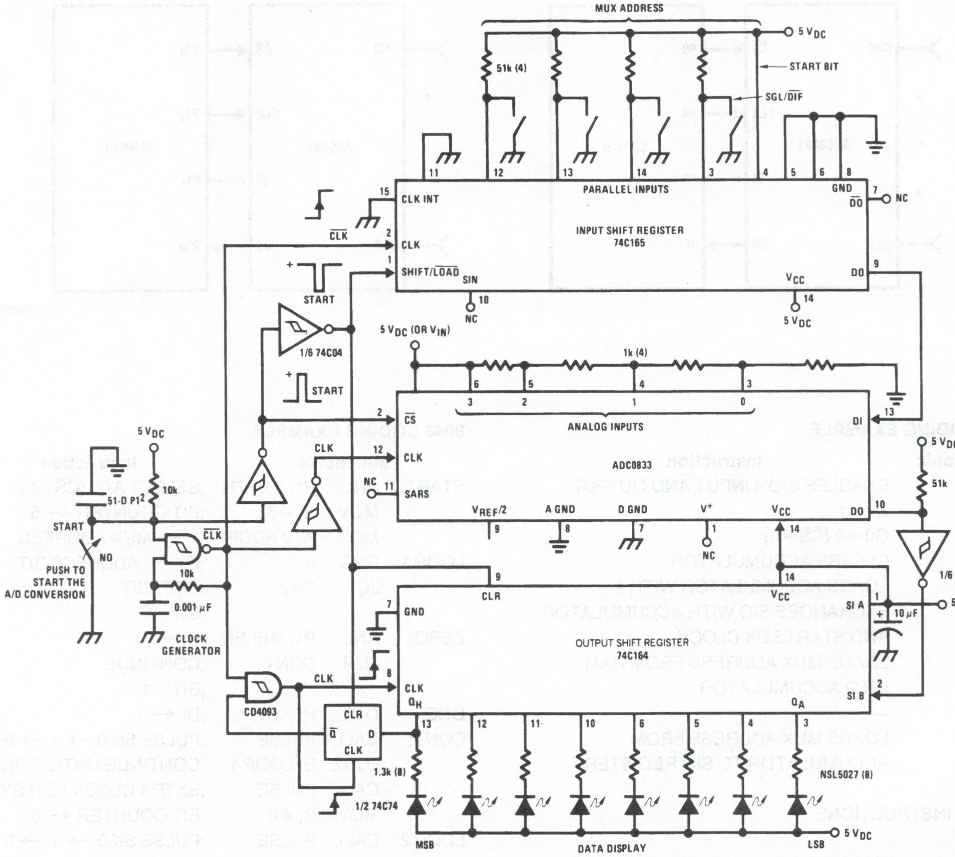
Mnemonic	Instruction
LEI	ENABLES SIO's INPUT AND OUTPUT
SC	C = 1
OGI	G0 = 0 ($\overline{CS}$ = 0)
CLR A	CLEARS ACCUMULATOR
AISC 1	LOADS ACCUMULATOR WITH 1
XAS	EXCHANGES SIO WITH ACCUMULATOR AND STARTS SK CLOCK
LDD	LOADS MUX ADDRESS FROM RAM INTO ACCUMULATOR
NOP	—
XAS	LOADS MUX ADDRESS FROM ACCUMULATOR TO SIO REGISTER
↑ 8 INSTRUCTIONS ↓	
XAS	READS HIGH ORDER NIBBLE (4 BITS) INTO ACCUMULATOR
XIS	PUTS HIGH ORDER NIBBLE INTO RAM
CLR A	CLEARS ACCUMULATOR
RC	C = 0
XAS	READS LOW ORDER NIBBLE INTO ACCUMULATOR AND STOPS SK
XIS	PUTS LOW ORDER NIBBLE INTO RAM
OGI	G0 = 1 ($\overline{CS}$ = 1)
LEI	DISABLES SIO's INPUT AND OUTPUT

8048 CODING EXAMPLE

```
         Mnemonic                   Instruction
START:   ANL   P1, #0F7H    ;SELECT A/D (CS=0)
         MOV   B, #5        ;BIT COUNTER ← 5
         MOV   A, #ADDR     ;A ← MUX ADDRESS
LOOP 1:  RRC   A            ;CY ← ADDRESS BIT
         JC    ONE          ;TEST BIT
                            ;BIT=0
ZERO:    ANL   P1, #0FEH    ;DI ← 0
         JMP   CONT         ;CONTINUE
                            ;BIT=1
ONE:     ORL   P1, #1       ;DI ← 1
CONT:    CALL  PULSE        ;PULSE SK 0 → 1 → 0
         DJNZ  B, LOOP 1    ;CONTINUE UNTIL DONE
         CALL  PULSE        ;EXTRA CLOCK FOR SYNC
         MOV   B, #8        ;BIT COUNTER ← 8
LOOP 2:  CALL  PULSE        ;PULSE SK 0 → 1 → 0
         IN    A, P1        ;CY ← DO
         RRC   A
         RRC   A
         MOV   A, C         ;A ← RESULT
         RLC   A            ;A(0) ← BIT AND SHIFT
         MOV   C, A         ;C ← RESULT
         DJNZ  B, LOOP 2    ;CONTINUE UNTIL DONE
RETR
                            ;PULSE SUBROUTINE
PULSE:   ORL   P1, #04      ;SK ← 1
         NOP                ;DELAY
         ANL   P1, #0FBH    ;SK ← 0
         RET
```

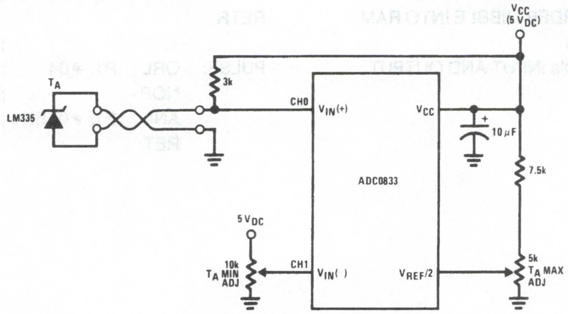
Applications (Continued)

A "Stand-Alone" Hook-Up for ADC0833 Evaluation



MUX ADDRESS
5 V_{DC}
START BIT
SGL/$\overline{DIF}$
51k (4)
11
12
13
14
3
4
5
6
8
PARALLEL INPUTS
GND
7
$\overline{DO}$
NC
15
CLK INT
$\overline{CLK}$
2
CLK
1
SHIFT/$\overline{LOAD}$
SIN
INPUT SHIFT REGISTER
74C165
V_{CC}
DO
9
10
NC
14
5 V_{DC}
START
1/6 74C04
5 V_{DC} (OR V_{IN})
1k (4)
6
5
4
3
2
1
0
START
ANALOG INPUTS
13
DI
5 V_{DC}
$\overline{CS}$
CLK
12
CLK
NC
11
SARS
ADC0833
V_{REF}/2
A GND
D GND
V^{+}
V_{CC}
DO
9
8
7
1
NC
14
10
51k
1/6 74C14
5 V_{DC}
10k
51-D P1
START
$\overline{CLK}$
NO
PUSH TO START THE A/D CONVERSION
10k
0.001 µF
CLOCK GENERATOR
9
CLR
14
V_{CC}
SI A
10 µF
5 V_{DC}
7
GND
OUTPUT SHIFT REGISTER
74C164
8
CLK
CLK
Q_H
CD4093
CLR
$\overline{Q}$
D
CLK
2
SI B
Q_A
13
12
11
10
6
5
4
3
1.3k (8)
NSL5027 (8)
1/2 74C74
MSB
DATA DISPLAY
LSB
5 V_{DC}

Low Cost Remote Temperature Sensor

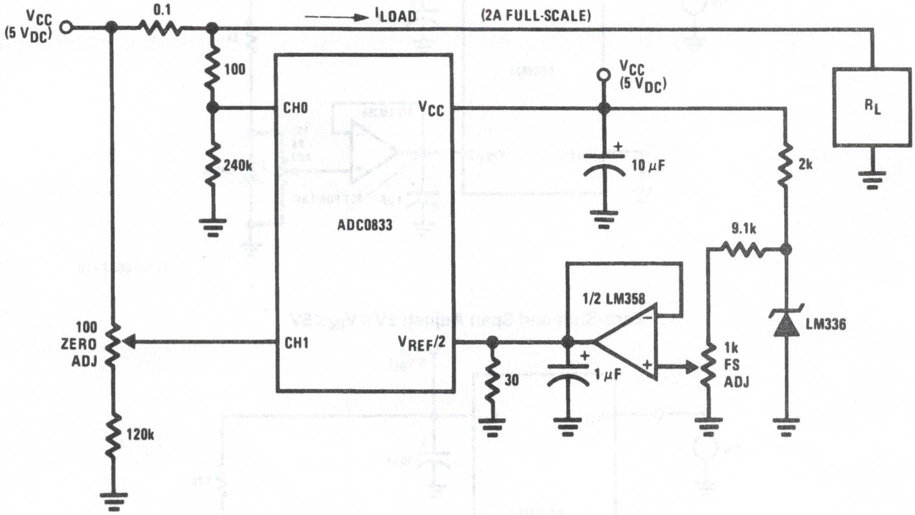


V_{CC} (5 V_{DC})
T_A
LM335
3k
CH0
$V_{IN}(+)$
V_{CC}
10 µF
ADC0833
7.5k
5 V_{DC}
10k
T_A MIN ADJ
CH1
$V_{IN}(-)$
V_{REF}/2
5k
T_A MAX ADJ

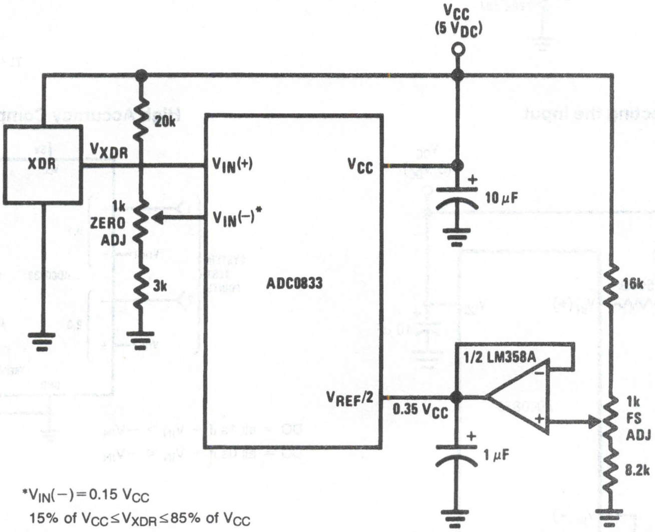
TL/H/5607-11

Applications (Continued)

Digitizing a Current Flow


VCC (5 VDC)
0.1
ILOAD
(2A FULL-SCALE)
100
240k
CH0
VCC
ADC0833
VCC (5 VDC)
10 µF
2k
RL
9.1k
1/2 LM358
LM336
100 ZERO ADJ
CH1
VREF/2
30
1 µF
1k FS ADJ
120k

Operating with Automotive Ratiometric Transducers


VCC (5 VDC)
20k
XDR
VXDR
VIN(+)
VCC
10 µF
1k ZERO ADJ
VIN(−)*
3k
ADC0833
16k
1/2 LM358A
VREF/2
0.35 VCC
1k FS ADJ
1 µF
8.2k

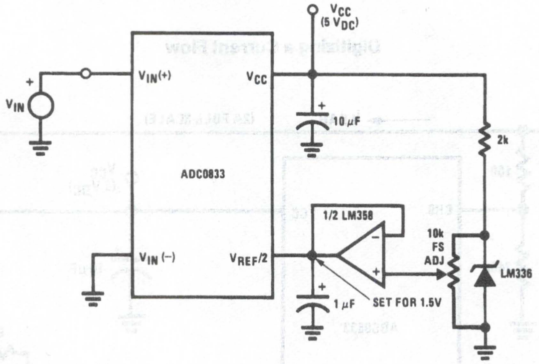
*$V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

TL/H/5607–12

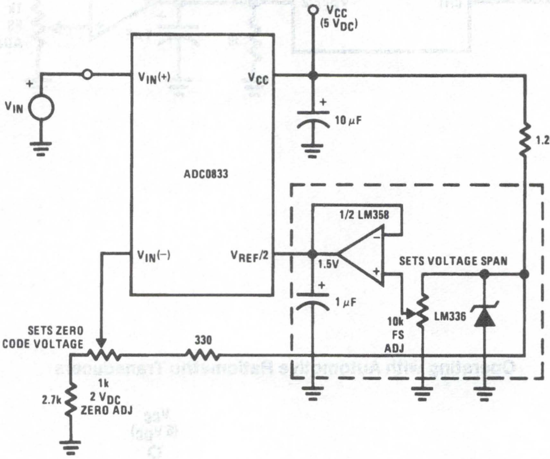
Applications (Continued)

Span Adjust: $0V \leq V_{IN} \leq 3V$


VCC
(5 VDC)
VIN(+)
VCC
+
VIN
10 µF
2k
ADC0833
1/2 LM358
10k
FS
ADJ
LM336
VIN(−)
VREF/2
1 µF
SET FOR 1.5V

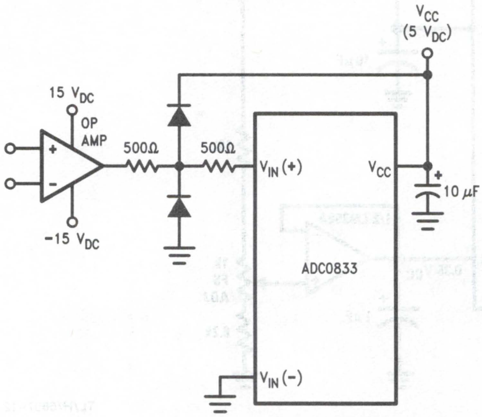
TL/H/5607-18

Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$


VCC
(5 VDC)
VIN(+)
VCC
+
VIN
10 µF
1.2k
ADC0833
1/2 LM358
VIN(−)
VREF/2
1.5V
SETS VOLTAGE SPAN
1 µF
10k
FS
ADJ
LM336
SETS ZERO
CODE VOLTAGE
330
1k
2.7k
2 VDC
ZERO ADJ

TL/H/5607-19

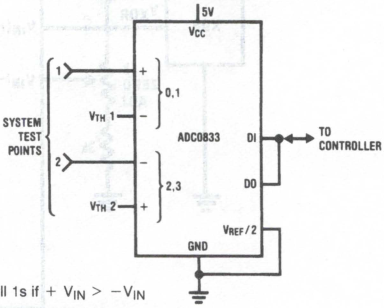
Protecting the Input


VCC
(5 VDC)
15 VDC
OP
AMP
500Ω
500Ω
VIN (+)
VCC
10 µF
−15 VDC
ADC0833
VIN (−)

Diodes are 1N914

TL/H/5607-20

High Accuracy Comparators


5V
VCC
1
+
0,1
VTH 1
−
SYSTEM
TEST
POINTS
ADC0833
DI
TO
CONTROLLER
2
−
2,3
DO
VTH 2
+
VREF/2
GND

DO = all 1s if $+V_{IN} > -V_{IN}$

DO = all 0s if $+V_{IN} < -V_{IN}$

TL/H/5607-13

For additional application ideas, refer to the data sheet for the ADC0831 family of serial data converters.

Ordering Information

Part Number	Temperature Range	Total Unadjusted Error
ADC0833BCJ	−40°C to +85°C	±1/2 LSB
ADC0833BCN	0°C to +70°C	
ADC0833BJ	−55°C to +125°C	
ADC0833CCJ	−40°C to +85°C	±1 LSB
ADC0833CCN	0°C to +70°C	
ADC0833CJ	−55°C to +125°C	

National
Semiconductor
Corporation

ADC0841 8-Bit µP Compatible A/D Converter

General Description

The ADC0841 is a CMOS 8-bit successive approximation A/D converter. Differential inputs provide low frequency input common mode rejection and allow offsetting the analog range of the converter. In addition, the reference input can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

The A/D is designed to operate with the control bus of a variety of microprocessors. TRI-STATE® output latches that directly drive the data bus permit the A/D to be configured as a memory location or I/O device to the microprocessor with no interface logic necessary.

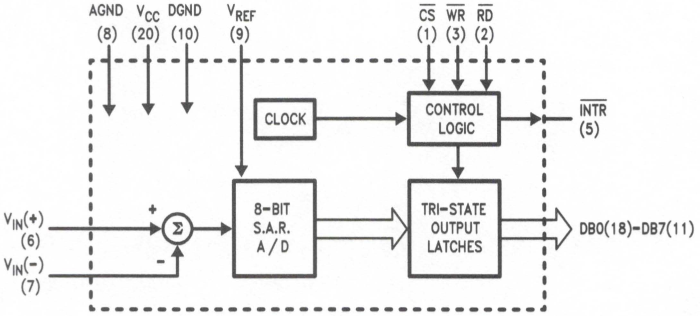
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- Internal clock
- 0V to 5V input range with single 5V power supply
- 0.3″ standard width 20-pin package
- 20 Pin Molded Chip Carrier Package

Key Specifications

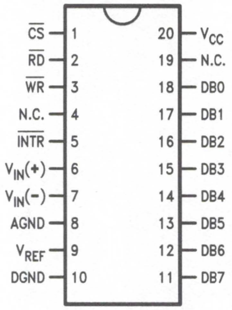
■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	40 µs

Block and Connection Diagrams


AGND (8)
V_{CC} (20)
DGND (10)
V_{REF} (9)
$\overline{CS}$ (1)
$\overline{WR}$ (3)
$\overline{RD}$ (2)
CLOCK
CONTROL LOGIC
$\overline{INTR}$ (5)
$V_{IN}(+)$ (6)
$V_{IN}(-)$ (7)
+
-
Σ
8-BIT S.A.R. A/D
TRI-STATE OUTPUT LATCHES
DB0(18)-DB7(11)

TL/H/8557-1

Dual-In-Line Package

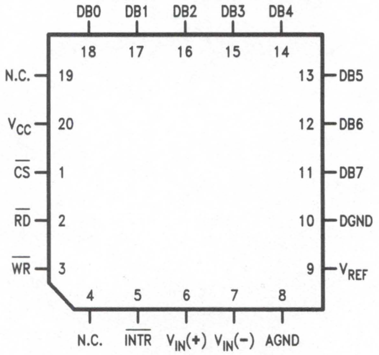

$\overline{CS}$ 1
$\overline{RD}$ 2
$\overline{WR}$ 3
N.C. 4
$\overline{INTR}$ 5
$V_{IN}(+)$ 6
$V_{IN}(-)$ 7
AGND 8
V_{REF} 9
DGND 10
20 V_{CC}
19 N.C.
18 DB0
17 DB1
16 DB2
15 DB3
14 DB4
13 DB5
12 DB6
11 DB7

Top View

TL/H/8557-2

(N.C.-No Connection)

Molded Chip Carrier Package


DB0 18
DB1 17
DB2 16
DB3 15
DB4 14
N.C. 19
V_{CC} 20
$\overline{CS}$ 1
$\overline{RD}$ 2
$\overline{WR}$ 3
13 DB5
12 DB6
11 DB7
10 DGND
9 V_{REF}
4 N.C.
5 $\overline{INTR}$
6 $V_{IN}(+)$
7 $V_{IN}(-)$
8 AGND

TL/H/8557-3

Top View

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage	
Logic Control Inputs	$-0.3V$ to $V_{CC}+0.3V$
At Other Inputs and Outputs	$-0.3V$ to $V_{CC}+0.3V$
Input Current Per Pin (Note 3)	±5 mA
Input Current Per Package (Note 3)	±20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at $T_A=25°C$	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 10)	800V

Operating Conditions (Notes 1 and 2)

Supply Voltage (V_{CC})	$4.5\ V_{DC}$ to $6.0\ V_{DC}$
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0841BCN, ADC0841CCN	$0°C \le T_A \le 70°C$
ADC0841BCJ, ADC0841CCJ, ADC0841BCV, ADC0841CCV	$-40°C \le T_A \le 85°C$
ADC0841BJ, ADC0841CJ	$-55°C \le T_A \le 125°C$

Electrical Characteristics

The following specifications apply for $V_{CC}=5\ V_{DC}$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A=T_j=25°C$.

Parameter	Conditions	ADC0841BJ, ADC0841BCJ ADC0841CJ, ADC0841CCJ			ADC0841BCN, ADC0841CCN ADC0841BCV, ADC0841CCV			Units
		Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Maximum Total Unadjusted Error	$V_{REF}=5.00\ V_{DC}$ (Note 4)							
ADC0841BCN, BCV						±½	**±½**	LSB
ADC0841BJ, BCJ			**±½**					LSB
ADC0841CCN, CCV						±1	**±1**	LSB
ADC0841CJ, CCJ			**±1**					LSB
Minimum Reference Input Resistance		2.4	**1.1**		2.4	1.2	**1.1**	kΩ
Maximum Reference Input Resistance		2.4	**5.9**		2.4	5.4	**5.9**	kΩ
Maximum Common-Mode Input Voltage	(Note 5)		**V_{CC}+0.05**			V_{CC}+0.05	**V_{CC}+0.05**	V
Minimum Common-Mode Input Voltage	(Note 5)		**GND−0.05**			GND−0.05	**GND−0.05**	V
DC Common-Mode Error	Differential Mode	±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
Power Supply Sensitivity	$V_{CC}=5V\pm5\%$	±1/16	**±⅛**		±1/16	±⅛	**±⅛**	LSB

Electrical Characteristics

The following specifications apply for $V_{CC}=5\ V_{DC}$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A=T_j=25°C$. (Continued)

Symbol	Parameter	Conditions	ADC0841BJ, ADC0841BCJ ADC0841CJ, ADC0841CCJ Typ (Note 6)	 Tested Limit (Note 7)	 Design Limit (Note 8)	ADC0841BCN, ADC0841CCN ADC0841BCV, ADC0841CCV Typ (Note 6)	 Tested Limit (Note 7)	 Design Limit (Note 8)	Units
DIGITAL AND DC CHARACTERISTICS									
$V_{IN(1)}$	Logical "1" Input Voltage (Min)	$V_{CC}=5.25V$		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$	Logical "0" Input Voltage (Max)	$V_{CC}=4.75V$		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$	Logical "1" Input Current (Max)	$V_{IN}=5.0V$	0.005	**1**		0.005		**1**	µA
$I_{IN(0)}$	Logical "0" Input Current (Max)	$V_{IN}=0V$	−0.005	**−1**		−0.005		**−1**	µA
$V_{OUT(1)}$	Logical "1" Output Voltage (Min)	$V_{CC}=4.75V$ $I_{OUT}=-360\ \mu A$ $I_{OUT}=-10\ \mu A$		 **2.4** **4.5**			 2.8 4.6	 **2.4** **4.5**	 V V
$V_{OUT(0)}$	Logical "0" Output Voltage (Max)	$V_{CC}=4.75V$ $I_{OUT}=1.6\ mA$		**0.4**			0.34	**0.4**	V
I_{OUT}	TRI-STATE Output Current (Max)	$V_{OUT}=0V$ $V_{OUT}=5V$	−0.01 0.01	**−3** **3**		−0.01 0.01	−0.3 0.3	**−3** **3**	µA µA
I_{SOURCE}	Output Source Current (Min)	$V_{OUT}=0V$	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}	Output Sink Current (Min)	$V_{OUT}=V_{CC}$	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}	Supply Current (Max)	$\overline{CS}=1$, V_{REF} Open	1	**2.5**		1	2.3	**2.5**	mA

AC Characteristics

The following specifications apply for $V_{CC} = 5V_{DC}$, $t_r = t_f = 10$ ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_C	Maximum Conversion Time (See Graph)		30	40	**60**	µs
$t_{W(\overline{WR})}$	Minimum $\overline{WR}$ Pulse Width	(Note 9)	50	150		ns
t_{ACC}	Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF (Note 9)	145	225		ns
t_{1H}, t_{0H}	TRI-STATE Control (Maximum Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$C_L = 10$ pF, $R_L = 10k$, $t_r = 20$ ns (Note 9)	125		200	ns
t_{WI}, t_{RI}	Maximum Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$	(Note 9)	200	400		ns
C_{IN}	Capacitance of Logic Inputs		5			pF
C_{OUT}	Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground pins.

Note 3: During over-voltage conditions ($V_{IN} < 0V$ and $V_{IN} > V_{CC}$) the maximum input current at any one pin is ±5 mA. If the current is limited to ±5 mA at all the pins no more than four pins can be in this condition in order to meet the Input Current Per Package (±20 mA) specification.

Note 4: Total undajusted error includes offset, full-scale, and linearity.

Note 5: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

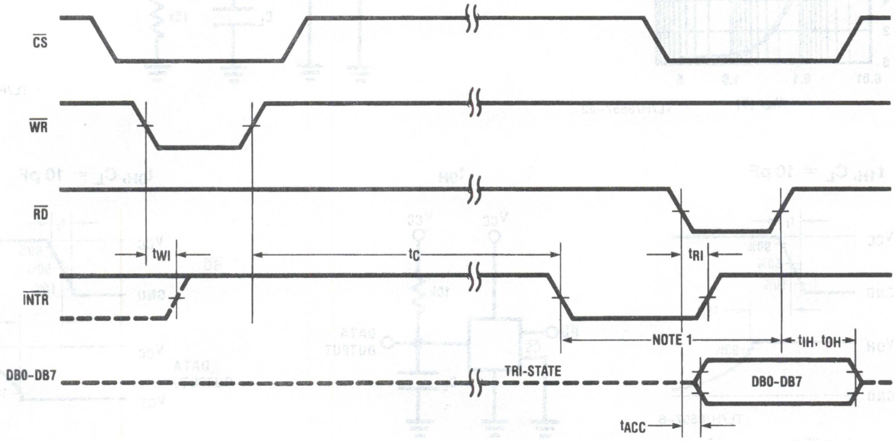
Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 9: The temperature coefficient is 0.3%/°C.

Note 10: Human body model, 100 pF discharged through 1.5 kΩ resistor.

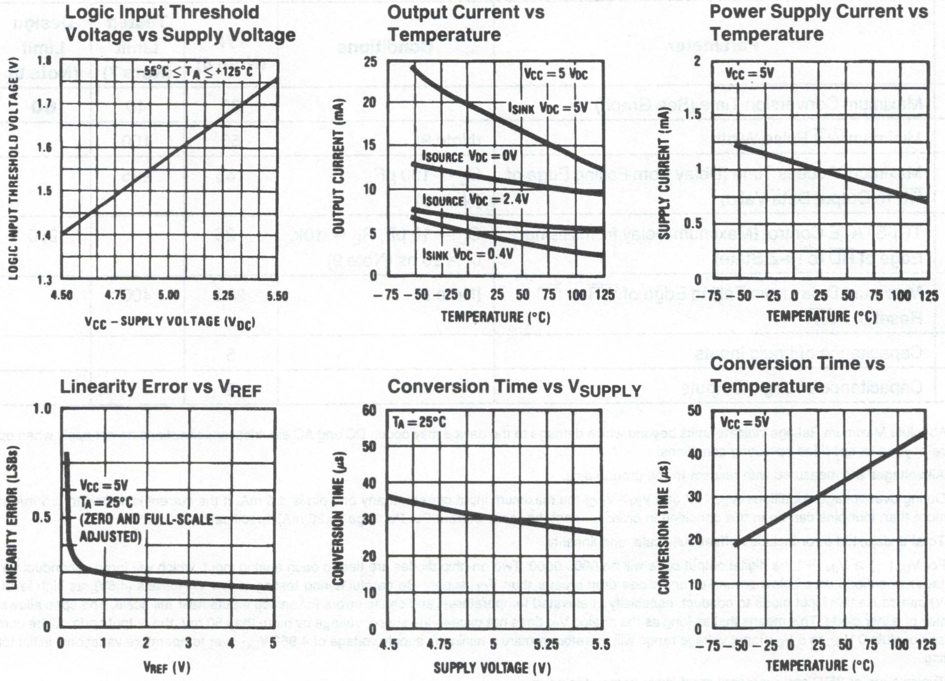
Timing Diagram



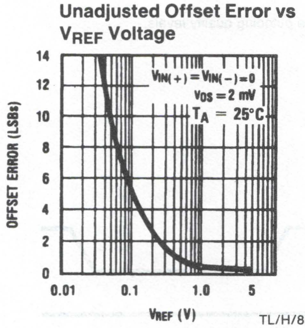
TL/H/8557-9

Note 1: Read strobe must occur at least 600 ns after the assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Performance Characteristics

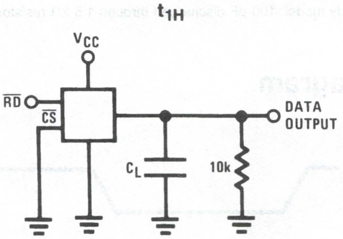


TL/H/8557–4

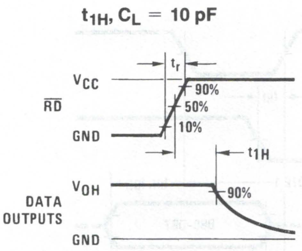


TL/H/8557–22

TRI-STATE Test Circuits and Waveforms

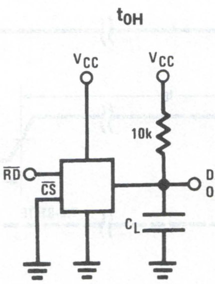

t_{1H}
V_{CC}
$\overline{RD}$
$\overline{CS}$
DATA OUTPUT
C_L
10k

TL/H/8557–5

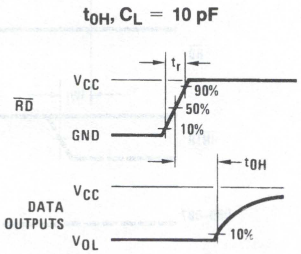

t_{1H}, C_L = 10 pF
t_r
V_{CC}
$\overline{RD}$
GND
90%
50%
10%
t_{1H}
V_{OH}
DATA OUTPUTS
GND
90%

TL/H/8557–6

t_r = 20 ns


t_{0H}
V_{CC}
V_{CC}
10k
$\overline{RD}$
$\overline{CS}$
DATA OUTPUT
C_L

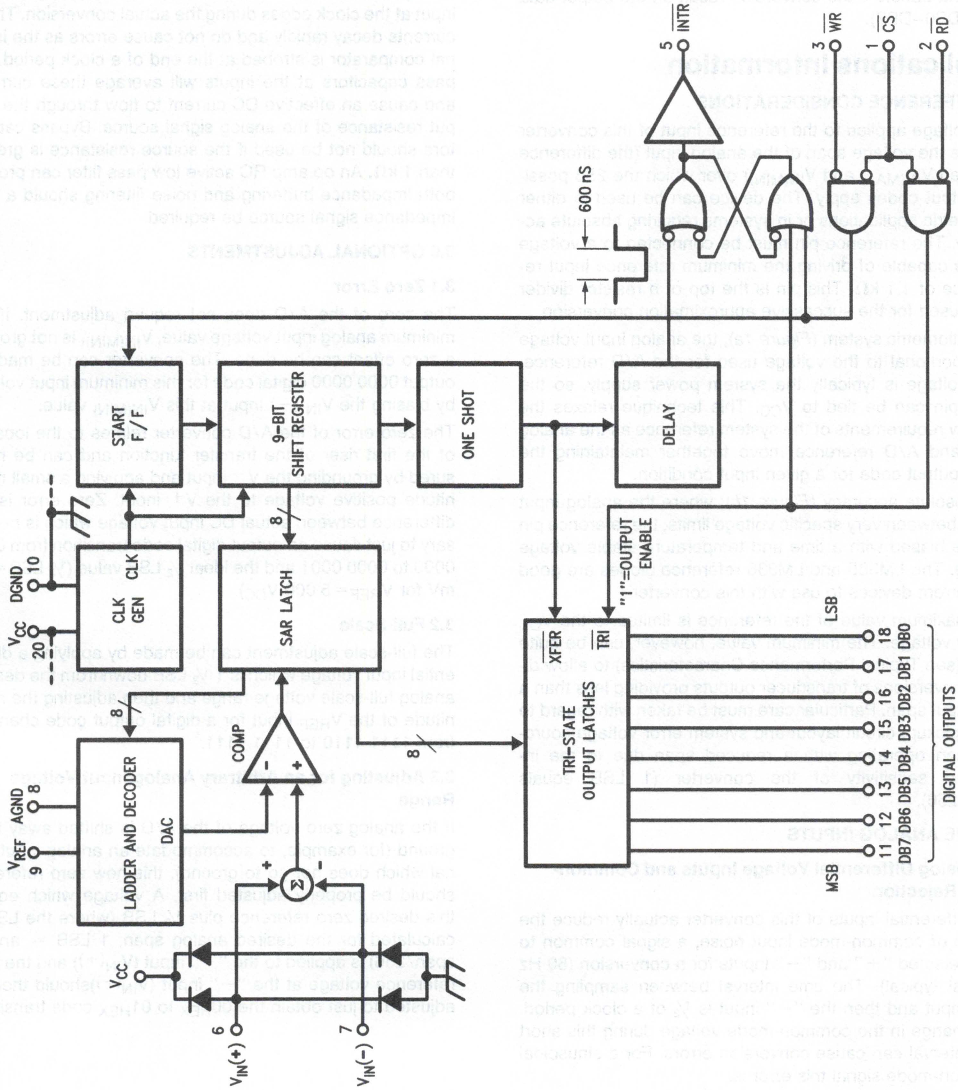
TL/H/8557–7


t_{0H}, C_L = 10 pF
t_r
V_{CC}
$\overline{RD}$
GND
90%
50%
10%
t_{0H}
V_{CC}
DATA OUTPUTS
V_{OL}
10%

TL/H/8557–8

t_r = 20 ns

Functional Block Diagram


V_REF 9
AGND 8
V_CC 20
DGND 10
LADDER AND DECODER
DAC
CLK GEN
CLK
START F/F
8
V_CC
6
V_IN(+)
7
V_IN(−)
Σ
+
−
COMP
SAR LATCH
9-BIT SHIFT REGISTER
8
ONE SHOT
DELAY
8
600 nS
TRI-STATE OUTPUT LATCHES
XFER
TRI
"1"=OUTPUT ENABLE
5 INTR
3 WR
1 CS
2 RD
MSB
LSB
11 DB7
12 DB6
13 DB5
14 DB4
15 DB3
16 DB2
17 DB1
18 DB0
DIGITAL OUTPUTS

TL/H/8557–10

Functional Description

A conversion is initiated via the $\overline{CS}$ and $\overline{WR}$ lines. If the data from a previous conversion is not read, the $\overline{INTR}$ line will be low. The falling edge of $\overline{WR}$ will reset the $\overline{INTR}$ line high and ready the A/D for a conversion cycle. The rising edge of $\overline{WR}$ starts a conversion. After the conversion cycle ($t_C \leq 60$ μsec), which is set by the internal clock frequency, the digital data is transferred to the output latch and the $\overline{INTR}$ is asserted low. Taking $\overline{CS}$ and $\overline{RD}$ low resets $\overline{INTR}$ output high and transfers the conversion result on the output data lines (DB0–DB7).

Applications Information

1.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input of this converter defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The device can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the minimum reference input resistance of 1.1 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 1a*), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 1b*), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with this converter.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).

2.0 THE ANALOG INPUTS

2.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential inputs of this converter actually reduce the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{ERROR(MAX)} = V_{peak}\,(2\pi\, f_{CM}) \times 0.5 \times \left(\frac{t_C}{8}\right)$$

where f_{CM} is the frequency of the common-mode signal, Vpeak is its peak voltage value and t_C is the conversion time.

For a 60 Hz common-mode signal to generate a ¼ LSB error ($\approx$5 mV) with the converter running at 40 μS, its peak value would have to be 5.43V. This large a common-mode signal is much greater than that generally found in a well designed data acquisition system.

2.2 Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

3.0 OPTIONAL ADJUSTMENTS

3.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the V_{IN} (−) input at this $V_{IN(MIN)}$ value.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V^- input and applying a small magnitude positive voltage to the V^+ input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF} = 5.000\ V_{DC}$).

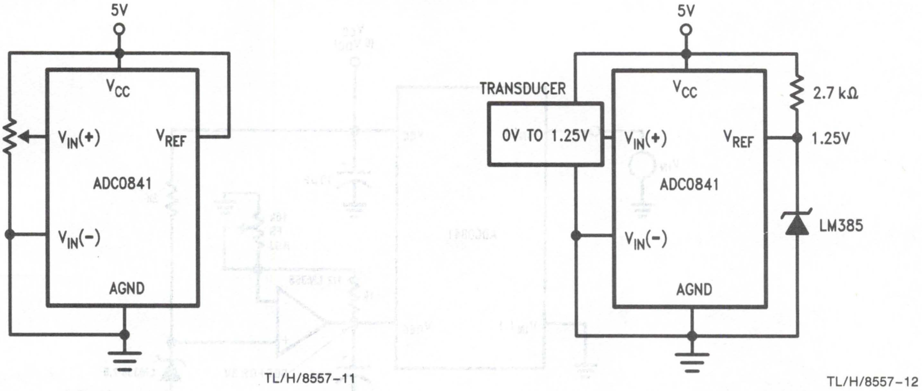
3.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code changing from 1111 1110 to 1111 1111.

3.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to the "+" input ($V_{IN}{}^{(+)}$) and the zero reference voltage at the "−" input ($V_{IN}{}^{(-)}$)should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

Applications Information (Continued)


5V
V_{CC}
$V_{IN}(+)$
V_{REF}
ADC0841
$V_{IN}(-)$
AGND
TL/H/8557-11
5V
TRANSDUCER
0V TO 1.25V
V_{CC}
$V_{IN}(+)$
V_{REF}
ADC0841
$V_{IN}(-)$
AGND
2.7 kΩ
1.25V
LM385
TL/H/8557-12

a) Ratiometric

b) Absolute with a Reduced Span

FIGURE 1. Referencing Examples

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

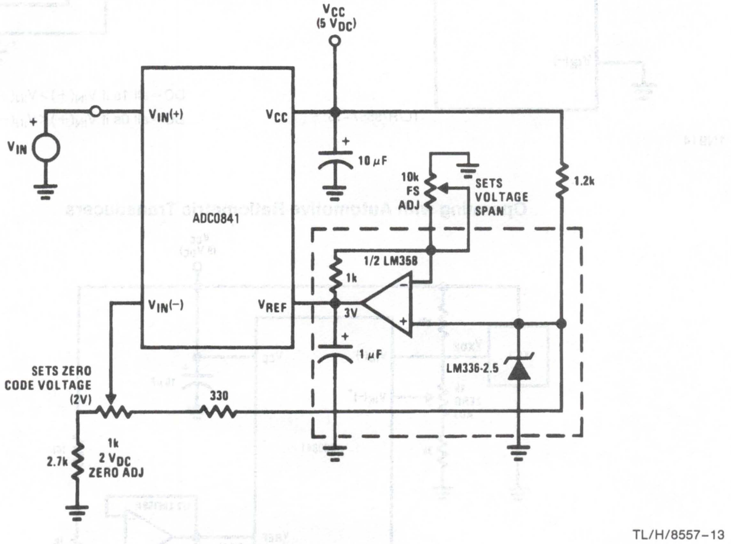
$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX}-V_{MIN})}{256}\right]$$

where V_{MAX} = the high end of the analog input range and V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

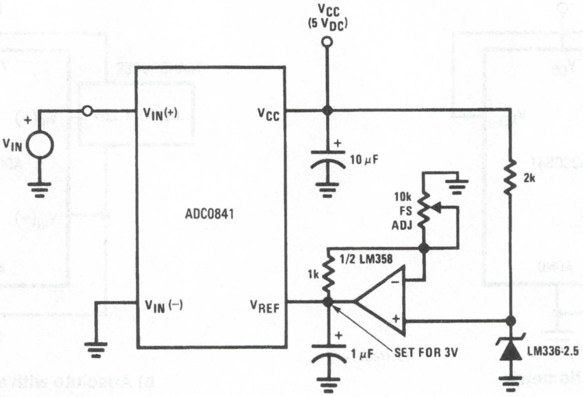
For an example see the Zero-Shift and Span Adjust circuit below.

Zero-Shift and Span Adjust ($2V \leq V_{IN} \leq 5V$)


V_{CC} ($5\ V_{DC}$)
$V_{IN}(+)$
V_{CC}
+
V_{IN}
+
10 µF
10k FS ADJ
SETS VOLTAGE SPAN
1.2k
ADC0841
1/2 LM358
1k
3V
$V_{IN}(-)$
V_{REF}
+
1 µF
LM336-2.5
SETS ZERO CODE VOLTAGE (2V)
330
2.7k
1k $2\ V_{DC}$ ZERO ADJ
TL/H/8557-13

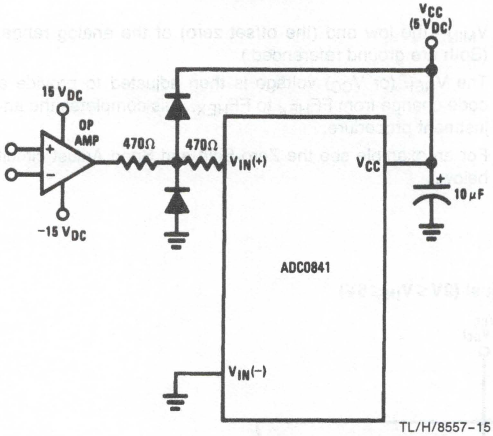
Applications Information (Continued)

Span Adjust $0V \le V_{IN} \le 3V$


VCC (5 VDC)
VIN(+)
VCC
VIN
+
10 µF
ADC0841
2k
10k FS ADJ
1/2 LM358
1k
VIN(−)
VREF
+
1 µF
SET FOR 3V
LM336-2.5

TL/H/8557-14

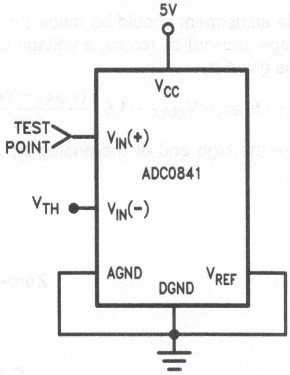
Protecting the Input


VCC (5 VDC)
15 VDC
OP AMP
470Ω
470Ω
VIN(+)
VCC
+
−
−15 VDC
10 µF
ADC0841
VIN(−)

TL/H/8557-15

Diodes are 1N914

High Accuracy Comparator

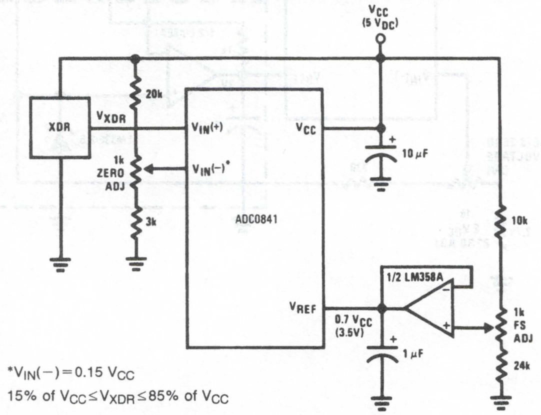

5V
VCC
TEST POINT
VIN(+)
ADC0841
VTH
VIN(−)
AGND
DGND
VREF

TL/H/8557-16

DO = all 1s if $V_{IN}(+) > V_{IN}(-)$

DO = all 0s if $V_{IN}(+) < V_{IN}(-)$

Operating with Automotive Ratiometric Transducers


VCC (5 VDC)
XDR
VXDR
20k
VIN(+)
VCC
1k ZERO ADJ
VIN(−)*
+
10 µF
3k
ADC0841
10k
1/2 LM358A
VREF
0.7 VCC (3.5V)
+
1 µF
1k FS ADJ
24k

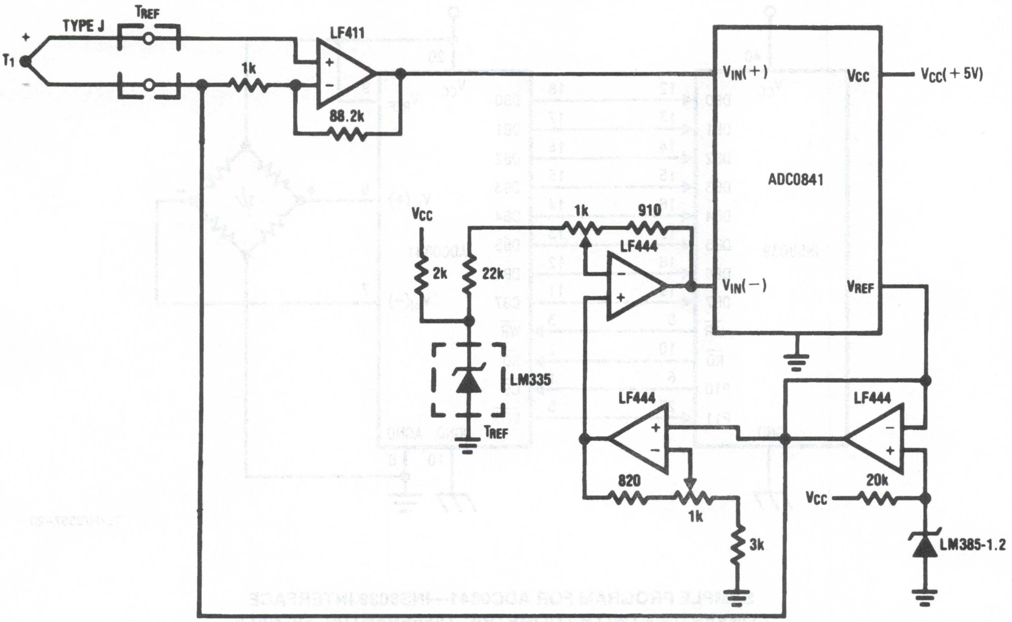
$^*V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \le V_{XDR} \le$ 85% of V_{CC}

TL/H/8557-17

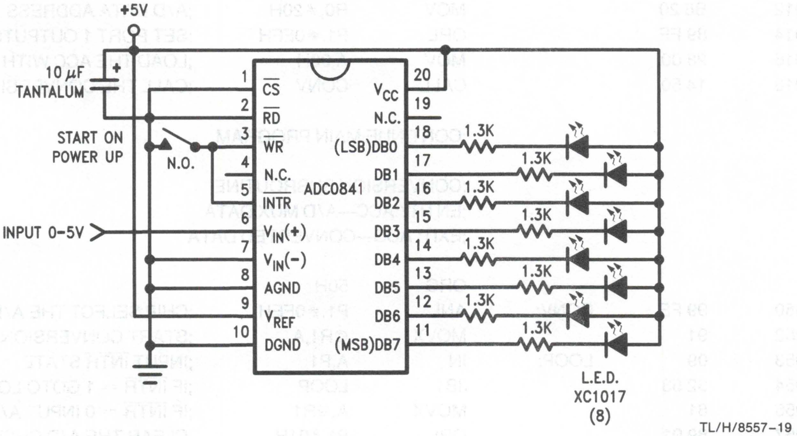
Applications Information (Continued)

Converting a Thermocouple with Cold-Junction Compensation


TYPE J
TREF
+
T1
−
1k
LF411
88.2k
VIN(+)
VCC
VCC(+5V)
ADC0841
VCC
1k
910
LF444
2k
22k
VIN(−)
VREF
LM335
TREF
LF444
LF444
820
1k
3k
20k
VCC
LM385-1.2

TL/H/8557–18

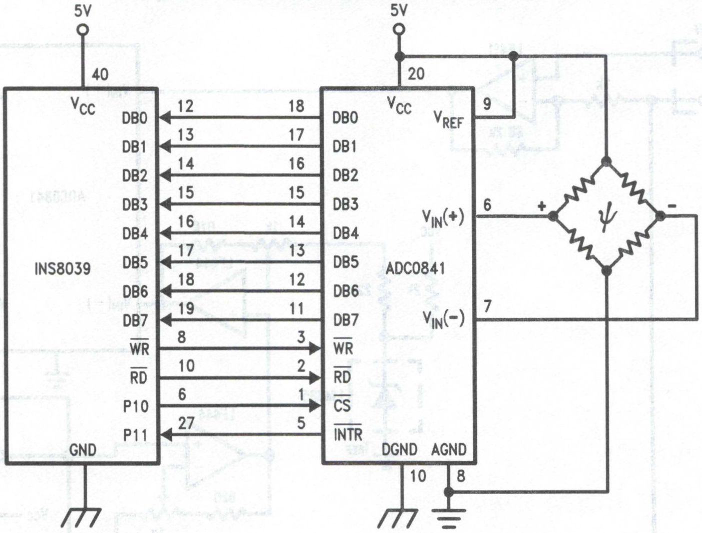
Continuous Conversion


+5V
10 μF
TANTALUM
START ON
POWER UP
N.O.
INPUT 0–5V
1
2
3
4
5
6
7
8
9
10
CS
RD
WR
N.C.
INTR
VIN(+)
VIN(−)
AGND
VREF
DGND
ADC0841
20
19
18
17
16
15
14
13
12
11
VCC
N.C.
(LSB)DB0
DB1
DB2
DB3
DB4
DB5
DB6
(MSB)DB7
1.3K
L.E.D.
XC1017
(8)

TL/H/8557–19

Applications Information (Continued)

ADC0841—INS8039 Interface


5V
5V
40
VCC
INS8039
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
WR
RD
P10
P11
GND
12
13
14
15
16
17
18
19
8
10
6
27
18
17
16
15
14
13
12
11
3
2
1
5
20
VCC
VREF
9
ADC0841
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
WR
RD
CS
INTR
VIN(+)
6
VIN(−)
7
DGND
AGND
10
8
+
−

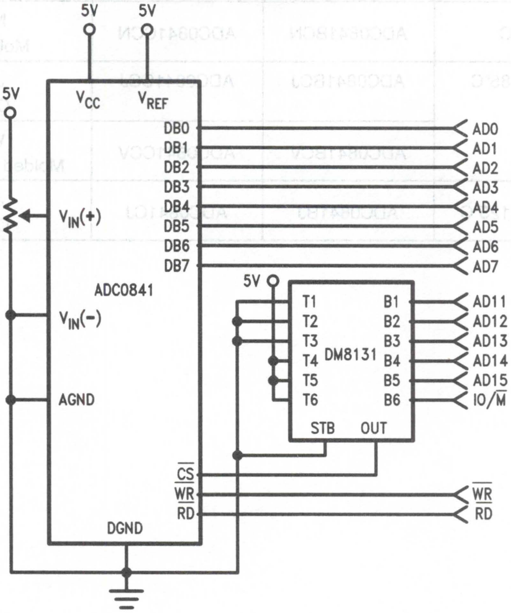
TL/H/8557-20

SAMPLE PROGRAM FOR ADC0841—INS8039 INTERFACE CONVERTING TWO RATIOMETRIC, DIFFERENTIAL SIGNALS

```
                                 ORG     0H
0000    04 10                    JMP     BEGIN        ;START PROGRAM AT ADDR 10
                                 ORG     10H          ;MAIN PROGRAM
0010    B9 FF      BEGIN:        MOV     R1,#0FFH     ;LOAD R1 WITH A UNUSED ADDR
                                                      ;LOCATION
0012    B8 20                    MOV     R0,#20H      ;A/D DATA ADDRESS
0014    89 FF                    ORL     P1,#0FFH     ;SET PORT 1 OUTPUTS HIGH
0016    23 00                    MOV     A,00H        ;LOAD THE ACC WITH 00
0018    14 50                    CALL    CONV         ;CALL THE CONVERSION SUBROUTINE

                                 ;CONTINUE MAIN PROGRAM

                                 ;CONVERSION SUBROUTINE
                                 ;ENTRY:ACC—A/D MUX DATA
                                 ;EXIT: ACC—CONVERTED DATA

                                 ORG     50H
0050    99 FE      CONV:         ANL     P1,#0FEH     ;CHIP SELECT THE A/D
0052    91                       MOVX    @R1,A        ;START CONVERSION
0053    09         LOOP:         IN      A,P1         ;INPUT INTR STATE
0054    32 53                    JB1     LOOP         ;IF INTR = 1 GOTO LOOP
0056    81                       MOVX    A,@R1        ;IF INTR = 0 INPUT A/D DATA
0057    89 01                    ORL     P1,&01H      ;CLEAR THE A/D CHIP SELECT
0059    A0                       MOV     @R0,A        ;STORE THE A/D DATA
005A    83                       RET                  ;RETURN TO MAIN PROGRAM
```

Applications Information (Continued)

I/O Interface to NSC800™


5V
5V
5V
VCC
VREF
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
VIN(+)
ADC0841
VIN(−)
AGND
5V
T1
T2
T3
T4
T5
T6
DM8131
B1
B2
B3
B4
B5
B6
STB
OUT
AD11
AD12
AD13
AD14
AD15
IO/M̄
C̄S̄
W̄R̄
RD
DGND
W̄R̄
RD

TL/H/8557–21

SAMPLE PROGRAM FOR ADC0841—NSC800 INTERFACE

```
0010            NCONV     EQU     16          ;TWICE THE NUMBER OF REQUIRED
                                              ;CONVERSIONS
000F            DEL       EQU     15          ;DELAY 60 µsec CONVERSION
001F            CS        EQU     1FH         ;THE BOARD ADDRESS
3C00            ADDTA     EQU     003CH       ;START OF RAM FOR A/D
                                              ;DATA
0000'   00      DTA:      DB      08H         ; DATA
0001'   0E 1F   START:    LD      C,CS
0003'   06 16             LD      B,NCONV
0005'   21 0000'          LD      HL,DTA
0008'   11 003C           LD      DE,ADDTA
000B'   ED A3   STCONV:   OUTI                ;START A CONVERSION
000D'   EB                EX      DE,HL       ;HL=RAM ADDRESS FOR THE
                                              ;A/D DATA
000E'   3E 0F             LD      A,DEL
0010'   3D      WAIT:     DEC     A           ;WAIT 60 µsec FOR THE
0011'   C2 0013'          JP      NZ,WAIT     ;CONVERSION TO FINISH
0014'   ED A2             INI                 ;STORE THE A/D'S DATA
                                              ;THE REQUIRED CONVERSIONS COMPLETED?
0016'   EB                EX      DE,HL
0017'   C2 000E'          JP      NZ,STCONV   ;IF NOT GOTO STCONV

                          END
```

Note: A conversion is started, then a 60 µs wait for the A/D to complete a conversion and the data is stored at address ADDTA for the first conversion, ADDTA + 1 for the second conversion, etc. for a total of 8 conversions.

Ordering Information

Temperature Range	Total Unadjusted Error		Package Outline
	±½ LSB	±1 LSB	
0°C to +70°C	ADC0841BCN	ADC0841CCN	N20A Molded Dip
−40°C to +85°C	ADC0841BCJ	ADC0841CCJ	J20A Cerdip
	ADC0841BCV	ADC0841CCV	V20A Molded Chip Carrier
−55°C to +125°C	ADC0841BJ	ADC0841CJ	J20A Cerdip

National Semiconductor Corporation

ADC0844/ADC0848 8-Bit μP Compatible A/D Converters with Multiplexer Options

General Description

The ADC0844 and ADC0848 are CMOS 8-bit successive approximation A/D converters with versatile analog input multiplexers. The 4-channel or 8-channel multiplexers can be software configured for single-ended, differential or pseudo-differential modes of operation.

The differential mode provides low frequency input common mode rejection and allows offsetting the analog range of the converter. In addition, the A/D's reference can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

The A/Ds are designed to operate from the control bus of a wide variety of microprocessors. TRI-STATE® output latches that directly drive the data bus permit the A/Ds to be configured as memory locations or I/O devices to the microprocessor with no interface logic necessary.

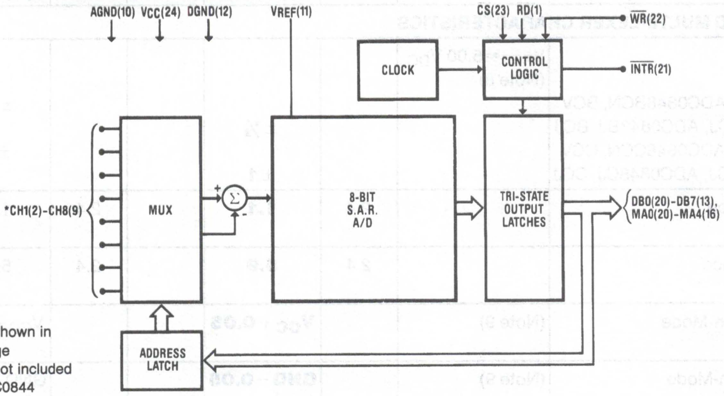
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 4-channel or 8-channel multiplexer with address logic
- Internal clock
- 0V to 5V input range with single 5V power supply
- 0.3″ standard width 20-pin or 24-pin DIP
- 28 Pin Molded Chip Carrier Package

Key Specifications

Resolution	8 Bits
Total Unadjusted Error	±½ LSB and ± 1 LSB
Single Supply	5 V_{DC}
Low Power	15 mW
Conversion Time	40 μs

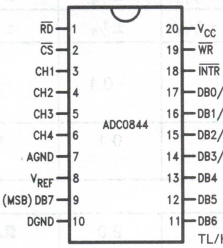
Block and Connection Diagrams


AGND(10)
VCC(24)
DGND(12)
VREF(11)
CS(23)
RD(1)
WR(22)
CLOCK
CONTROL LOGIC
INTR(21)
*CH1(2)-CH8(9)
MUX
+
−
Σ
8-BIT S.A.R. A/D
TRI-STATE OUTPUT LATCHES
DB0(20)-DB7(13), MA0(20)-MA4(16)
ADDRESS LATCH

*ADC0848 shown in DIP Package
CH5-CH8 not included on the ADC0844

TL/H/5016–1

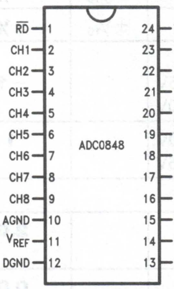
Dual-In-Line Package


RD 1
CS 2
CH1 3
CH2 4
CH3 5
CH4 6
AGND 7
VREF 8
(MSB) DB7 9
DGND 10
20 VCC
19 WR
18 INTR
17 DB0/MA0
16 DB1/MA1
15 DB2/MA2
14 DB3/MA3
13 DB4
12 DB5
11 DB6
ADC0844

TL/H/5016–2

Top View

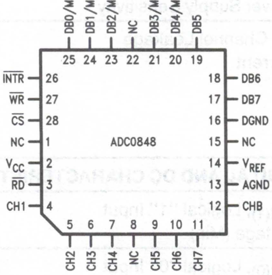
Dual-In-Line Package


RD 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
CH8 9
AGND 10
VREF 11
DGND 12
24 VCC
23 CS
22 WR
21 INTR
20 DB0/MA0
19 DB1/MA1
18 DB2/MA2
17 DB3/MA3
16 DB4/MA4
15 DB5
14 DB6
13 DB7
ADC0848

TL/H/5016–30

Top View

Molded Chip Carrier Package


DB0/MAO
DB1/MA1
DB2/MA2
NC
DB3/MA3
DB4/MA4
DB5
25 24 23 22 21 20 19
INTR 26
WR 27
CS 28
NC 1
VCC 2
RD 3
CH1 4
18 DB6
17 DB7
16 DGND
15 NC
14 VREF
13 AGND
12 CHB
5 6 7 8 9 10 11
CH2
CH3
CH4
NC
CH5
CH6
CH7
ADC0848

TL/H/5016–29

Top View

See Ordering Information

3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage	
Logic Control Inputs	−0.3V to +15V
At Other Inputs and Outputs	−0.3V to V_{CC}+0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 4)	800V
Lead Temperature (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Conditions (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0844BCN, ADC0844CCN, ADC0848BCN, ADC0848CCN	0°C≤T_A≤70°C
ADC0844BCJ, ADC0844CCJ, ADC0848BCJ, ADC0848CCJ ADC0848BCV, ADC0848CCV	−40°C≤T_A≤85°C
ADC0844BJ, ADC0844CJ, ADC0848BJ, ADC0848CJ	−55°C≤T_A≤125°C

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits T_A = T_j = 25°C.

Parameter	Conditions	ADC0844BJ, ADC0844BCJ ADC0844CJ, ADC0844CCJ ADC0848BJ, ADC0848BCJ ADC0848CJ, ADC0848CCJ			ADC0844BCN, ADC0844CCN ADC0848BCN, ADC0848CCN ADC0848BCV, ADC0848CCV			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Maximum Total Unadjusted Error	V_{REF}=5.00 V_{DC} (Note 8)							
ADC0844BCN, ADC0848BCN, BCV						±½	**±½**	LSB
ADC0844BJ, BCJ, ADC0848BJ, BCJ			**±½**					LSB
ADC0844CCN, ADC0848CCN, CCV						±1	**±1**	LSB
ADC0844CJ, CCJ, ADC0848CJ, CCJ			**±1**					LSB
Minimum Reference Input Resistance		2.4	**1.1**		2.4	1.2	**1.1**	kΩ
Maximum Reference Input Resistance		2.4	**5.9**		2.4	5.4	**5.9**	kΩ
Maximum Common-Mode Input Voltage	(Note 9)		**V_{CC}+0.05**			V_{CC}+0.05	**V_{CC}+0.05**	V
Minimum Common-Mode Input Voltage	(Note 9)		**GND−0.05**			GND−0.05	**GND−0.05**	V
DC Common-Mode Error	Differential Mode	±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
Power Supply Sensitivity	V_{CC}=5V±5%	±1/16	**±⅛**		±1/16	±⅛	**±⅛**	LSB
Off Channel Leakage Current	(Note 10) On Channel=5V, Off Channel=0V		**−1**			−0.1	**−1**	μA
	On Channel=0V, Off Channel=5V		**1**			0.1	**1**	μA
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC}=5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC}=4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN}=5.0V	0.005	**1**		0.005		**1**	μA

Electrical Characteristics

The following specifications apply for $V_{CC} = 5\ V_{DC}$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j = 25°C$. (Continued)

Parameter	Conditions	ADC0844BJ, ADC0844BCJ ADC0844CJ, ADC0844CCJ ADC0848BJ, ADC0848BCJ ADC0848CJ, ADC0848CCJ			ADC0844BCN, ADC0844CCN ADC0848BCN, ADC0848CCN ADC0848BCV, ADC0848CCV			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
DIGITAL AND DC CHARACTERISTICS (Continued)								
$I_{IN(0)}$, Logical "0" Input Current (Max)	$V_{IN} = 0V$	−0.005	**−1**		−0.005		**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	$V_{CC} = 4.75V$ $I_{OUT} = -360\ \mu A$		**2.4**			2.8	**2.4**	V
	$I_{OUT} = -10\ \mu A$		**4.5**			4.6	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	$V_{CC} = 4.75V$ $I_{OUT} = 1.6\ mA$		**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	$V_{OUT} = 0V$	−0.01	**−3**		−0.01	−0.3	**−3**	μA
	$V_{OUT} = 5V$	0.01	**3**		0..01	0.3	**3**	μA
I_{SOURCE}, Output Source Current (Min)	$V_{OUT} = 0V$	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SNK}, Output Sink Current (Min)	$V_{OUT} = V_{CC}$	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max)	$\overline{CS} = 1$, V_{REF} Open	1	**2.5**		1	2.3	**2.5**	mA

AC Electrical Characteristics

The following specifications apply for $V_{CC} = 5V_{DC}$, $t_r = t_f = 10$ ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Units
t_C, Maximum Conversion Time (See Graph)		30	40	**60**	μs
$t_{W(\overline{WR})}$, Minimum $\overline{WR}$ Pulse Width	(Note 11)	50	150		ns
t_{ACC}, Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF (Note 11)	145		225	ns
t_{1H}, t_{0H}, TRI-STATE Control (Maximum Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$C_L = 10$ pF, $R_L = 10k$ (Note 11)	125		200	ns
t_{WI}, t_{RI}, Maximum Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$	(Note 11)	200	400		ns
t_{DS}, Minimum Data Set-Up Time	(Note 11)	50	100		ns
t_{DH}, Minimum Data Hold Time	(Note 11)	0	50		ns
C_{IN}, Capacitance of Logic Inputs		5			pF
C_{OUT}, Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground pins.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Design limits are guaranteed by not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 8: Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.

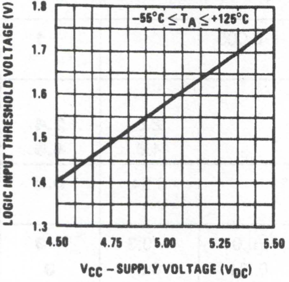
Note 9: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 10: Off channel leakage current is measured after the channel selection.

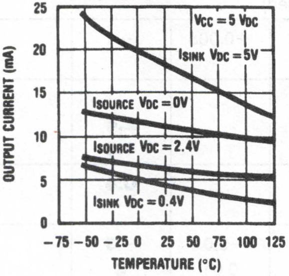
Note 11: The temperature coefficient is 0.3%/°C.

Typical Performance Characteristics

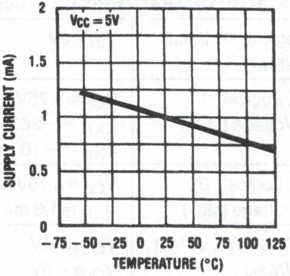
Logic Input Threshold Voltage vs Supply Voltage



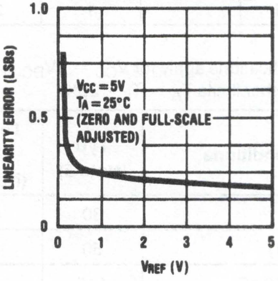
Output Current vs Temperature



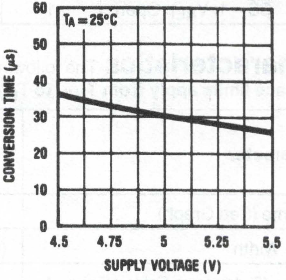
Power Supply Current vs Temperature



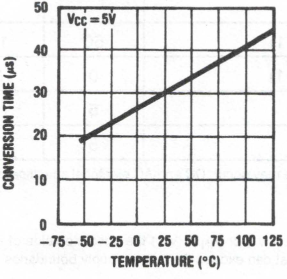
Linearity Error vs V_{REF}



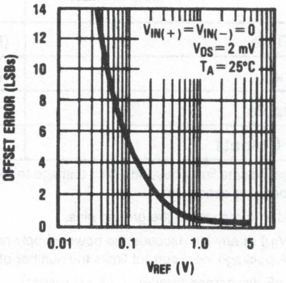
Conversion Time vs V_{SUPPLY}



Conversion Time vs Temperature



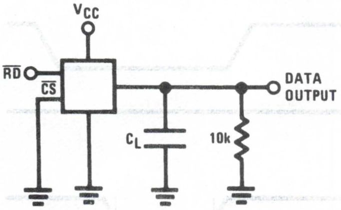
Unadjusted Offset Error vs V_{REF} Voltage



TL/H/5016-3

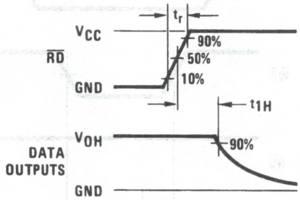
TRI-STATE Test Circuits and Waveforms

t_{1H}


VCC
RD
CS
DATA OUTPUT
CL
10k

TL/H/5016-4

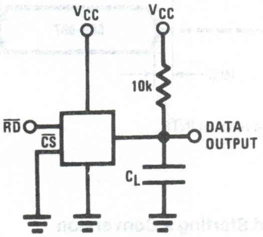
t_{1H}, $C_L = 10$ pF


tr
VCC
RD
GND
90%
50%
10%
t1H
VOH
DATA OUTPUTS
90%
GND

TL/H/5016-5

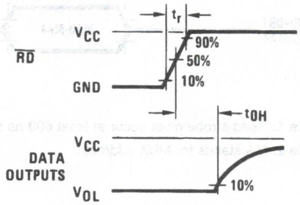
$t_r = 20$ ns

t_{OH}


VCC
VCC
10k
RD
CS
DATA OUTPUT
CL

TL/H/5016-6

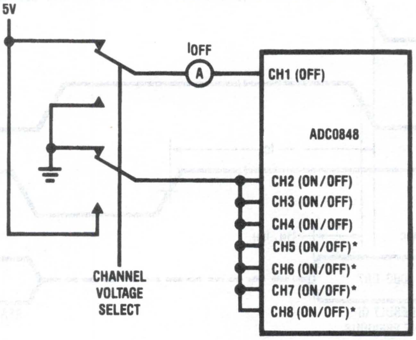
t_{OH}, $C_L = 10$ pF


tr
VCC
RD
GND
90%
50%
10%
tOH
VCC
DATA OUTPUTS
VOL
10%

TL/H/5016-7

$t_r = 20$ ns

Leakage Current Test Circuit

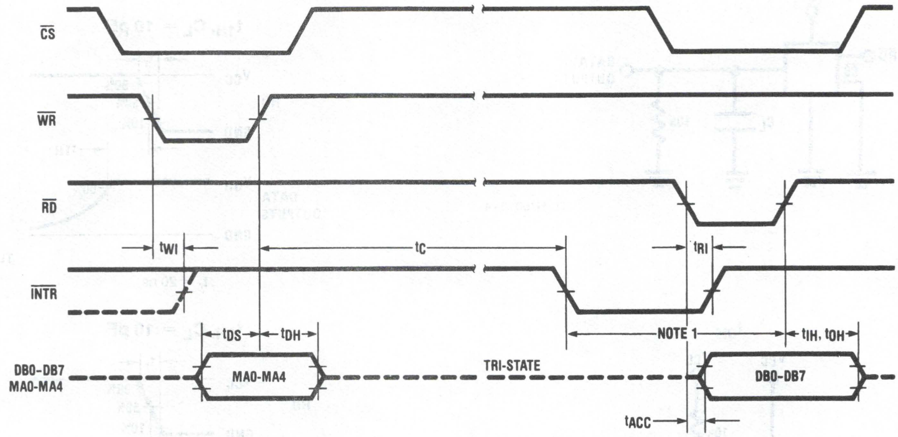

5V
IOFF
A
CH1 (OFF)
ADC0848
CH2 (ON/OFF)
CH3 (ON/OFF)
CH4 (ON/OFF)
CH5 (ON/OFF)*
CH6 (ON/OFF)*
CH7 (ON/OFF)*
CH8 (ON/OFF)*
CHANNEL VOLTAGE SELECT

*NOT INCLUDED ON ADC0844

TL/H/5016-8

Timing Diagrams

Programming New Channel Configuration and Starting a Conversion

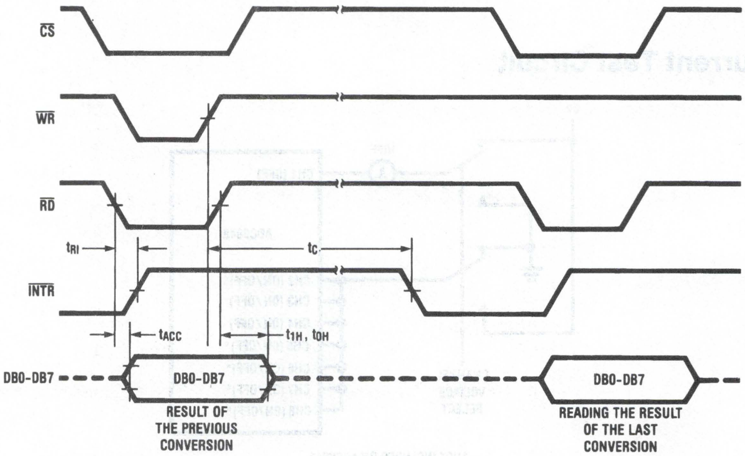

CS
WR
RD
INTR
DB0-DB7
MA0-MA4
tWI
tC
tRI
tDS
tDH
NOTE 1
tIH, tOH
MA0-MA4
TRI-STATE
DB0-DB7
tACC

TL/H/5016-9

Note 1: Read strobe must occur at least 600 ns after the assertion of interrupt to guarantee reset of $\overline{\text{INTR}}$.

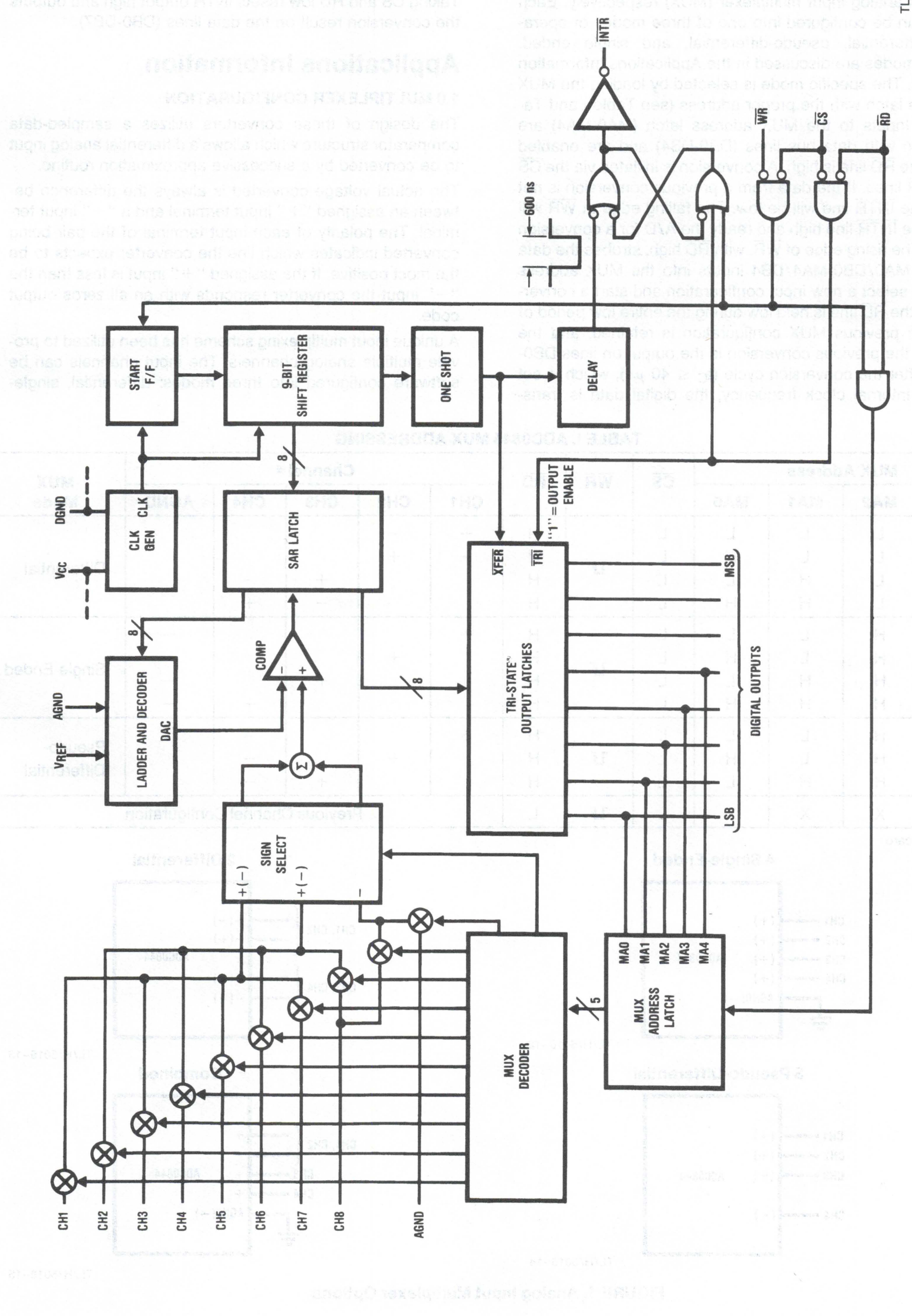
Note 2: MA stands for MUX address.

Using the Previously Selected Channel Configuration and Starting a Conversion


CS
WR
RD
tRI
tC
INTR
tACC
t1H, tOH
DB0-DB7
DB0-DB7
RESULT OF THE PREVIOUS CONVERSION
DB0-DB7
READING THE RESULT OF THE LAST CONVERSION

TL/H/5016-10

ADC0848 Functional Block Diagram


CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
AGND
MUX DECODER
5
MUX ADDRESS LATCH
MA0
MA1
MA2
MA3
MA4
+(−)
SIGN SELECT
+(−)
−
Σ
COMP
−
+
VREF
AGND
LADDER AND DECODER
DAC
8
VCC
DGND
CLK GEN
CLK
SAR LATCH
8
START F/F
9-BIT SHIFT REGISTER
8
ONE SHOT
DELAY
TRI-STATE® OUTPUT LATCHES
XFER
TRI
"1" = OUTPUT ENABLE
LSB
MSB
DIGITAL OUTPUTS
600 ns
INTR
WR
CS
RD

TL/H/5016-11

Functional Description

The ADC0844 and ADC0848 contain a 4-channel and 8-channel analog input multiplexer (MUX) respectively. Each MUX can be configured into one of three modes of operation differential, pseudo-differential, and single ended. These modes are discussed in the Applications Information Section. The specific mode is selected by loading the MUX address latch with the proper address (see Table I and Table II). Inputs to the MUX address latch (MA0-MA4) are common with data bus lines (DB0-DB4) and are enabled when the $\overline{RD}$ line is high. A conversion is initiated via the $\overline{CS}$ and $\overline{WR}$ lines. If the data from a previous conversion is not read, the $\overline{INTR}$ line will be low. The falling edge of $\overline{WR}$ will reset the $\overline{INTR}$ line high and ready the A/D for a conversion cycle. The rising edge of $\overline{WR}$, with $\overline{RD}$ high, strobes the data on the MA0/DB0-MA4/DB4 inputs into the MUX address latch to select a new input configuration and start a conversion. If the $\overline{RD}$ line is held low during the entire low period of $\overline{WR}$ the previous MUX configuration is retained, and the data of the previous conversion is the output on lines DB0-DB7. After the conversion cycle ($t_C \leq 40\ \mu s$), which is set by the internal clock frequency, the digital data is transferred to the output latch and the $\overline{INTR}$ is asserted low. Taking $\overline{CS}$ and $\overline{RD}$ low resets $\overline{INTR}$ output high and outputs the conversion result on the data lines (DB0-DB7).

Applications Information

1.0 MULTIPLEXER CONFIGURATION

The design of these converters utilizes a sampled-data comparator structure which allows a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

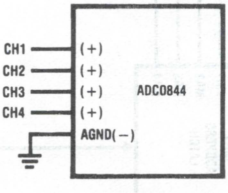
A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single-

TABLE I. ADC0844 MUX ADDRESSING

MUX Address				$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel #					MUX Mode
MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	AGND	
X	L	L	L	L		H	+	−				Differential
X	L	L	H	L	⊔	H	−	+				
X	L	H	L	L		H			+	−		
X	L	H	H	L		H			−	+		
L	H	L	L	L		H	+				−	Single-Ended
L	H	L	H	L	⊔	H		+			−	
L	H	H	L	L		H			+		−	
L	H	H	H	L		H				+	−	
H	H	L	L	L		H	+			−		Pseudo-Differential
H	H	L	H	L	⊔	H		+		−		
H	H	H	L	L		H			+	−		
X	X	X	X	L	⊔	L	Previous Channel Configuration					

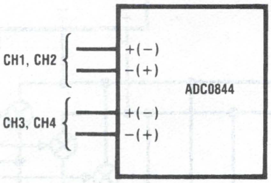
X = don't care

4 Single-Ended



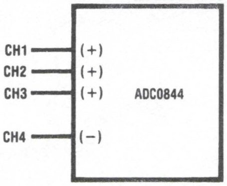
TL/H/5016-12

2 Differential



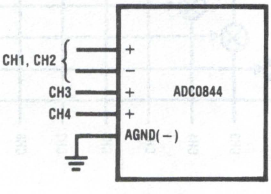
TL/H/5016-13

3 Pseudo-Differential



TL/H/5016-14

Combined



TL/H/5016-15

FIGURE 1. Analog Input Multiplexer Options

Applications Information (Continued)

ended, or pseudo-differential. *Figure 1* shows the three modes using the 4-channel MUX ADC0844. The eight inputs of the ADC0848 can also be configured in any of the three modes. In the differential mode, the ADC0844 channel inputs are grouped in pairs, CH1 with CH2 and CH3 with CH4. The polarity assignment of each channel in the pair is interchangeable. The single-ended mode has CH1–CH4 assigned as the positive input with the negative input being the analog ground (AGND) of the device. Finally, in the pseudo-differential mode CH1–CH3 are positive inputs referenced to CH4 which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input of these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the minimum reference input resistance of 1.1 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 2a*), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 2b*), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).

3.0 THE ANALOG INPUTS

3.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the

TABLE II. ADC0848 MUX Addressing

MUX Address					$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel									MUX Mode
MA4	MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	AGND	
X	L	L	L	L	L	⊔	H	+	−								Differential
X	L	L	L	H	L		H	−	+								
X	L	L	H	L	L		H			+	−						
X	L	L	H	H	L		H			−	+						
X	L	H	L	L	L		H					+	−				
X	L	H	L	H	L		H					−	+				
X	L	H	H	L	L		H							+	−		
X	L	H	H	H	L		H							−	+		
L	H	L	L	L	L	⊔	H	+								−	Single-Ended
L	H	L	L	H	L		H		+							−	
L	H	L	H	L	L		H			+						−	
L	H	L	H	H	L		H				+					−	
L	H	H	L	L	L		H					+				−	
L	H	H	L	H	L		H						+			−	
L	H	H	H	L	L		H							+		−	
L	H	H	H	H	L		H								+	−	
H	H	L	L	L	L	⊔	H	+							−		Pseudo-Differential
H	H	L	L	H	L		H		+						−		
H	H	L	H	L	L		H			+					−		
H	H	L	H	H	L		H				+				−		
H	H	H	L	L	L		H					+			−		
H	H	H	L	H	L		H						+		−		
H	H	H	H	L	L		H							+	−		
X	X	X	X	X	L	⊔	L	Previous Channel Configuration									

Applications Information (Continued)

"+" input and then the "−" inputs is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{ERROR(MAX)} = V_{peak} (2\pi f_{CM}) \times 0.5 \times \left(\frac{t_C}{8}\right)$$

where f_{CM} is the frequency of the common-mode signal, V_{peak} is its peak voltage value and t_C is the conversion time.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 40 μS, its peak value would have to be 5.43V. This large a common-mode signal is much greater than that generally found in a well designed data acquisition system.

3.2 Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

3.3 Input Source Resistance

The limitation of the input source resistance due to the DC leakage currents of the input multiplexer is important. A worst-case leakage current of ± 1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

4.0 OPTIONAL ADJUSTMENTS

4.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This is useful for either differential or pseudo-differential modes of input channel configuration.

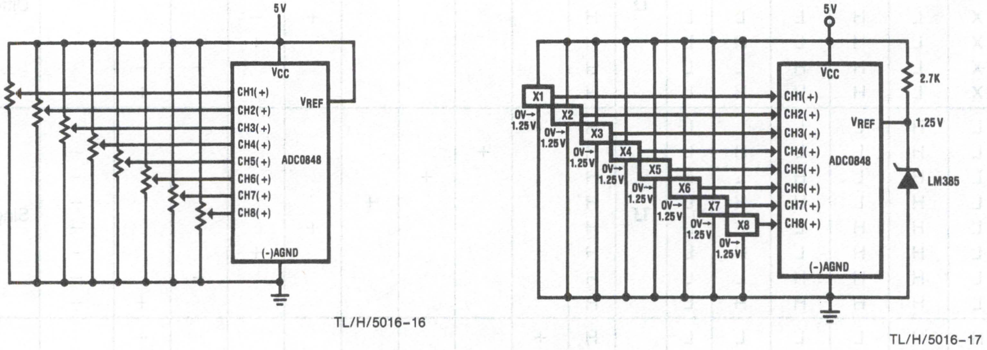
The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V^- input and applying a small magnitude positive voltage to the V^+ input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF} = 5.000\ V_{DC}$).

4.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code changing from 1111 1110 to 1111 1111.

4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.



a) Ratiometric

b) Absolute with a Reduced Span

FIGURE 2. Referencing Examples

Applications Information (Continued)

The full-scale adjustment should be made [with the proper V_{IN} (−) voltage applied] by forcing a voltage to the V_{IN} (+) input which is given by:

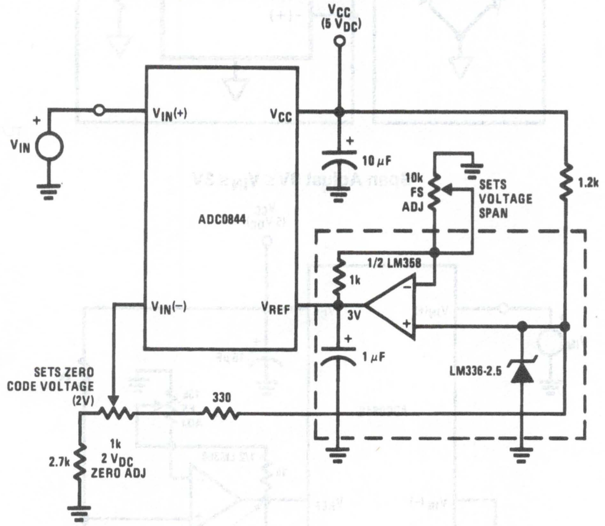
$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX}-V_{MIN})}{256}\right]$$

where V_{MAX} = the high end of the analog input range and V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

For an example see the Zero-Shift and Span Adjust circuit below.

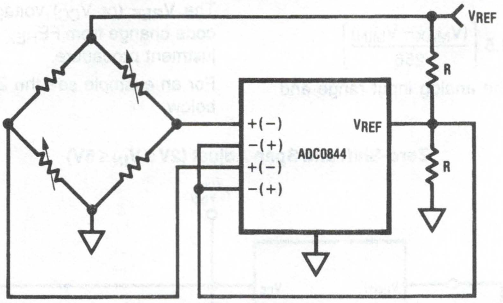
Zero-Shift and Span Adjust (2V ≤ V_{IN} ≤ 5V)


VCC (5 VDC)
VIN(+)
VCC
+
VIN
+
10 µF
10k FS ADJ
SETS VOLTAGE SPAN
1.2k
ADC0844
1/2 LM358
1k
VIN(−)
VREF
3V
+
1 µF
LM336-2.5
SETS ZERO CODE VOLTAGE (2V)
330
1k 2 VDC ZERO ADJ
2.7k

TL/H/5016-18

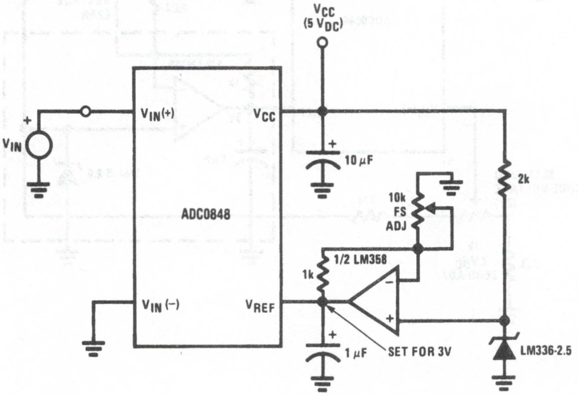
Applications Information (Continued)

Differential Voltage Input 9-Bit A/D


VREF
R
+(−)
−(+)
+(−)
−(+)
ADC0844
VREF
R

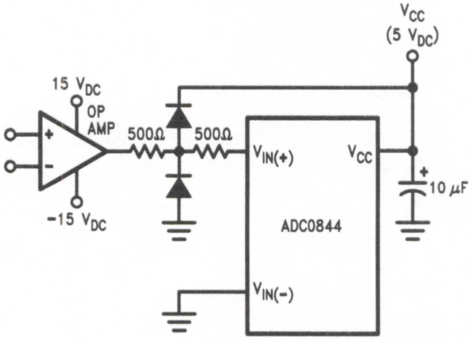
TL/H/5016-19

Span Adjust 0V ≤ V_{IN} ≤ 3V


VCC
(5 VDC)
VIN(+)
VCC
+
VIN
+
10 µF
2k
10k
FS
ADJ
ADC0848
1/2 LM358
1k
−
+
VIN(−)
VREF
+
1 µF
SET FOR 3V
LM336-2.5

TL/H/5016-20

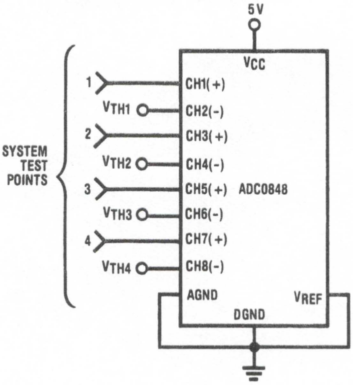
Protecting the Input


VCC
(5 VDC)
15 VDC
OP
AMP
+
−
500Ω
500Ω
VIN(+)
VCC
+
10 µF
ADC0844
−15 VDC
VIN(−)

TL/H/5016-21

Diodes are 1N914

High Accuracy Comparators


5 V
VCC
1
CH1(+)
VTH1
CH2(-)
2
CH3(+)
SYSTEM
TEST
POINTS
VTH2
CH4(-)
3
CH5(+)
ADC0848
VTH3
CH6(-)
4
CH7(+)
VTH4
CH8(-)
AGND
VREF
DGND

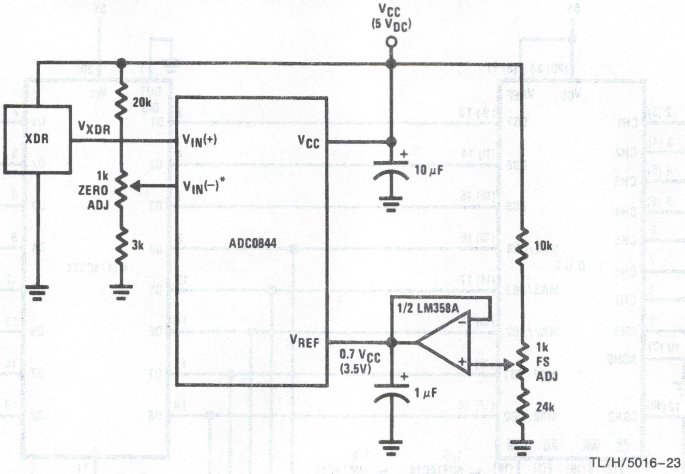
TL/H/5016-22

DO = all 1s if $V_{IN}(+) > V_{IN}(-)$

DO = all 0s if $V_{IN}(+) < V_{IN}(-)$

Applications Information (Continued)

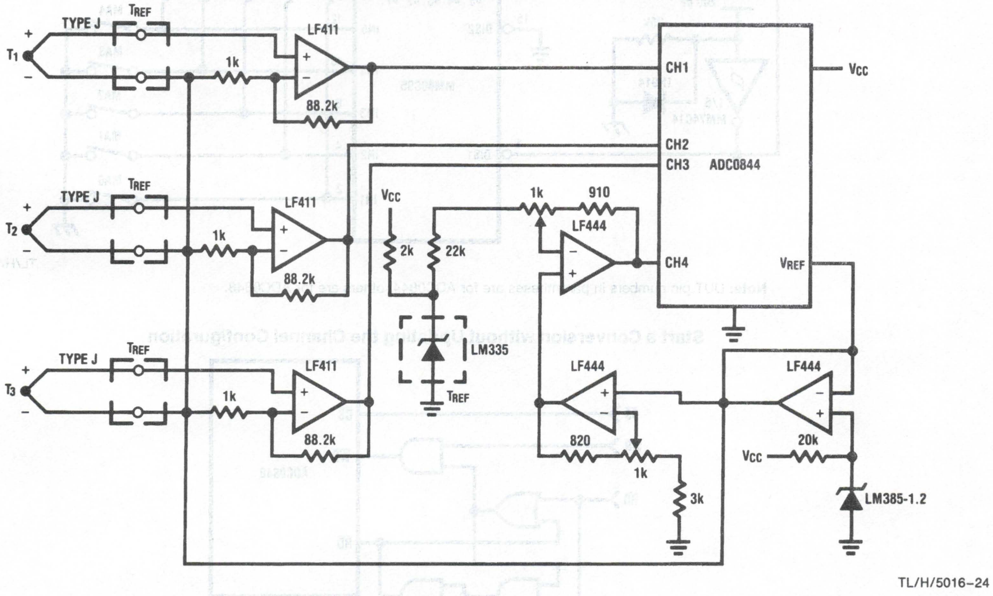
Operating with Automotive Ratiometric Transducers


V_CC (5 V_DC)
20k
XDR
V_XDR
V_IN(+)
V_CC
10 µF
1k ZERO ADJ
V_IN(−)*
3k
ADC0844
10k
1/2 LM358A
V_REF
0.7 V_CC (3.5V)
1 µF
1k FS ADJ
24k
TL/H/5016-23

$^*V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

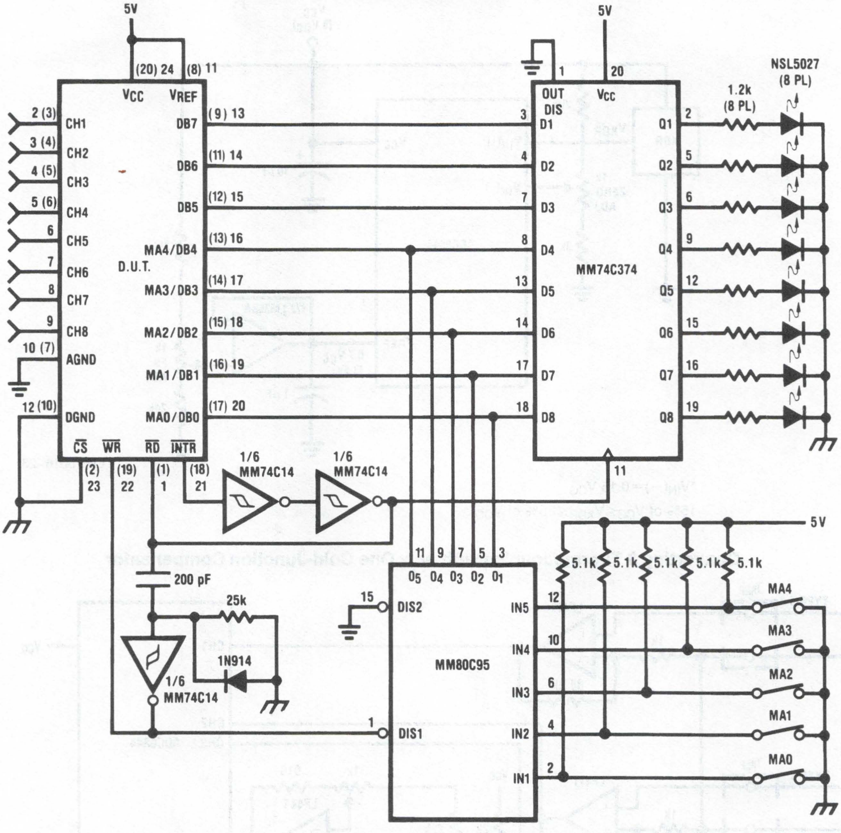
Converting 3 Thermocouples with only One Cold-Junction Compensator


TYPE J
T_REF
+
T1
−
1k
LF411
88.2k
CH1
V_CC
CH2
CH3
ADC0844
TYPE J
T_REF
T2
LF411
1k
88.2k
V_CC
2k
22k
1k
910
LF444
CH4
V_REF
LM335
T_REF
TYPE J
T_REF
T3
LF411
1k
88.2k
LF444
820
1k
3k
LF444
V_CC
20k
LM385-1.2
TL/H/5016-24

Uses the pseudo-differential mode to keep the differential inputs constant with changes in reference temperature (T_{REF}).

Applications Information (Continued)

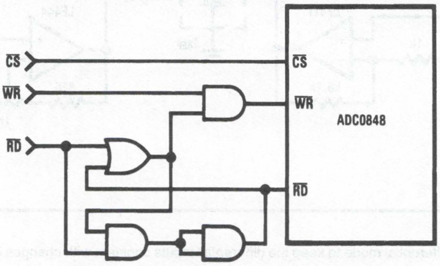
A Stand Alone Circuit


5V
(20) 24
(8) 11
VCC
VREF
2 (3) CH1
3 (4) CH2
4 (5) CH3
5 (6) CH4
6 CH5
7 CH6
8 CH7
9 CH8
10 (7) AGND
12 (10) DGND
D.U.T.
DB7 (9) 13
DB6 (11) 14
DB5 (12) 15
MA4/DB4 (13) 16
MA3/DB3 (14) 17
MA2/DB2 (15) 18
MA1/DB1 (16) 19
MA0/DB0 (17) 20
CS (2) 23
WR (19) 22
RD (1) 1
INTR (18) 21
1/6 MM74C14
1/6 MM74C14
200 pF
25k
1N914
1/6 MM74C14
5V
1 OUT DIS
20 VCC
3 D1
4 D2
7 D3
8 D4
13 D5
14 D6
17 D7
18 D8
MM74C374
Q1 2
Q2 5
Q3 6
Q4 9
Q5 12
Q6 15
Q7 16
Q8 19
11
1.2k (8 PL)
NSL5027 (8 PL)
5V
5.1k
5.1k
5.1k
5.1k
5.1k
11 9 7 5 3
O5 O4 O3 O2 O1
15 DIS2
1 DIS1
MM80C95
IN5 12
IN4 10
IN3 6
IN2 4
IN1 2
MA4
MA3
MA2
MA1
MA0

TL/H/5016-25

Note: DUT pin numbers in parentheses are for ADC0844, others are for ADC0848.

Start a Conversion without Updating the Channel Configuration


CS
WR
RD
CS
WR
RD
ADC0848

TL/H/5016-26

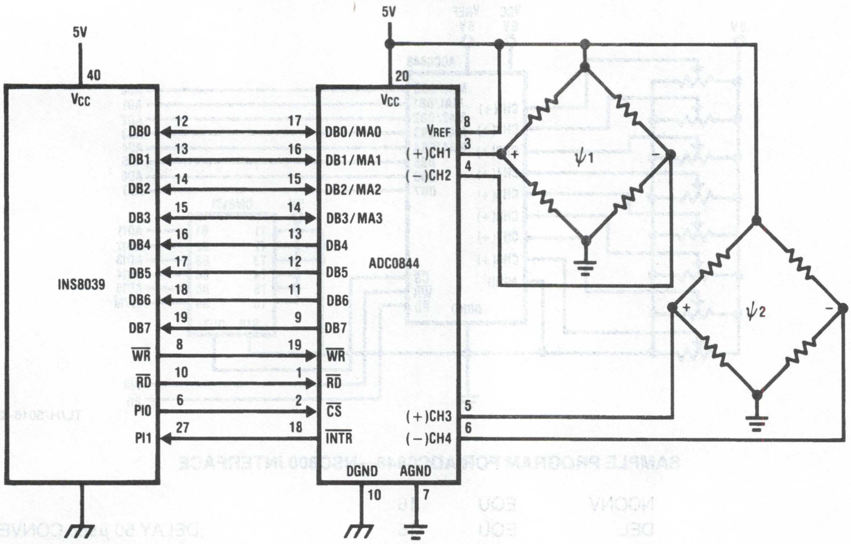
$\overline{\text{CS}}\bullet\overline{\text{WR}}$ will update the channel configuration and start a conversion.

$\overline{\text{CS}}\bullet\overline{\text{RD}}$ will read the conversion data and start a new conversion without updating the channel configuration.

Waiting for the end of this conversion is not necessary. A $\overline{\text{CS}}\bullet\overline{\text{WR}}$ can immediately follow the $\overline{\text{CS}}\bullet\overline{\text{RD}}$.

Applications Information (Continued)

ADC0844—INS8039 Interface


5V
40
Vcc
INS8039
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
WR
RD
PI0
PI1
12
13
14
15
16
17
18
19
8
10
6
27
17
16
15
14
13
12
11
9
19
1
2
18
5V
20
Vcc
ADC0844
DB0/MA0
DB1/MA1
DB2/MA2
DB3/MA3
DB4
DB5
DB6
DB7
WR
RD
CS
INTR
VREF
(+)CH1
(−)CH2
(+)CH3
(−)CH4
8
3
4
5
6
DGND
AGND
10
7
+
−
ψ1
ψ2

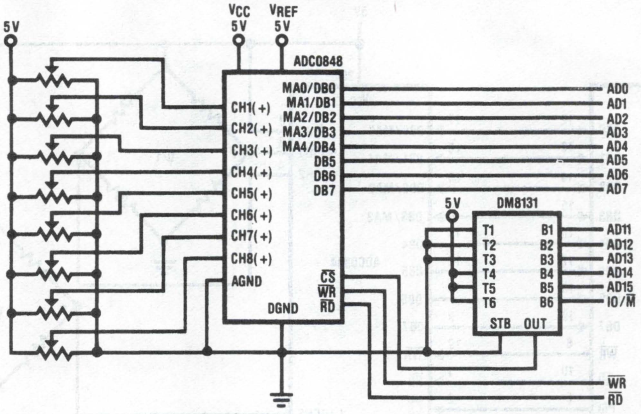
TL/H/5016-27

SAMPLE PROGRAM FOR ADC0844—INS8039 INTERFACE CONVERTING TWO RATIOMETRIC, DIFFERENTIAL SIGNALS

```
                                ORG     0H
0000        04 10               JMP     BEGIN       ;START PROGRAM AT ADDR 10
                                ORG     10H         ;MAIN PROGRAM
0010        B9 FF     BEGIN:    MOV     R1,#0FFH    ;LOAD R1 WITH A UNUSED ADDR
                                                    ;LOCATION
0012        B8 20               MOV     R0,#20H     ;A/D DATA ADDRESS
0014        89 FF               ORL     P1,#0FFH    ;SET PORT 1 OUTPUTS HIGH
0016        23 00               MOV     A,00H       ;LOAD THE ACC WITH A/D MUX DATA
                                                    ;CH1 AND CH2 DIFFERENTIAL
0018        14 50               CALL    CONV        ;CALL THE CONVERSION SUBROUTINE
001A        23 02               MOV     A,#02H      ;LOAD THE ACC WITH A/D MUX DATA
                                                    ;CH3 AND CH4 DIFFERENTIAL
001C        18                  INC     R0          ;INCREMENT THE A/D DATA ADDRESS
001D        14 50               CALL    CONV        ;CALL THE CONVERSION SUBROUTINE

                                ;CONTINUE MAIN PROGRAM

                                ;CONVERSION SUBROUTINE
                                ;ENTRY:ACC—A/D MUX DATA
                                ;EXIT: ACC—CONVERTED DATA

                                ORG     50H
0050        99 FE     CONV:     ANL     P1,#0FEH    ;CHIP SELECT THE A/D
0052        91                  MOVX    @R1,A       ;LOAD A/D MUX & START CONVERSION
0053        09        LOOP:     IN      A,P1        ;INPUT INTR STATE
0054        32 53               JB1     LOOP        ;IF INTR = 1 GOTO LOOP
0056        81                  MOVX    A,@R1       ;IF INTR = 0 INPUT A/D DATA
0057        89 01               ORL     P1,&01H     ;CLEAR THE A/D CHIP SELECT
0059        A0                  MOV     @R0,A       ;STORE THE A/D DATA
005A        83                  RET                 ;RETURN TO MAIN PROGRAM
```

Applications Information (Continued)

I/O Interface to NSC800



VCC 5V
VREF 5V
5V
ADC0848
CH1(+)
CH2(+)
CH3(+)
CH4(+)
CH5(+)
CH6(+)
CH7(+)
CH8(+)
AGND
DGND
MA0/DB0
MA1/DB1
MA2/DB2
MA3/DB3
MA4/DB4
DB5
DB6
DB7
CS
WR
RD
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
5V
DM8131
T1
T2
T3
T4
T5
T6
B1
B2
B3
B4
B5
B6
STB
OUT
AD11
AD12
AD13
AD14
AD15
IO/M
WR
RD

TL/H/5016–28

SAMPLE PROGRAM FOR ADC0848—NSC800 INTERFACE

```
0008                     NCONV      EQU     16
000F                     DEL        EQU     15            ;DELAY 50 µsec CONVERSION
001F                     CS         EQU     1FH           ;THE BOARD ADDRESS
3C00                     ADDTA      EQU     003CH         ;START OF RAM FOR A/D
                                                          ;DATA
0000'     08 09 0A 0B    MUXDTA:    DB      08H,09H,0AH,0BH ;MUX DATA
0004'     0C 0D 0E 0F               DB      0CH,0DH,0EH,0FH
0008'     0E 1F          START:     LD      C,CS
000A'     06 16                     LD      B,NCONV
000C'     21 0000'                  LD      HL,MUXDTA
000F'     11 003C                   LD      DE,ADDTA
0012'     ED A3          STCONV:    OUTI                  ;LOAD A/D'S MUX DATA
                                                          ;AND START A CONVERSION
0014'     EB                        EX      DE,HL         ;HL=RAM ADDRESS FOR THE
                                                          ;A/D DATA
0015'     3E 0F                     LD      A,DEL
0017'     3D             WAIT:      DEC     A             ;WAIT 50 µsec FOR THE
0018'     C2 0013'                  JP      NZ,WAIT       ;CONVERSION TO FINISH
001B'     ED A2                     INI                   ;STORE THE A/D'S DATA
                                                          ;CONVERTED ALL INPUTS?
001D'     EB                        EX      DE,HL
001E'     C2 000E'                  JP      NZ,STCONV     ;IF NOT GOTO STCONV

                                    END
```

Note: This routine sequentially programs the MUX data latch in the signal-ended mode. For CH1-CH8 a conversion is started, then a 50 µs wait for the A/D to complete a conversion and the data is stored at address ADDTA for CH1, ADDTA + 1 for CH2, etc.

Ordering Information

Temperature Range	Total Unadjusted Error		MUX Channels	Package Outline
	±½ LSB	±1 LSB		
0°C to +70°C	ADC0844BCN	ADC0844CCN	4	N20A Molded Dip
	ADC0848BCN	ADC0848CCN	8	N24C Molded Dip
−40°C to +85°C	ADC0844BCJ	ADC0844CCJ	4	J20A Cerdip
	ADC0848BCJ	ADC0848CCJ	8	J24F Cerdip
	ADC0848BCV	ADC0848CCV	8	V28A Molded Chip Carrier
−55°C to +125°C	ADC0844BJ	ADC0844CJ	4	J20A Cerdip
	ADC0848BJ	ADC0848CJ	8	J24F Cerdip

National Semiconductor Corporation

ADC0852/ADC0854
Multiplexed Comparator with 8-Bit Reference Divider

General Description

The ADC0852 and ADC0854 are CMOS devices that combine a versatile analog input multiplexer, voltage comparator, and an 8-bit DAC which provides the comparator's threshold voltage (V_{TH}). The comparator provides a "1-bit" output as a result of a comparison between the analog input and the DAC's output. This allows for easy implementation of set-point, on-off or "bang-bang" control systems with several advantages over previous devices.

The ADC0854 has a 4 input multiplexer that can be software configured for single ended, pseudo-differential, and full-differential modes of operation. In addition the DAC's reference input is brought out to allow for reduction of the span.

The ADC0852 has a two input multiplexer that can be configured as 2 single-ended or 1 differential input pair. The DAC reference input is internally tied to V_{CC}.

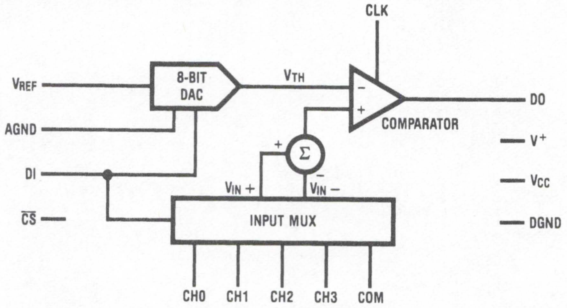
The multiplexer and 8-bit DAC are programmed via a serial data input word. Once programmed the output is updated once each clock cycle up to a maximum clock rate of 400 kHz.

Features

- 2 or 4 channel multiplexer
- Differential or Single-ended input, software controlled
- Serial digital data interface
- 256 programmable reference voltage levels
- Continuous comparison after programming
- Fixed, ratiometric, or reduced span reference capability (ADC 0854)

Key Specifications

- Accuracy, ± ½ LSB or ± 1 LSB of Reference (0.2%)
- Single 5V power supply
- Low Power, 15 mW

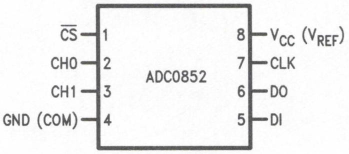


TL/H/5521-1

FIGURE 1. ADC0854 Simplified Block Diagram (ADC0852 has 2 input channels, COM tied to GND, V_{REF} tied to V_{CC}, V+ omitted, and one GND connection)

2 Channel and 4 Channel Pin Out

ADC0852 2-CHANNEL MUX
Dual-In-Line Package



TL/H/5521-10

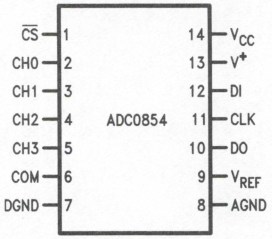
Top View

AGND and COM internally connected to GND

V_{REF} internally connected to V_{CC}

Order Number ADC0852
See NS Package Number J08A or N08E

ADC0854 4-CHANNEL MUX
Dual-In-Line Package



TL/H/5521-11

Top View

Order Number ADC0854
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Current into V^+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic and Analog Inputs	$-0.3V$ to V_{CC} $+0.3V$
Input Current per Pin	±5 mA
Input Current per Package	±20 mA
Storage Temperature	$-65°C$ to $+150°C$
Package Dissipation at $T_A = 25°C$ (Board Mount)	0.8W
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
ESD Susceptibility (Note 14)	2000V

Operating Conditions

Supply Voltage, V_{CC}	$4.5V_{DC}$ to $6.3V_{DC}$
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0854BJ, ADC0854CJ ADC0852BJ, ADC0852CJ	$-55°C \le T_A \le 125°C$
ADC0854BCJ, ADC0854CCJ ADC0852BCJ, ADC0852CCJ	$-40°C \le T_A \le 85°C$
ADC0854BCN, ADC0854CCN ADC0852BCN, ADC0852CCN	$0°C \le T_A \le 70°C$

Electrical Characteristics

The following specifications apply for $V_{CC} = V^+ = 5V$ (no V^+ on ADC0852), $V_{REF} \le V_{CC} + 0.1V$, $f_{CLK} = 250$ kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	ADC0852BCJ/CCJ/BJ/CJ ADC0854BCJ/CCJ/BJ/CJ			ADC0852BCN/CCN ADC0854BCN/CCN			Units
		Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Total Unadjusted Error (Note 7)	V_{REF} Forced to 5.000 V_{DC}							
ADC0852/4/BCN						±½	**±½**	LSB
ADC0852/4/BJ/BCJ			**±½**					LSB
ADC0852/4/CCN						±1	**±1**	LSB
ADC0852/4/CJ/CCJ			**±1**					LSB
Comparator Offset								
ADC0852/4/BCN		2.5			2.5		**10**	mV
ADC0852/4/BJ/BCJ		2.5	**10**		2.5			mV
ADC0852/4/CCN		2.5			2.5		**20**	mV
ADC0852/4/CCJ		2.5	**20**		2.5			mV
Minimum Total Ladder Resistance		3.5	**1.3**		3.5	1.3	**1.3**	kΩ
Maximum Total Ladder Resistance		3.5	**5.9**		3.5	5.4	**5.9**	kΩ
Minimum Common-Mode Input (Note 8)	All MUX Inputs and COM Input		**GND−0.05**			GND−0.05	**GND−0.05**	V
Maximum Common-Mode Input (Note 8)	All MUX Inputs and COM Input		**V_{CC} + 0.05**			V_{CC} + 0.05	**V_{CC} + 0.05**	V
DC Common-Mode Error		±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
Power Supply Sensitivity	$V_{CC} = 5V \pm 5\%$	±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
V_Z, Internal diode breakdown at V^+ (Note 3) MIN	15 mA into $V+$		**6.3**			6.3		V
MAX			**8.5**			8.5		V
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V		**−1** −200			 −200	**−1**	µA nA
	On Channel = 0V, Off Channel = 5V		**+1** +200			 +200	**+1**	µA nA

Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = V^+ = 5V$ (no V^+ on ADC0852), $f_{CLK} = 250$ kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	ADC0852BCJ/CCJ/BJ/CJ ADC0854BCJ/CCJ/BJ/CJ			ADC0852BCN/CCN ADC0854BCN/CCN			Units
		Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)								
I_{ON}, On Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V		**+1** +200			 +200	**+1**	µA nA
	On Channel = 0V, Off Channel = 5V		**−1** −200			 −200	**−1**	µA nA
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$	0.005	**1**		0.005	1	**1**	µA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1**		−0.005	−1	**−1**	µA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC} = 4.75V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		 **2.4** **4.5**			 2.4 4.5	 **2.4** **4.5**	 V V
$V_{OUT(0)}$, Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA, $V_{CC} = 4.75V$		**0.4**			0.4	**0.4**	V
I_{OUT}, TRI-STATE® Output Current (DO)	$\overline{CS}$ = Logical "1" $V_{OUT} = 0.4V$ $V_{OUT} = 5V$	 −0.1 0.1	 **−3** **3**		 −0.1 0.1	 −3 3	 **−3** **3**	 µA µA
I_{SOURCE}	V_{OUT} Short to GND	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}	V_{OUT} Short to V_{CC}	16	**8.0**		16	9.0	**8.0**	mA
I_{CC} Supply Current ADC0852	Includes DAC Ladder Current	2.7	**6.5**		2.7	6.5	**6.5**	mA
I_{CC} Supply Current ADC0854 (Note 3)	Does not Include DAC Ladder Current	0.9	**2.5**		0.9	2.5	**2.5**	mA

AC Characteristics $t_r = t_f = 20$ ns, $T_A = 25°C$

Symbol	Parameter		Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
f_{CLK}	Clock Frequency (Note 12)	MIN			10		kHz
		MAX				400	kHz
t_{D1}	Rising Edge of Clock to "DO" Enabled		$C_L = 100$ pF	650		1000	ns
t_r	Comparator Response Time (Note 13)		Not Including Addressing Time			$2 + 1$ μs	$1/f_{CLK}$
	Clock Duty Cycle (Note 10)	MIN			40		%
		MAX			60		%
t_{SET-UP}	CS Falling Edge or Data Input Valid to CLK Rising Edge	MAX				250	ns
t_{HOLD}	Data Input Valid after CLK Rising Edge	MIN				90	ns
t_{pd1}, t_{pd0}	CLK Falling Edge to Output Data Valid (Note 11)	MAX	$C_L = 100$ pF	650		1000	ns
t_{1H}, t_{0H}	Rising Edge of CS to Data Output Hi-Z	MAX	$C_L = 10$ pF, $R_L = 10k$	125		250	ns
			$C_L = 100$ pF, $R_L = 2k$ (see TRI-STATE Test Circuits)		500	500	ns
C_{IN}	Capacitance of Logic Input			5			pF
C_{OUT}	Capacitance of Logic Outputs			5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Internal zener diodes (approx. 7V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode ensures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore guaranteed for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+.

Note 4: Typicals are at 25°C and represent most likely parametric norm.

Note 5: Tested and guaranteed to National AOQL (Average Outgoing Quality Level).

Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: Total unadjusted error includes comparator offset, DAC linearity, and multiplexer error. It is expressed in LSBs of the threshold DAC's input code.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the output will be 0. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range ensures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits then 1.6 μS $\leq$ CLK Low $\leq$ 60 μS and 1.6 μS $\leq$ CLK HIGH $\leq \infty$.

Note 11: With $\overline{CS}$ low and programming complete, D0 is updated on each falling CLK edge. However, each new output is based on the comparison completed 0.5 clock cycles prior (see *Figure 5*).

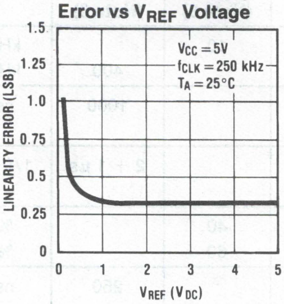
Note 12: Error specs are not guaranteed at 400 kHz (see graph: Comparator Error vs. f_{CLK}).

Note 13: See text, section 1.2.

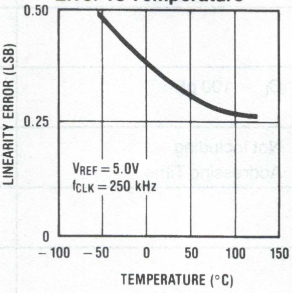
Note 14: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

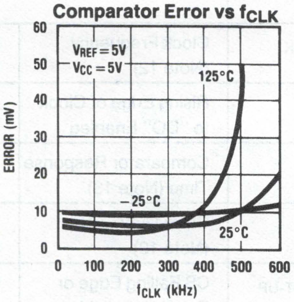
Internal DAC Linearity Error vs V_{REF} Voltage



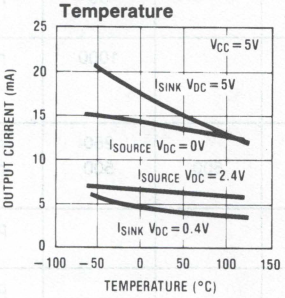
Internal DAC Linearity Error vs Temperature



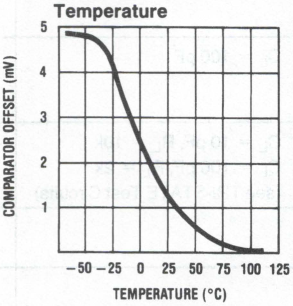
Comparator Error vs f_{CLK}



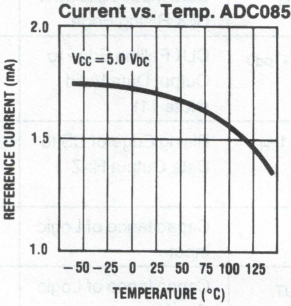
Output Current vs Temperature



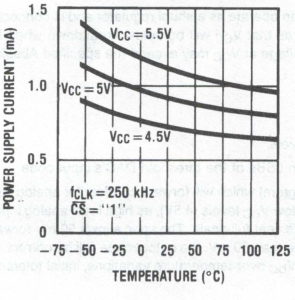
Comparator Offset vs Temperature



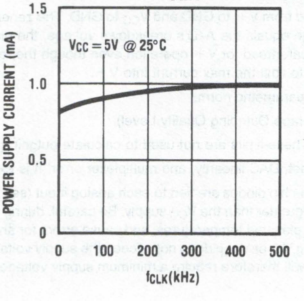
I_{REF}, Reference Current vs. Temp. ADC0854



I_{CC}, Power Supply Current vs. Temperature, ADC0854*



I_{CC}, Power Supply Current vs. f_{CLK}, ADC0854*

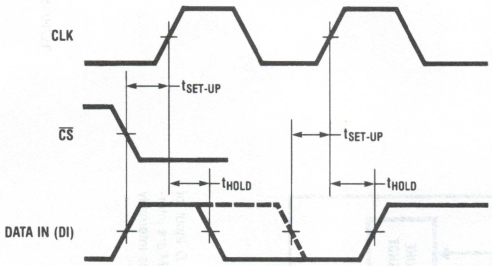


TL/H/5521-2

*For ADC0852 add I_{REF}

Timing Diagrams

Data Input Timing


CLK
$t_{SET\text{-}UP}$
$\overline{CS}$
$t_{SET\text{-}UP}$
t_{HOLD}
t_{HOLD}
DATA IN (DI)

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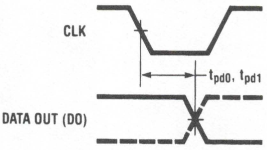
Data Output Timing


CLK
t_{pd0}, t_{pd1}
DATA OUT (DO)

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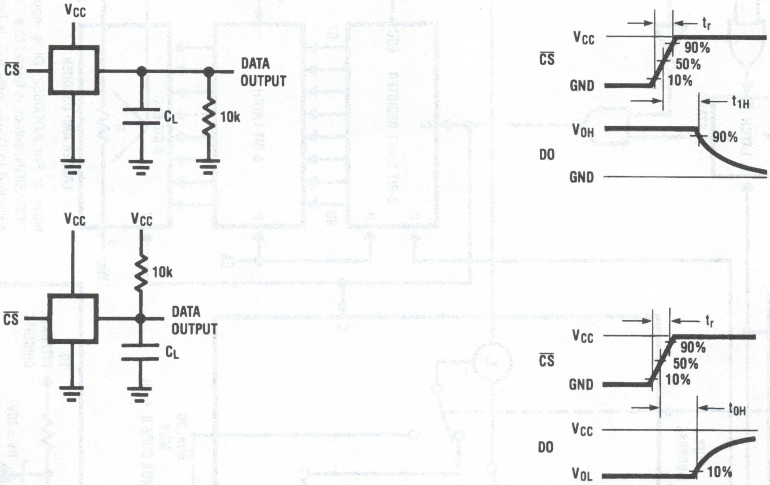
TRI-STATE Test Circuits and Waveforms


V_{CC}
$\overline{CS}$
DATA OUTPUT
C_L
10k
V_{CC}
V_{CC}
10k
$\overline{CS}$
DATA OUTPUT
C_L
t_r
V_{CC}
$\overline{CS}$
GND
90%
50%
10%
t_{1H}
V_{OH}
DO
GND
90%
t_r
V_{CC}
$\overline{CS}$
GND
90%
50%
10%
t_{0H}
V_{CC}
DO
V_{OL}
10%

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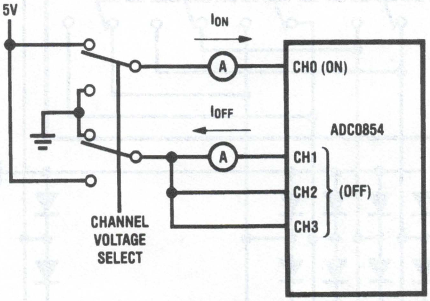
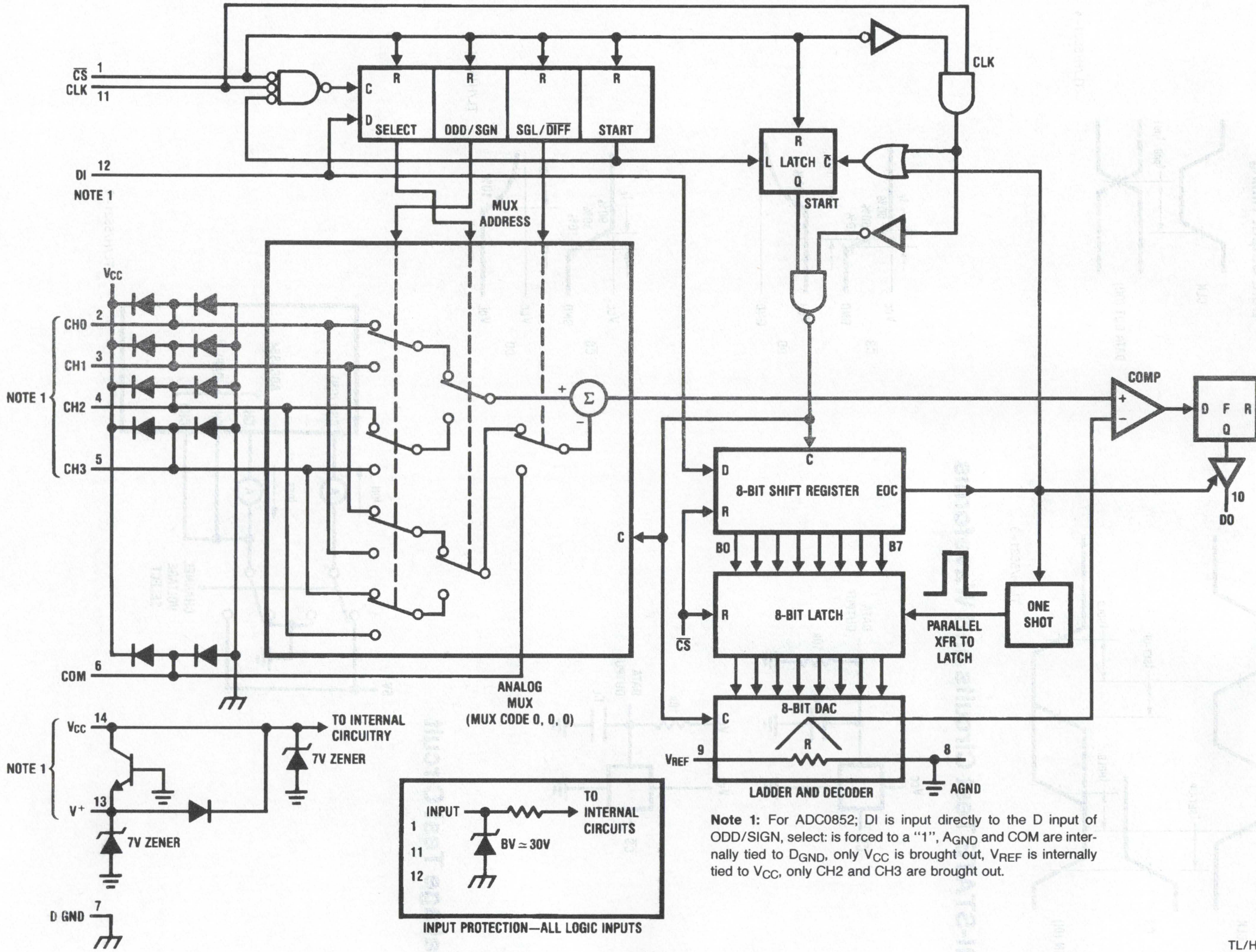
Leakage Test Circuit


5V
I_{ON}
A
CH0 (ON)
I_{OFF}
ADC0854
A
CH1
CH2
(OFF)
CH3
CHANNEL VOLTAGE SELECT

TL/H/5521-6


CS 1
CLK 11
DI 12
NOTE 1
C
D
R
SELECT
R
ODD/SGN
R
SGL/DIFF
R
START
CLK
R
L LATCH C
Q
START
MUX ADDRESS
Vcc
CH0 2
CH1 3
NOTE 1
CH2 4
CH3 5
COM 6
+
Σ
−
C
C
D
8-BIT SHIFT REGISTER EOC
R
B0
B7
R
8-BIT LATCH
CS
PARALLEL XFR TO LATCH
ONE SHOT
C
8-BIT DAC
R
VREF 9
8
AGND
LADDER AND DECODER
COMP
+
−
D F R
Q
CS
10
DO
ANALOG MUX (MUX CODE 0, 0, 0)
Vcc 14
TO INTERNAL CIRCUITRY
7V ZENER
NOTE 1
V+ 13
7V ZENER
D GND 7
INPUT
1
11
12
TO INTERNAL CIRCUITS
BV ≃ 30V
INPUT PROTECTION—ALL LOGIC INPUTS

Note 1: For ADC0852; DI is input directly to the D input of ODD/SIGN, select: is forced to a "1", A_{GND} and COM are internally tied to D_{GND}, only V_{CC} is brought out, V_{REF} is internally tied to V_{CC}, only CH2 and CH3 are brought out.

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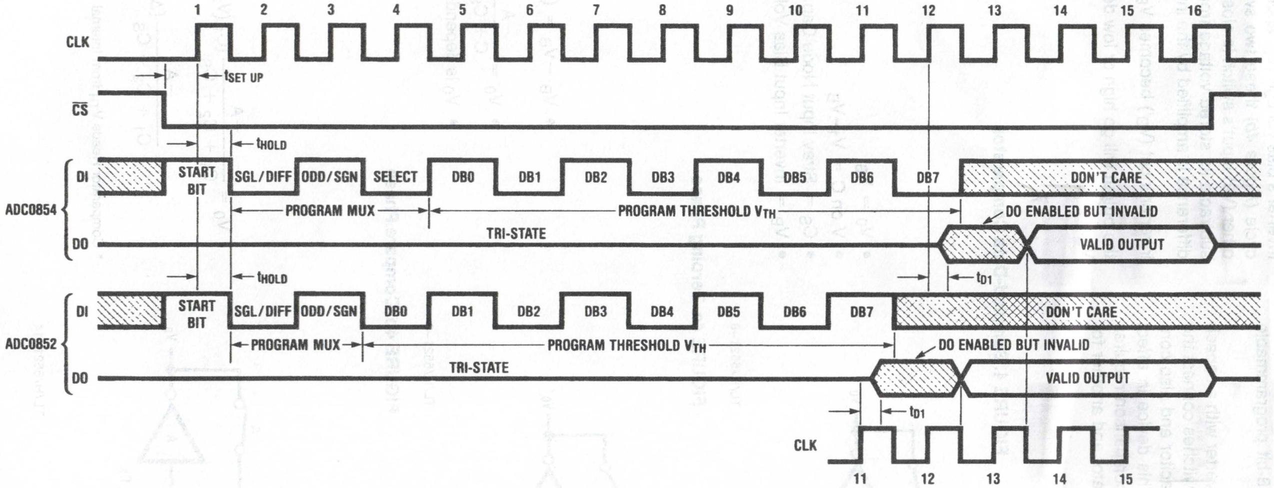
FIGURE 2. Detailed Block Diagram


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
CLK
tSET UP
CS
tHOLD
DI
START BIT
SGL/DIFF
ODD/SGN
SELECT
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DON'T CARE
ADC0854
PROGRAM MUX
PROGRAM THRESHOLD VTH
DO ENABLED BUT INVALID
DO
TRI-STATE
VALID OUTPUT
tD1
tHOLD
DI
START BIT
SGL/DIFF
ODD/SGN
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DON'T CARE
ADC0852
PROGRAM MUX
PROGRAM THRESHOLD VTH
DO ENABLED BUT INVALID
DO
TRI-STATE
VALID OUTPUT
tD1
CLK
11
12
13
14
15

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Note: Valid Output can change only on Falling Edge of CLK.

FIGURE 3. Timing Diagram

Functional Description

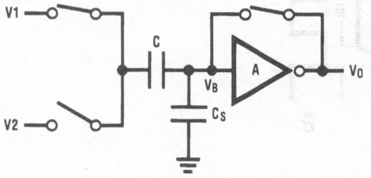
1. 1 The Sampled-data Comparator

The ADC0852 and ADC0854 utilize a sampled-data comparator structure to compare the analog difference between a selected "+" and "−" input to an 8-bit programmable threshold.

This comparator consists of a CMOS inverter with a capacitively coupled input (*Figure 4*). Analog switches connect the two comparator inputs to the input capacitor and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator and another for making the comparison.

In the first cycle (*Figure 4a*), one input switch and the inverter's feedback switch are closed. In this interval, the input capacitor (C) is charged to the connected input (V1) less the inverter's bias voltage (V_B, approx. 1.2 volts). In the second cycle (*Figure 4b*) these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter input ($V_B{}'$) becomes $V_B - (V1 - V2)\dfrac{C}{C + C_S}$ and the output will go high or low depending on the sign of $V_B{}' - V_B$.

FIGURE 4. Sampled-Data Comparator



- $V_O = V_B$
- V on C = $V_1 - V_B$
- C_S = Stray Input Node Cap.
- V_B = Inverter Input Bias Voltage

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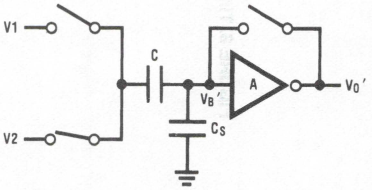
FIGURE 4a. Zeroing Phase



- $V_{B'} - V_B = (V_2 - V_1)\dfrac{C}{C + C_S}$
- $V_O = \dfrac{-A}{C + C_S}[CV_2 - CV_1]$
- V_O is dependent on $V_2 - V_1$

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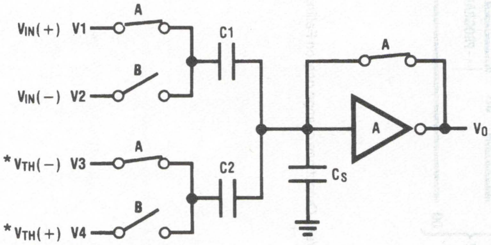
FIGURE 4b. Compare Phase



$$V_O = \frac{-A}{C_1 + C_2 + C_S}\left[C_1(V_2 - V_1) + C_2(V_4 - V_3)\right]$$

$$= \frac{-A}{C_1 + C_2 + C_S}\left[\Delta Q\, C_1 + \Delta Q\, C_2\right]$$

* Comparator Reads V_{TH} from Internal DAC Differentially

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FIGURE 4c. Multiple Differential Inputs

Functional Description (Continued)

In actual practice, the devices used in the ADC0852/4 are a simple but important expansion of the basic comparator described above. As shown in *Figure 4c*, multiple differential comparisons can be made. In this circuit, the feedback switch and one input switch on each capacitor (A switches) are closed in the first cycle. Then the other input on each capacitor is connected while all of the first switches are opened. The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor (C1, C2), will now depend on both input signal differences.

1.2 Input Sampling and Response Time

The input phases of the comparator relate to the device clock (CLK) as shown in *Figure 5.* Because the comparator is a sampling device, its response characteristics are somewhat different from those of linear comparators. The $V_{IN}(+)$ input is sampled first (CLK high) followed by $V_{IN}(-)$ (CLK low). The output responds to those inputs, one half cycle later, on CLK's falling edge.

The comparator's response time to an input step is dependent on the step's phase relation to the CLK signal. If an input step occurs too late to influence the most imminent comparator decision, one more CLK cycle will pass before the output is correct. In effect, the response time for the $V_{IN}(+)$ input has a minimum of 1 CLK cycle + 1 µS and a maximum of 2 CLK cycles + 1 µS. The $V_{IN}(-)$ input's delay will range from 1/2 CLK cycle + 1 µS to 1.5 CLK cycles + 1 µS since it is sampled after $V_{IN}(+)$.

The sampled inputs also affect the device's response to pulsed signals. As shown in the shaded areas in *Figure 5,* pulses that rise and/or fall near the latter part of a CLK half-cycle may be ignored.

1.3 Input Multiplexer

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or pseudo-differential operation. The analog signal conditioning required in transducer-input and other types of data acquisition systems is significantly simplified with this type of input flexibility. One device package can now handle ground referenced inputs as well as signals with some arbitrary reference voltage.

On the ADC0854, the "common" pin (pin 6) is used as the "−" input for all channels in single-ended mode. Since this input need not be at analog ground, it can be used as the common line for pseudo-differential operation. It may be tied to a reference potential that is common to all inputs and within the input range of the comparator. This feature is especially useful in single-supply applications where the analog circuitry is biased to a potential other than ground.

A particular input configuration is assigned during the MUX addressing sequence which occurs prior to the start of a comparison. The MUX address selects which of the analog channels is to be enabled, what the input mode will be, and the input channel polarity. One limitation is that differential inputs are restricted to adjacent channel pairs. For example, channel 0 and 1 may be selected as a differential pair but they cannot act differentially with any other channel.

The channel and polarity selection is done serially via the DI input. A complete listing of the input configurations and corresponding MUX addresses for the ADC0852 and ADC0854 is shown in tables I and II. *Figure 6* illustrates the analog connections for the various input options.

The analog input voltage for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading accuracy.

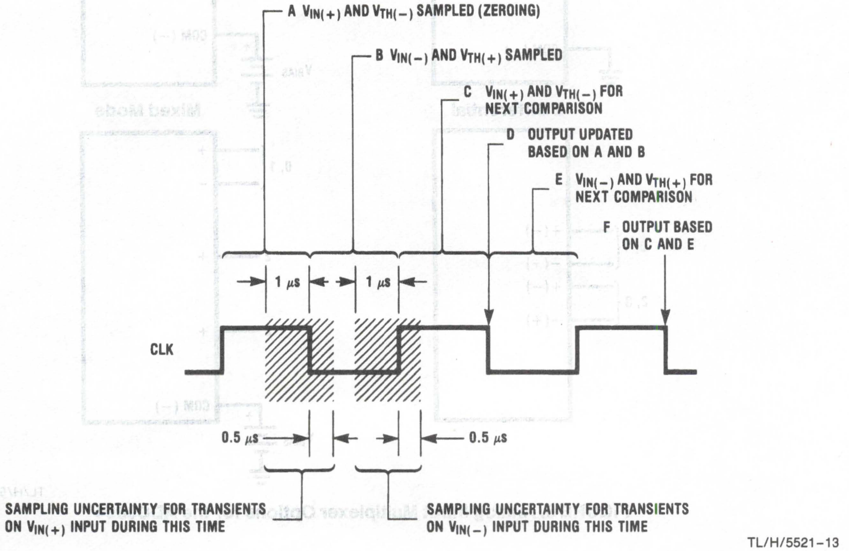
A $V_{IN(+)}$ AND $V_{TH(-)}$ SAMPLED (ZEROING)
B $V_{IN(-)}$ AND $V_{TH(+)}$ SAMPLED
C $V_{IN(+)}$ AND $V_{TH(-)}$ FOR NEXT COMPARISON
D OUTPUT UPDATED BASED ON A AND B
E $V_{IN(-)}$ AND $V_{TH(+)}$ FOR NEXT COMPARISON
F OUTPUT BASED ON C AND E
1 µs
1 µs
CLK
0.5 µs
0.5 µs
SAMPLING UNCERTAINTY FOR TRANSIENTS ON $V_{IN(+)}$ INPUT DURING THIS TIME
SAMPLING UNCERTAINTY FOR TRANSIENTS ON $V_{IN(-)}$ INPUT DURING THIS TIME

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FIGURE 5. Analog Input Timing

Functional Description (Continued)

TABLE I. MUX Addressing: ADC0854
Single-Ended MUX Mode

MUX Address			Channel				
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT	0	1	2	3	COM
1	0	0	+				−
1	0	1			+		−
1	1	0		+			−
1	1	1				+	−

Differential MUX Mode

MUX Address			Channel			
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

TABLE II. MUX Addressing: ADC0852
Single Ended MUX Mode

MUX Address		Channel	
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to A GND

Differential MUX Mode

MUX Address		Channel	
SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	0	1
0	0	+	−
0	1	−	+

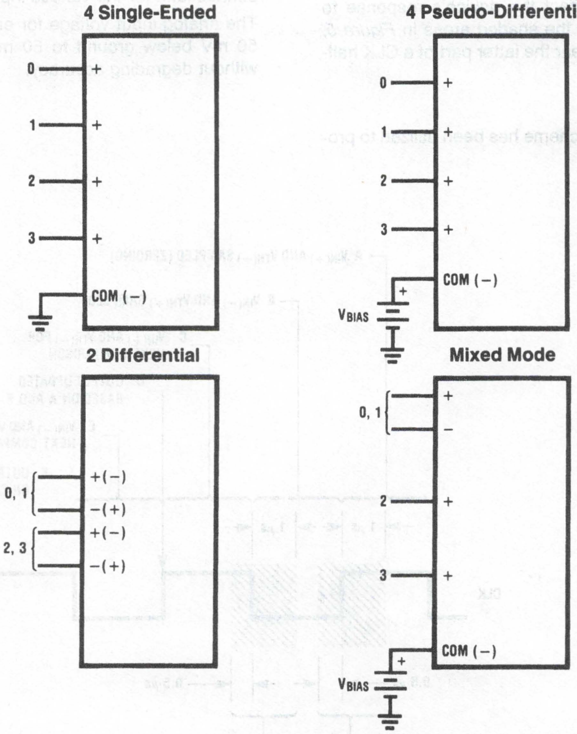
4 Single-Ended
0
1
2
3
+
COM (−)
2 Differential
0, 1
2, 3
+(−)
−(+)
4 Pseudo-Differential
VBIAS
Mixed Mode
−

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FIGURE 6. Analog Input Multiplexer Options for the ADC0854

Functional Description (Continued)

2.0 THE DIGITAL INTERFACE

An important characteristic of the ADC0852 and ADC0854 is their serial data link with the controlling processor. A serial communication format eliminates the transmission of low level analog signals by locating the comparator close to the signal source. Thus only highly noise immune digital signals need to be transmitted back to the host processor.

To understand the operation of these devices it is best to refer to the timing diagrams (*Figure 3*) and functional block diagram (*Figure 2*) while following a complete comparison sequence.

1. A comparison is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire addressing sequence and comparison. The comparator then waits for a start bit, its MUX assignment word, and an 8-bit code to set the internal DAC which supplies the comparator's threshold voltage (V_{TH}).

2. An external clock is applied to the CLK input. This clock can be applied continuously and need not be gated on and off.

3. On each rising edge of the clock, the level present on the DI line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line. All leading zeroes are ignored. After the start bit, the ADC0852 expects the next 2 bits to be the MUX assignment word while the ADC0854, with more MUX configurations, looks for 3 bits.

4. Immediately after the MUX assignment word has been clocked in, the shift register then reads the next eight bits as the input code to the internal DAC. This eight bit word is read LSB first and is used to set the voltage applied to the comparator's threshold input (internal).

5. After the rising edge of the 11th or 12th clock (ADC0852 or ADC0854 respectively) following the start bit, the comparator and DAC programming is complete. At this point the DI line is disabled and ignores further inputs. Also at this time the data out (DO) line comes out of TRI-STATE and enters a don't care state (undefined output) for 1.5 clock cycles.

6. The result of the comparison between the programmed threshold voltage and the difference between the two selected inputs ($V_{IN}(+) - V_{IN}(-)$) is output to the DO line on each subsequent high to low clock transition.

7. After programming, continuous comparison on the same selected channel with the same programmed threshold can be done indefinitely, without reprogramming the device, as long as $\overline{CS}$ remains low. Each new comparator decision will be shifted to the output on the falling edge of the clock. However, the output will, in effect, "lag" the analog input by 0.5 to 1.5 clock cycles because of the time required to make the comparison and latch the output (see *Figure 5*).

8. All internal registers are cleared when the $\overline{CS}$ line is brought high. If another comparison is desired $\overline{CS}$ must make a high to low transition followed by new address and threshold programming.

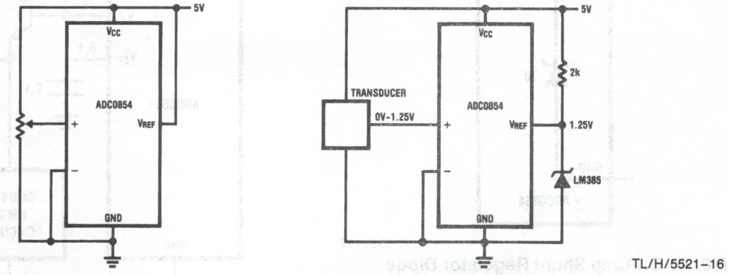
3.0 REFERENCE CONSIDERATIONS / RATIOMETRIC OPERATION

The voltage applied to the "V_{REF}" input of the DAC defines the voltage span that can be programmed to appear at the threshold input of the comparator. The ADC0854 can be used in either ratiometric applications or in systems with absolute references. The V_{REF} pin must be connected to a source capable of driving the DAC ladder resistance (typ. 2.4 kΩ) with a stable voltage.

In ratiometric systems, the analog input voltage is normally a proportion of the DAC's or A/D's reference voltage. For example, a mechanical position servo using a potentiometer to indicate rotation, could use the same voltage to drive the reference as well as the potentiometer. Changes in the value of V_{REF} would not affect system accuracy since only the relative value of these signals to each other is important. This technique relaxes the stability requirements of the system reference since the analog input and DAC reference move together, thus maintaining the same comparator output for a given input condition.

In the absolute case, the V_{REF} input can be driven with a stable voltage source whose output is insensitive to time and temperature changes. The LM385 and LM336 are good low current devices for this purpose.

The maximum value of V_{REF} is limited to the V_{CC} supply voltage. The minimum value can be quite small (see typical performance curves) allowing the effective resolution of the comparator threshold DAC to also be small ($V_{REF} = 0.5V$, DAC resolution = 2.0 mV). This in turn lets the designer have finer control over the comparator trip point. In such instances however, more care must be taken with regard to noise pickup, grounding, and system error sources.



a) Ratiometric

b) Absolute with a Reduced Span

FIGURE 7. Referencing Examples

Functional Description (Continued)

4.0 ANALOG INPUTS

4. 1 Differential Inputs

The serial interface of the ADC0852 and ADC0854 allows them to be located right at the analog signal source and to communicate with a controlling processor via a few fairly noise immune digital lines. This feature in itself greatly reduces the analog front end circuitry often needed to maintain signal integrity. Nevertheless, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common mode voltage.

The differential input of the comparator actually reduces the effect of common-mode input noise, i.e. signals common to both selected "+" and "−" inputs such as 60 Hz line noise. The time interval between sampling the "+" input and then the "−" input is ½ of a clock period (see *Figure 5*).

The change in the common-mode voltage during this short time interval can cause comparator errors. For a sinusoidal common-mode signal this error is:

$$V_{ERROR}\ (MAX) = V_{PEAK}\ (2\pi\ f_{CM}/2\ f_{CLK})$$

where f_{CM} is the frequency of the common-mode signal, V_{peak} is its peak voltage value, and f_{CLK} is the DAC clock frequency.

For example, 1 V_{PP} 60 Hz noise superimposed on both sides of a differential input signal would cause an error (referred to the input) of 0.75 mV. This amounts to less than $1/25$ of an LSB referred to the threshold DAC, (assuming V_{REF} = 5V and f_{CLK} = 250 kHz).

4. 2 Input Currents and Filtering

Due to the sampling nature of the analog inputs, short spikes of current enter the "+" input and leave the "−" at the clock edges during a comparison. These currents decay rapidly and do not cause errors as the comparator is strobed at the end of the clock period (see *Figure 5*).

The source resistance of the analog input is important with regard to the DC leakage currents of the input multiplexer. The worst-case leakage currents of ±1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op-amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance source be required.

4. 3 Arbitrary Analog Input/Reference Range

The total span of the DAC output and hence the comparator's threshold voltage is determined by the DAC reference. For example, if V_{REF} is set to 1 volt then the comparator's threshold can be programmed over a 0 to 1 volt range with 8 bits of resolution. From the analog input's point of view, this span can also be shifted by applying an offset potential to one of the comparator's selected analog input lines (usually "−"). This gives the designer greater control of the ADC0852/4's input range and resolution and can help simplify or eliminate expensive signal conditioning electronics.

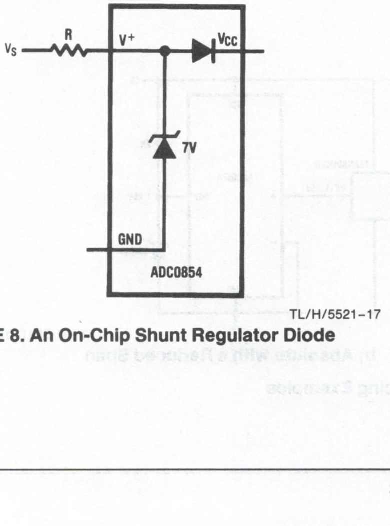
An example of this capability is shown in the "Load Cell Limit Comparator" of *Figure 15*. In this circuit, the ADC0852 allows the load-cell signal conditioning to be done with only one dual op-amp and without complex, multiple resistor matching.

5.0 POWER SUPPLY

A unique feature of the ADC0854 is the inclusion of a 7 volt zener diode connected from the "V+" terminal to ground (*Figures 2* and *8*) "V+" also connects to "V_{CC}" via a silicon diode. The zener is intended for use as a shunt voltage regulator to eliminate the need for additional regulating components. This is especially useful if the ADC0854 is to be remotely located from the system power source.

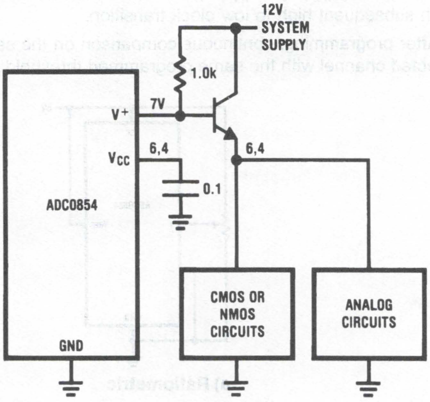
An important use of the interconnecting diode between V+ and V_{CC} is shown in *Figures 10* and *11*. Here this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the comparator clock. The low device current requirements and the relatively high clock frequencies used (10 kHz–400 kHz) allows use of the small value filter capacitor shown. The shunt zener regulator can also be used in this mode however this requires a clock voltage swing in excess of 7 volts. Current limiting for the zener is also needed, either built into the clock generator or through a resistor connected from the clock to V+.

Typical Applications



TL/H/5521–17

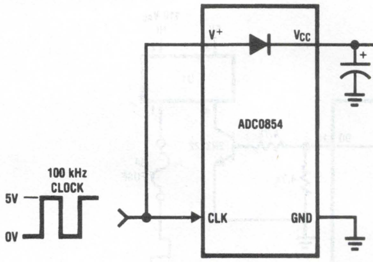
FIGURE 8. An On-Chip Shunt Regulator Diode



TL/H/5521–18

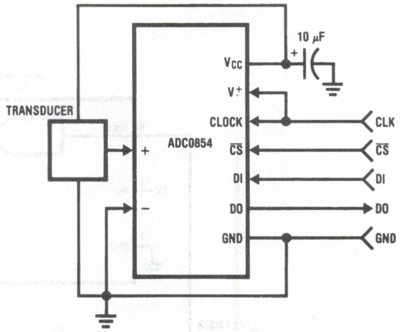
FIGURE 9. Using the ADC0854 as the System Supply Regulator

Typical Applications (Continued)


V+
Vcc
Vcc
+
10 μF
ADC0854
100 kHz
CLOCK
5V
0V
CLK
GND

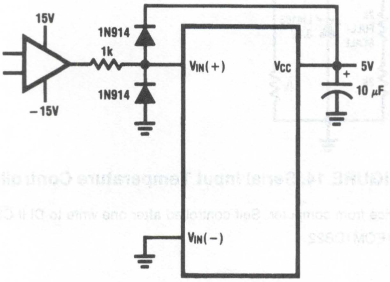
TL/H/5521–19

FIGURE 10. Generating V_{CC} from the Comparator Clock


10 μF
+
Vcc
V+
TRANSDUCER
CLOCK
ADC0854
+
CS
DI
−
DO
GND
CLK
CS
DI
DO
GND

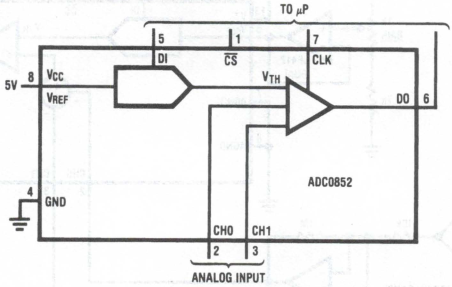
TL/H/5521–20

FIGURE 11. Remote Sensing—Clock and Power on One Wire


15V
1N914
1k
VIN(+)
Vcc
5V
+
10 μF
1N914
−15V
VIN(−)

TL/H/5521–21

FIGURE 12. Protecting the Analog Input


TO μP
5
1
7
DI
CS
CLK
5V
8
Vcc
VREF
VTH
DO
6
ADC0852
4
GND
CHO
CH1
2
3
ANALOG INPUT

TL/H/5521–22

FIGURE 13. One Component Window Comparator

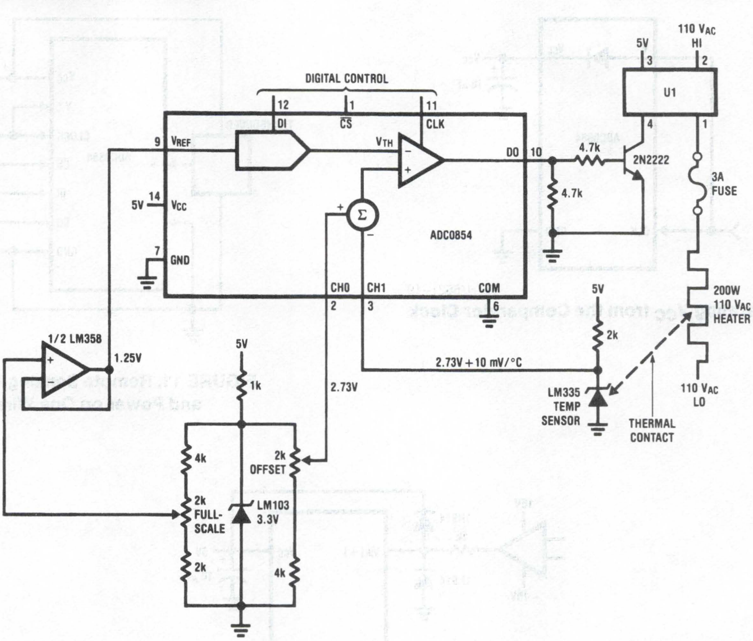
Requires no additional parts. Window comparisons can be accomplished by inputting the upper and lower window limits into DI on successive comparisons and observing the two outputs:

Two high outputs → input > window

Two low outputs → input < window

One low and one high → input is within window

Typical Applications (Continued)


DIGITAL CONTROL
12
DI
1
CS
11
CLK
9
VREF
VTH
DO
10
14
5V
VCC
7
GND
ADC0854
CH0
CH1
COM
2
3
6
4.7k
4.7k
2N2222
5V
3
4
U1
110 VAC
HI
2
1
3A
FUSE
200W
110 VAC
HEATER
110 VAC
LO
5V
2k
2.73V + 10 mV/°C
LM335
TEMP
SENSOR
THERMAL
CONTACT
1/2 LM358
1.25V
5V
1k
2.73V
4k
2k
OFFSET
2k
FULL-
SCALE
LM103
3.3V
2k
4k

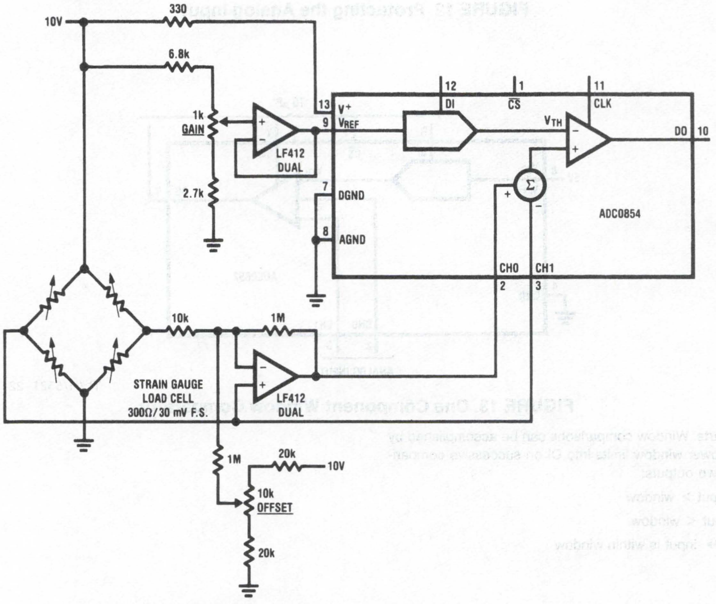
TL/H/5521-23

FIGURE 14. Serial Input Temperature Controller

Note 1: ADC0854 does not require constant service from computer. Self controlled after one write to DI if $\overline{CS}$ remains low.

Note 2: U_1: Solid State Relay, Potter Brumfield #EOM1DB22

Note 3: Set Temp via. DI. Range: 0 to 125°C

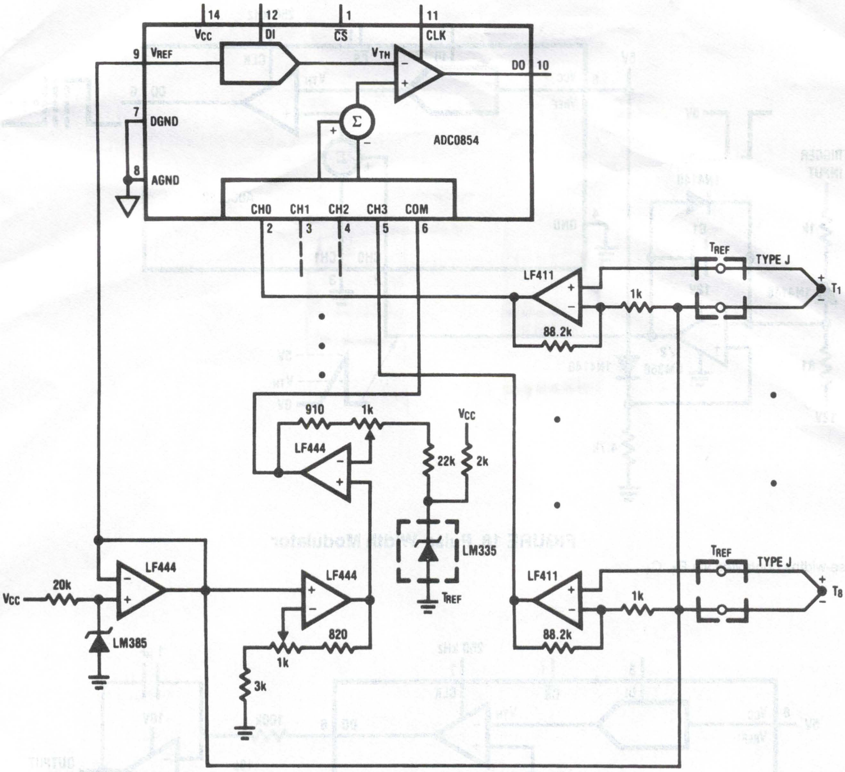

10V
330
6.8k
1k
GAIN
2.7k
LF412
DUAL
13
V+
9
VREF
7
DGND
8
AGND
12
DI
1
CS
11
CLK
VTH
DO
10
ADC0854
CH0
CH1
2
3
10k
1M
STRAIN GAUGE
LOAD CELL
300Ω/30 mV F.S.
LF412
DUAL
1M
20k
10V
10k
OFFSET
20k

TL/H/5521-24

FIGURE 15. Load Cell Limit Comparator

- Differential Input elliminates need for instrumentation amplifier
- A total of 4 load cells can be monitored by ADC0854

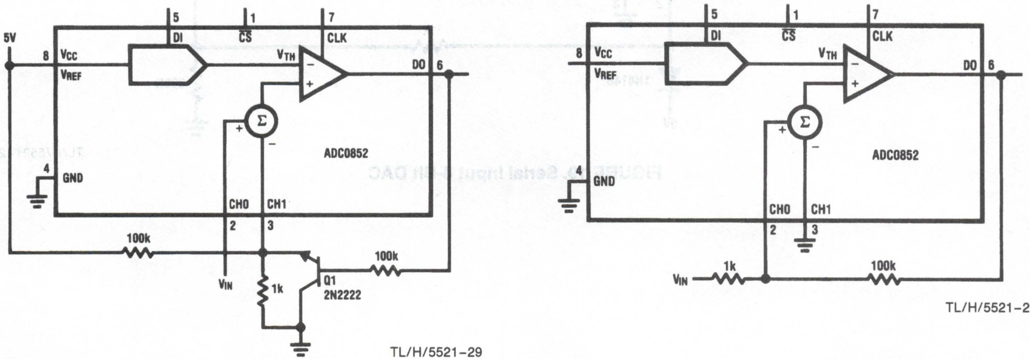
Typical Applications (Continued)


14
12
1
11
VCC
DI
CS
CLK
9
VREF
VTH
DO
10
7
DGND
Σ
ADC0854
8
AGND
CH0
CH1
CH2
CH3
COM
2
3
4
5
6
LF411
TREF
TYPE J
T1
1k
88.2k
910
1k
VCC
LF444
22k
2k
LM335
TREF
LF444
20k
VCC
LM385
LF444
820
1k
3k
LF411
TREF
TYPE J
T8
1k
88.2k

TL/H/5521-25

FIGURE 16. 4 Channel Temperature Alarm

- Uses pseudo-differential input MUX mode
- 4 Thermocouple channels need only 1 cold-junction compensation network (T_{REF})
- Range 0 to 300°C


5V
5
1
7
8
VCC
VREF
DI
CS
VTH
CLK
DO
6
Σ
ADC0852
4
GND
CH0
CH1
2
3
100k
100k
VIN
1k
Q1
2N2222
5
1
7
8
VCC
VREF
DI
CS
VTH
CLK
DO
6
Σ
ADC0852
4
GND
CH0
CH1
2
3
VIN
1k
100k

TL/H/5521-29

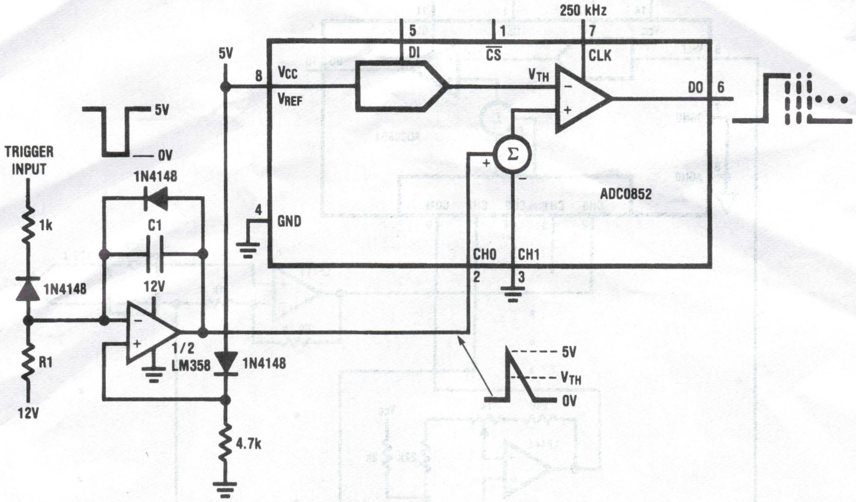
TL/H/5521-26

* Q_1 used in inverted mode for low V_{SAT}

Hysteresis band = 50 mV

FIGURE 17. Adding Comparator Hysteresis

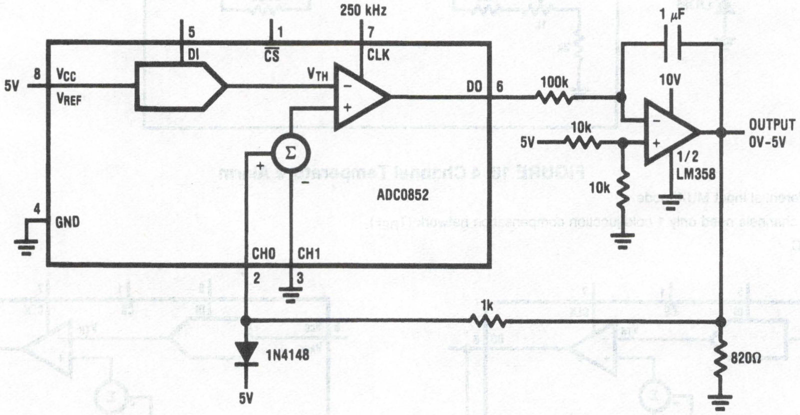
Typical Applications (Continued)


250 kHz
5
1
7
DI
CS
CLK
5V
8
Vcc
VREF
VTH
DO
6
5V
0V
TRIGGER INPUT
1N4148
1k
C1
4
GND
ADC0852
1N4148
12V
CH0
CH1
2
3
1/2 LM358
1N4148
R1
12V
4.7k
5V
VTH
0V

TL/H/5521-27

FIGURE 18. Pulse-Width Modulator

- Range of pulse-widths controlled via R_1, C_1


250 kHz
5
1
7
DI
CS
CLK
5V
8
Vcc
VREF
VTH
DO
6
100k
1 µF
10V
5V
10k
10k
OUTPUT 0V-5V
1/2 LM358
4
GND
ADC0852
CH0
CH1
2
3
1k
1N4148
5V
820Ω

TL/H/5521-28

FIGURE 19. Serial Input 8-Bit DAC

Ordering Information

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0852BJ	2	±½	J08A	−55°C to +125°C
ADC0852BCJ				−40°C to +85°C
ADC0852BCN			N08E	0°C to 70°C
ADC0852CCJ		±1	J08A	−40°C to +85°C
ADC0852CCN			N08E	0°C to 70°C
ADC0854BJ	4	±½	J14A	−55°C to +125°C
ADC0854BCJ				−40°C to +85°C
ADC0854BCN			N14A	0°C to 70°C
ADC0854CCJ		±1	J14A	−40°C to +85°C
ADC0854CCN			N14A	0°C to 70°C

National Semiconductor Corporation

ADC1001, ADC1021 10-Bit µP Compatible A/D Converters

General Description

The ADC1001 and ADC1021 are CMOS, 10-bit successive approximation A/D converters. The 20-pin ADC1001 is pin compatible with the ADC0801 8-bit A/D family. The 10-bit data word is read in two 8-bit bytes, formatted left justified and high byte first. The six least significant bits of the second byte are set to zero, as is proper for a 16-bit word.

The 24-pin ADC1021 outputs 10 bits parallel and is intended for interface to a 16-bit data bus.

Differential inputs provide low frequency input common mode rejection and allow offsetting the analog range of the converter. In addition, the reference input can be adjusted enabling the conversion of reduced analog ranges with 10-bit resolution.

Features

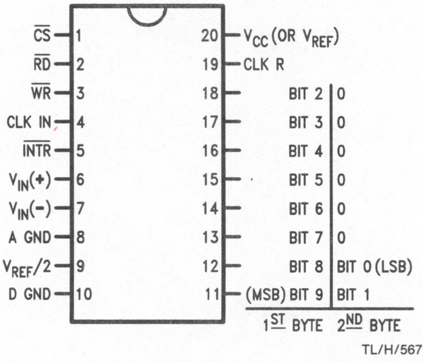
- ADC1001 is pin compatible with ADC0801 series 8-bit A/D converters
- Compatible with NSC800 and 8080 µP derivatives—no interfacing logic needed
- Easily interfaced to 6800 µP derivatives with minimal external logic
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference
- 0.3″ standard width 20-pin DIP package or 24 pins with 10-bit parallel output

Key Specifications

Resolution	10 bits
Linearity error	±1 LSB
Conversion time	200µS

Connection Diagrams

ADC1001 (for an 8-bit data bus)
Dual-In-Line Package

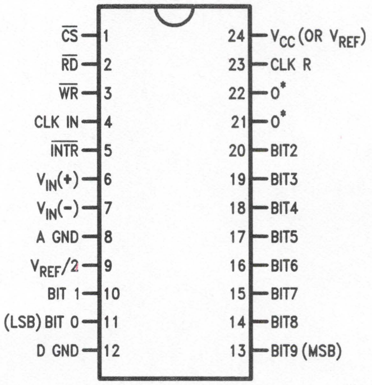


CS 1
RD 2
WR 3
CLK IN 4
INTR 5
VIN(+) 6
VIN(−) 7
A GND 8
VREF/2 9
D GND 10
20 VCC (OR VREF)
19 CLK R
18 BIT 2 | 0
17 BIT 3 | 0
16 BIT 4 | 0
15 BIT 5 | 0
14 BIT 6 | 0
13 BIT 7 | 0
12 BIT 8 | BIT 0 (LSB)
11 (MSB) BIT 9 | BIT 1
1ST BYTE 2ND BYTE

TL/H/5675–11

Top View

ADC1021 (for all 10-bit outputs in parallel)
Dual-In-Line Package



CS 1
RD 2
WR 3
CLK IN 4
INTR 5
VIN(+) 6
VIN(−) 7
A GND 8
VREF/2 9
BIT 1 10
(LSB) BIT 0 11
D GND 12
24 VCC (OR VREF)
23 CLK R
22 0*
21 0*
20 BIT2
19 BIT3
18 BIT4
17 BIT5
16 BIT6
15 BIT7
14 BIT8
13 BIT9 (MSB)

TL/H/5675–12

Top View

*TRI-STATE output buffers which output 0 during RD.

Ordering Information

Temperature Range	0°C to +70°C		−40°C to +85°C	
Order Number	ADC1001CCJ-1	ADC1021CCJ-1	ADC1001CCJ	ADC1021CCJ
Package Outline	J20A	J24A	J20A	J24A

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Logic Control Inputs	−0.3V to +18V
Voltage at Other Inputs and Outputs	−0.3V to (V_{CC}+0.3V)
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 10)	800V

Operating Conditions (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1001CCJ ADC1021CCJ	$-40°C \le T_A \le +85°C$
ADC1001CCJ-1 ADC1021CCJ-1	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Converter Characteristics

Converter Specifications: V_{CC}=5 V_{DC}, $V_{REF}/2$=2.500 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=410 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC1001C, ADC1021C:					
Linearity Error				±1	LSB
Zero Error				±2	LSB
Full-Scale Error				±2	LSB
Total Ladder Resistance (Note 9)	Input Resistance at Pin 9	2.2	4.8		KΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±⅛		LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC}±5% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±⅛		LSB

AC Electrical Characteristics

Timing Specifications: V_{CC}=5 V_{DC} and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_c	Conversion Time	(Note 5) f_{CLK}=410 kHz	82 200		89 217	$1/f_{CLK}$ μS
f_{CLK}	Clock Frequency	(Note 8)	100		1260	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$=0 V_{DC}, f_{CLK}=410 kHz			4600	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$=0 V_{DC} (Note 6)	150			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		170	300	ns
t_{1H}, t_{0H}	TRI-STATE® Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
t_{1rs}	$\overline{INTR}$ to 1st Read Set-Up Time		550	400		ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

DC Electrical Characteristics

The following specifications apply for $V_{CC}=5\ V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except CLK IN)	$V_{CC}=5.25\ V_{DC}$	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except CLK IN)	$V_{CC}=4.75\ V_{DC}$			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	$V_{IN}=5\ V_{DC}$		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" input Current (All Inputs)	$V_{IN}=0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN						
V_T+	CLK IN Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
OUTPUTS AND $\overline{\text{INTR}}$						
$V_{OUT}(0)$	Logical "0" Output Voltage	$I_{OUT}=1.6\ mA,\ V_{CC}=4.75\ V_{DC}$			0.4	V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O=-360\ \mu A,\ V_{CC}=4.75\ V_{DC}$ $I_O=-10\ \mu A,\ V_{CC}=4.75\ V_{DC}$	2.4 4.5			V_{DC} V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT}=0.4\ V_{DC}$ $V_{OUT}=5\ V_{DC}$		0.1 0.1	−100 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to GND, $T_A=25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A=25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	$f_{CLK}=410\ kHz$, $V_{REF}/2=NC$, $T_A=25°C$ and $\overline{CS}=1$		2.5	5.0	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified. The separate A GND point should always be wired to the D GND.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be all zeros. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near fullscale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 1*.

Note 6: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see Timing Diagrams).

Note 7: All typical values are for $T_A=25°C$.

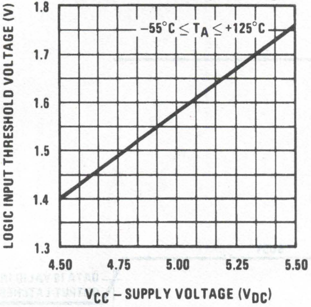
Note 8: Accuracy is guaranteed at $f_{CLK}=410$ kHz. At higher clock frequencies accuracy can degrade.

Note 9: The $V_{REF/2}$ pin is the center point of a two resistor divider (each resistor is 2.4kΩ) connected from V_{CC} to ground. Total ladder input resistance is the sum of these two equal resistors.

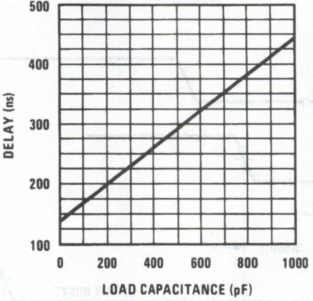
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

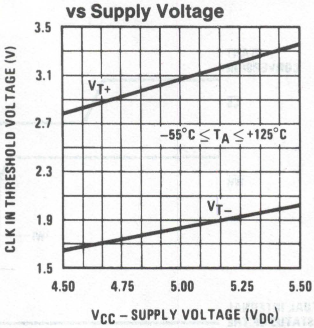
Logic Input Threshold Voltage vs Supply Voltage



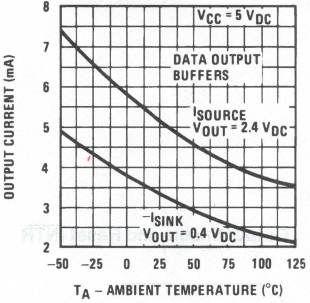
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs Load Capacitance



CLK IN Schmitt Trip Levels vs Supply Voltage



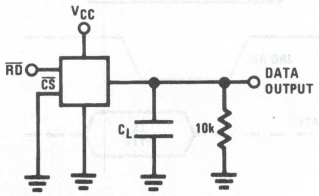
Output Current vs Temperature



TL/H/5675-2

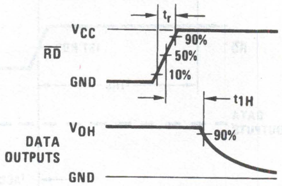
TRI-STATE Test Circuits and Waveforms

t_{1H}


V$_{CC}$
$\overline{RD}$
$\overline{CS}$
DATA OUTPUT
C$_L$
10k

TL/H/5675-3

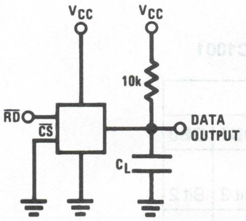
t_{1H}, $C_L = 10$ pF


t$_r$
V$_{CC}$
$\overline{RD}$
GND
90%
50%
10%
t$_{1H}$
V$_{OH}$
DATA OUTPUTS
90%
GND

TL/H/5675-4

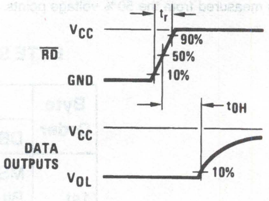
$t_r = 20$ ns

t_{0H}


V$_{CC}$
V$_{CC}$
10k
$\overline{RD}$
$\overline{CS}$
DATA OUTPUT
C$_L$

TL/H/5675-5

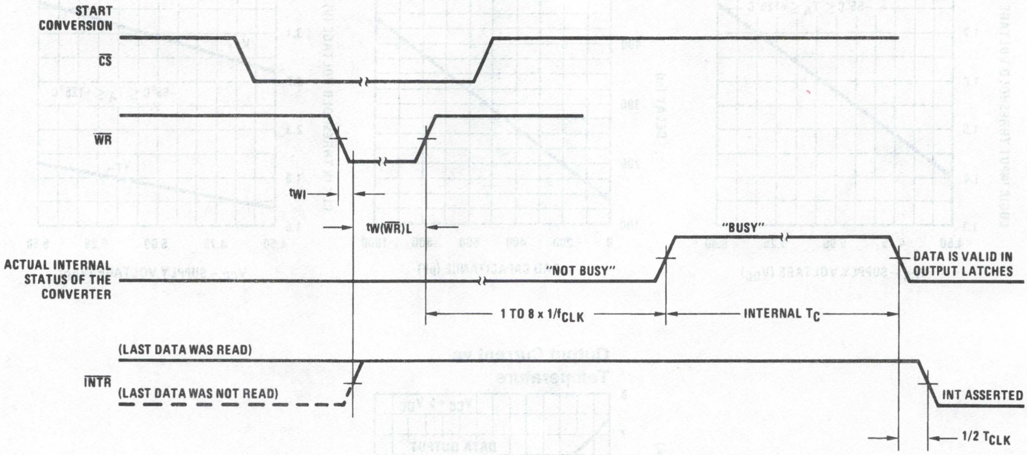
t_{0H}, $C_L = 10$ pF


t$_r$
V$_{CC}$
$\overline{RD}$
GND
90%
50%
10%
t$_{0H}$
V$_{CC}$
DATA OUTPUTS
V$_{OL}$
10%

TL/H/5675-6

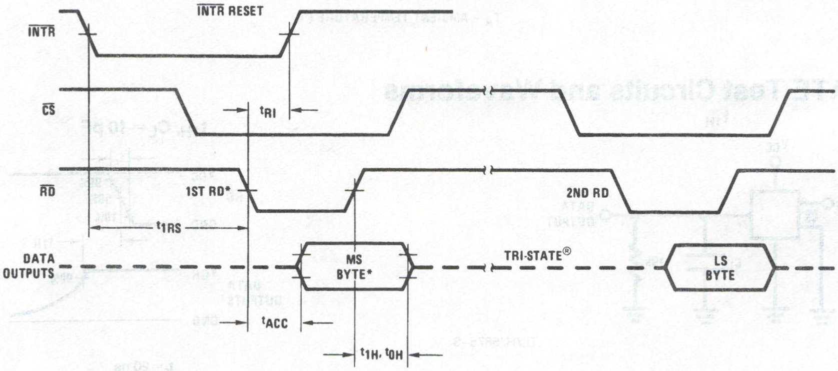
$t_r = 20$ ns

Timing Diagrams


START CONVERSION
CS
WR
tWI
tW(WR)L
"BUSY"
ACTUAL INTERNAL STATUS OF THE CONVERTER
"NOT BUSY"
DATA IS VALID IN OUTPUT LATCHES
1 TO 8 x 1/fCLK
INTERNAL TC
(LAST DATA WAS READ)
INTR
(LAST DATA WAS NOT READ)
INT ASSERTED
1/2 TCLK

TL/H/5675-7

Output Enable and Reset $\overline{INTR}$


INTR
INTR RESET
CS
tRI
RD
1ST RD*
t1RS
2ND RD
DATA OUTPUTS
MS BYTE*
TRI-STATE®
LS BYTE
tACC
t1H, t0H

TL/H/5675-8

*The 24-pin ADC1021 outputs all 10 bits on each RD.

Note: All timing is measured from the 50% voltage points.

BYTE SEQUENCING FOR THE 20-PIN ADC1001

Byte Order	8-Bit Data Bus Connection							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1st	MSB Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
2nd	Bit 1	LSB Bit 0	0	0	0	0	0	0

Functional Description

The ADC1001, ADC1021 use an advanced potentiometric resistive ladder network. The analog inputs, as well as the taps of this ladder network, are switched into a weighted capacitor array. The output of this capacitor array is the input to a sampled data comparator. This comparator allows the successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to taps on the R network. The most significant bit is tested first and after 10 comparisons (80 clock cycles) a digital 10-bit binary code (all "1"s = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ inut with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion in process can be interrupted by issuing a second start command.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 1*. All of the inputs and outputs are shown and the major logic control paths are drawn in heavier weight lines.

The conversion is initialized by taking $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 10-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 10-bit shift register then can have the "1" clocked in, which allows the conversion process to continue. If the set signal were to still be present, this reset pulse would have no effect and the 10-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

After the "1" is clocked through the 10-bit shift register (which completes the SAR search) it causes the new digital word to transfer to the TRI-STATE output latches. When this XFER signal makes a high-to-low transition the one shot fires, setting the INTR F/F. An inverting buffer then supplies the $\overline{INTR}$ output signal.

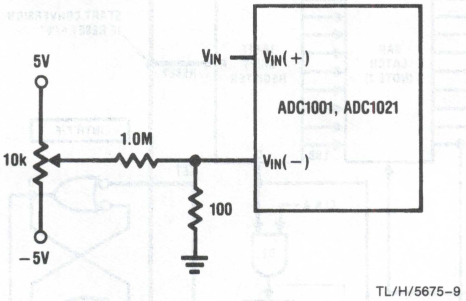
Note that this $\overline{SET}$ control of the INTR F/F remains low for aproximately 400 ns. If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of the conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled.

Zero and Full-Scale Adjustment

Zero error can be adjusted as shown in *Figure 2*. $V_{IN}(+)$ is forced to +2.5 mV (+½ LSB) and the potentiometer is adjusted until the digital output code changes from 00 0000 0000 to 00 0000 0001.

Full-scale is adjusted as shown in *Figure 3*, with the $V_{REF}/2$ input. With $V_{IN}(+)$ forced to the desired full-scale voltage less 1½ LSBs ($V_{FS} - 1½$ LSBs), $V_{REF}/2$ is adjusted until the digital output code changes from 11 1111 1110 to 11 1111 1111.



NOTE: $V_{IN}(-)$ should be biased so that $V_{IN}(-) \geq -0.05V$ when potentiometer wiper is set at most negative voltage position.

FIGURE 2. Zero Adjust Circuit

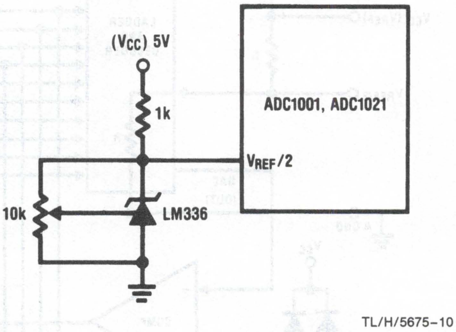
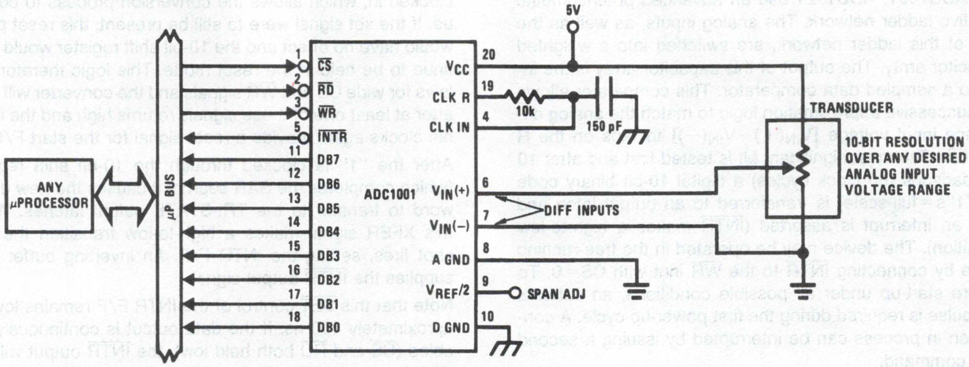


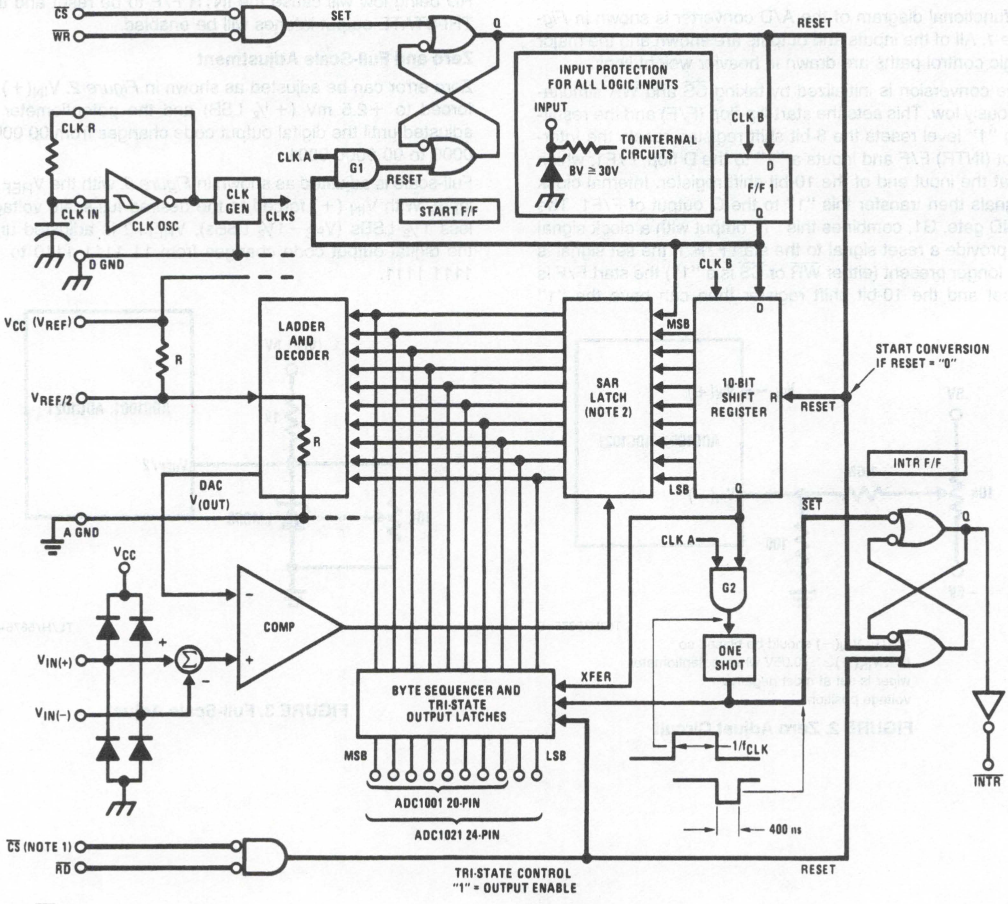
FIGURE 3. Full-Scale Adjust

Typical Application


5V
ANY µPROCESSOR
µP BUS
1 CS
2 RD
3 WR
5 INTR
11 DB7
12 DB6
13 DB5
14 DB4
15 DB3
16 DB2
17 DB1
18 DB0
ADC1001
20 VCC
19 CLK R
4 CLK IN
6 VIN(+)
7 VIN(−)
8 A GND
9 VREF/2
10 D GND
10k
150 pF
TRANSDUCER
10-BIT RESOLUTION OVER ANY DESIRED ANALOG INPUT VOLTAGE RANGE
DIFF INPUTS
SPAN ADJ

TL/H/5675–1

Block Diagram


CS
WR
SET
Q
RESET
INPUT PROTECTION FOR ALL LOGIC INPUTS
INPUT
BV ≅ 30V
TO INTERNAL CIRCUITS
CLK B
D
F/F 1
Q
CLK R
CLK IN
CLK OSC
CLK GEN
CLKS
D GND
CLK A
G1
RESET
START F/F
VCC (VREF)
VREF/2
R
LADDER AND DECODER
R
DAC
V(OUT)
A GND
VCC
VIN(+)
VIN(−)
COMP
CLK B
D
MSB
SAR LATCH (NOTE 2)
LSB
10-BIT SHIFT REGISTER
R
Q
RESET
START CONVERSION IF RESET = "0"
INTR F/F
SET
Q
CLK A
G2
ONE SHOT
XFER
BYTE SEQUENCER AND TRI-STATE OUTPUT LATCHES
MSB
LSB
ADC1001 20-PIN
ADC1021 24-PIN
1/fCLK
400 ns
INTR
CS (NOTE 1)
RD
TRI-STATE CONTROL "1" = OUTPUT ENABLE
RESET

Note 1: CS shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

TL/H/5675–13

FIGURE 1

National Semiconductor Corporation

ADC1005, ADC1025 10-Bit μP Compatible A/D Converters

General Description

The ADC1005 and ADC1025 are CMOS 10-bit successive approximation A/D converters. The 20-pin ADC1005 outputs 10-bit data in a two-byte format for interface with 8-bit microprocessors.

The 24-pin ADC1025 outputs 10 bits in parallel and is intended for 16-bit data buses or stand-alone applications.

Both A-to-Ds have differential inputs to permit rejection of common-mode signals, allow the analog input range to be offset, and also to permit the conversion of signals not referred to ground. In addition, the reference voltage can be adjusted, allowing smaller voltage spans to be measured with 10-bit resolution.

Features

- Easy interface to all microprocessors
- Differential analog voltage inputs
- Operates ratiometrically or with 5 V_{DC} voltage reference or analog span adjusted voltage reference
- 0V to 5V analog input voltage range with single 5V supply
- On-chip clock generator
- TLL/MOS input/output compatible
- 0.3″ standard width 20-pin DIP or 24-pin DIP with 10-bit parallel output
- Available in 20-pin or 28-pin molded chip carrier package

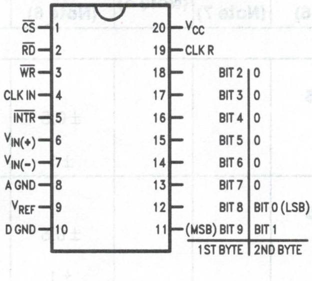
Key Specifications

■ Resolution	10 bits
■ Linearity Error	±½ LSB and ±1 LSB
■ Conversion Time	50 μs

Connection Diagrams

ADC1005 (for an 8-bit data bus)

Dual-In-Line Package



CS 1
RD 2
WR 3
CLK IN 4
INTR 5
VIN(+) 6
VIN(−) 7
A GND 8
VREF 9
D GND 10
20 VCC
19 CLK R
18 BIT 2 | 0
17 BIT 3 | 0
16 BIT 4 | 0
15 BIT 5 | 0
14 BIT 6 | 0
13 BIT 7 | 0
12 BIT 8 | BIT 0 (LSB)
11 (MSB) BIT 9 | BIT 1
1ST BYTE | 2ND BYTE

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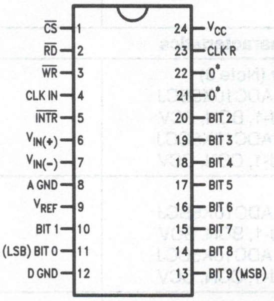
Top View

ADC1025 (10-bit parallel outputs)

Dual-In-Line Package



CS 1
RD 2
WR 3
CLK IN 4
INTR 5
VIN(+) 6
VIN(−) 7
A GND 8
VREF 9
BIT 1 10
(LSB) BIT 0 11
D GND 12
24 VCC
23 CLK R
22 0*
21 0*
20 BIT 2
19 BIT 3
18 BIT 4
17 BIT 5
16 BIT 6
15 BIT 7
14 BIT 8
13 BIT 9 (MSB)

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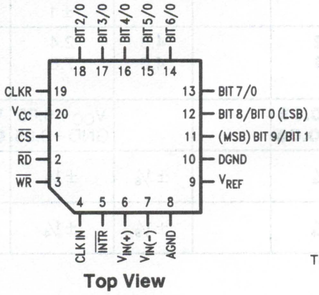
Top View

ADC1005 Molded Chip Carrier Package

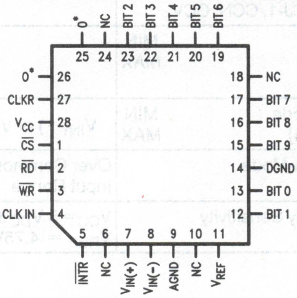


BIT 2/0
BIT 3/0
BIT 4/0
BIT 5/0
BIT 6/0
18 17 16 15 14
CLKR 19
VCC 20
CS 1
RD 2
WR 3
13 BIT 7/0
12 BIT 8/BIT 0 (LSB)
11 (MSB) BIT 9/BIT 1
10 DGND
9 VREF
4 5 6 7 8
CLK IN
INTR
VIN(+)
VIN(−)
AGND

TL/H/5261–19

Top View

ADC1025 Molded Chip Carrier Package



0*
NC
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
25 24 23 22 21 20 19
0* 26
CLKR 27
VCC 28
CS 1
RD 2
WR 3
CLK IN 4
18 NC
17 BIT 7
16 BIT 8
15 BIT 9
14 DGND
13 BIT 0
12 BIT 1
5 6 7 8 9 10 11
INTR
NC
VIN(+)
VIN(−)
AGND
NC
VREF

TL/H/5261–20

Top View

*TRI-STATE® output buffers which output 0 during $\overline{RD}$

See Ordering Information

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Logic Control Inputs	−0.3V to +15V
Voltage at Other Inputs and Outputs	−0.3V to V_{CC} +0.3V
Input Current Per Pin	±5 mA
Input Current Per Package	±20 mA
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$	875 mW
Lead Temperature (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	800V

Operating Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5V to 6.0V
Temperature Range	$T_{MN} \leq T_A \leq T_{MAX}$
ADC1005BJ, ADC1005CJ ADC1025BJ, ADC1025CJ	$-55°C \leq T_A \leq +125°C$
ADC1005BCJ, ADC1005CCJ ADC1025BCJ, ADC1025CCJ	$-40°C \leq T_A \leq +85°C$
ADC1005BCJ-1, ADC1005CCJ-1 ADC1025BCJ-1, ADC1025CCJ-1 ADC1005BCN, ADC1005CCN ADC1025BCN, ADC1025CCN ADC1005BCV, ADC1005CCV ADC1025BCV, ADC1025CCV	$0°C \leq T_A \leq 70°C$

Electrical Characteristics

The following specifications apply for $V_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.8$ MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits $T_A = T_j = 25°C$.

Parameter	Conditions	ADC10X5BJ, ADC10X5BCJ ADC10X5CJ, ADC10X5CCJ			ADC10X5BCJ-1, ADC10X5CCJ-1 ADC10X5BCN, ADC10X5CCN ADC10X5BCV, ADC10X5CCV			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
Converter Characteristics								
Linearity Error (Note 3)								
ADC10X5BJ, ADC10X5BCJ			**±0.5**					LSB
ADC10X5BCJ-1, BCN, BCV						±0.5	**±0.5**	LSB
ADC10X5CJ, ADC10X5CCJ			**±1**					LSB
ADC10X5CCJ-1, CCN, CCV						±1	**±1**	LSB
Zero Error								
ADC10X5BJ, ADC10X5BCJ			**±0.5**					LSB
ADC10X5BCJ-1, BCN, BCV						±0.5	**±0.5**	LSB
ADC10X5CJ, ADC10X5CCJ			**±1**					LSB
ADC10X5CCJ-1, CCN, CCV						±1	**±1**	LSB
Fullscale Error								
ADC10X5BJ, ADC10X5BCJ			**±0.5**					LSB
ADC10X5BCJ-1, BCN, BCV						±0.5	**±0.5**	LSB
ADC10X5CJ, ADC10X5CCJ			**±1**					LSB
ADC10X5CCJ-1, CCN, CCV						±1	**±1**	LSB
Reference Input Resistance MIN		4.8	**2.2**		4.8	2.4	**2.2**	kΩ
MAX		4.8	**8.3**		4.8	7.6	**8.3**	kΩ
Common-Mode Input (Note 4) MIN	$V_{IN}(+)$ or $V_{IN}(-)$		**V_{CC}+0.05**			V_{CC}+0.05	**V_{CC}+0.05**	V
MAX			**GND−0.05**			GND−0.05	**GND−0.05**	V
DC Common-Mode Error	Over Common-Mode Input Range	±⅛	**±¼**		±⅛	±¼	**±¼**	LSB
Power Supply Sensitivity	$V_{CC} = 5 V_{DC} \pm 5\%$ $V_{REF} = 4.75V$	±⅛	**±¼**		±⅛	±¼	**±¼**	LSB

Electrical Characteristics

(Continued) The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 1.8 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits T_A = T_j = 25°C.

Parameter	Conditions	ADC10X5BJ, ADC10X5BCJ ADC10X5CJ, ADC10X5CCJ			ADC10X5BCJ-1, ADC10X5CCJ-1 ADC10X5BCN, ADC10X5CCN ADC10X5BCV, ADC10X5CCV			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
DC Characteristics								
$V_{IN(1)}$, Logical "1" Input Voltage MIN	V_{CC}=5.25V (except CLK_{IN})		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage MAX	V_{CC}=4.75V (Except CLK_{IN})		**0.8**			0.8	**0.8**	V
I_{IN}, Logical "1" Input Current MAX	V_{IN}=5.0V	0.005	**1**		0.005	1	**1**	µA
I_{IN}, Logical "0" Input Current MAX	V_{IN}=0V	−0.005	**−1**		−0.005	−1	**−1**	µA
$V_{T+(MIN)}$, Minimum CLK_{IN} Positive going Threshold Voltage		3.1	**2.7**		3.1	2.7	**2.7**	V
$V_{T(MAX)}$, Maximum CLK_{IN} Positive going Threshold Voltage		3.1	**3.5**		3.1	3.5	**3.5**	V
$V_{T-(MIN)}$, Minimum CLK_{IN} Negative going Threshold Voltage		1.8	**1.5**		1.8	1.5	**1.5**	V
$V_{T-(MAX)}$, Maximum CLK_{IN} Negative going Threshold Voltage		1.8	**2.1**		1.8	2.1	**2.1**	V
$V_{H(MIN)}$, Minimum CLK_{IN} Hysteresis (V_{T+}-V_{T-})		1.3	**0.6**		1.3	0.6	**0.6**	V
$V_{H(MAX)}$, Maximum CLK_{IN} Hysteresis (V_{T+}-V_{T-})		1.3	**2.0**		1.3	2.0	**2.0**	V
$V_{OUT(1)}$, Logical "1" Output Voltage MIN	V_{CC}=4.75V I_{OUT}=−360 µA I_{OUT}=−10 µA		 **2.4** **4.5**			 2.8 4.6	 **2.4** **4.5**	 V V
$V_{OUT(0)}$, Logical "0" Output Voltage MAX	V_{CC}=4.75V I_{OUT}=1.6 mA		**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current MAX	V_{OUT} = 0V V_{OUT} = 5V	−0.01 0.01	**3** **3**		−0.01 0.01	−0.3 0.3	**−3** **3**	µA µA
I_{SOURCE}, Output Source Current MIN	V_{OUT}=0V	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}, Output Sink Current MIN	V_{OUT}=5V	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current MAX	f_{CLK}=1.8 MHz $\overline{CS}$="1"	1.5	**3**		1.5	2.5	**3**	mA

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, t_r = t_f = 20 ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits T_A = T_j = 25°C.

Parameter	Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Limit Units
f_{CLK}, Clock Frequency MIN MAX			0.2 2.6	0.2 2.6	MHz MHz
Clock Duty Cycle MIN MAX			40 60	40 60	% %

AC Electrical Characteristics

The following specifications apply for $V_{CC} = 5V$, $V_{REF} = 5V$, $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits $T_A = T_j = 25°C$. (Continued)

Parameter		Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Limit Units
t_C, Conversion Time	MIN			80	80	$1/f_{CLK}$
	MAX			90	90	$1/f_{CLK}$
	MIN	$f_{CLK} = 1.8$ MHz		45	45	µs
	MAX	$f_{CLK} = 1.8$ MHz		50	50	µs
$t_{W(\overline{WR})L}$, Minimum $\overline{WR}$ Pulse Width		$\overline{CS} = 0$	100	150	150	ns
t_{ACC}, Access Time (Delay from falling edge of $\overline{RD}$ to Output Data Valid)		$\overline{CS} = 0$ $C_L = 100$ pF, $R_L = 2k$	170	300	300	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)		$R_L = 10k$, $C_L = 10$ pF $R_L = 2k$, $C_L = 100$ pF	125 145		200 230	ns ns
t_{WI}, t_{RI}, Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	450	ns
t_{IRS}, $\overline{INTR}$ to 1st Read Set-up Time			400	550	550	ns
C_{IN}, Capacitance of Logic Inputs			5		7.5	pF
C_{OUT}, Capacitance of Logic Outputs			5		7.5	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line which passes through the end points of the transfer characteristic.

Note 4: For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 00 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

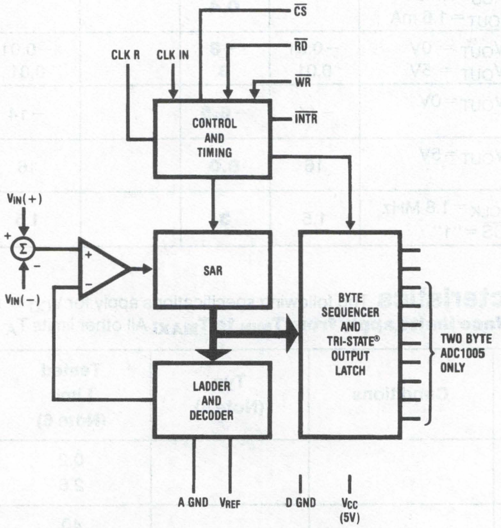
Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

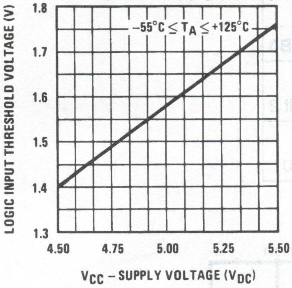
Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

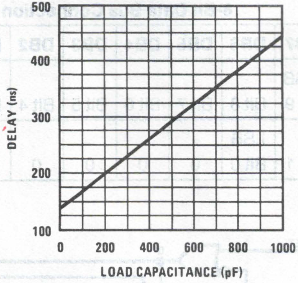
Functional Diagram

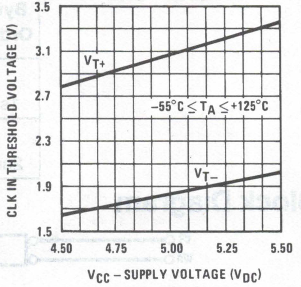


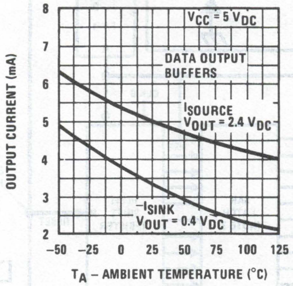
TL/H/5261-3

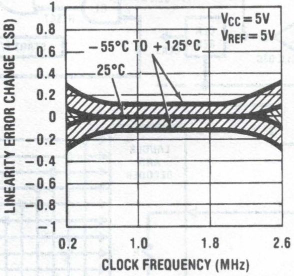
Typical Performance Characteristics


Logic Input Threshold Voltage vs Supply Voltage


Delay from Falling Edge of RD to Output Data Valid vs Load Capacitance


CLK IN Schmitt Trip Levels vs Supply Voltage

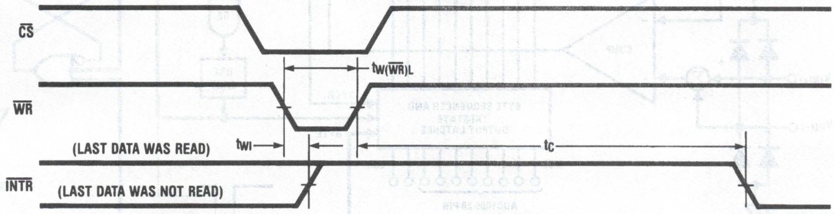

Output Current vs Temperature


Typical Linearity Error vs Clock Frequency

TL/H/5261-4

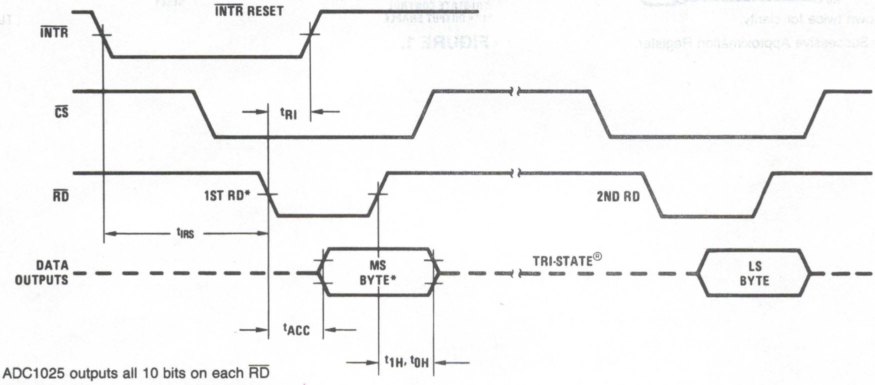
Timing Diagrams

Start Conversion


CS
WR
t_W(WR)L
t_WI
t_C
(LAST DATA WAS READ)
INTR
(LAST DATA WAS NOT READ)

TL/H/5261-5

Output Enable and Reset INTR


INTR
INTR RESET
CS
t_RI
RD
1ST RD*
2ND RD
t_IRS
DATA OUTPUTS
MS BYTE*
TRI-STATE®
LS BYTE
t_ACC
t_1H, t_0H

TL/H/5261-6

*The 24-pin ADC1025 outputs all 10 bits on each RD

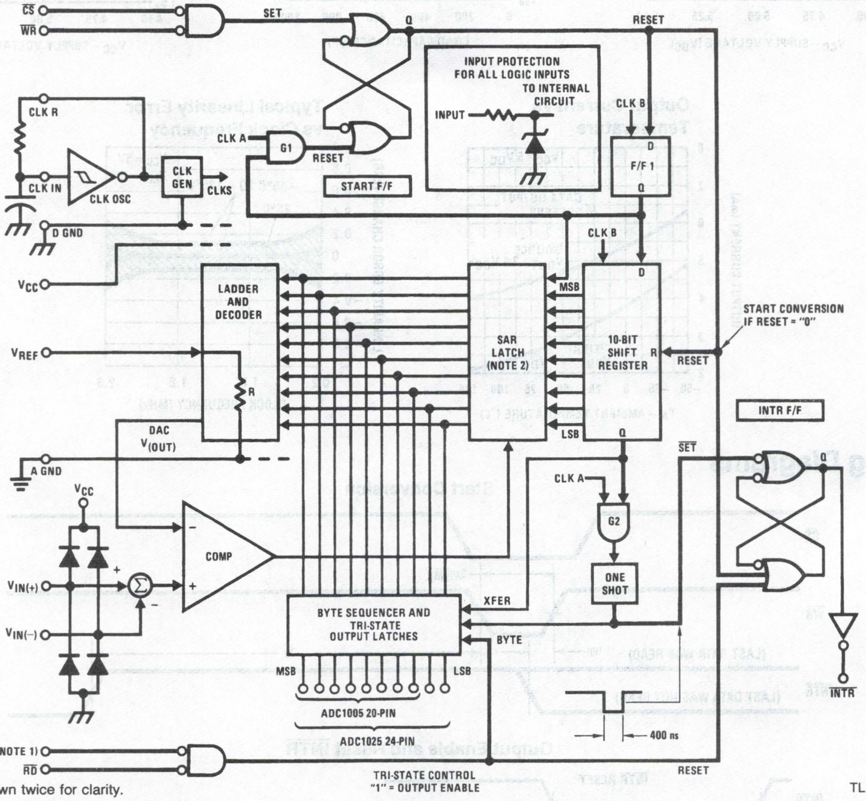
Note: All timing is measured from the 50% voltage points.

Timing Diagrams (Continued)

Byte Sequencing for the 20-Pin ADC1005

Byte Order	8-Bit Data Bus Connection							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1st	MSB Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
2nd	Bit 1	LSB Bit 0	0	0	0	0	0	0

Block Diagram


$\overline{CS}$
$\overline{WR}$
SET
Q
RESET
INPUT PROTECTION FOR ALL LOGIC INPUTS TO INTERNAL CIRCUIT
INPUT
CLK B
D
F/F 1
Q
CLK R
CLK A
G1
RESET
START F/F
CLK IN
CLK OSC
CLK GEN
CLKS
D GND
CLK B
D
V_{CC}
MSB
LADDER AND DECODER
START CONVERSION IF RESET = "0"
V_{REF}
SAR LATCH (NOTE 2)
10-BIT SHIFT REGISTER
R
RESET
R
LSB
Q
INTR F/F
DAC $V_{(OUT)}$
$\overline{SET}$
Q
A GND
CLK A
G2
V_{CC}
COMP
ONE SHOT
$V_{IN(+)}$
$V_{IN(-)}$
XFER
BYTE SEQUENCER AND TRI-STATE OUTPUT LATCHES
BYTE
MSB
LSB
ADC1005 20-PIN
ADC1025 24-PIN
400 ns
$\overline{INTR}$
$\overline{CS}$ (NOTE 1)
$\overline{RD}$
RESET
TRI-STATE CONTROL "1" = OUTPUT ENABLE

Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 1.

TL/H/5261-11

Functional Description

1.0 GENERAL OPERATION

A block diagram of the A/D converter is shown in *Figure 1* All of the inputs and outputs are shown and the major logic control paths are drawn in heavier weight lines.

1.1 Converter Operation

The ADC1005, ADC1025 use an advanced potentiometric resistive ladder network. The analog inputs, as well as the taps of this ladder network are switched into a weighted capacitor array. The output of this capacitor array is the input to a sampled data comparator. This comparator allows the successive approximation logic to match the analog input voltage $[V_{IN}(+) - V_{IN}(-)]$ to taps on the R network. The most significant bit is tested first and after 10 comparisons (80 clock cycles) a digital 10-bit binary code (all "1"s = full-scale) is transferred to an output latch.

1.2 Starting a Conversion

The conversion is initialized by taking $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 10-bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 10-bit shift register. Internal clock signals then transfer this "1" to the Q ouput of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 10-bit shift register then can have the "1" clocked in, allowing the conversion process to continue. If the set signal were still present, this reset pulse would have no effect and the 10-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals. The converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

To summarize, on the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start after at least one of these inputs makes a low-to-high transition.*

1.3 Output Control

After the "1" is clocked through the 10-bit shift register (which completes the SAR search) it causes the new digital word to transfer to the TRI-STATE output latches. When the XFER signal makes a high-to-low transition the one shot fires, setting the INTR F/F. An inverting buffer then supplies the $\overline{INTR}$ output signal.

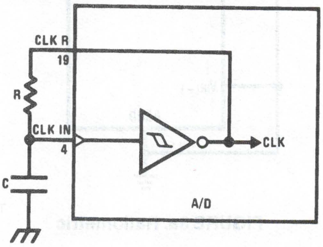
Note that this $\overline{SET}$ control of the INTR F/F remains low for approximately 400 ns. If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low) the $\overline{INTR}$ output will still signal the end of the conversion (by a high-to-low transition). This is because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled.

1.4 Free-Running and Self-Clocking Modes

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to ensure start up.

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN makes use of a Schmitt trigger as shown in *Figure 2.*



TL/H/5261-12

$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

FIGURE 2. Self-Clocking the A/D

2.0 REFERENCE VOLTAGE

The voltage applied to the reference input of these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 1024 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 4.8 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 3a*) the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system references as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 3b*), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be small to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout, and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/1024$).

Functional Description (Continued)

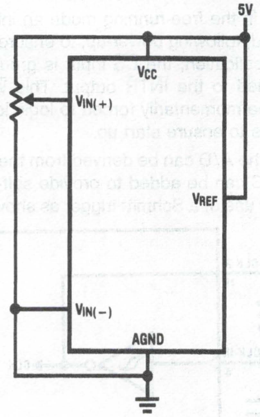


FIGURE 3a. Ratiometric

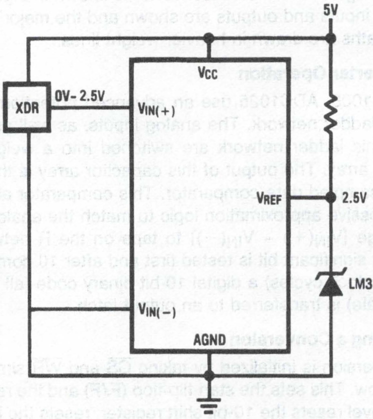


FIGURE 3b. Absolute with a Reduced Span

3.0 THE ANALOG INPUTS

3.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential inputs of these converters reduce the effects of common-mode input noise, which is defined as noise common to both selected "+" and "−" inputs (60 Hz is most typical). The time interval between sampling the "+" input and the "−" input is half of an internal clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal, this error is:

$$V_{ERROR(MAX)} = V_{PEAK} (2\pi f_{CM}) \times \frac{4}{f_{CLK}}$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value and f_{CLK} is the clock frequency at the CLK IN pin.

For a 60 Hz common-mode signal to generate a 1/4 LSB error (1.2 mV) with the converter running at 1.8 MHz, its peak value would have to be 1.46V. A common-mode signal this large is much greater than that generally found in data aquisition systems.

3.2 Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the clock rising edges during the conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period.

3.3 Input Bypass Capacitors

Bypass capacitors at the inputs will average the current spikes noted in 3.2 and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full scale. For continuous conversions with a 1.8 MHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the V_{REF} pin* for high resistance sources (>1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a linear function of the differential input voltage.

3.4 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* if the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications (≤0.1 kΩ) a 4700 pF bypass capacitor at the inputs will prevent pickup due to series lead induction of a long wire. A 100Ω series resistor can be used to isolate this capacitor – both the R and the C are placed outside the feedback loop – from the output of an op amp, if used.

3.5 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 1 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, can reduce system noise pickup but can create analog scale errors. See section 3.2, 3.3, and 3.4 if input filtering is to be used.

Functional Description (Continued)

4.0 OFFSET AND REFERENCE ADJUSTMENT

4.1 Zero Offset

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V(−) input and applying a small magnitude positive voltage to the V(+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 00 0000 0000 to 00 0000 0001 and the ideal 1/2 LSB value (1/2 LSB = 2.45 mV for V_{REF} = 5.0 V_{DC}).

The zero of the A/D normally does not require adjustment. However, for cases where $V_{IN(MIN)}$ is not ground and in reduced span applications ($V_{REF} < 5V$), an offset adjustment may be desired. The converter can be made to output an all zero digital code for an arbitrary input by biasing the A/D's $V_{IN}(-)$ input at that voltage. This utilizes the differential input operation of the A/D.

4.2 Full Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code that is just changing from 11 1111 1110 to 11 1111 1111.

4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus 1/2 LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/1024) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 000_{HEX} 001_{HEX} code transition.

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input given by:

$$V_{IN}(+)\ \text{FS adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{1024}\right]$$

where V_{MAX} = the high end of the analog input range and V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced).

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from $3FF_{HEX}$ to $3FE_{HEX}$. This completes the adjustment procedure.

For an example see the Zero-Shift and Span-Adjust circuit below.

5.0 POWER SUPPLIES

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and the other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to the digital ground. Any V_{REF} bypass capacitors, analog input filters capacitors, or input signal shielding should be returned to the analog ground point.

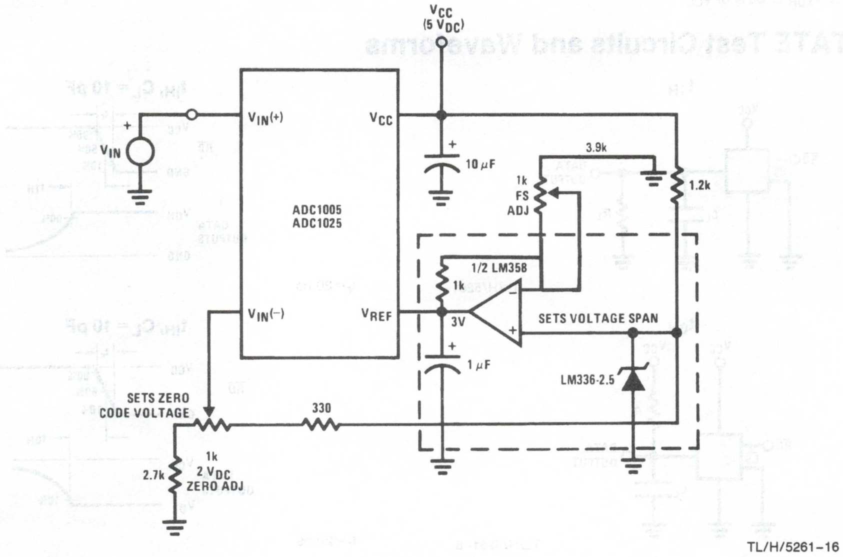
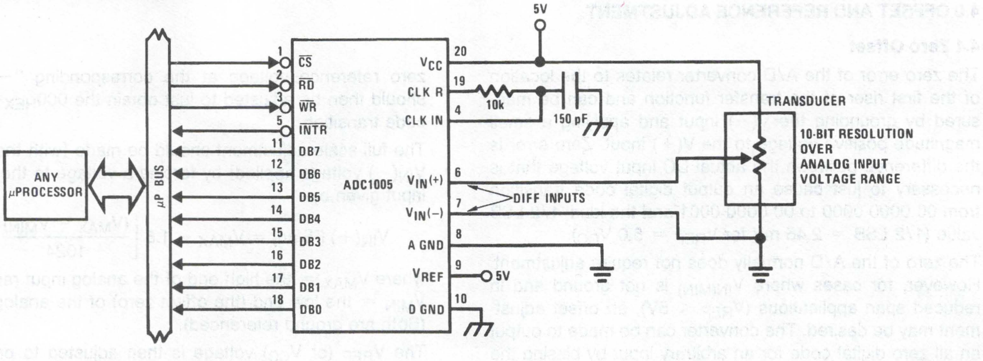


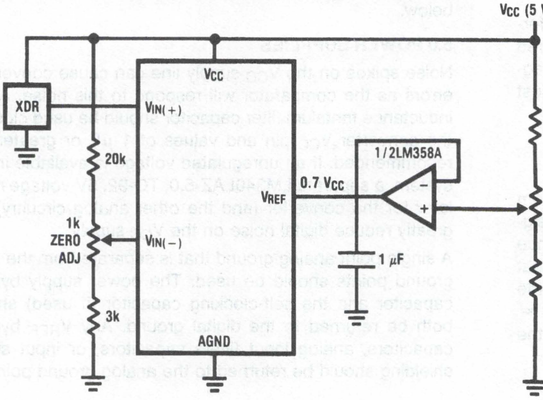
Figure 4. Zero-Shift and Span-Adjust (2V ≤ V_{IN} ≤ 5V)

Typical Applications


5V
1 CS
2 RD
3 WR
5 INTR
11 DB7
12 DB6
13 DB5
14 DB4
15 DB3
16 DB2
17 DB1
18 DB0
ANY μPROCESSOR
μP BUS
ADC1005
20 VCC
19 CLK R
4 CLK IN
6 VIN(+)
7 VIN(−)
8 A GND
9 VREF
10 D GND
10k
150 pF
TRANSDUCER
10-BIT RESOLUTION OVER ANALOG INPUT VOLTAGE RANGE
DIFF INPUTS
5V

TL/H/5261-13

Operating with Ratiometric Transducers

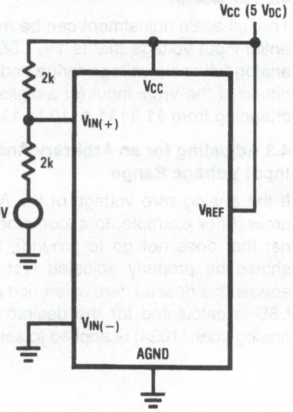

VCC (5 VDC)
XDR
20k
1k ZERO ADJ
3k
VCC
VIN(+)
VREF
VIN(−)
AGND
1/2LM358A
0.7 VCC
1 μF
3.3k
1k 10 TURN TRIM POT
7.5k

$V_{IN}(-) = 0.15\ V_{CC}$

$15\%\ \text{of}\ V_{CC} \le V_{XDR} \le 85\%\ \text{of}\ V_{CC}$

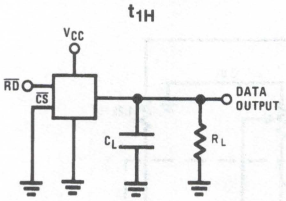
TL/H/5261-14

Handling ±5V Analog Inputs

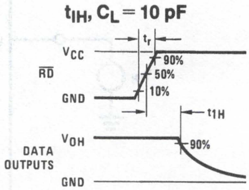

VCC (5 VDC)
2k
2k
±5V
VCC
VIN(+)
VREF
VIN(−)
AGND

TL/H/5261-15

TRI-STATE Test Circuits and Waveforms

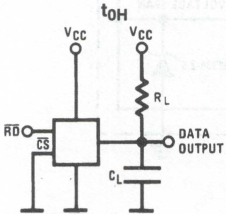

t1H
VCC
RD
CS
DATA OUTPUT
CL
RL

TL/H/5261-7

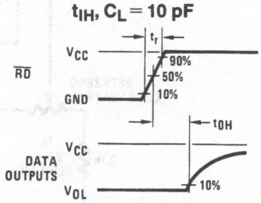

t1H, CL = 10 pF
VCC
RD
GND
tr
90%
50%
10%
t1H
VOH
90%
DATA OUTPUTS
GND

tr = 20 ns

TL/H/5261-9


t0H
VCC
VCC
RL
RD
CS
DATA OUTPUT
CL

TL/H/5261-8


t0H, CL = 10 pF
VCC
RD
GND
tr
90%
50%
10%
t0H
VCC
DATA OUTPUTS
VOL
10%

tr = 20 ns

TL/H/5261-10

Ordering Information

Part Number	Package Outline	Temperature Range	Linearity Error
ADC1005BCN	N20A	0°C to +70°C	±½ LSB
ADC1025BCN	N24C		
ADC1005BCV	V20A		
ADC1025BCV	V28A		
ADC1005BCJ-1	J20A		
ADC1025BCJ-1	J24F		
ADC1005BCJ	J20A	−40°C to +85°C	
ADC1025BCJ	J24F		
ADC1005BJ	J20A	−55°C to +125°C	
ADC1025BJ	J24F		

Part Number	Package Outline	Temperature Range	Linearity Error
ADC1005CCN	N20A	0°C to +70°C	±1 LSB
ADC1025CCN	N24C		
ADC1005CCV	V20A		
ADC1025CCV	V28A		
ADC1005CCJ-1	J20A		
ADC1025CCJ-1	J24F		
ADC1005CCJ	J20A	−40°C to +85°C	
ADC1025CCJ	J24F		
ADC1005CJ	J20A	−55°C to +125°C	
ADC1025CJ	J24F		

National Semiconductor Corporation

ADC1205/ADC1225 12-Bit Plus Sign μP Compatible A/D Converters

General Description

The ADC1205 and ADC1225 are CMOS, 12-bit plus sign successive approximation A/D converters. The 24-pin ADC1205 outputs the 13-bit data result in two 8-bit bytes, formatted high-byte first with sign extended. The 28-pin ADC1225 outputs a 13-bit word in parallel for direct interface to a 16-bit data bus.

Negative numbers are represented in 2's complement data format. All digital signals are fully TTL and MOS compatible.

A unipolar input (0V to 5V) can be accommodated with a single 5V supply, while a bipolar input (−5V to +5V) requires the addition of a 5V negative supply.

The ADC1205B and ADC1225B have a maximum non-linearity over temperature of 0.012% of Full Scale, and the ADC1205C and ADC1225C have a maximum non-linearity of 0.0224% of Full Scale.

Key Specifications

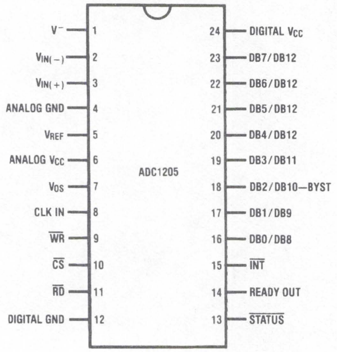
- Resolution—12 bits plus sign
- Linearity Error—±½ LSB and ±1 LSB
- Conversion Time—100 μs

Features

- Compatible with all μPs
- True differential analog voltage inputs
- 0V to 5V analog voltage range with single 5V supply
- TTL/MOS input/output compatible
- Low power—25 mW max
- Standard 24-pin or 28-pin DIP

Connection and Functional Diagrams

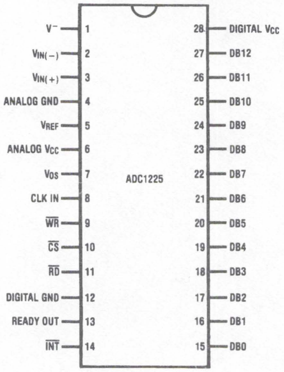
Dual-In-Line Package


V⁻ 1
VIN(−) 2
VIN(+) 3
ANALOG GND 4
VREF 5
ANALOG Vcc 6
VOS 7
CLK IN 8
WR 9
CS 10
RD 11
DIGITAL GND 12
ADC1205
24 DIGITAL Vcc
23 DB7/DB12
22 DB6/DB12
21 DB5/DB12
20 DB4/DB12
19 DB3/DB11
18 DB2/DB10—BYST
17 DB1/DB9
16 DB0/DB8
15 INT
14 READY OUT
13 STATUS

Top View

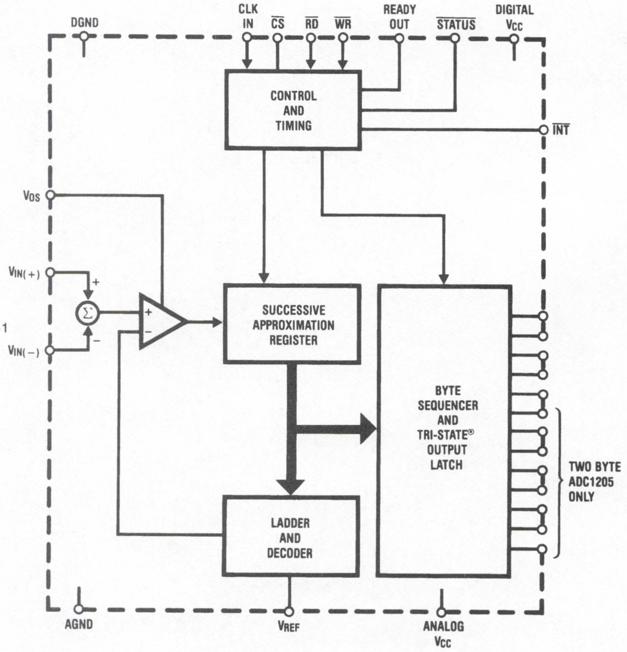
TL/H/5676-1

Dual-In-Line Package


V⁻ 1
VIN(−) 2
VIN(+) 3
ANALOG GND 4
VREF 5
ANALOG Vcc 6
VOS 7
CLK IN 8
WR 9
CS 10
RD 11
DIGITAL GND 12
READY OUT 13
INT 14
ADC1225
28 DIGITAL Vcc
27 DB12
26 DB11
25 DB10
24 DB9
23 DB8
22 DB7
21 DB6
20 DB5
19 DB4
18 DB3
17 DB2
16 DB1
15 DB0

Top View

TL/H/5676-2


DGND
CLK IN
CS
RD
WR
READY OUT
STATUS
DIGITAL Vcc
CONTROL AND TIMING
INT
VOS
VIN(+)
VIN(−)
+
−
Σ
SUCCESSIVE APPROXIMATION REGISTER
BYTE SEQUENCER AND TRI-STATE® OUTPUT LATCH
TWO BYTE ADC1205 ONLY
LADDER AND DECODER
AGND
VREF
ANALOG Vcc

TL/H/5676-3

See Ordering Information

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (DV_{CC} and AV_{CC})	6.5V
Negative Supply Voltage (V^-)	−15V to GND
Logic Control Inputs	−0.3V to +15V
Voltage at Analog Inputs [$V_{IN(+)}$, $V_{IN(-)}$]	$(V^-)-0.3V$ to $V_{CC}+0.3V$
Voltage at All Outputs, V_{REF}, V_{OS}	−0.3V to $(V_{CC}+0.3V)$
Input Current per Pin	±5mA
Input Current per Package	±20mA
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A=25°C$	875 mW
Lead Temp. (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 12)	800V

Operating Conditions (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1205BCJ, ADC1205CCJ ADC1225BCJ, ADC1225CCJ	$-40°C \le T_A \le +85°C$
ADC1205BCJ-1, ADC1205CCJ-1 ADC1225BCJ-1, ADC1225CCJ-1	$0°C \le T_A \le 70°C$
Supply Voltage (DV_{CC} and AV_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Negative Supply Voltage (V^-)	−15V to GND

Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.0$ MHz, $V^- = -5V$ for bipolar input range, or $V^- = GND$ for unipolar input range unless otherwise specified. Bipolar input range is defined as $-5.05V \le V_{IN(+)} \le 5.05V$; $-5.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. Unipolar input range is defined as $-0.05V \le V_{IN(+)} \le 5.05V$; $-0.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A = T_J = 25°C$ (Notes 3, 4, 5, 6, 7).

Parameter	Conditions	ADC1205BCJ, ADC1205CCJ ADC1225BCJ, ADC1225CCJ			ADC1205BCJ-1, ADC1205CCJ-1 ADC1225BCJ-1, ADC1225CCJ-1			Limit Units
		Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CONVERTER CHARACTERISTICS								
Linearity Error	Unipolar Input Range (Note 11)							
ADC1205BCJ, ADC1225BCJ			**±½**					LSB
ADC1205BCJ-1, ADC1225BCJ-1						±½	**±½**	LSB
ADC1205CCJ, ADC1225CCJ			**±1**					LSB
ADC1205CCJ-1, ADC1225CCJ-1						±1	**±1**	LSB
Unadjusted Zero Error	Unipolar Input Range		**±2**			±2	**±2**	LSB
Unadjusted Positive and Negative Full-Scale Error	Unipolar Input Range		**±30**			±30	**±30**	LSB
Negative Full-Scale Error	Unipolar Input Range, Full Scale Adj. to Zero			**±½**			**±½**	LSB
Linearity Error	Bipolar Input Range (Note 11)							
ADC1205BCJ, ADC1225BCJ			**±1.5**					LSB
ADC1205BCJ-1, ADC1225BCJ-1						±1.5	**±1.5**	LSB
ADC1205CCJ, ADC1225CCJ			**±2**					LSB
ADC1205CCJ-1, ADC1225CCJ-1						±2	**±2**	LSB
Unadjusted Zero Error	Bipolar Input Range		**±2**			±2	**±2**	LSB
Unadjusted Positive and Negative Full-Scale Error	Bipolar Input Range		**±30**			±30	**±30**	LSB
Negative Full-Scale Error	Bipolar Input Range, Full Scale Adj. to Zero		**±2**			±2	**±2**	LSB
Maximum Gain Temperature Coefficient		6		**15**	6		**15**	ppm/°C
Maximum Offset Temperature Coefficient		0.5		**1.5**	0.5		**1.5**	ppm/°C
Minimum V_{REF} Input Resistance		4.0	**2**		4.0	2	**2**	kΩ
Maximum V_{REF} Input Resistance		4.0	**8**		4.0	8	**8**	kΩ

Electrical Characteristics (Continued)

The following specifications apply for $DV_{CC} = AV_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.0$ MHz, $V^- = -5V$ for bipolar input range, or $V^- = GND$ for unipolar input range unless otherwise specified. Bipolar input range is defined as $-5.05V \le V_{IN(+)} \le 5.05V$; $-5.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. Unipolar input range is defined as $-0.05V \le V_{IN(+)} \le 5.05V$; $-0.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$ (Notes 3, 4, 5, 6, 7).

Parameter	Conditions	ADC1205BCJ, ADC1205CCJ ADC1225BCJ, ADC1225CCJ			ADC1205BCJ-1, ADC1205CCJ-1 ADC1225BCJ-1, ADC1225CCJ-1			Limit Units
		Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CONVERTER CHARACTERISTICS (Continued)								
Minimum Analog Input Voltage	Unipolar Input Range		**GND-0.05**			GND-0.05	**GND-0.05**	V
	Bipolar Input Range		**$-V_{CC}-0.05$**			$-V_C-0.05$	**$-V_{CC}-0.05$**	V
Maximum Analog Input Voltage	Unipolar Input Range		**$V_{CC}+0.05$**			$V_{CC}+0.05$	**$V_{CC}+0.05$**	V
	Bipolar Input Range	**$V_{CC}+0.05$**				$V_{CC}+0.05$	**$V_{CC}+0.05$**	V
DC Common-Mode Error		±1/8	±1/2		±1/8	±1/2	±1/2	LSB
Power Supply Sensitivity	$AV_{CC}=DV_{CC}=5V\pm5\%$, $V^-=-5V\pm5\%$							
Zero Error			±3/4			±3/4	±3/4	LSB
Positive and Negative Full-Scale Error			±3/4			±3/4	±3/4	LSB
Linearity Error			±1/4			±1/4	±1/4	LSB
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	$V_{CC}=5.25V$, All Inputs except CLK IN		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	$V_{CC}=4.75V$, All Inputs except CLK IN		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	$V_{IN}=5V$	0.005	**1**		0.005		**1**	μA
$I_{IN(0)}$, Logical "0" Input Current (Max)	$V_{IN}=0V$	−0.005	**−1**		−0.005		**−1**	μA
V_T+ (Min), Minimum Positive-Going Threshold Voltage	CLK IN	3.1	**2.7**		3.1	2.7	**2.7**	V
V_T+ (Max), Maximum Positive-Going Threshold Voltage	CLK IN	3.1	**3.5**		3.1	3.5	**3.5**	V
V_T- (Min), Minimum Negative-Going Threshold Voltage	CLK IN	1.8	**1.4**		1.8	1.4	**1.4**	V
V_T- (Max), Maximum Negative-Going Threshold Voltage	CLK IN	1.8	**2.1**		1.8	2.1	**2.1**	V
V_H(Min), Minimum Hysteresis $[V_T+(Min)-V_T-(Max)]$	CLK IN	1.3	**0.6**		1.3	0.6	**0.6**	V
V_H(Max), Maximum Hysteresis $[V_T+(Max)-V_T-(Min)]$	CLK IN	1.3	**2.1**		1.3	2.1	**2.1**	V

Electrical Characteristics (Continued)

The following specifications apply for $DV_{CC} = AV_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.0$ MHz, $V^- = -5V$ for bipolar input range, or $V^- = GND$ for unipolar input range unless otherwise specified. Bipolar input range is defined as $-5.05V \leq V_{IN(+)} \leq 5.05V$; $-5.05V \leq V_{IN(-)} \leq 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \leq 5.05V$. Unipolar input range is defined as $-0.05V \leq V_{IN(+)} \leq 5.05V$; $-0.05V \leq V_{IN(-)} \leq 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \leq 5.05V$. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$ (Notes 3, 4, 5, 6, 7).

Parameter	Conditions	ADC1205BCJ, ADC1205CCJ ADC1225BCJ, ADC1225CCJ			ADC1205BCJ-1, ADC1205CCJ-1 ADC1225BCJ-1, ADC1225CCJ-1			Limit Units
		Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
DIGITAL AND DC CHARACTERISTICS (Continued)								
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	$V_{CC} = 4.75V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		 **2.4** **4.5**			 2.4 4.5	 **2.4** **4.5**	 V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	$V_{CC} = 4.75V$ $I_{OUT} = 1.6$ mA		**0.4**			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Leakage Current (Max)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−0.01 0.01	**−3** **3**		−0.01 0.01	−0.3 0.3	**−3** **3**	µA µA
I_{SOURCE}, Output Source Current (Min)	$V_{OUT} = 0V$	−12	**−6.0**		−12	−7.0	**−6.0**	mA
I_{SINK}, Output Sink Current (Min)	$V_{OUT} = 5V$	16	**8.0**		16	9.0	**8.0**	mA
DI_{CC}, DV_{CC} Supply Current (Max)	$f_{CLK} = 1$ MHz, $\overline{CS} = 1$	1	**3**		1	2.5	**3**	mA
AI_{CC}, AV_{CC} Supply Current (Max)	$f_{CLK} = 1$ MHz, $\overline{CS} = 1$	1	**3**		1	2.5	**3**	mA
I^-, V^- Supply Current (Max)	$f_{CLK} = 1$ MHz, $\overline{CS} = 1$	10	**100**		10	100	**100**	µA

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = 5.0V$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise specified.

Parameter		Conditions	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Limit Units
f_{CLK}, Clock Frequency	MIN MAX		1.0 1.0	0.3 1.5		MHz MHz
Clock Duty Cycle	MIN MAX				40 60	% %
T_C, Conversion Time	MIN MAX MIN MAX	 $f_{CLK} = 1.0$ MHz $f_{CLK} = 1.0$ MHz			108 109 108 109	$1/f_{CLK}$ $1/f_{CLK}$ µs µs
$t_{W(\overline{WR})L}$, $\overline{WR}$ Pulse Width	MAX		220		350	ns
t_{ACC}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid) (Max)		$C_L = 100$ pF	210		340	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State) (Max)		$R_L = 2k$, $C_L = 100$ pF	170		290	ns
$t_{PD(READYOUT)}$, $\overline{RD}$ or $\overline{WR}$ to READYOUT Delay (Max)			250		400	ns
$t_{PD(INT)}$, $\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$ (Max)			250		400	ns

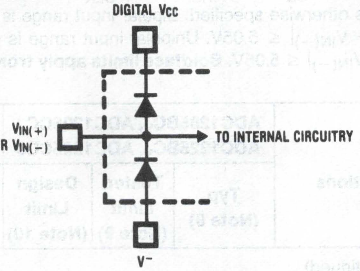
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: All voltages are measured with respect to ground, unless otherwise specified.

Note 3: A parasitic zener diode exists internally from AV_{CC} and DV_{CC} to ground. This parasitic zener has a typical breakdown voltage of 7 V_{DC}.

AC Electrical Characteristics (Continued)

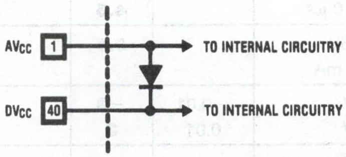
Note 4: Two on-chip diodes are tied to each analog input as shown below.


DIGITAL Vcc
VIN(+) OR VIN(−)
TO INTERNAL CIRCUITRY
V−

TL/H/5676-4

Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV. This means that if AV_{CC} and DV_{CC} are minimum (4.75 V_{DC}) and V^- is minimum (−4.75V_{DC}), full-scale must be ≤ 4.8V_{DC}.

Note 5: A diode exists between analog V_{CC} and digital V_C.


AVCC
1
TO INTERNAL CIRCUITRY
DVCC
40
TO INTERNAL CIRCUITRY

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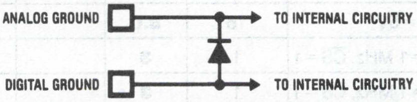
To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.

Note 6: A diode exists between analog ground and digital ground.


ANALOG GROUND
TO INTERNAL CIRCUITRY
DIGITAL GROUND
TO INTERNAL CIRCUITRY

TL/H/5676-21

To guarantee accuracy, it is required that the analog ground and digital ground be connected together externally.

Note 7: Accuracy is guaranteed at f_{CLK} = 1.0 MHz. At higher clock frequencies accuracy may degrade.

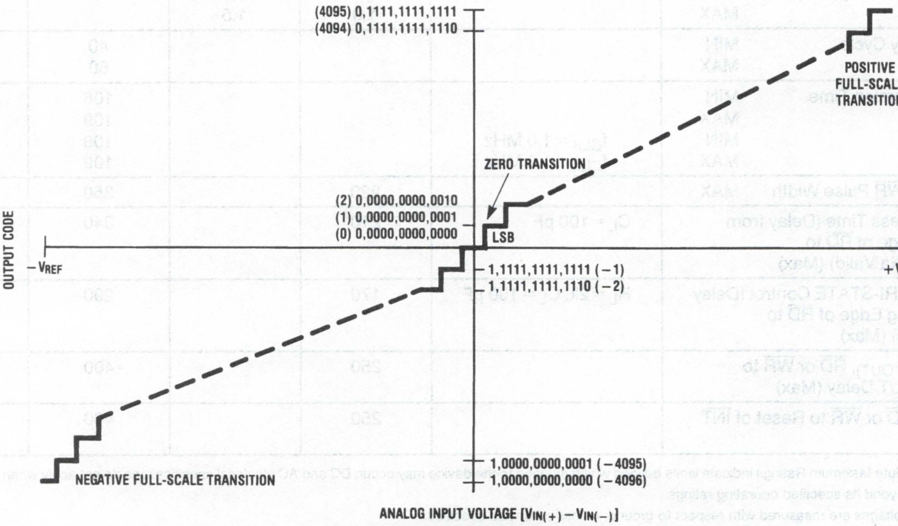
Note 8: Typicals are at 25°C and represent most likely parametric norm.

Note 9: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

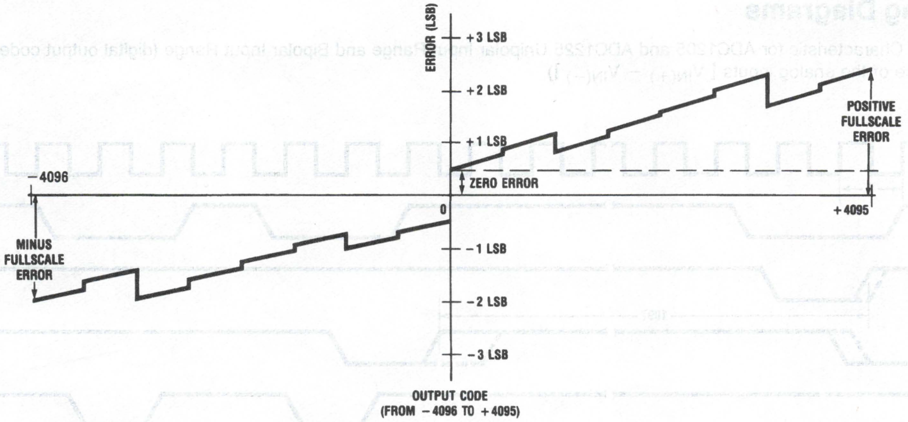
Note 11: Linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line which passes through positive full scale and zero, after adjusting zero error. (See *Figures 1b* and *1c*).

Note 12: Human body model; 100 pF discharged through a 1.5 kΩ resistor.



TL/H/5676-8

FIGURE 1a. Transfer Characteristic



TL/H/5676-22

FIGURE 1b. Simplified Error Curve vs. Output Code Without Zero and Fullscale Adjustment

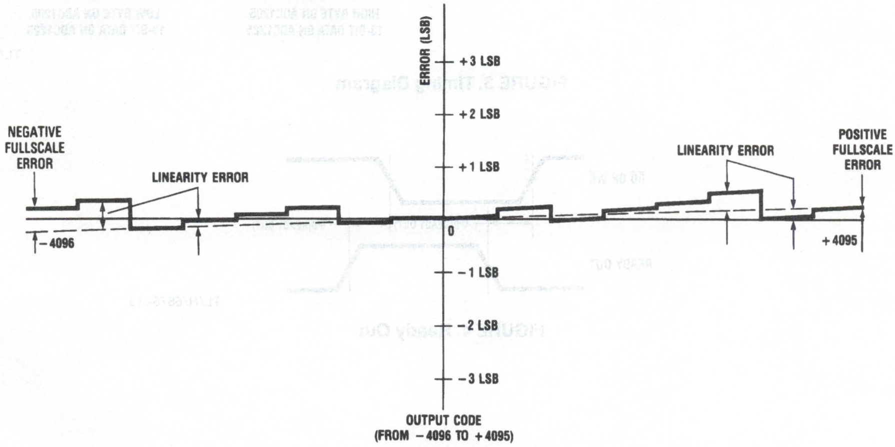


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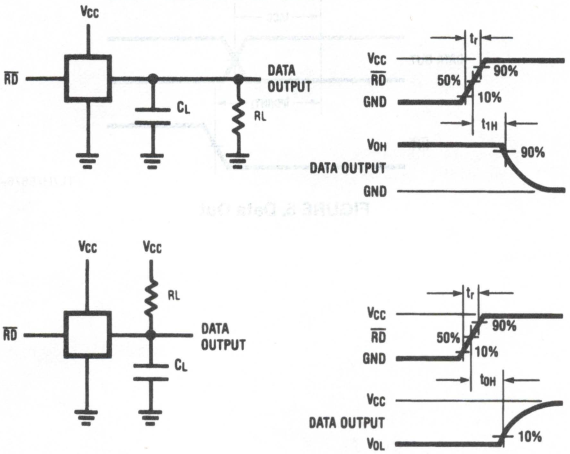
FIGURE 1c. Simplified Error Curve vs. Output Code after Zero/Fullscale Adjustment


Vcc
RD
DATA OUTPUT
CL
RL
tr
Vcc
RD
GND
50%
90%
10%
t1H
VOH
DATA OUTPUT
GND
90%
Vcc
Vcc
RL
RD
DATA OUTPUT
CL
tr
Vcc
RD
GND
50%
90%
10%
t0H
Vcc
DATA OUTPUT
VOL
10%

TL/H/5676-7

FIGURE 2. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

Transfer Characteristic for ADC1205 and ADC1225 Unipolar Input Range and Bipolar Input Range (digital output codes vs the difference of the analog inputs [$V_{IN(+)} - V_{IN(-)}$])

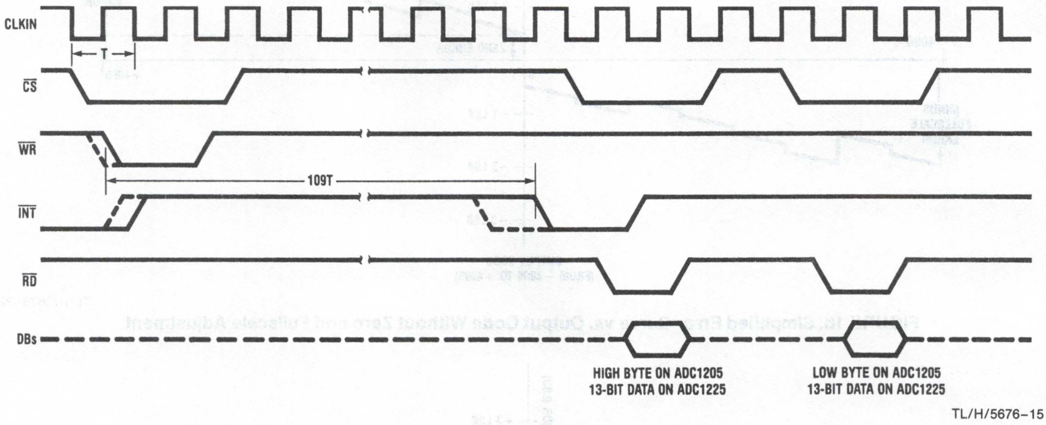

CLKIN
T
CS
WR
109T
INT
RD
DBs
HIGH BYTE ON ADC1205
13-BIT DATA ON ADC1225
LOW BYTE ON ADC1205
13-BIT DATA ON ADC1225
TL/H/5676-15

FIGURE 3. Timing Diagram

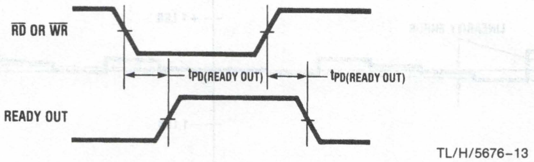

RD OR WR
tPD(READY OUT)
tPD(READY OUT)
READY OUT
TL/H/5676-13

FIGURE 4. Ready Out

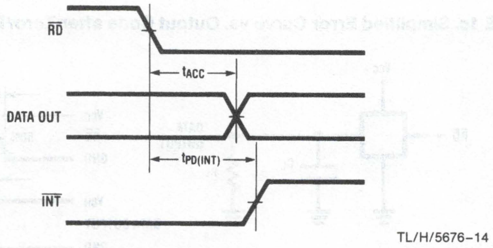

RD
tACC
DATA OUT
tPD(INT)
INT
TL/H/5676-14

FIGURE 5. Data Out

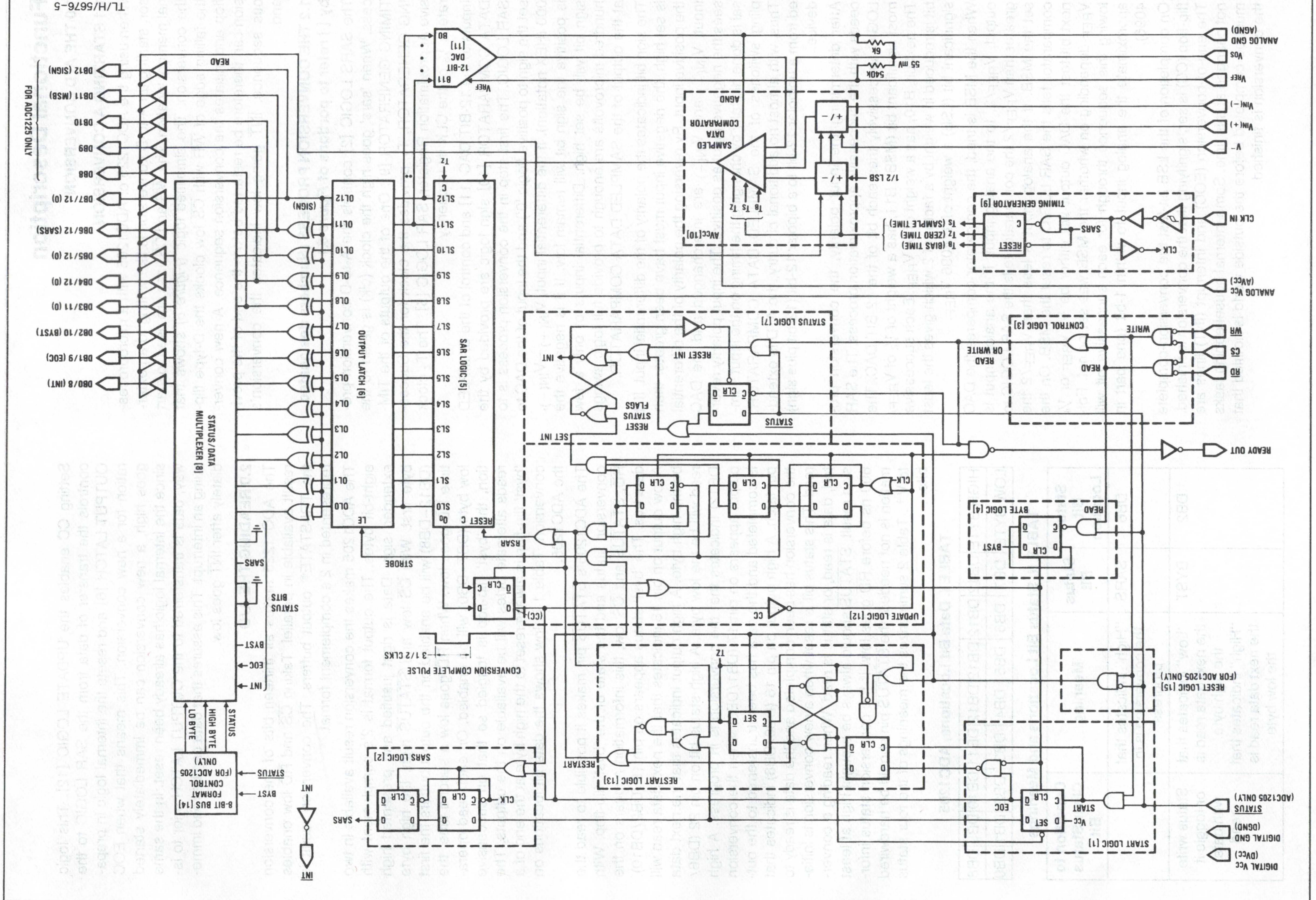

DB0/8 (INT)
DB1/9 (EOC)
DB2/10 (BYST)
DB3/11 (0)
DB4/12 (0)
DB5/12 (0)
DB6/12 (SARS)
DB7/12 (0)
DB8
DB9
DB10
DB11 (MSB)
DB12 (SIGN)
FOR ADC1225 ONLY
TL/H/5676–5
READ
STATUS/DATA MULTIPLEXER [8]
OUTPUT LATCH [6]
OL0
OL1
OL2
OL3
OL4
OL5
OL6
OL7
OL8
OL9
OL10
OL11
OL12
(SIGN)
LE
SAR LOGIC [5]
RESET C Q0
SL0
SL1
SL2
SL3
SL4
SL5
SL6
SL7
SL8
SL9
SL10
SL11
SL12
C
TZ
VREF
B11
12-BIT DAC [11]
B0
SAMPLED DATA COMPARATOR
AGND
AVCC[10]
TB TS TZ
1/2 LSB
+/−
540K
6K
55 mV
TIMING GENERATOR [9]
RESET
C
SARS
CLK
TB (BIAS TIME)
TZ (ZERO TIME)
TS (SAMPLE TIME)
STATUS LOGIC [7]
STATUS
RESET STATUS FLAGS
RESET INT
SET INT
INT
CONTROL LOGIC [3]
READ OR WRITE
WRITE
READ
BYTE LOGIC [4]
BYST
UPDATE LOGIC [12]
CC
(CC)
CLK
RSAR
STROBE
CONVERSION COMPLETE PULSE
3 1/2 CLKS
RESTART LOGIC [13]
RESTART
SET
CLR
D Q
RESET LOGIC [15] (FOR ADC1205 ONLY)
START LOGIC [1]
START
EOC
VCC
SARS LOGIC [2]
SARS
STATUS BITS
BYST
EOC
INT
LO BYTE
HIGH BYTE
STATUS
8-BIT BUS [14] FORMAT CONTROL (FOR ADC1205 ONLY)
BYST
STATUS
INT
READY OUT
RD
CS
WR
CLK IN
V−
VIN(+)
VIN(−)
VREF
VOS
ANALOG GND (AGND)
ANALOG VCC (AVCC)
DIGITAL VCC (DVCC)
DIGITAL GND (DGND)
STATUS (ADC1205 ONLY)

FIGURE 6. Functional Block Diagram

Functional Description

1.0 THE A/D CONVERSION

1.1 STARTING A CONVERSION

When using the ADC1225 or ADC1205 with a microprocessor, starting an A-to-D conversion is like writing to an external memory location. The $\overline{WR}$ and $\overline{CS}$ lines are used to start the conversion. The simplified logic (*Figure 6*) shows that the falling edge of $\overline{WR}$ with $\overline{CS}$ low clocks the D-type flip-flop and initiates the conversion sequence. A new conversion can therefore be restarted before the end of the previous sequence. $\overline{INT}$ going low indicates the conversion's end.

1.2 THE CONVERSION PROCESS (Numbers designated by [ ] refer to portions of *Figure 6.*)

The SARS LOGIC [2] controls the A-to-D conversion process. When 'sars' goes high the clock (clk) is gated to the TIMING GENERATOR [9]. One of the outputs of the TIMING GENERATOR, T_Z, provides the clock for the Successive Approximation Register, SAR LOGIC [5]. The T_Z clock rate is ⅛ of the CLK IN frequency.

Inputs to the 12-BIT DAC [11] and control of the SAMPLED DATA COMPARATOR [10] sign logic are provided by the SAR LOGIC. The first step in the conversion process is to set the sign to positive (logic '0') and the input of the DAC to 000 (HEX notation). If the differential input, $V_{IN(+)}-V_{IN(-)}$, is positive the sign bit will remain low. If it is negative the sign bit will be set high. Differential inputs of only a few hundred microvolts are enough to provide full logic swings at the output of the SAMPLED DATA COMPARATOR.

The sign bit indicates the polarity of the differential input. If it is set high, the negative input must have been greater than the positive input. By reversing the polarity of the differential input, $V_{IN(+)}$ and $V_{IN(-)}$ are interchanged and the DAC sees the negative input as positive. The input polarity reversal is done digitally by changing the timing on the input sampling switches of the SAMPLED DATA COMPARATOR. Thus, with almost no additional circuitry, the A/D is extended from a unipolar 12-bit to a bipolar 12-bit (12-bit plus sign) device.

After determining the input polarity, the conversion proceeds with the successive approximation process. The SAR LOGIC successively tries each bit of the 12-BIT DAC. The most significant bit (MSB), B11, has a weight of ½ of V_{REF}. The next bit, B10, has a weight of ¼ V_{REF}. Each successive bit is reduced in weight by a factor of 2 which gives the least significant bit (LSB) a weight of 1/4096 V_{REF}.

When the MSB is tried, the comparator compares the DAC output, $V_{REF}/2$, to the analog input. If the analog input is greater than $V_{REF}/2$ the comparator tells the SAR LOGIC to set the MSB. If the analog input is less than $V_{REF}/2$ the comparator tells the SAR LOGIC to reset the MSB. On the next bit-test the DAC output will either be ¾ V_{REF} or ¼ V_{REF} depending on whether the MSB was set or not. Following this sequence through for each successive bit will approximate the analog input to within 1-bit (one part in 4096).

On completion of the LSB bit-test the conversion-complete flip-flop (CC) is set, signifying that the conversion is finished. The end-of-conversion (EOC) and interrupt ($\overline{INT}$) lines are not changed at this time. Some internal housekeeping tasks must be completed before the outside world is notified that the conversion is finished.

Setting CC enables the UPDATE LOGIC [12]. This logic controls the transfer of data from the SAR LOGIC to the OUTPUT LATCH [6] and resets the internal logic in preparation for a new conversion. This means that when EOC goes high, a new conversion can be immediately started since the internal logic has already been reset. In the same way, data is transferred to the OUTPUT LATCH prior to issuing an interrupt. This assures that data can be read immediately after $\overline{INT}$ goes low.

2.0 READING THE A/D

The ADC 1225 makes all thirteen bits of the conversion result available in parallel. Taking $\overline{CS}$ and $\overline{RD}$ low enables the TRI-STATE® output buffers. The conversion result is represented in 2's complement format.

The ADC1205 makes the conversion result available in two eight-bit bytes. The output format is 2's complement with extended sign. Data is right justified and presented high byte first. With $\overline{CS}$ low and $\overline{STATUS}$ high, the high byte (DB12–DB8) will be enabled on the output buffers the first time $\overline{RD}$ goes low. When $\overline{RD}$ goes low a second time, the low byte (DB7–DB0) will be enabled. On each read operation, the 'byst' flip-flop is toggled so that on successive reads alternate bytes will be available on the outputs. The 'byst' flip-flop is always reset to the high byte at the end of a conversion. Table 1 below shows the data bit locations on the ADC1205.

The ADC1205's $\overline{STATUS}$ pin makes it possible to read the conversion status and the state of the 'byst' flip-flop. With $\overline{RD}$, $\overline{STATUS}$ and $\overline{CS}$ low, this information appears on the data bus. The 'byst' status appears on pin 18 (DB2/DB10). A low output on pin 18 indicates that the next data read will be the high byte. A high output indicates that the next data read will be the low byte. A high status bit on pin 22 (DB6/DB12) indicates that the conversion is in progress. A high output appears on pin 17 (DB1/DB9) when the conversion is completed and the data has been transferred to the output latch. A high output on pin 16 (DB0/DB8) indicates that the conversion has been completed and the data is ready to read. This status bit is reset when a new conversion is initiated, data is read, or status is read. When reading a conversion result, $\overline{STATUS}$ should always be brought high at least 600 ns before $\overline{RD}$ goes low. If the conversion status information is not needed, the $\overline{STATUS}$ pin should be hardwired to V+. Table 2 summarizes the meanings of the four status bits.

TABLE I. Data Bit Locations, ADC1205

HIGH BYTE	DB12	DB12	DB12	DB12	DB11	DB10	DB9	DB8
LOW BYTE	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

TABLE II. Status Bit Locations and Meanings

Status Bit Location	Status Bit	Meaning	Condition to Clear Status Bit
DB6	SARS	"High" indicates that the conversion is in progress	
DB2	BYST	"Low" indicates that the next data read is the high byte. "High" indicates that the next data read is the low byte	Status write or toggle it with data read

Functional Description (Continued)

TABLE II. Status Bit Locations and Meanings (Continued)

Status Bit Location	Status Bit	Meaning	Condition to Clear Status Bit
DB1	EOC	"High" indicates that the conversion is completed and data is transferred to the output latch.	
DB0	INT	"High" indicates that it is the end of the conversion and the data is ready to read	Data read or status read or status write

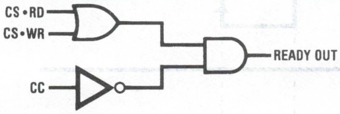
3.0 INTERFACE

3.1 RESET OF INTERRUPT

$\overline{\mathrm{INT}}$ goes low at the end of the conversion and indicates that data is transferred to the output latch. By reading data, $\overline{\mathrm{INT}}$ will be reset to high on the leading edge of the first read ($\overline{\mathrm{RD}}$ going low). $\overline{\mathrm{INT}}$ is also reset on the leading (falling) edge of $\overline{\mathrm{WR}}$ when starting a conversion.

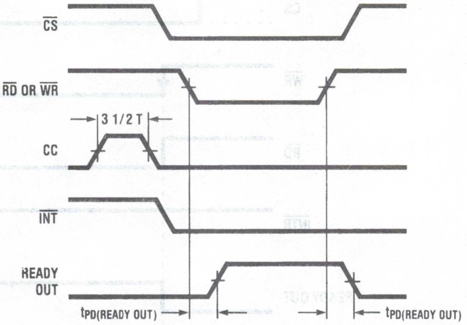
3.2 READY OUT

To simplify the hardware connection to high speed microprocessors, a READY OUT line is provided. This allows the A-to-D to insert a wait state in the μP's read cycle. The equivalent circuit and the timing diagram for READY OUT is shown in *Figures 7* and *8*.



TL/H/5676-9

FIGURE 7. READY OUT Equivalent Circuit



TL/H/5676-10

FIGURE 8. READY OUT Timing Diagram

3.3 RESETTING THE A/D

All the internal logic can be reset, which will abort any conversion in process and reset the status bits. The reset function is achieved by performing a status write ($\overline{\mathrm{CS}}$, $\overline{\mathrm{WR}}$ and $\overline{\mathrm{STATUS}}$ are low).

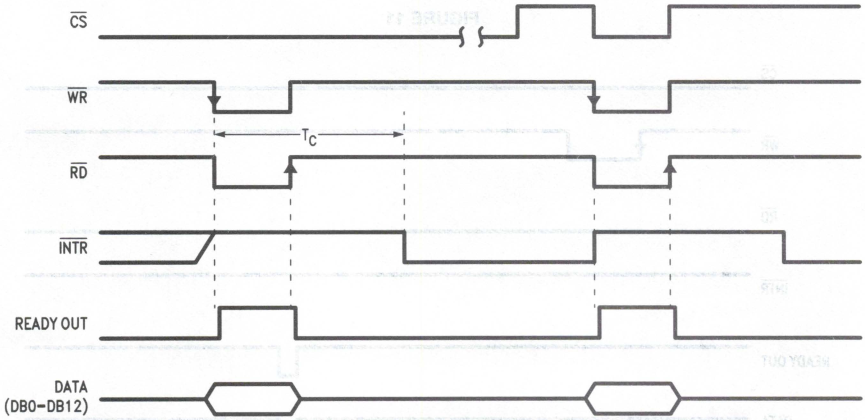
3.4 ADDITIONAL TIMING AND INTERFACE OPTIONS

ADC1225

1. $\overline{\mathrm{WR}}$ and $\overline{\mathrm{RD}}$ can be tied together with $\overline{\mathrm{CS}}$ low continuously or strobed. The previous conversion's data will be available when the $\overline{\mathrm{WR}}$ and $\overline{\mathrm{RD}}$ are low as shown below.

One drawback is that, since the conversion is started on the falling edge and the data read on the rising edge of $\overline{\mathrm{WR}}/\overline{\mathrm{RD}}$, the first data access will have erroneous information depending on the power-up state of the internal output latches.

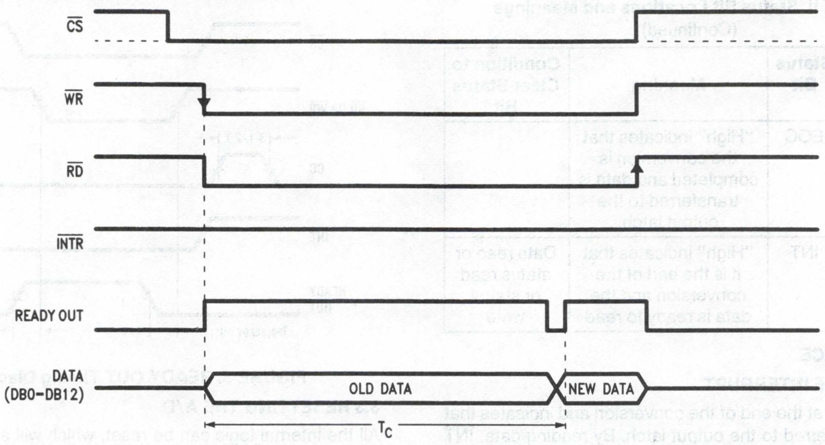
If the $\overline{\mathrm{WR}}/\overline{\mathrm{RD}}$ strobe is longer than the conversion time, $\overline{\mathrm{INTR}}$ will never go low to signal the end of a conversion. The conversion will be completed and the output latches will be updated. In this case the READY OUT signal can be used to sense the end of the conversion since it will go low when the output latches are being updated.



TL/H/5676-24

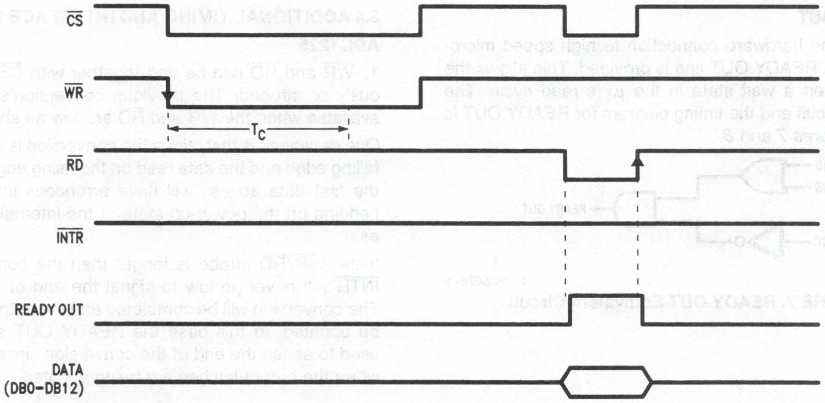
FIGURE 9

Functional Description (Continued)


CS
WR
RD
INTR
READY OUT
DATA (DB0–DB12)
OLD DATA
NEW DATA
T_C

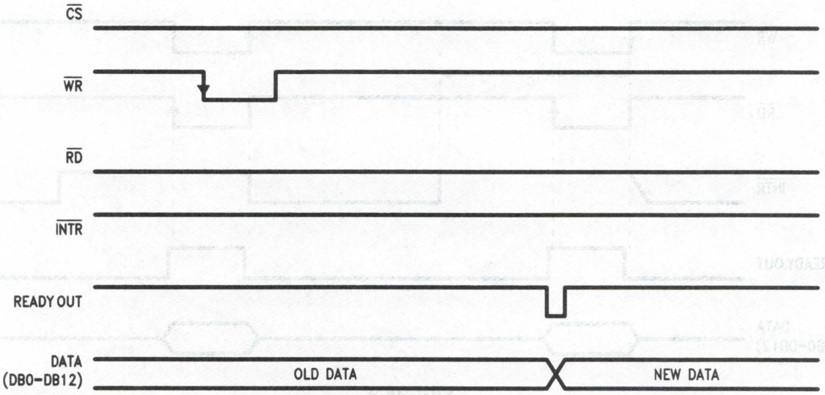
TL/H/5676–25

FIGURE 10


CS
WR
T_C
RD
INTR
READY OUT
DATA (DB0–DB12)

TL/H/5676–26

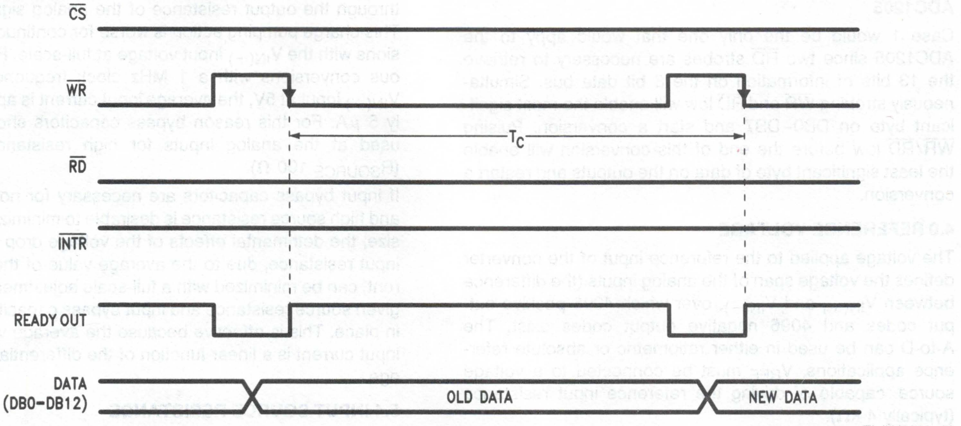
FIGURE 11


CS
WR
RD
INTR
READY OUT
DATA (DB0–DB12)
OLD DATA
NEW DATA

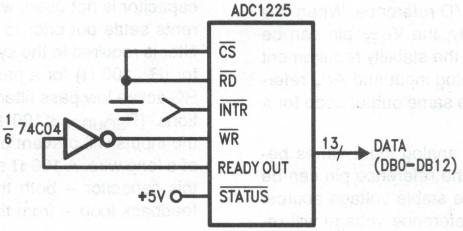
TL/H/5676–27

FIGURE 12

Functional Description (Continued)


$\overline{CS}$
$\overline{WR}$
T_C
$\overline{RD}$
$\overline{INTR}$
READY OUT
DATA (DB0–DB12)
OLD DATA
NEW DATA

TL/H/5676–28


ADC1225
$\overline{CS}$
$\overline{RD}$
$\overline{INTR}$
$\overline{WR}$
READY OUT
STATUS
$\frac{1}{6}$ 74C04
+5V
13
DATA (DB0–DB12)

TL/H/5676–29

FIGURE 13

When using this method of conversion only one strobe is necessary and the rising edge of $\overline{WR}/\overline{RD}$ can be used to read the current conversion results. These methods reduce the throughput time of the conversion since the RD and WR cycles are combined.

2. With the standard timing $\overline{WR}$ pulse width longer than the conversion time a conversion is completed but the $\overline{INTR}$ will never go low to signal the end of a conversion. The output latches will be updated and valid information will be available when the $\overline{RD}$ cycle is accomplished.

3. Tying $\overline{CS}$ and $\overline{RD}$ low continuously and strobing $\overline{WR}$ to initiate a conversion will also yield valid data. The $\overline{INTR}$ will never go low to signal the end of a conversion and the digital outputs will always be enabled, so using $\overline{INTR}$ to strobe the $\overline{WR}$ line for a continuous conversion cannot be done with this part.

A simple stand-alone circuit can be accomplished by driving $\overline{WR}$ with the inverse of the READY OUT signal using a simple inverter as shown below.

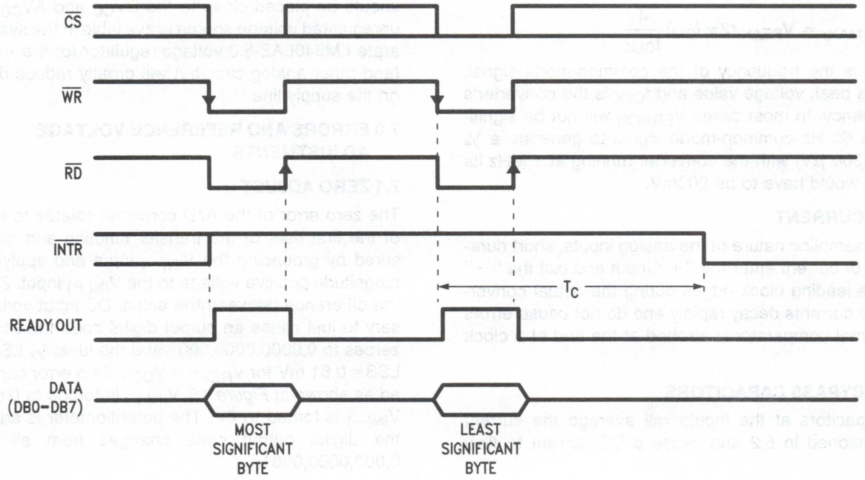

$\overline{CS}$
$\overline{WR}$
$\overline{RD}$
$\overline{INTR}$
T_C
READY OUT
DATA (DB0–DB7)
MOST SIGNIFICANT BYTE
LEAST SIGNIFICANT BYTE

FIGURE 14

TL/H/5676–30

Functional Description (Continued)

ADC1205

Case 1 would be the only one that would appy to the ADC1205 since two $\overline{RD}$ strobes are necessary to retrieve the 13 bits of information on the 8 bit data bus. Simultaneously strobing $\overline{WR}$ and $\overline{RD}$ low will enable the most significant byte on DB0–DB7 and start a conversion. Pulsing $\overline{WR}/\overline{RD}$ low before the end of this conversion will enable the least significant byte of data on the outputs and restart a conversion.

4.0 REFERENCE VOLTAGE

The voltage applied to the reference input of the converter defines the voltage span of the analog inputs (the difference between $V_{IN(+)}$ and $V_{IN(-)}$, over which 4096 positive output codes and 4096 negative output codes exist. The A-to-D can be used in either ratiometric or absolute reference applications. V_{REF} must be connected to a voltage source capable of driving the reference input resistance (typically 4 kΩ).

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirement of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. In general, the magnitude of the reference voltage will require an initial adjustment to null out full-scale errors.

5.0 THE ANALOG INPUTS

5.1 DIFFERENTIAL VOLTAGE INPUTS AND COMMON MODE REJECTION

The differential inputs of the ADC1225 and ADC1205 actually reduce the effects of common-mode input noise, i.e., signals common to both $V_{IN(+)}$ and $V_{IN(-)}$ inputs (60 Hz is most typical). The time interval between sampling the "+" and "−" input is 4 clock periods. Therefore, a change in the common-mode voltage during this short time interval may cause conversion errors. For a sinusoidal common-mode signal the error would be:

$$V_{ERROR(MAX)} = V_{PEAK} (2\pi f_{CM}) \frac{4}{f_{CLK}}$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value and f_{CLK} is the converter's clock frequency. In most cases V_{ERROR} will not be significant. For a 60 Hz common-mode signal to generate a ¼ LSB error (300 μV) with the converter running at 1 MHz its peak value would have to be 200mV.

5.2 INPUT CURRENT

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the leading clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period.

5.3 INPUT BYPASS CAPACITORS

Bypass capacitors at the inputs will average the current spikes mentioned in 5.2 and cause a DC current to flow through the output resistance of the analog signal source. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full-scale. For continuous conversions with a 1 MHz clock frequency and the $V_{IN(+)}$ input at 5V, the average input current is approximately 5 μA. For this reason bypass capacitors should not be used at the analog inputs for high resistance sources (R_{SOURCE} 100 Ω).

If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, due to the average value of the input current, can be minimized with a full-scale adjustment while the given source resistance and input bypass capacitor are both in place. This is effective because the average value of the input current is a linear function of the differential input voltage.

5.4 INPUT SOURCE RESISTANCE

Large values of source resistance where an input bypass capacitor is not used, will not cause errors as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($R \leq 100$ Ω) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ($R_{SOURCE} \leq 100$ Ω) a 0.001 μF bypass capacitor at the inputs will prevent pickup due to series lead inductance of a long wire. A 100 Ω series resistor can be used to isolate this capacitor – both the R and C are placed outside the feedback loop – from the output of an op amp, if used.

5.5 NOISE

The leads to the analog inputs should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause errors. Input filtering can be used to reduce the effects of these sources, but careful note should be taken of sections 5.3 and 5.4 if this route is taken.

6.0 POWER SUPPLIES

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. Low inductance tantalum capacitors of 1 μF or greater are recommended for supply bypassing. Separate bypass caps should be placed close to the DV_{CC} and AV_{CC} pins. If an unregulated voltage source is available in the system, a separate LM340LAZ-5.0 voltage regulator for the A-to-D's V_{CC} (and other analog circuitry) will greatly reduce digital noise on the supply line.

7.0 ERRORS AND REFERENCE VOLTAGE ADJUSTMENTS

7.1 ZERO ADJUST

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage necessary to just cause an output digital code transition from all zeroes to 0,0000,0000,0001 and the ideal ½ LSB value (½ LSB = 0.61 mV for $V_{REF} = 5$ V_{DC}). Zero error can be adjusted as shown in *Figure 15*. $V_{IN(+)}$ is forced to 0.61 mV, and $V_{IN(-)}$ is forced to 0V. The potentiometer is adjusted until the digital output code changes from all zeroes to 0,000,0000,0001.

Functional Description (Continued)

A simpler, although slightly less accurate, approach is to ground $V_{IN(+)}$ and $V_{IN(-)}$, and adjust for all zeros at the output. Error will be well under ½ LSB if the adjustment is done so that the potentiometer is "centered" within the 0,000,000 range. A positive voltage at the V_{OS} input will reduce the output code. The adjustment range is +4 to −30 LSB.

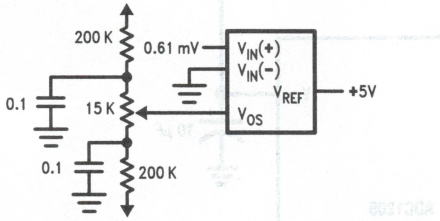

200 K
0.61 mV
$V_{IN}(+)$
$V_{IN}(-)$
V_{REF}
+5V
0.1
15 K
V_{OS}
0.1
200 K
TL/H/5676-11

FIGURE 15. Zero Adjust Circuit

7.2 POSITIVE AND NEGATIVE FULL-SCALE ADJUSTMENT

Unipolar Inputs

Apply a differential input voltage which is 1.5 LSB below the desired analog full-scale voltage (V_F) and adjust the magnitude of the V_{REF} input so that the output code is just changing from 0,1111,1111,1110 to 0,1111,1111,1111.

Bipolar Inputs

Do the same procedure outlined above for the unipolar case and then change the differential input voltage so that the digital output code is just changing from 1,0000,0000,0001 to 1,0000,0000,0000. Record the differential input voltage, V_X. the ideal differential input voltage for that transition should be;

$$\left(-V_F + \frac{V_F}{8192}\right)$$

Calculate the difference between Vx and the ideal voltage;

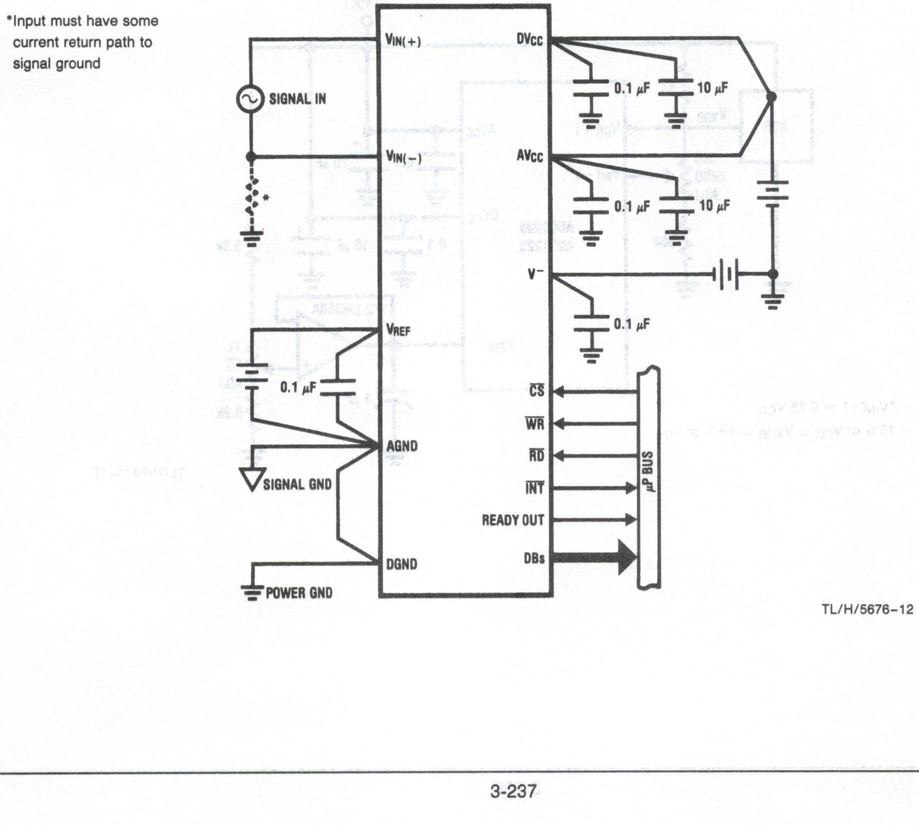
$$\Delta = V_X - \left(-V_F + \frac{V_F}{8192}\right)$$

Then apply a differential input voltage of;

$$\left(V_X - \frac{\Delta}{2}\right)$$

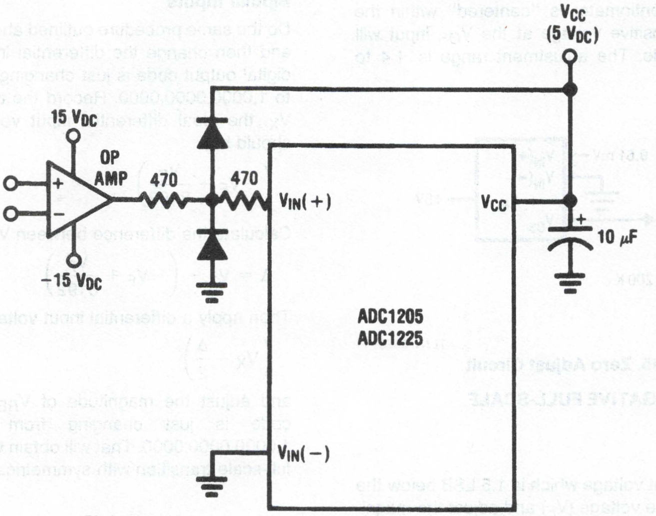
and adjust the magnitude of V_{REF} so the digital output code is just changing from 1,0000,0000,0001 to 1,0000,0000,0000. That will obtain the positive and negative full-scale transition with symmetrical minimum error.

Typical Applications


*Input must have some current return path to signal ground
$V_{IN(+)}$
DVcc
0.1 µF
10 µF
SIGNAL IN
$V_{IN(-)}$
AVcc
0.1 µF
10 µF
*
V−
0.1 µF
V_{REF}
0.1 µF
CS
WR
RD
INT
READY OUT
DBs
µP BUS
AGND
SIGNAL GND
DGND
POWER GND
TL/H/5676-12

Typical Applications (Continued)

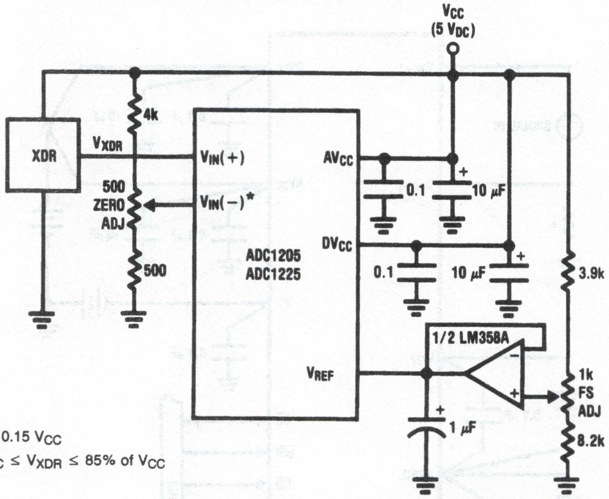
Protecting the Input


VCC
(5 VDC)
15 VDC
OP
AMP
470
470
VIN(+)
VCC
10 µF
−15 VDC
ADC1205
ADC1225
VIN(−)

Diodes are 1N914

TL/H/5676-16

Operating with Ratiometric Transducers


VCC
(5 VDC)
4k
XDR
VXDR
VIN(+)
AVCC
500
ZERO
ADJ
VIN(−)*
0.1
10 µF
500
ADC1205
ADC1225
DVCC
0.1
10 µF
3.9k
1/2 LM358A
VREF
1k
FS
ADJ
1 µF
8.2k

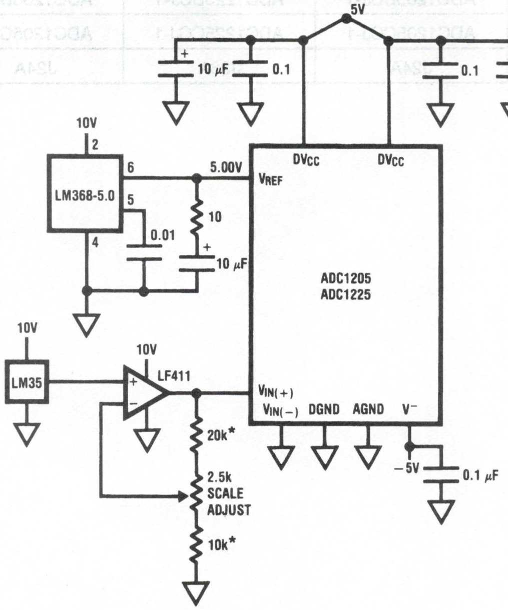
$^*V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \le V_{XDR} \le$ 85% of V_{CC}

TL/H/5676-17

Typical Applications (Continued)

Bipolar Input Temperature Converter

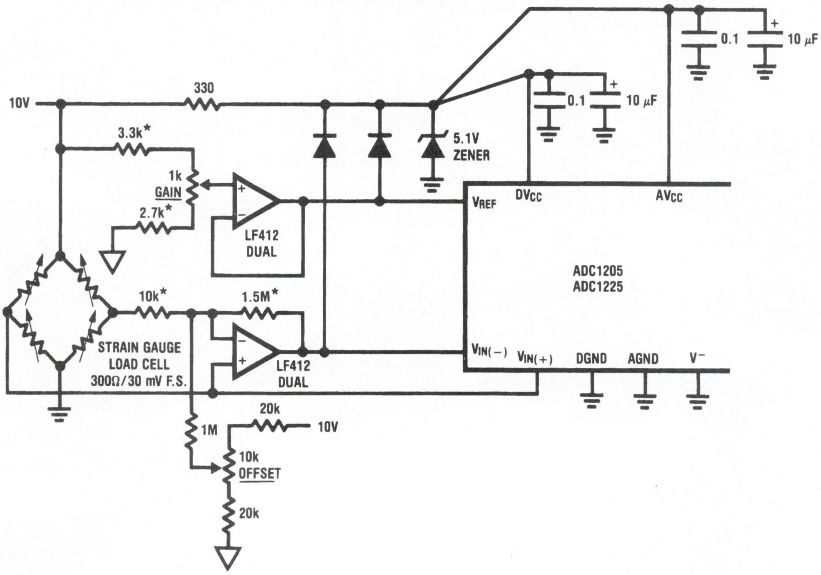

5V
+
10 μF
0.1
0.1
+
10 μF
10V
2
LM368-5.0
6
5
4
5.00V
10
0.01
+
10 μF
DVCC
DVCC
VREF
ADC1205
ADC1225
10V
LM35
10V
+
−
LF411
VIN(+)
VIN(−)
DGND
AGND
V−
20k*
2.5k
SCALE
ADJUST
10k*
−5V
0.1 μF

TL/H/5676-18

+150 to −55°C with 0.04°C resolution

Note: * resistors are 1% metal film types

Strain Gauge Converter with .025% Resolution and Single Power Supply


0.1
+
10 μF
330
10V
0.1
+
10 μF
3.3k*
5.1V
ZENER
1k
GAIN
2.7k*
+
−
LF412
DUAL
VREF
DVCC
AVCC
ADC1205
ADC1225
10k*
1.5M*
−
+
LF412
DUAL
STRAIN GAUGE
LOAD CELL
300Ω/30 mV F.S.
VIN(−)
VIN(+)
DGND
AGND
V−
1M
20k
10V
10k
OFFSET
20k

TL/H/5676-19

Note: 1)* resistors are 1% metal film types

2) LF412 power +10V and ground

Ordering Information

Temperature Range		0°C to 70°C		−40°C to +85°C	
Non-Linearity	0.012%	ADC1205BCJ-1	ADC1225BCJ-1	ADC1205BCJ	ADC1225BCJ
	0.024%	ADC1205CCJ-1	ADC1225CCJ-1	ADC1205CCJ	ADC1225CCJ
Package Outline		J24A	J28A	J24A	J28A

National Semiconductor Corporation

ADC1210, ADC1211 12-Bit CMOS A/D Converters

General Description

The ADC1210, ADC1211 are low power, medium speed, 12-bit successive approximation, analog-to-digital converters. The devices are complete converters requiring only the application of a reference voltage and a clock for operation. Included within the device are the successive approximation logic, CMOS analog switches, precision laser trimmed thin film R-2R ladder network and FET input comparator.

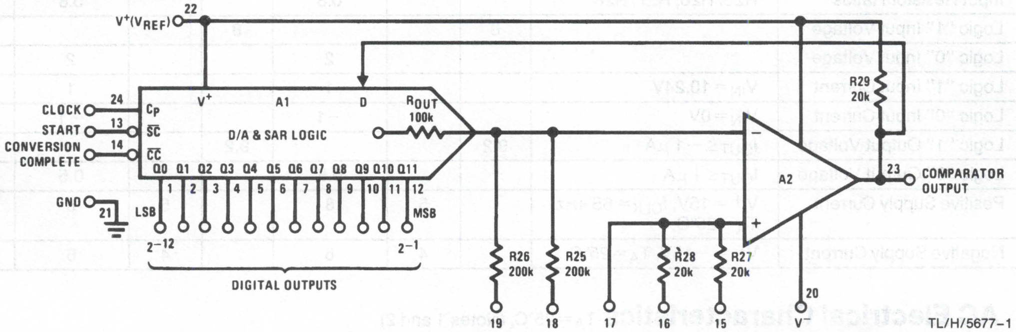
The ADC1210 offers 12-bit resolution and 12-bit accuracy, and the ADC1211 offers 12-bit resolution with 10-bit accuracy. The inverted binary outputs are directly compatible with CMOS logic. The ADC1210, ADC1211 will operate over a wide supply range, convert both bipolar and unipolar analog inputs, and operate in either a continuous conversion mode or logic-controlled START-STOP conversion mode. The devices are capable of making a 12-bit conversion in 100 µs typ, and can be connected to convert 10 bits in 30 µs.

Both devices are available in military and industrial temperature ranges.

Features

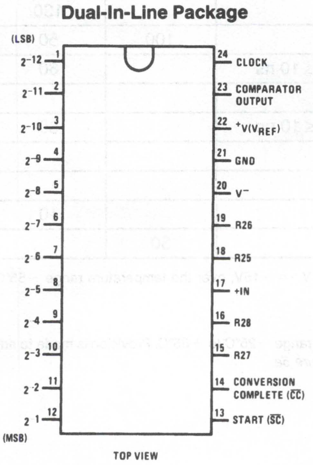
- 12-bit resolution
- ±¾ LSB or ±2 LSB nonlinearity
- Single +5V to ±15V supply range
- 100 µs 12-bit, 30 µs 10-bit conversion rate
- CMOS compatible outputs
- Bipolar or unipolar analog inputs
- 200 kΩ analog input impedance

Block Diagram


22
V+(VREF)
CLOCK
START
CONVERSION COMPLETE
24
13
14
Cp
SC
CC
V+
A1
D
ROUT 100k
D/A & SAR LOGIC
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11
1 2 3 4 5 6 7 8 9 10 11 12
GND
21
LSB
MSB
2−12
2−1
DIGITAL OUTPUTS
R26 200k
R25 200k
R28 20k
R27 20k
R29 20k
A2
23
COMPARATOR OUTPUT
20
19
18
17
16
15
V−

TL/H/5677–1

Connection Diagram


Dual-In-Line Package
(LSB)
2−12 1
2−11 2
2−10 3
2−9 4
2−8 5
2−7 6
2−6 7
2−5 8
2−4 9
2−3 10
2−2 11
2−1 12
(MSB)
24 CLOCK
23 COMPARATOR OUTPUT
22 +V(VREF)
21 GND
20 V−
19 R26
18 R25
17 +IN
16 R28
15 R27
14 CONVERSION COMPLETE (CC)
13 START (SC)
TOP VIEW

TL/H/5677–2

Order Number ADC1210HD, ADC1210HCD, ADC1211HD, ADC1211HCD
See NS Package D24D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Maximum Reference Supply Voltage (V+)	16V
Maximum Negative Supply Voltage (V−)	−20V
Voltage At Any Logic Pin	V+ +0.3V
Analog Input Voltage	±15V
Maximum Digital Output Current	±10 mA
Maximum Comparator Output Current	50 mA
Comparator Output Short-Circuit Duration	5 Seconds
Power Dissipation	See Curves
Operating Temperature Range	
ADC1210HD, ADC1211HD	−55°C to +125°C
ADC1210HCD, ADC1211HCD	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 4)	TBD V

DC Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	ADC1210			ADC1211			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		12			12			Bits
Linearity Error	(Note 3) $f_{CLK}=65$ kHz, $T_A=25°C$ $f_{CLK}=65$ kHz			 ±0.0183 ±0.0366			 ±0.0488	 % FS % FS
Full Scale Error	$T_A=25°C$, Unadjusted			0.20			0.50	% FS
Zero Scale Error	$T_A=25°C$, Unadjusted			0.20			0.50	% FS
Quantization Error				±1/2			±1/2	LSB
Input Resistor Values	R27, R28		20			20		kΩ
Input Resistor Values	R25, R26		200			200		kΩ
Input Resistor Ratios	R25/R26, R27/R28			0.8			0.8	%
Logic "1" Input Voltage		8			8			V
Logic "0" Input Voltage				2			2	V
Logic "1" Input Current	$V_{IN}=10.24V$			1			1	μA
Logic "0" Input Current	$V_{IN}=0V$			−1			−1	μA
Logic "1" Output Voltage	$I_{OUT}\leq -1\ \mu A$	9.2			9.2			V
Logic "0" Output Voltage	$I_{OUT}\leq 1\ \mu A$			0.5			0.5	V
Positive Supply Current	$V^+=15V$, $f_{CLK}=65$ kHz, $T_A=25°C$		5	8		5	8	mA
Negative Supply Current	$V^-=-15V$, $T_A=25°C$		4	6		4	6	mA

AC Electrical Characteristics $T_A=25°C$, (Notes 1 and 2)

Parameter	Conditions	Min	Typ	Max	Units
Conversion Time			100	200	μs
Maximum Clock Frequency			130	65	kHz
Clock Pulse Width		100	50		ns
Propagation Delay From Clock to Data Output (Q0 to Q11)	$t_r\leq t_f\leq 10$ ns		60	150	ns
Propagation Delay from Clock to Conversion Complete	$t_r\leq t_f\leq 10$ ns		60	150	ns
Clock Rise and Fall Time				5	μs
Input Capacitance			10		pF
Start Conversion Set-Up Time		30			ns

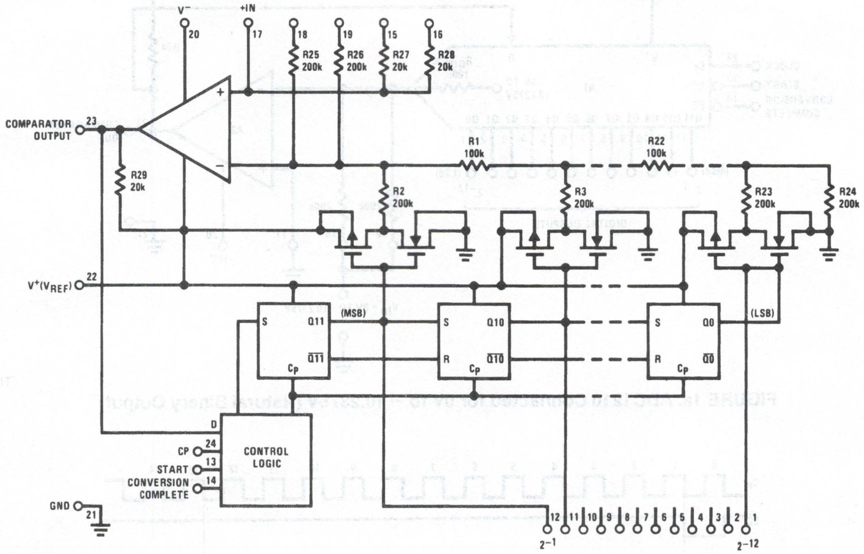
Note 1: Unless otherwise noted, these specifications apply for $V^+=10.240V$, $V^-=-15V$, over the temperature range −55°C to +125°C for the ADC1210HD, ADC1211HD, and −25°C to +85°C for the ADC1210HCD, ADC1211HCD.

Note 2: All typical values are for $T_A=25°C$.

Note 3: Unless otherwise noted, this specification applies over the temperature range −25°C to +85°C. Provision is made to adjust zero scale error to 0V and full-scale to 10.2375V during testing. Standard linearity test circuit is shown in *Figure 5a*.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

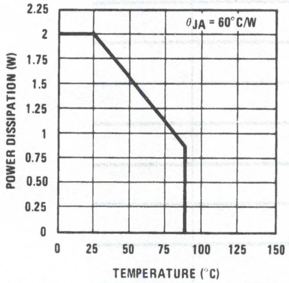
Schematic Diagram


V⁻
20
+IN
17
18
19
15
16
R25 200k
R26 200k
R27 20k
R28 20k
COMPARATOR OUTPUT
23
R29 20k
R1 100k
R22 100k
R2 200k
R3 200k
R23 200k
R24 200k
V⁺(V_REF)
22
S
Q11
(MSB)
$\overline{Q11}$
Cp
R
S
Q10
$\overline{Q10}$
Cp
R
S
Q0
(LSB)
$\overline{Q0}$
Cp
D
CP
24
START
13
CONVERSION COMPLETE
14
CONTROL LOGIC
GND
21
12
11
10
9
8
7
6
5
4
3
2
1
2⁻¹
2⁻¹²

TL/H/5677-3

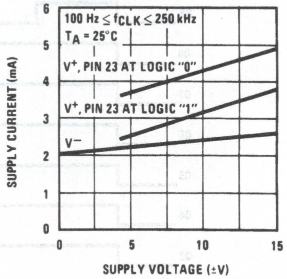
Note: 3 bits shown for clarity

Power Dissipation vs Temperature



TL/H/5677-4

Supply Current vs Supply Voltage



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1.0 THEORY OF OPERATION

The ADC1210, ADC1211 are successive approximation analog-to-digital converters, i.e., the conversion takes place 1 bit at a time by comparing the output of the internal D/A to the (unknown) input voltage. The START input (pin 13), when taken low, causes the register to reset synchronously on the next CLOCK low-to-high transition. The MSB, Q11 is set to the low state, and the remaining bits, Q0 through Q10, will be set to the high state. The register will remain in this state until the $\overline{\text{SC}}$ input is taken high. When START goes high, the conversion will begin on the low-to-high transition of the CLOCK pulse. Q11 will then assume the state of pin 23. If pin 23 is high, Q11 will be high; if pin 23 is low, Q11 will remain low. At the same time, the next bit Q10 is set low. All remaining bits, Q0–Q9 will remain unchanged (high). This process will continue until the LSB (Q0) is found. When the conversion process is completed, it is indicated by CONVERSION COMPLETE ($\overline{\text{CC}}$) (pin 14) going low. The logic levels at the data output pins (pins 1–12) are the complemented-binary representation of the converted analog signal with Q11 being the MSB and Q0 being the LSB. The register will remain in the above state until the $\overline{\text{SC}}$ is again taken low.

An application example is shown in *Figure 1*. In this case, a 0 to −10.2375V input is being converted using the ADC1210 with V+ = 10.240V, V− = −15V. *Figure 1b* is the timing diagram for full scale input. *Figure 1c* is the timing diagram for zero scale input, *Figure 1d* is the timing diagram for −3.4125V input (010101010101 = output).

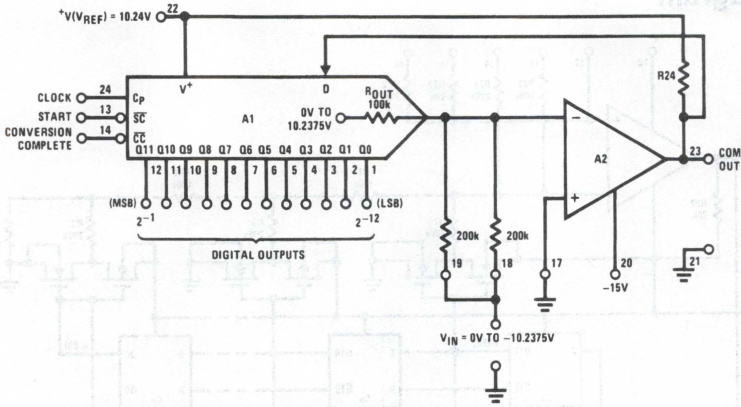
+V(VREF) = 10.24V
22
V+
D
CLOCK
START
CONVERSION COMPLETE
24
13
14
CP
SC
CC
A1
ROUT 100k
0V TO 10.2375V
Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
12 11 10 9 8 7 6 5 4 3 2 1
(MSB)
(LSB)
2^-1
2^-12
DIGITAL OUTPUTS
200k
200k
19
18
17
20
-15V
21
R24
A2
23
COMPARATOR OUT
VIN = 0V TO -10.2375V

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FIGURE 1a. ADC1210 Connected for 0V to − 10.2375V (Natural Binary Output)

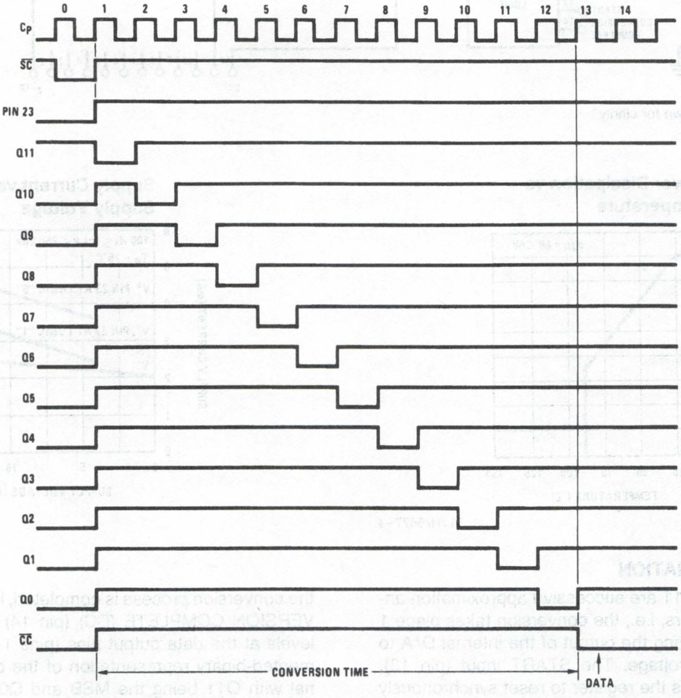
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
CP
SC
PIN 23
Q11
Q10
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
CC
CONVERSION TIME
DATA

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FIGURE 1b. Timing Diagram for V_{IN} = Full Scale Input

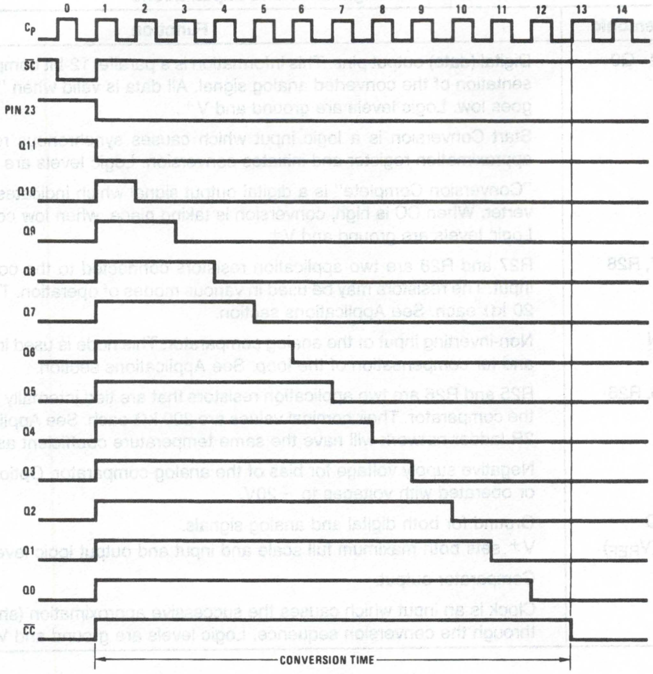
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
Cp
SC
PIN 23
Q11
Q10
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
CC
CONVERSION TIME

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FIGURE 1c. Timing Diagram for V_{IN} = Zero Scale

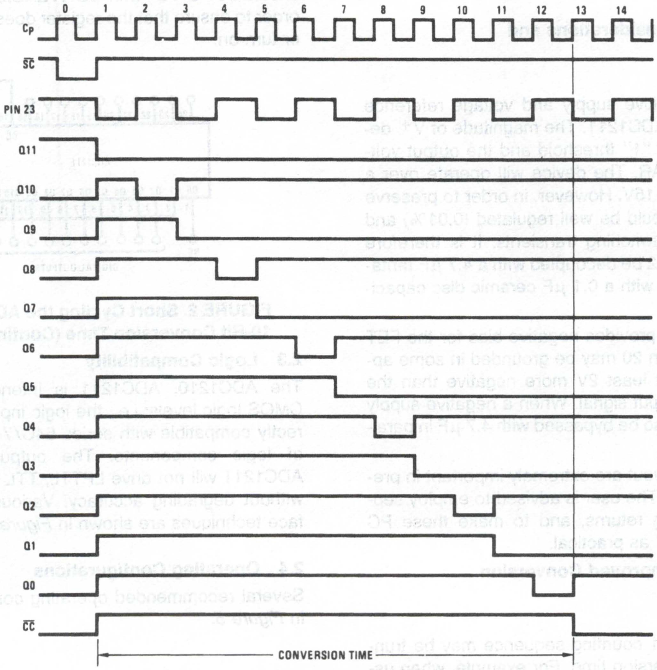
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
Cp
SC
PIN 23
Q11
Q10
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
CC
CONVERSION TIME

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FIGURE 1d. Timing Diagram for V_{IN} = −3.4125V (010101010101)

TABLE 1. Pin Assignments and Explanations

Pin Number	Mnemonic	Function
1–12	Q11–Q0	Digital (data) output pins. This information is a parallel 12-bit complemented binary representation of the converted analog signal. All data is valid when "Conversion Complete" goes low. Logic levels are ground and V+.
13	$\overline{SC}$	Start Conversion is a logic input which causes synchronous reset of the successive approximation register and initiates conversion. Logic levels are ground and V+.
14	$\overline{CC}$	"Conversion Complete" is a digital output signal which indicates the status of the converter. When $\overline{CC}$ is high, conversion is taking place, when low conversion is completed. Logic levels are ground and V+.
15, 16	R27, R28	R27 and R28 are two application resistors connected to the comparator non-inverting input. The resistors may be used in various modes of operation. Their nominal values are 20 kΩ each. See Applications section.
17	+IN	Non-inverting input of the analog comparator. This node is used in various configurations and for compensation of the loop. See Applications section.
18, 19	R25, R26	R25 and R26 are two application resistors that are tied internally to the inverting input of the comparator. Their nominal values are 200 kΩ each. See Applications section. The R-2R ladder network will have the same temperature coefficient as these resistors.
20	V−	Negative supply voltage for bias of the analog comparator. Optionally may be grounded or operated with voltages to −20V.
21	GND	Ground for both digital and analog signals.
22	V+ (V_{REF})	V+ sets both maximum full scale and input and output logic levels.
23	CO	Comparator output.
24	C_P	Clock is an input which causes the successive approximation (shift) register to advance through the conversion sequence. Logic levels are ground and V+.

2.0 APPLICATIONS

2.1 Power Supply Considerations and Decoupling

Pin 22 is both the positive supply and voltage reference input to the ADC1210, ADC1211. The magnitude of V+ determines the input logic "1" threshold and the output voltage from the CMOS SAR. The device will operate over a range of V+ from 5V to 15V. However, in order to preserve 12-bit accuracy, V+ should be well regulated (0.01%) and isolated from external switching transients. It is therefore recommended that pin 22 be decoupled with a 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic disc capacitor.

The V− supply (pin 20) provides negative bias for the FET comparator. Although pin 20 may be grounded in some applications, it must be at least 2V more negative than the most negative analog input signal. When a negative supply is used, pin 20 should also be bypassed with 4.7 μF in parallel with 0.1 μF.

Grounding and circuit layout are extremely important in preserving 12-bit accuracy. The user is advised to employ separate digital and analog returns, and to make these PC board traces as "heavy" as practical.

2.2 Short Cycle for Improved Conversion Time (Figure 2)

The ADC1210, ADC1211 counting sequence may be truncated to decrease conversion time. For example, when using the ADC1211, 2 clock intervals may be "saved" if 10-bit conversion accuracy is taking place. The Q2 output should be "OR'd" with CONVERSION COMPLETE ($\overline{CC}$) in order to ensure that the register does not lock-up upon power turn-on.

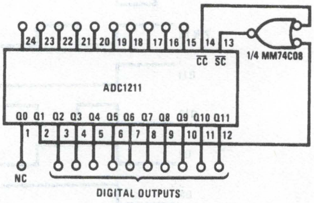

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FIGURE 2. Short Cycling the ADC1211 to improve 10-Bit Conversion Time (Continuous Conversion)

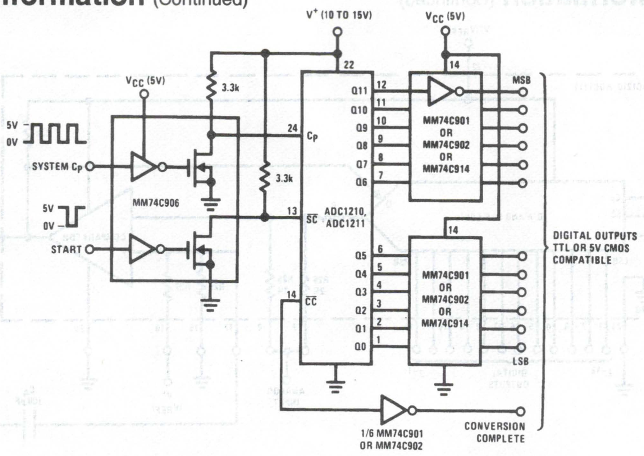
2.3 Logic Compatibility

The ADC1210, ADC1211 is intended to interface with CMOS logic levels: i.e., the logic inputs and outputs are directly compatible with series 54C/74C and CD4000 family of logic components. The outputs of the ADC1210, ADC1211 will not drive LPTTL, TTL or PMOS logic directly without degrading accuracy. Various recommended interface techniques are shown in *Figures 3 and 4*.

2.4 Operating Configurations

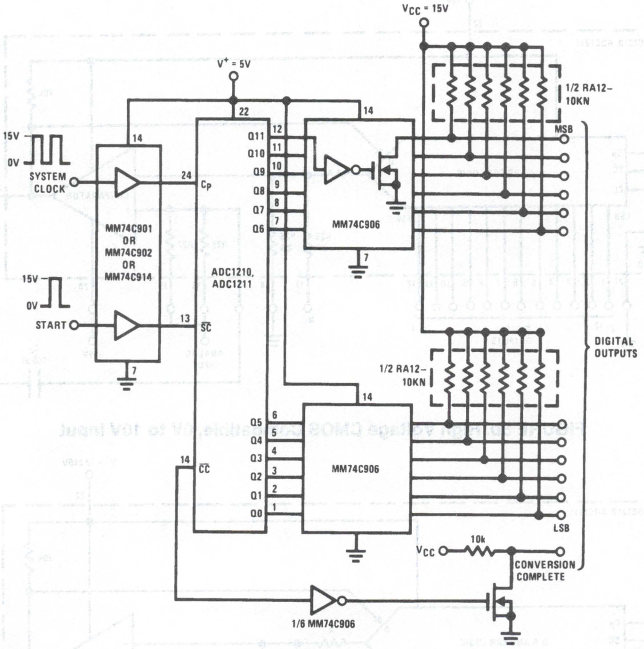
Several recommended operating configurations are shown in *Figure 5*.

Applications Information (Continued)


V+ (10 TO 15V)
VCC (5V)
VCC (5V)
3.3k
3.3k
5V
0V
SYSTEM Cp
5V
0V
START
MM74C906
22
24
13
14
Cp
SC
CC
ADC1210, ADC1211
Q11
Q10
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
MM74C901 OR MM74C902 OR MM74C914
MM74C901 OR MM74C902 OR MM74C914
MSB
LSB
DIGITAL OUTPUTS TTL OR 5V CMOS COMPATIBLE
1/6 MM74C901 OR MM74C902
CONVERSION COMPLETE

TL/H/5677-11

FIGURE 3. Interfacing an ADC1210, ADC1211 Running on $V^+ > V_{CC}$. Example: $V^+ = 10.24V$, System $V_{CC} = 5V$


VCC = 15V
V+ = 5V
1/2 RA12-10KN
1/2 RA12-10KN
15V
0V
SYSTEM CLOCK
15V
0V
START
MM74C901 OR MM74C902 OR MM74C914
ADC1210, ADC1211
Cp
SC
CC
Q11
Q10
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
MM74C906
MM74C906
MSB
LSB
DIGITAL OUTPUTS
VCC
10k
CONVERSION COMPLETE
1/6 MM74C906

TL/H/5677-12

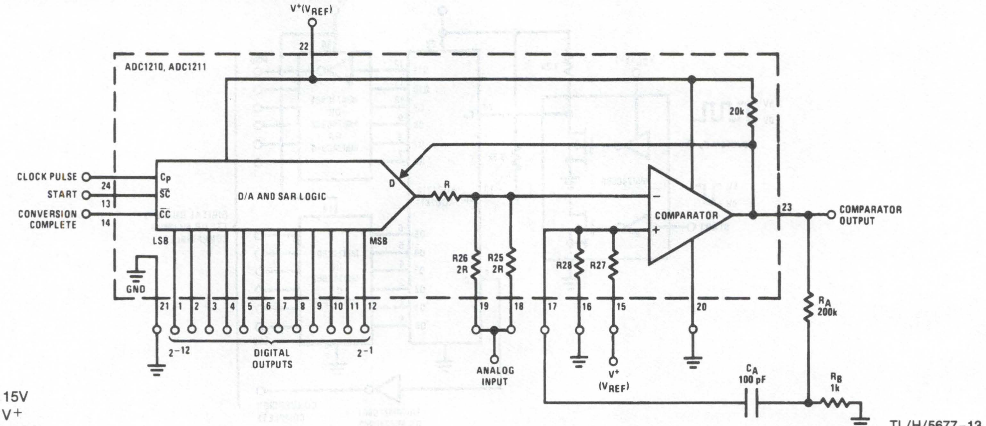
FIGURE 4. Interfacing an ADC1210, ADC1211 Running on $V^+ < V_{CC}$. Example: $V^+ = 5V$, $V_{CC} = 15V$

2.5 Offset and Full Scale Adjust

A variety of techniques may be employed to adjust Offset and Full Scale on the ADC1210, ADC1211. A straight-forward Full Scale Adjust is to incrementally vary V^+ (V_{REF}) to match the analog input voltage. A recommended technique is shown in *Figure 6*. An LM199 and low drift op amp(e.g., the LH0044) are used to provide the precision reference. The ADC1210, ADC1211 is put in the continuous convert mode by shorting pins 13 and 14. An analog voltage equal to V_{REF} minus 1½ LSB (10.23625V) is applied to pins 18 and 19, and R1 is adjusted until the LSB flickers equally between logic "1" and logic "0" (all other outputs must be stable logic "0"). Offset Null is accomplished by then applying an analog input voltage equal to ½ LSB at pins 18 and 19. R2 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other bits are stable). In the circuit of *Figure 6*, the ADC1210, ADC1211 is configured for Complementary Binary logic and the values shown are for $V^+ = 10.240V$, $V_{FS} = 10.2375V$, LSB = 2.5 mV.

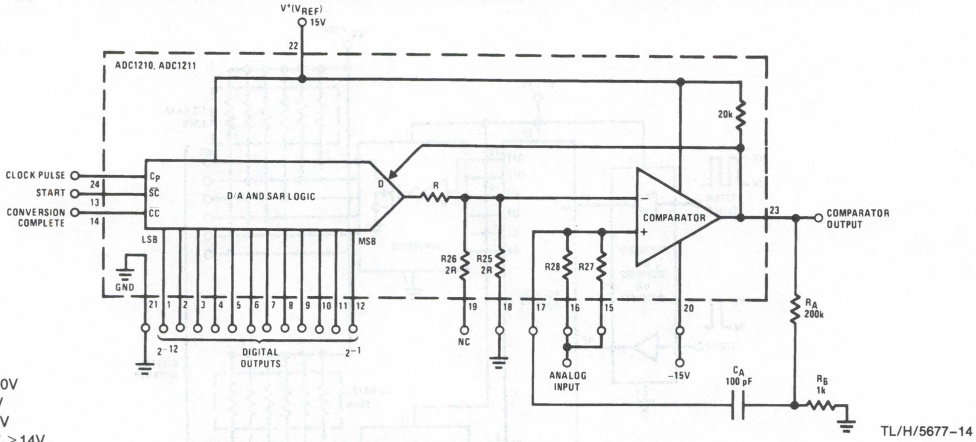
An alternate technique is shown in *Figure 7*. In this instance, an LH0071 is used to provide the reference voltage. An analog input voltage equal to V_{REF} minus 1½ LSB (10.23625V) is applied to pins 18 and 19.

Applications Information (Continued)


V+(VREF)
22
ADC1210, ADC1211
CLOCK PULSE
START
CONVERSION COMPLETE
24
13
14
Cp
SC
CC
D/A AND SAR LOGIC
D
R
LSB
MSB
GND
21 1 2 3 4 5 6 7 8 9 10 11 12
2-12
DIGITAL OUTPUTS
2-1
R26 2R
R25 2R
R28
R27
19 18 17 16 15 20
ANALOG INPUT
V+ (VREF)
COMPARATOR
20k
23
COMPARATOR OUTPUT
RA 200k
CA 100 pF
RB 1k
TL/H/5677-13

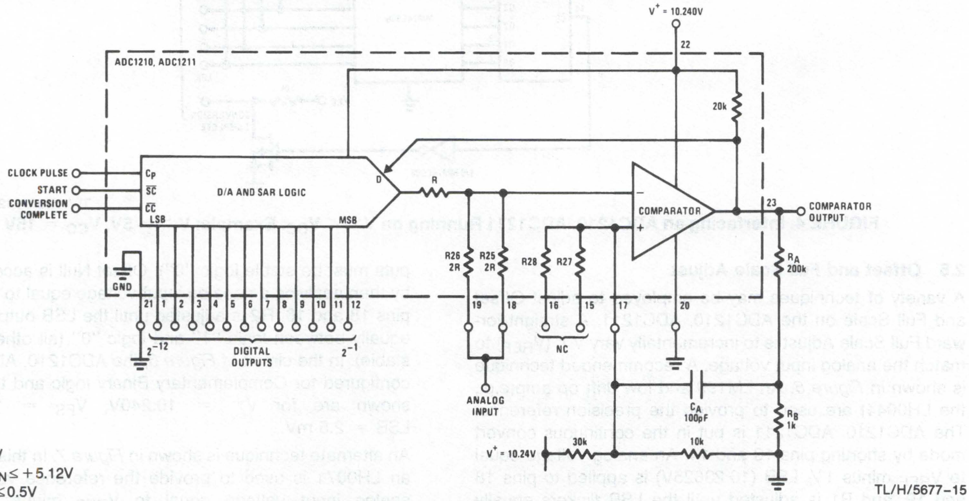
$5V \le V^+ \le 15V$
$0V \le V_{IN} \le V^+$
Logical "1" $\le 0.5V$
Logical "0" $\cong V^+$

FIGURE 5a. Single Supply Configuration, Complementary Logic


V+(VREF)
15V
22
ADC1210, ADC1211
CLOCK PULSE
START
CONVERSION COMPLETE
24
13
14
Cp
SC
CC
D/A AND SAR LOGIC
D
R
LSB
MSB
GND
21 1 2 3 4 5 6 7 8 9 10 11 12
2-12
DIGITAL OUTPUTS
2-1
R26 2R
R25 2R
R28
R27
19 18 17 16 15 20
NC
ANALOG INPUT
−15V
COMPARATOR
20k
23
COMPARATOR OUTPUT
RA 200k
CA 100 pF
RB 1k
TL/H/5677-14

$V^+ = 15.000V$
$V^- = -15V$
$0 \le V_{IN} \le 10V$
Logical "1" $\ge 14V$
Logical "0" $\le 0.5V$

FIGURE 5b. High Voltage CMOS Compatible, 0V to 10V Input


V+ = 10.240V
22
ADC1210, ADC1211
CLOCK PULSE
START
CONVERSION COMPLETE
Cp
SC
CC
D/A AND SAR LOGIC
D
R
LSB
MSB
GND
21 1 2 3 4 5 6 7 8 9 10 11 12
2-12
DIGITAL OUTPUTS
2-1
R26 2R
R25 2R
R28
R27
19 18 16 15 17 20
NC
ANALOG INPUT
COMPARATOR
20k
23
COMPARATOR OUTPUT
RA 200k
CA 100pF
RB 1k
V+ = 10.24V
30k
10k
TL/H/5677-15

$V^+ = 10.24V$
$-5.12V \le V_{IN} \le +5.12V$
Logical "1" $\le 0.5V$
Logical "0" $\cong 10V$

FIGURE 5c. Bipolar Input, Complementary Logic

Applications Information (Continued)

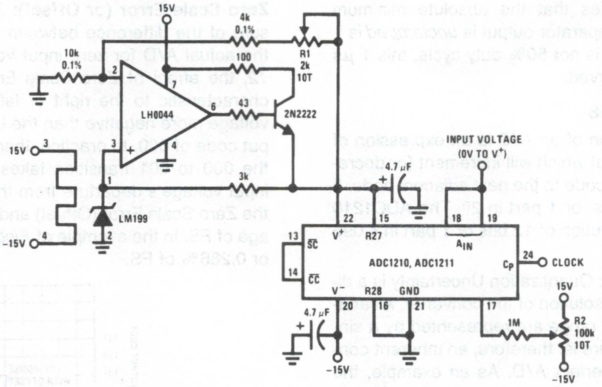

15V
4k
0.1%
R1
2k
10T
10k
0.1%
100
2
7
LH0044
43
2N2222
15V
3
6
4
1
3k
LM199
2
-15V
4
INPUT VOLTAGE
(0V TO V+)
4.7 µF
22
15
18
19
13
SC
V+
R27
AIN
ADC1210, ADC1211
Cp
24
CLOCK
14
CC
V-
R28
GND
15V
20
16
21
17
4.7 µF
1M
R2
100k
10T
-15V
-15V

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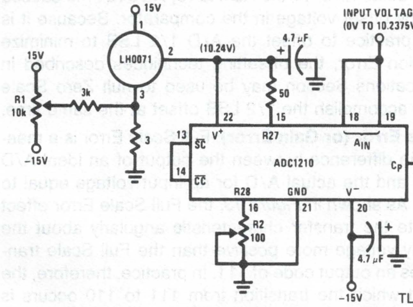
FIGURE 6. Offset and Full Scale Adjustment for Complementary Binary

R1 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other outputs must be a stable logic "0"). For Offset Null, an analog voltage equal to 1/2 LSB (1.25 mV) is then applied to pins 18 and 19, and R2, is adjusted until the LSB output flickers equally between logic "1" and "0".


15V
1
INPUT VOLTAGE
(0V TO 10.2375V)
4.7 µF
(10.24V)
15V
LH0071
2
R1
10k
3k
3
50
3
-15V
13
SC
V+
22
R27
15
18
19
AIN
ADC1210
Cp
24
CLOCK
14
CC
R28
GND
V-
16
21
20
R2
100
4.7 µF
-15V

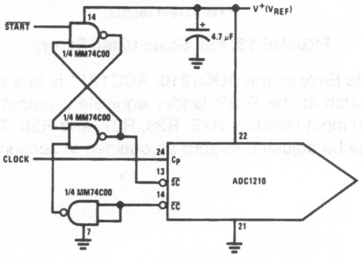
TL/H/5677-17

FIGURE 7. Offset and Full-Scale Adjustment Technique Using LH0071

In both techniques shown, adjusting the Full-Scale first and then Offset minimizes adjustment interaction. At least one iteration is recommended as a self-check.

2.6 START PULSE CONSIDERATIONS

To assure reliable conversion accuracy, the $\overline{\text{START}}$ ($\overline{\text{SC}}$) pulse applied to pin 13 of the ADC1210 should be synchronized to the conversion clock. One simple way to do that is the circuit shown in *Figure 8*. Note that once a conversion cycle is initiated, the $\overline{\text{START}}$ signal cannot effect the conversion operation until it is completed.


V+(VREF)
START
14
4.7 µF
1/4 MM74C00
1/4 MM74C00
22
CLOCK
24
Cp
13
SC
ADC1210
1/4 MM74C00
14
CC
7
21

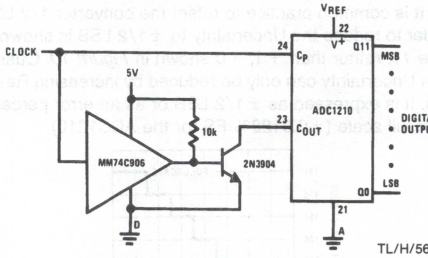
TL/H/5677-19

FIGURE 8. Synchronizing the $\overline{\text{START}}$ Pulse

The circuit insures that in no case can the ADC1210 make an error in the Most Significant Bit (MSB) decision. Without the circuit, it is possible for energy from the trailing edge of an asynchronous $\overline{\text{START}}$ pulse to be coupled into the ADC1210's comparator. If the analog input is near half-scale, the charge injected can force an error in the MSB decision. The circuit allows one clock period for this energy to dissipate before the decision is recorded.

2.7 ADC1210 CONVERSION AT 26 µs

The ADC1210 can run at 500 kHz clock frequency, or 12-bit conversion time of 26 µs (*Figure 9*). The comparator output is clamped low until the successive approximation register (SAR) is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions, eliminating the need for the AC hysteresis circuit above clock frequency of 65 kHz that is recommended.


VREF
22
V+
CLOCK
24
Cp
Q11
MSB
5V
ADC1210
DIGITAL OUTPUT
23
COUT
10k
MM74C906
2N3904
LSB
Q0
D
21
A

TL/H/5677-18

FIGURE 9. Conversion at 26 µs

A complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The same signal is buffered and inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in normal working order. The last half cycle of the clock unclamps the comparator output. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propogation delay such that the comparator output data is held long enough to resolve any internal logic setup time requirements.

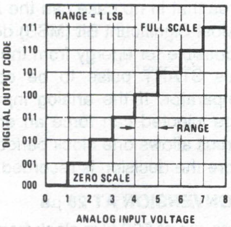
Applications Information (Continued)

The 500 kHz clock implies that the absolute minimum amount of time for the comparator output is *unclamped* is 1 µs. Therefore, if the clock is not 50% duty cycle, this 1 µs requirement must be observed.

3.0 DEFINITION OF TERMS

Resolution: The Resolution of an A/D is an expression of the smallest change in input which will increment (or decrement) the output from one code to the next adjacent code. It is defined in number of bits, or 1 part in 2^n. The ADC1210 and ADC1211 have a resolution of 12 bits or 1 part in 4,096 (0.0244%).

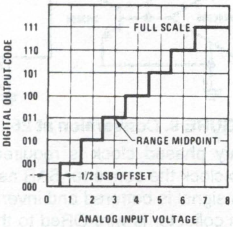
Quantization Uncertainty: Quantization Uncertainty is a direct consequence of the resolution of the converter. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an inherent conversion error even for a perfect A/D. As an example, the transfer characteristic of a perfect 3-bit A/D is shown in *Figure 10*.



TL/H/5677-21

FIGURE 10. Quantization Uncertainty of a Perfect 3-Bit A/D

As can be seen, all input voltages between 0V and 1V are represented by an output code of 000. All input voltages between 1V and 2V are represented by an output code of 001, etc. If the midpoint of the range is assumed to be the nominal value (e.g., 0.5V), there is an Uncertainty of ±1/2 LSB. It is common practice to offset the converter 1/2 LSB in order to reduce the Uncertainty to ±1/2 LSB is shown in *Figure 11*, rather than +1, −0 shown in *Figure 10*. Quantization Uncertainty can only be reduced by increasing Resolution. It is expressed as ±1/2 LSB or as an error percentage of full scale (±0.0122% FS for the ADC1210).

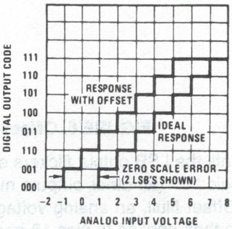


TL/H/5677-22

FIGURE 11. Transfer Characteristic Offset 1/2 LSB to Minimize Quantizing Uncertainty

Linearity Error: Linearity Error is the maximum deviation from a straight line passing through the end points of the A/D transfer characteristic. It is measured after calibrating Zero and Full Scale Error. Linearity is a performance characteristic intrinsic to the device and cannot be externally adjusted.

Zero Scale Error (or Offset): Zero Scale Error is a measure of the difference between the output of an ideal and the actual A/D for zero input voltage. As shown in *Figure 12*, the effect of Zero Scale Error is to shift the transfer characteristic to the right or left along the abscissa. Any voltage more negative than the LSB transition gives an output code of 000. In practice, therefore, the voltage at which the 000 to 001 transition takes place is ascertained, this input voltage's departure from the ideal value is defined as the Zero Scale Error (Offset) and is expressed as a percentage of FS. In the example of *Figure 12*, the offset is 2 LSB's or 0.286% of FS.



TL/H/5677-20

FIGURE 12. A/D Transfer Characteristic with Offset

The Zero Scale Error of the ADC1210, ADC1211 is caused primarily by offset voltage in the comparator. Because it is common practice to offset the A/D 1/2 LSB to minimize Quantization Error, the offsetting techniques described in the Applications Section may be used to null Zero Scale Error and accomplish the 1/2 LSB offset at the same time.

Full Scale Error (or Gain Error): Full Scale Error is a measure of the difference between the output of an ideal A/D converter and the actual A/D for an input voltage equal to full scale. As shown in *Figure 13*, the Full Scale Error effect is to rotate the transfer characteristic angularly about the origin. Any voltage more positive than the Full Scale transition gives an output code of 111. In practice, therefore, the voltage at which the transition from 111 to 110 occurs is ascertained. The input voltage's departure from the ideal value is defined as Full Scale Error and is expressed as a percentage of FS. In the example of *Figure 13*, Full Scale Error is 1 1/2 LSB's or 0.214% of FS.

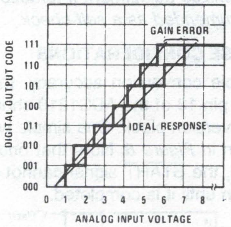


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FIGURE 13. Full Scale (Gain Error)

Full Scale Error of the ADC1210, ADC1211 is due primarily to mismatch in the R-2R ladder equivalent output impedance and input resistors R25, R26, R27, and R28. The gain error may be adjusted to zero as outlined in section 2.5.

Applications Information (Continued)

Monotonicity and Missing Codes: Monotonicity is a property of a D/A which requires an increasing or constant output voltage for an increasing digital input code. Monotonicity of a D/A converter does not, in itself, guarantee that an A/D built with that D/A will not have missing codes. However, the ADC1210 and ADC1211 are guaranteed to have no missing codes.

Conversion Time: The ADC1210, ADC1211 are successive approximation A/D converters requiring 13 clock intervals for a conversion to specified accuracy for the ADC1210 and 11 clocks for the ADC1211. There is a trade-off between accuracy and clock frequency due to settling time of the ladder and propagation delay through the comparator. By modifying the hysteresis network around the comparator, conversions with 10-bit accuracy can be made in 30 µs. Replace R_A, R_B and C_A in *Figure 5* with a 10 MΩ resistor between pin 23 (Comparator Output) and pin 17 (+ IN), and increase the clock rate to 366 kHz.

In order to prevent errors during conversion, the analog input voltage should not be allowed to change by more than ±1/2 LSB. This places a maximum slew rate of 12.5 µV/µs on the analog input voltage. The usual solution to this restriction is to place a Sample and Hold in front of the A/D. For additional application information, refer to application note AN245.

National Semiconductor Corporation

PRELIMINARY

ADC3511 3½-Digit Microprocessor Compatible A/D Converter

ADC3711 3¾-Digit Microprocessor Compatible A/D Converter

General Description

The ADC3511 and ADC3711 (MM74C937, MM74C938-1) monolithic A/D converter circuits are manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and indicated on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available.

The ADC3511 and ADC3711 have been designed to provide addressed BCD data and are intended for use with microprocessors and other digital systems. BCD digits are selected on demand via 2 Digit Select (D0, D1) inputs. Digit Select inputs are latched by a low-to-high transition on the Digit Latch Enable (DLE) input and will remain latched as long as DLE remains high. A start conversion input and a conversion complete output are included on both the ADC3511 and the ADC3711.

Features

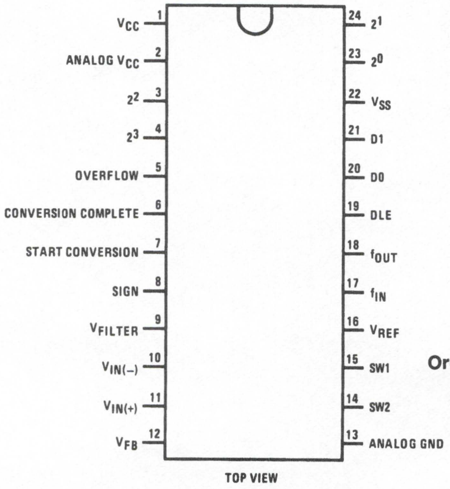
- Operates from single 5V supply
- ADC3511 converts 0 to ±1999 counts
- ADC3711 converts 0 to ±3999 counts
- Addressed BCD outputs
- No external precision components necessary
- Easily interfaced to microprocessors or other digital systems
- Medium speed—200 ms/conversion
- TTL compatible
- Internal clock set with RC network or driven externally
- Overflow indicated by hex "EEEE" output reading as well as an overflow output

Applications

- Low cost analog-to-digital converter
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram

Dual-In-Line Package



TL/H/5678–1

Order Number ADC3511CCN or ADC3711CCN
NS Package N24A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range (T_A)	−40°C to +85°C
Package Dissipation at $T_A = 25°C$	500 mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C
ESD Susceptibility (Note 5)	TBD V

DC Electrical Characteristics ADC3511CC, ADC3711CC

$4.75V \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage (Except f_{IN})		$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage (Except f_{IN})				1.5	V
$V_{IN(1)}$	Logical "1" Input Voltage (f_{IN})		$V_{CC} - 0.6$			V
$V_{IN(0)}$	Logical "0" Input Voltage (f_{IN})				0.6	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Except 2^0, 2^1, 2^2, 2^3)	$I_O = 360\ \mu A$	$V_{CC} - 0.4$			V
$V_{OUT(1)}$	Logical "1" Output Voltage (2^0, 2^1, 2^2, 2^3)	$I_O = 360\ \mu A$	$V_{CC} - 1.0$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.4	V
$I_{IN(1)}$	Logical "1" Input Current (SC, DLE, D0, D1)	$V_{IN} = V_{CC}$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (SC, DLE, D0, D1)	$V_{IN} = 0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	All Outputs Open		0.5	5.0	mA

AC Electrical Characteristics ADC3511CC, ADC3711CC

$V_{CC} = 5V$; $T_A = 25°C$, $C_L = 50$ pF; $t_r = t_f = 20$ ns; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
f_{OSC}	Oscillator Frequency			0.6/RC		Hz
f_{IN}	Clock Frequency		100		640	kHz
f_{CONV}	Conversion Rate	ADC3511CC ADC3711CC		$f_{IN}/64,512$ $f_{IN}/129,024$		conversions/sec conversions/sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns
t_{pd0}, t_{pd1}	Propagation Delay D0, D1, to 2^0, 2^1, 2^2, 2^3	DLE = 0V		2.0	5.0	μs
t_{pd0}, t_{pd1}	Propagation Delay DLE to 2^0, 2^1, 2^2, 2^3			2.0	5.0	μs
$t_{SET\text{-}UP}$	Set-Up Time D0, D1, to DLE	$t_{HOLD} = 0$ ns		100	200	ns
t_{PWDLE}	Minimum Pulse Width Digit Latch Enable (Low)			100	200	ns

Converter Characteristics ADC3511CC, ADC3711CC $4.75 \le V_{CC} \le 5.25V$; $-40°C \le T_A \le +85°C$, $f_C = 5$ conv./sec (ADC3511CC); 2.5 conv./sec (ADC3711CC); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
	Non-Linearity	$V_{IN} = 0–2V$ Full Scale $V_{IN} = 0–200$ mV Full Scale	−0.05	±0.025	+0.05	% of Full-Scale (Note 3)
	Quantization Error		−1		+0	Counts
	Offset Error	$V_{IN} = 0V$	−0.5	+1.0	+3.0	mV (Note 4)
	Rollover Error		−0		+0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	$T_A = 25°C$	−5	±1	+5	nA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All typicals are given for $T_A = 25°C$.

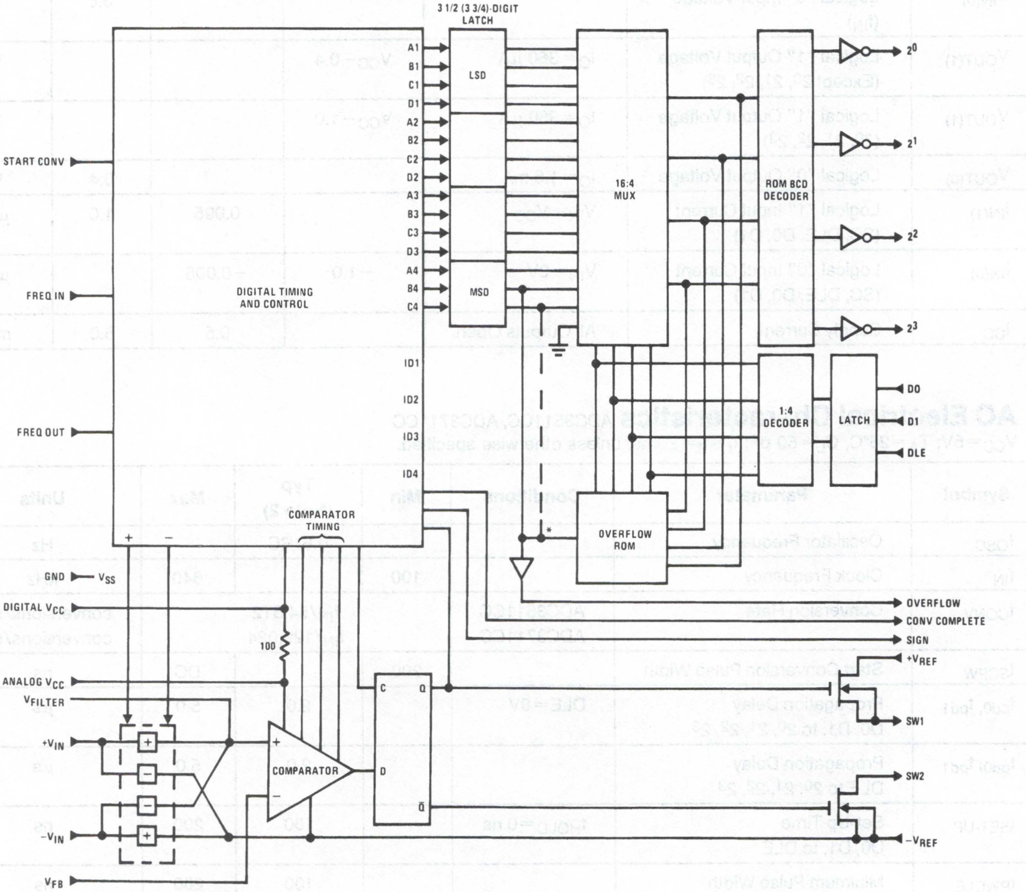
Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore 0.025% of full-scale = ½ count and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 count.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

Note 5: Human body model, 100 pF discharged through a 1.5Ω resistor.

Block Diagram

ADC3511 3 ½-Digit A/D (*ADC3711 3 ¾-Digit A/D)


3 1/2 (3 3/4)-DIGIT LATCH
START CONV
FREQ IN
FREQ OUT
DIGITAL TIMING AND CONTROL
A1
B1
C1
D1
A2
B2
C2
D2
A3
B3
C3
D3
A4
B4
C4
LSD
MSD
16:4 MUX
ROM BCD DECODER
2^0
2^1
2^2
2^3
ID1
ID2
ID3
ID4
1:4 DECODER
LATCH
D0
D1
DLE
OVERFLOW ROM
*
COMPARATOR TIMING
+
−
GND
V_{SS}
DIGITAL V_{CC}
ANALOG V_{CC}
V_{FILTER}
100
$+V_{IN}$
$-V_{IN}$
V_{FB}
COMPARATOR
C
Q
D
$\bar{Q}$
OVERFLOW
CONV COMPLETE
SIGN
$+V_{REF}$
SW1
SW2
$-V_{REF}$

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Applications Information

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure 1.* The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times (f_{IN})$$

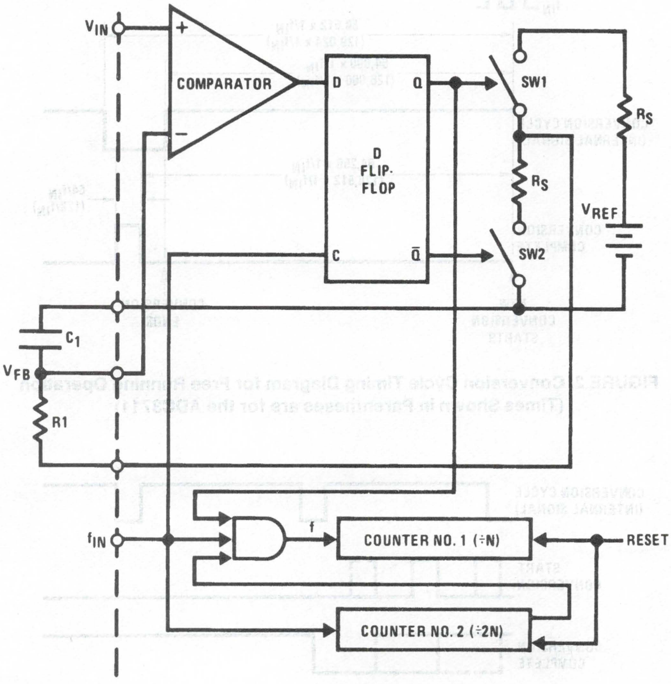
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{(count)} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.

For the ADC3711 N = 4000.



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$$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$$

$$f = \text{(duty cycle)} \times f_{IN}$$

$$\text{Count in counter no. 1} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times f_{IN}}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE 1. Analog Loop Schematic Pulse Modulation A/D Converter

Applications Information (Continued)

GENERAL INFORMATION

The timing diagram, shown in *Figure 2,* gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the digit latches are updated at a rate equal to 64,512 × $1/f_{IN}$ for the ADC3511, or 129,024 for the ADC3711.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the digit latches. This information will remain in the digit latches until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to $64 \times 1/f_{IN}$ on the ADC3511, or $128 \times 1/f_{IN}$ on the ADC3711.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ADC3511 and ADC3711 are always continuously converting the analog voltage present at their inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the digit latches.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3,* the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 × $1/f_{IN}$ (129,024 × $1/f_{IN}$ for the ADC3711) and the minimum time is 256 × $1/f_{IN}$ (512 × $1/f_{IN}$) for the ADC3711).

SYSTEM DESIGN CONSIDERATIONS

The ADC3511 and ADC3711 have reduced the problem of high resolution, high accuracy analog-to-digital conversion to nearly the level of simplicity, economy, and compactness usually associated with digital logic circuitry. However, they are truly high precision analog devices, and require the same kind of design considerations given to all analog circuits. While great care has been taken in the design of the ADC3511 and ADC3711 to make their application as easy as possible, in order to utilize them to their full performance potential, good grounding, power supply distribution, decoupling, and regulation techniques should be exercised.

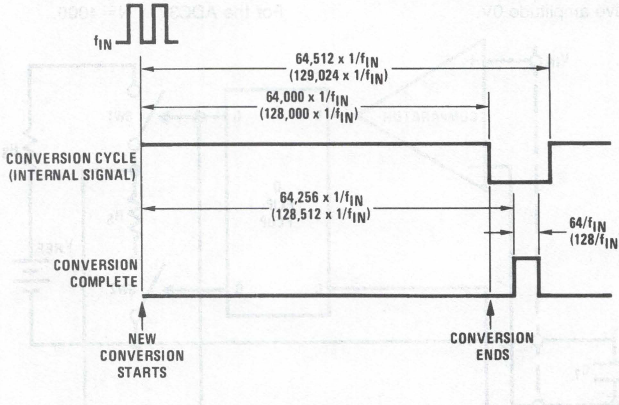

FIGURE 2. Conversion Cycle Timing Diagram for Free Running Operation (Times Shown in Parentheses are for the ADC3711)

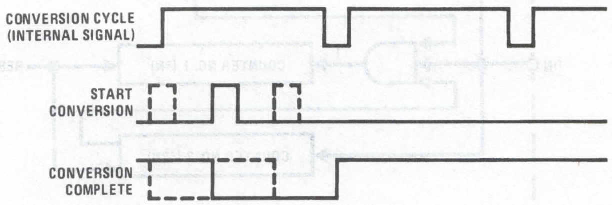

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FIGURE 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Truth Table

DIGIT SELECT INPUTS			SELECTED DIGIT
DLE	D1	D0	
L	L	L	Digit 0 (LSD)
L	L	H	Digit 1
L	H	L	Digit 2
L	H	H	Digit 3 (MSD)
H	X	X	Unchanged

L = low logic level
H = high logic level
X = irrelevant logic level

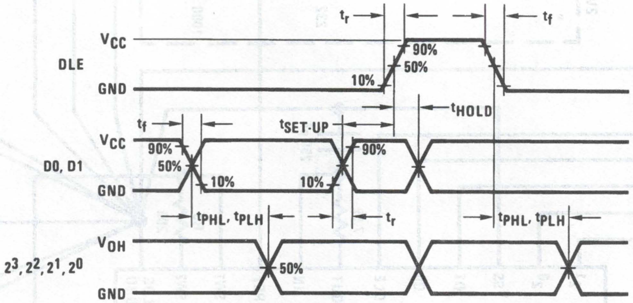
The value of the Selected Digit is presented at the 2^3, 2^2, 2^1 and 2^0 outputs in BCD format.

Note 1: If the value of a digit changes while it is selected, that change *will* be reflected at the outputs.

Note 2: An overflow condition will be indicated by a high level on the OVERFLOW output (pin 5) and E16 in all digits.

Note 3: The sign of the input voltage, when these devices are operated in the bipolar mode, is indicated by the SIGN output (pin 8). A high level indicates a positive voltage, a low level a negative.

Timing Diagrams



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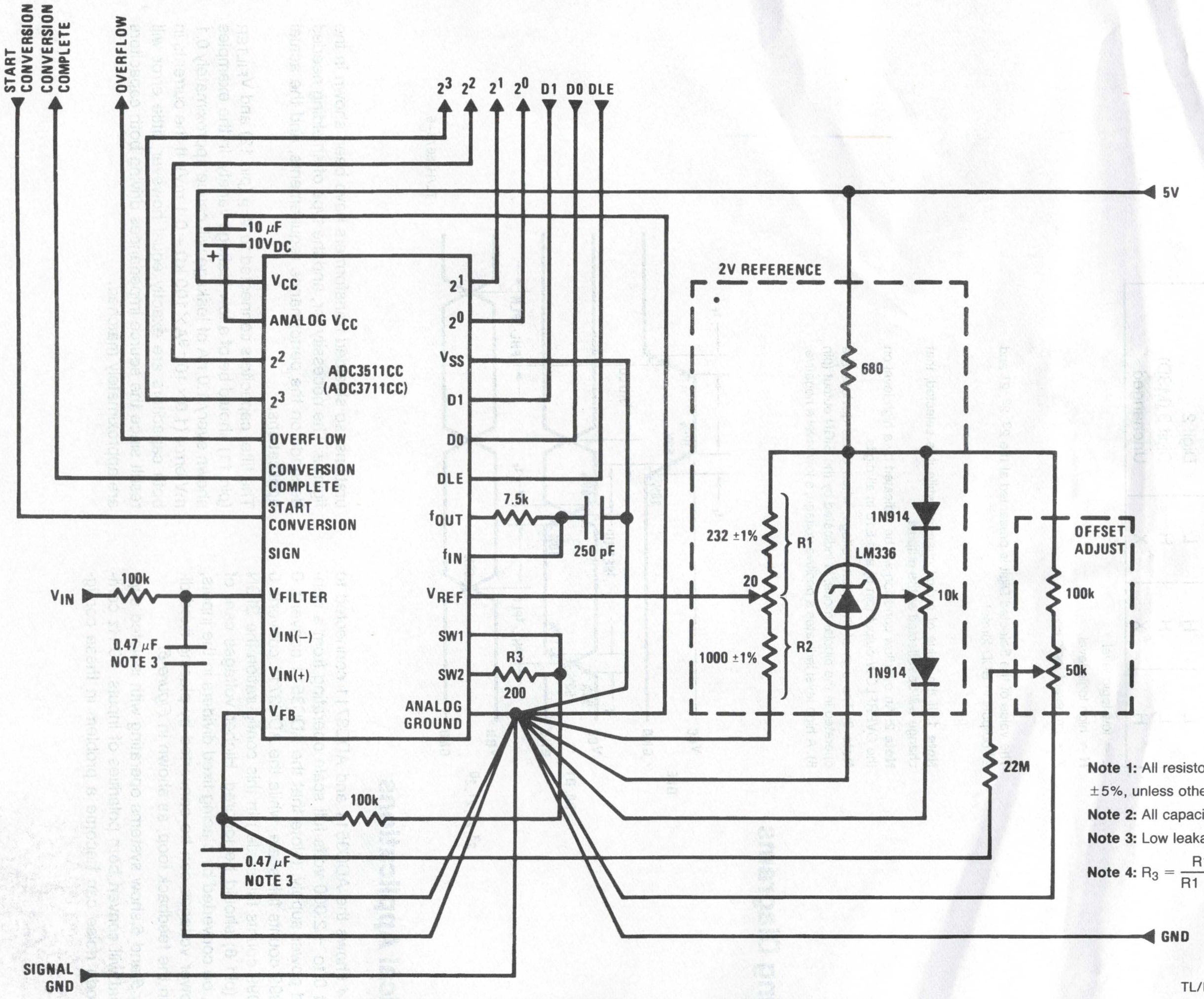
Typical Applications

Figure 4 shows the ADC3511 and ADC3711 connected to convert 0 to +2.000 volts full scale operating from a non-isolated power supply. (Note that the ADC3511 converts 0 to +1999 counts full scale, while the ADC3711 converts 0 to +3999 counts full scale.) In this configuration the SIGN output (pin 8) should be ignored. Higher voltages can, of course, be converted by placing fixed dividers in the inputs, while lower voltages can be converted by placing fixed dividers in the feedback loop, as shown in *Figure 6*.

Figures 5 and *6* show systems operating with isolated supplies that will convert both polarities of inputs. 60 Hz common-mode noise can become a problem in these configurations, so shielded transformers have been shown in the figures. The necessity for, and the type of shielding needed depends on the performance requirements, and the actual applications.

The filter capacitors connected to V_{FB} (pin 12) and V_{FILTER} (pin 11) should be of a low leakage variety. In the examples shown every 1.0 nA of leakage will cause approximately 0.1 mV error ($1.0 \times 10^{-9}A \times 100\ k\Omega = 0.1\ mV$). If the currents in both capacitors are exactly equal however, little error will result since the source impedances driving both capacitors are approximately matched.

Typical Applications (Continued)


START CONVERSION
CONVERSION COMPLETE
OVERFLOW
2^3 2^2 2^1 2^0 D1 D0 DLE
5V
10 μF
10V_{DC}
+
V_{CC}
ANALOG V_{CC}
2^2
2^3
OVERFLOW
CONVERSION COMPLETE
START CONVERSION
SIGN
V_{FILTER}
$V_{IN(-)}$
$V_{IN(+)}$
V_{FB}
ADC3511CC
(ADC3711CC)
2^1
2^0
V_{SS}
D1
D0
DLE
f_{OUT}
f_{IN}
V_{REF}
SW1
SW2
ANALOG GROUND
7.5k
250 pF
R3
200
2V REFERENCE
680
232 ±1%
20
1000 ±1%
R1
R2
1N914
LM336
10k
1N914
OFFSET ADJUST
100k
50k
22M
V_{IN}
100k
0.47 μF
NOTE 3
100k
0.47 μF
NOTE 3
SIGNAL GND
GND
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Note 1: All resistors ¼ watt, and ±5%, unless otherwise specified.

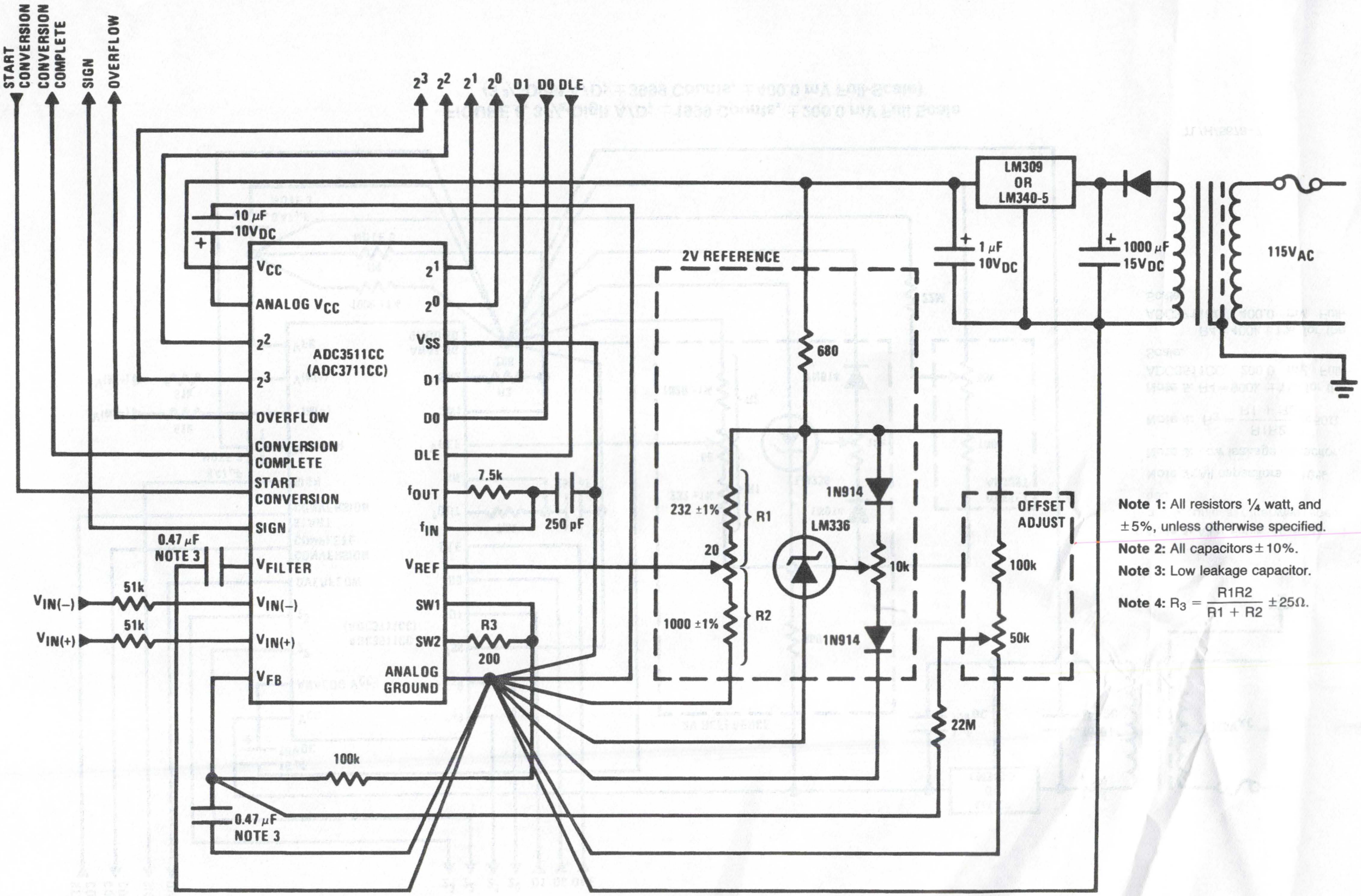
Note 2: All capacitors ±10%.

Note 3: Low leakage capacitor.

Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 25\Omega$.

FIGURE 4. 3 ½-Digit A/D; +1999 Counts, +2.000 Volts Full Scale
(3 ¾-Digit A/D; +3999 Counts, +2.000 Volts Full Scale)

Typical Applications (Continued)


START CONVERSION
CONVERSION COMPLETE
SIGN
OVERFLOW
2^3 2^2 2^1 2^0 D1 D0 DLE
10 μF
$10V_{DC}$
V_{CC}
ANALOG V_{CC}
2^2
2^3
ADC3511CC
(ADC3711CC)
OVERFLOW
CONVERSION COMPLETE
START CONVERSION
SIGN
V_{FILTER}
$V_{IN(-)}$
$V_{IN(+)}$
V_{FB}
2^1
2^0
V_{SS}
D1
D0
DLE
f_{OUT}
f_{IN}
V_{REF}
SW1
SW2
ANALOG GROUND
7.5k
250 pF
R3
200
0.47 μF
NOTE 3
$V_{IN(-)}$
$V_{IN(+)}$
51k
51k
100k
0.47 μF
NOTE 3
2V REFERENCE
680
232 ±1%
R1
20
1000 ±1%
R2
1N914
LM336
10k
1N914
OFFSET ADJUST
100k
50k
22M
LM309
OR
LM340-5
1 μF
$10V_{DC}$
1000 μF
$15V_{DC}$
$115V_{AC}$
TL/H/5678–6

Note 1: All resistors ¼ watt, and ±5%, unless otherwise specified.

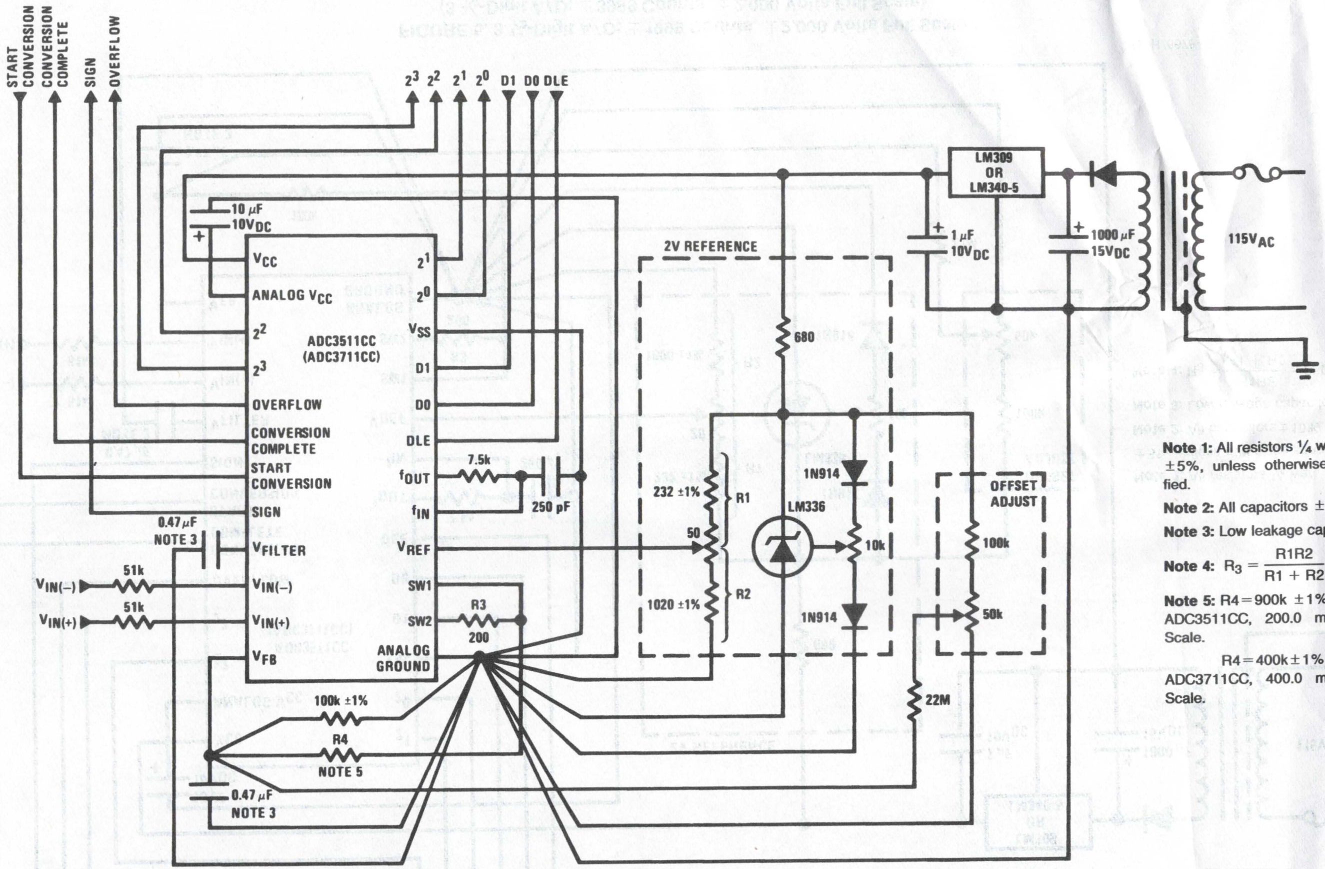
Note 2: All capacitors ±10%.

Note 3: Low leakage capacitor.

Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 25\Omega$.

FIGURE 5. 3 ½-Digit A/D; ±1999 Counts, ±2.000 Volts Full Scale
(3 ¾-Digit A/D; ±3999 Counts, ±2.000 Volts Full Scale)

Typical Applications (Continued)


START CONVERSION
CONVERSION COMPLETE
SIGN
OVERFLOW
2^3 2^2 2^1 2^0 D1 D0 DLE
10 µF
10V$_{DC}$
V$_{CC}$
ANALOG V$_{CC}$
2^2
2^3
OVERFLOW
CONVERSION COMPLETE
START CONVERSION
SIGN
V$_{FILTER}$
V$_{IN(-)}$
V$_{IN(+)}$
V$_{FB}$
ADC3511CC
(ADC3711CC)
2^1
2^0
V$_{SS}$
D1
D0
DLE
f$_{OUT}$
f$_{IN}$
V$_{REF}$
SW1
SW2
ANALOG GROUND
7.5k
250 pF
R3
200
0.47 µF
NOTE 3
51k
51k
V$_{IN(-)}$
V$_{IN(+)}$
100k ±1%
R4
NOTE 5
0.47 µF
NOTE 3
2V REFERENCE
680
232 ±1%
R1
50
1020 ±1%
R2
LM336
1N914
10k
1N914
OFFSET ADJUST
100k
50k
22M
LM309
OR
LM340-5
1 µF
10V$_{DC}$
1000 µF
15V$_{DC}$
115V$_{AC}$

Note 1: All resistors ¼ watt, and ±5%, unless otherwise specified.

Note 2: All capacitors ±10%

Note 3: Low leakage capacitor.

Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 50\Omega$

Note 5: R4 = 900k ±1% for the ADC3511CC, 200.0 mV Full-Scale.

R4 = 400k ± 1% for the ADC3711CC, 400.0 mV Full-Scale.

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FIGURE 6. 3 ½-Digit A/D; ±1999 Counts, ±200.0 mV Full Scale
(3 ¾-Digit A/D; ±3999 Counts, ±400.0 mV Full-Scale)

National Semiconductor Corporation

ADD3501 3½ Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3501 monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3501 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included on all 4 versions of this product.

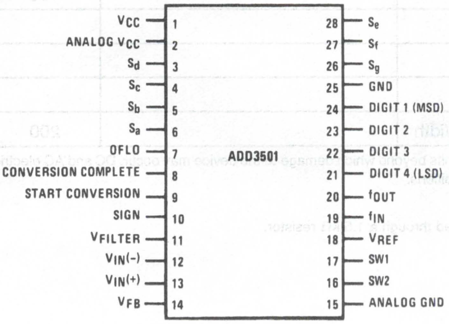
Features

- Operates from single 5V supply
- Converts 0V to ±1.999V
- Multiplexed 7-segment
- Drives segments directly
- No external precision component necessary
- Accuracy specified over temperature
- Medium speed - 200ms/conversion
- Internal clock set with RC network or driven externally
- Overrange Indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram



TL/H/5681–1

Order Number ADD3501CCN
See NS Package Number N28B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range (T_A)	−40°C to +85°C
ESD Susceptibility (Note 3)	TBDV
Package Dissipation at $T_A = 25°C$	800 mW
derate at $\theta_{JA(MAX)} = 125°C/Watt$ above $T_A = 25°C$	
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temp. (Soldering, 10 seconds)	260°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics ADD3501

4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ(2)	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs except Digit Outputs)	$I_O = 1.1$ mA			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	$I_O = 0.7$ mA			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	$I_O = 50$ mA@$T_J = 25°C$ $V_{CC} = 5V$ $I_O = 30$ mA@$T_J = 100°C$	$V_{CC}-1.6$ $V_{CC}-1.6$	$V_{CC}-1.3$ $V_{CC}-1.3$		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs except Segment Outputs)	$I_O = 500\mu A$ (Digit Outputs) $I_O = 360\mu A$ (Conv. Complete, +/−, Oflo Outputs)	$V_{CC}-0.4$			V
I_{SOURCE}	Output Source Current (Digit Outputs)	$V_{OUT} = 1.0V$	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	$V_{IN} = 1.5V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	$V_{IN} = 0V$	−1.0			μA
I_{CC}	Supply Current	Segments and Digits Open		0.5	10	mA
f_{OSC}	Oscillator Frequency			0.6/RC		kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			$f_{IN}/64,512$		conv./sec
f_{MUX}	Digit Mux Rate			$f_{IN}/256$		Hz
t_{BLANK}	Inter Digit Blanking Time			$1/(32f_{MUX})$		sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All typicals given for $T_A = 25°C$.

Note 3: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

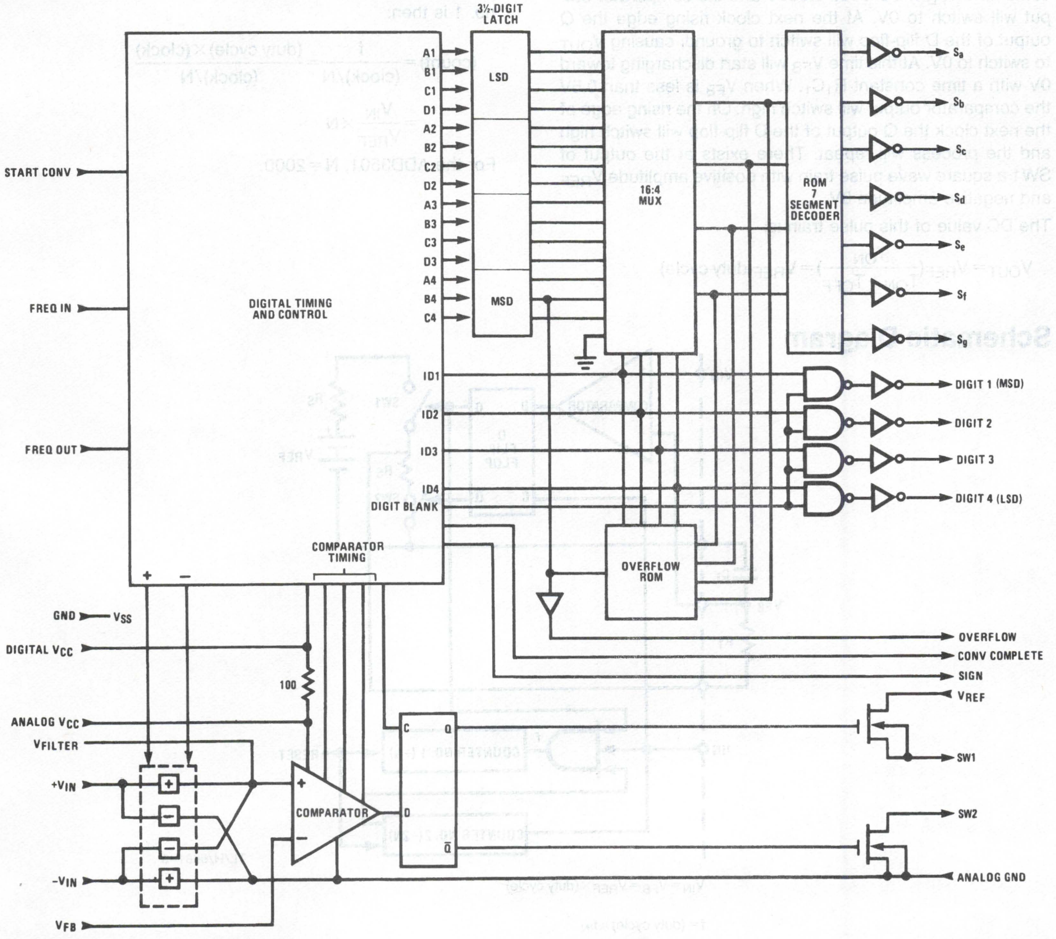
Electrical Characteristics ADD3501

$t_C = 5$ conversions/second, $0°C \le T_A \le 70°C$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Non-Linearity	$V_{IN} = 0 - 2V$ Full Scale $V_{IN} = 0 - 200mV$ Full Scale	−0.05 −0.05	±0.025 ±0.025	+0.05 +0.05	% of full scale
Quantization Error		−1		+0	counts
Offset Error, $V_{IN} = 0V$		−0.5	+1.5	+3	mV
Rollover Error		−0		+0	counts
Analog Input Current ($V_{IN}+$, $V_{IN}-$)	$T_A = 25°C$	−5	±0.5	+5	nA

Block Diagram

ADD3501 3½-Digit DVM Block Diagram


3½-DIGIT LATCH
LSD
MSD
A1
B1
C1
D1
A2
B2
C2
D2
A3
B3
C3
D3
A4
B4
C4
START CONV
FREQ IN
FREQ OUT
DIGITAL TIMING AND CONTROL
16:4 MUX
ROM 7 SEGMENT DECODER
S_a
S_b
S_c
S_d
S_e
S_f
S_g
ID1
ID2
ID3
ID4
DIGIT BLANK
DIGIT 1 (MSD)
DIGIT 2
DIGIT 3
DIGIT 4 (LSD)
OVERFLOW ROM
COMPARATOR TIMING
+
−
GND
V_{SS}
DIGITAL V_{CC}
100
ANALOG V_{CC}
V_{FILTER}
+V_{IN}
−V_{IN}
V_{FB}
COMPARATOR
C
Q
D
Q̄
OVERFLOW
CONV COMPLETE
SIGN
VREF
SW1
SW2
ANALOG GND

TL/H/5681-2

Theory of Operation

A schematic for the analog loop is shown in *Figure 1.* The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level $V_{OUT}=V_{REF}$ and if Q is at a low level $V_{OUT}=0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and Q outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time V_{FB} will start discharging toward 0V with a time constant R_1C_1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT}=V_{REF}\left(\frac{T_{ON}}{T_{ON}+T_{OFF}}\right)=V_{REF}(\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB}=V_{REF}(\text{duty cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN}=V_{FB}=V_{REF}(\text{duty cycle})$$

or

$$\frac{V_{IN}}{V_{REF}}=(\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f=(\text{duty cycle})\times(\text{clock})$$

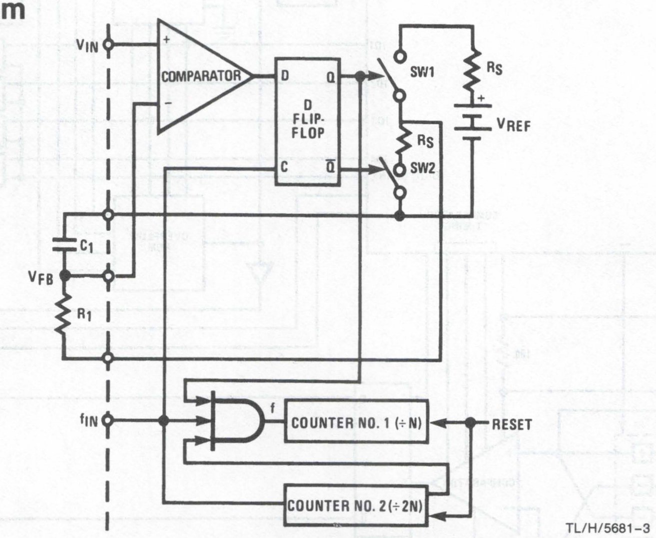
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count})=\frac{f}{(\text{clock})/N}=\frac{(\text{duty cycle})\times(\text{clock})}{(\text{clock})/N}$$

$$=\frac{V_{IN}}{V_{REF}}\times N$$

For the ADD3501, N = 2000.

Schematic Diagram



$V_{IN}=V_{FB}=V_{REF}\times(\text{duty cycle})$

$f=(\text{duty cycle})\times f_{IN}$

$$\text{Count in Counter No. 1}=\frac{f}{f_{IN}/N}=\frac{(\text{duty cycle})\times f_{In}}{f_{IN}/N}=\frac{V_{IN}}{V_{REF}}\times N$$

Figure 1. Analog Loop Schematic Pulse Modulation A/D Converter

General Information

The timing diagram, shown in *Figure 2*, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to $64{,}512 \times 1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to $64 \times 1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way.

Internally the ADD3501 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3*, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is $64{,}512 \times 1/f_{IN}$ and the minimum time is $256 \times 1/f_{IN}$.

Timing Waveforms

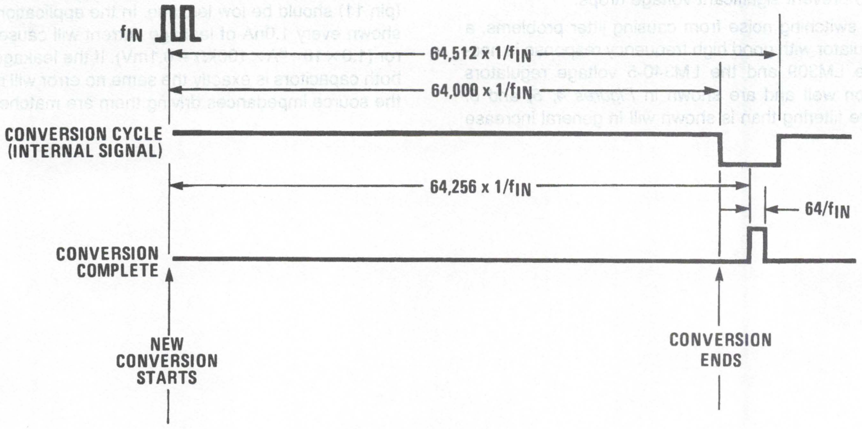

fIN
64,512 x 1/fIN
64,000 x 1/fIN
CONVERSION CYCLE (INTERNAL SIGNAL)
64,256 x 1/fIN
64/fIN
CONVERSION COMPLETE
NEW CONVERSION STARTS
CONVERSION ENDS

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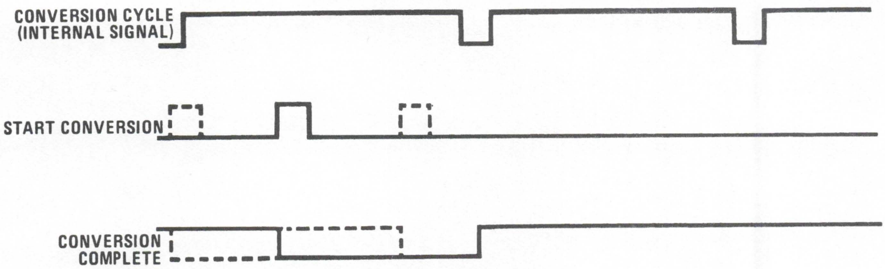
Figure 2. Conversion Cycle Timing Diagram for Free Running Operation


CONVERSION CYCLE (INTERNAL SIGNAL)
START CONVERSION
CONVERSION COMPLETE

TL/H/5681–5

Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3501 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3501 to minimize these problems but poor printed circuit layout can negate these features.

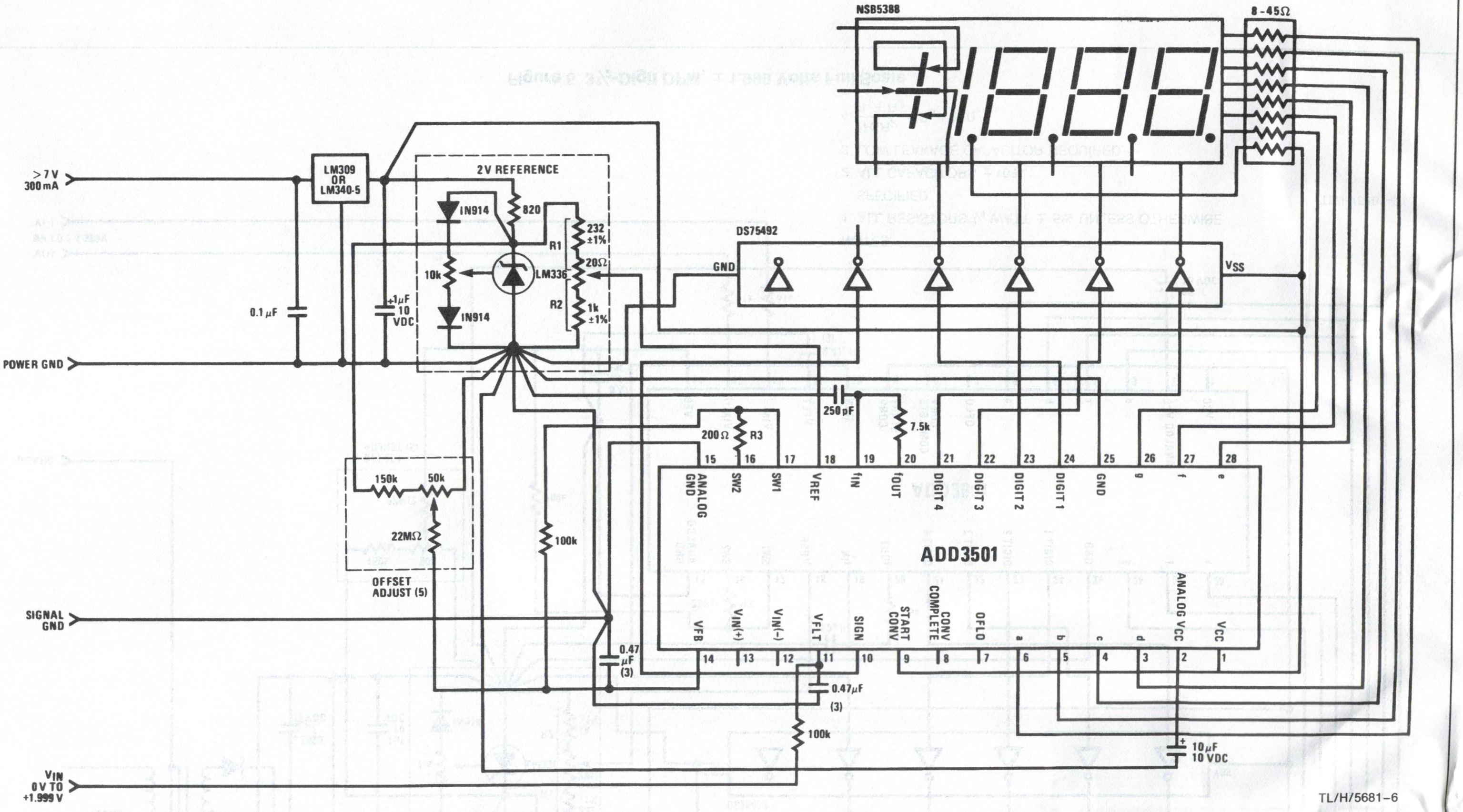
Figures 4, 5, and *6* show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators both function well and are shown in *Figures 4, 5,* and *6.* Adding more filtering than is shown will in general increase the jitter rather than decrease it. The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0V to 1.999V operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or − (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in *Figure 6.*

Figures 5 and *6* show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

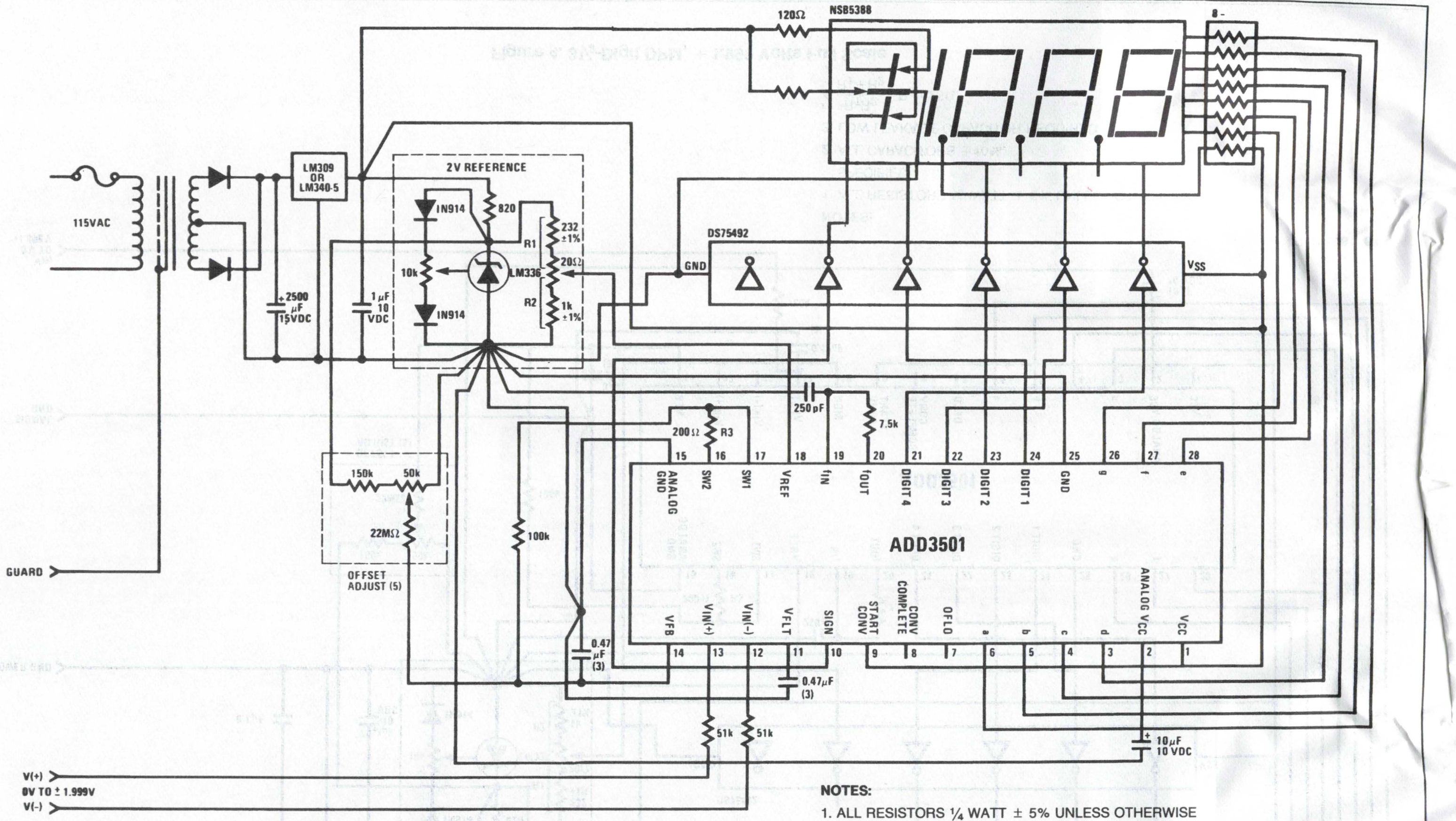
The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0nA of leakage current will cause 0.1mV error ($1.0 \times 10^{-9}A \times 100k\Omega = 0.1mV$). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.


NSB5388
8 - 45Ω
DS75492
GND
VSS
LM309 OR LM340-5
>7 V 300 mA
2V REFERENCE
IN914
820
10k
LM336
IN914
232 ±1%
R1
20Ω
R2
1k ±1%
0.1 µF
1µF 10 VDC
POWER GND
250 pF
7.5k
200Ω
R3
150k
50k
22MΩ
OFFSET ADJUST (5)
100k
SIGNAL GND
0.47 µF (3)
0.47µF (3)
100k
VIN 0V TO +1.999 V
10µF 10 VDC
ADD3501
15 ANALOG GND
16 SW2
17 SW1
18 VREF
19 fIN
20 fOUT
21 DIGIT 4
22 DIGIT 3
23 DIGIT 2
24 DIGIT 1
25 GND
26 g
27 f
28 e
14 VFB
13 VIN(+)
12 VIN(-)
11 VFLT
10 SIGN
9 START CONV
8 CONV COMPLETE
7 OFLO
6 a
5 b
4 c
3 d
2 ANALOG VCC
1 VCC
TL/H/5681-6

NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$

Figure 4. 3½-Digit DPM, + 1.999 Volts Full Scale

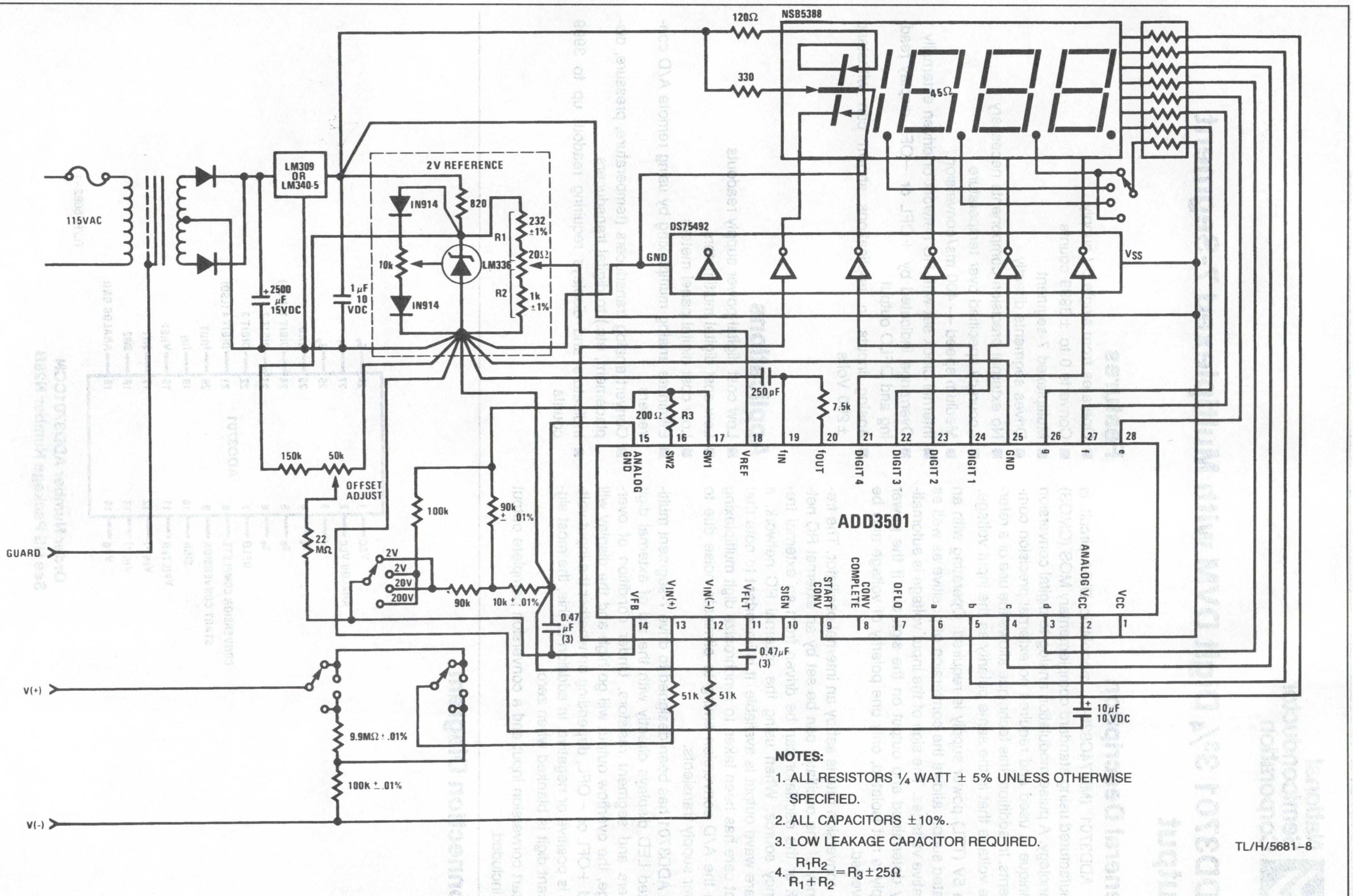

120Ω
NSB5388
8 -
LM309
OR
LM340-5
2V REFERENCE
115VAC
IN914
820
10k
LM336
R1
232
±1%
20Ω
R2
1k
±1%
IN914
+2500
μF
15VDC
1 μF
10
VDC
DS75492
GND
VSS
250 pF
200Ω
R3
7.5k
150k
50k
22MΩ
OFFSET
ADJUST (5)
100k
GUARD
0.47
μF
(3)
0.47μF
(3)
51k
51k
10μF
10 VDC
V(+)
0V TO ± 1.999V
V(-)
15
16
17
18
19
20
21
22
23
24
25
26
27
28
ANALOG
GND
SW2
SW1
VREF
fIN
fOUT
DIGIT 4
DIGIT 3
DIGIT 2
DIGIT 1
GND
g
f
e
ADD3501
VFB
VIN(+)
VIN(-)
VFLT
SIGN
START
CONV
CONV
COMPLETE
OFLO
a
b
c
d
ANALOG VCC
VCC
14
13
12
11
10
9
8
7
6
5
4
3
2
1

NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$

TL/H/5681-7

Figure 5. 3½-Digit DPM, ±1.999 Volts Full Scale


120Ω
NSB5388
330
45Ω
2V REFERENCE
LM309
OR
LM340-5
115VAC
IN914
820
R1
232
±1%
20Ω
10k
LM336
R2
1k
±1%
IN914
2500
μF
15VDC
1 μF
10
VDC
DS75492
GND
V_{SS}
250 pF
7.5k
200 Ω
R3
15
16
17
18
19
20
21
22
23
24
25
26
27
28
ANALOG GND
SW2
SW1
V_{REF}
f_{IN}
f_{OUT}
DIGIT 4
DIGIT 3
DIGIT 2
DIGIT 1
GND
g
f
e
ADD3501
VFB
$V_{IN}(+)$
$V_{IN}(-)$
VFLT
SIGN
START CONV
CONV COMPLETE
OFLO
a
b
c
d
ANALOG V_{CC}
V_{CC}
14
13
12
11
10
9
8
7
6
5
4
3
2
1
150k
50k
OFFSET
ADJUST
100k
90k
± .01%
GUARD
22
MΩ
2V
2V
20V
200V
90k
10k ± .01%
0.47
μF
(3)
0.47μF
(3)
51k
51k
10μF
10 VDC
V(+)
9.9MΩ ± .01%
100K ± .01%
V(-)

NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$

TL/H/5681-8

Figure 6. 3½-Digit DVM, Four Decade, ±0.2V, ±2V, ±20V and ±200V Full Scale

National
Semiconductor
Corporation

ADD3701 3¾ Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3701 (MM74C936-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3701 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included.

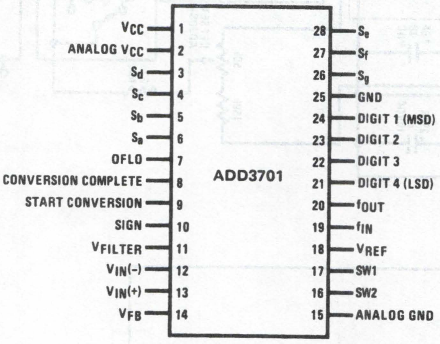
Features

- Operates from single 5V supply
- Converts 0 to ±3999 counts
- Multiplexed 7-segment
- Drives segments directly
- No external precision components necessary
- Accuracy specified over temperature
- Medium speed — 400 ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers
- Indicators and displays requiring readout up to 3999 counts

Connection Diagram



TL/H/5682-1

Order Number ADD3701CCN
See NS Package Number N28B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin except Start Conversion	$-0.3V$ to $V_{CC}+0.3V$
Voltage at Start Conversion	$-0.3V$ to $+15.0V$
ESD Susceptibility (Note 5)	TBDV

Operating Temperature Range (T_A)	−40°C to +85°C
Package Dissipation at $T_A=25°C$	800mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temp. (Soldering, 10 seconds)	260°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics

$4.75V \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$, unless otherwise specified.

	Parameter	Conditions	Min	Typ[2]	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs Except Digital Outputs)	$I_O=1.1$ mA			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	$I_O=0.7$ mA			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	$I_O=50$ mA @ $T_J=25°C$ $V_{CC}=5V$ $I_O=30$ mA @ $T_J=100°C$	$V_{CC}-1.6$ $V_{CC}-1.6$	$V_{CC}-1.3$ $V_{CC}-1.3$		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs Except Segment Outputs)	$I_O=500\ \mu A$ (Digit Outputs) $I_O=360\ \mu A$ (Conv. Complete, +/−, OFLO Outputs)	$V_{CC}-0.4$			V
I_{SOURCE}	Output Source Current (Digital Outputs)	$V_{OUT}=1.0$ V	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	$V_{IN}=15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	$V_{IN}=0V$	−1.0			μA
I_{CC}	Supply Current	Segments and Digits Open		0.5	10	mA
f_{OSC}	Oscillator Frequency			0.6/RC		kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			$f_{IN}/129{,}024$		conv./sec
f_{MUX}	Digit Mux Rate			$f_{IN}/512$		Hz
t_{BLANK}	Inter Digit Blanking Time			$1/(32f_{MUX})$		seconds
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All typicals given for $T_A=25°C$.

Note 3: Full scale=4000 counts; therefore 0.025% of full scale =1 count and 0.05% of full scale=2 counts.

Note 4: For 2.000 Volts full scale, 1 mV=2 counts.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

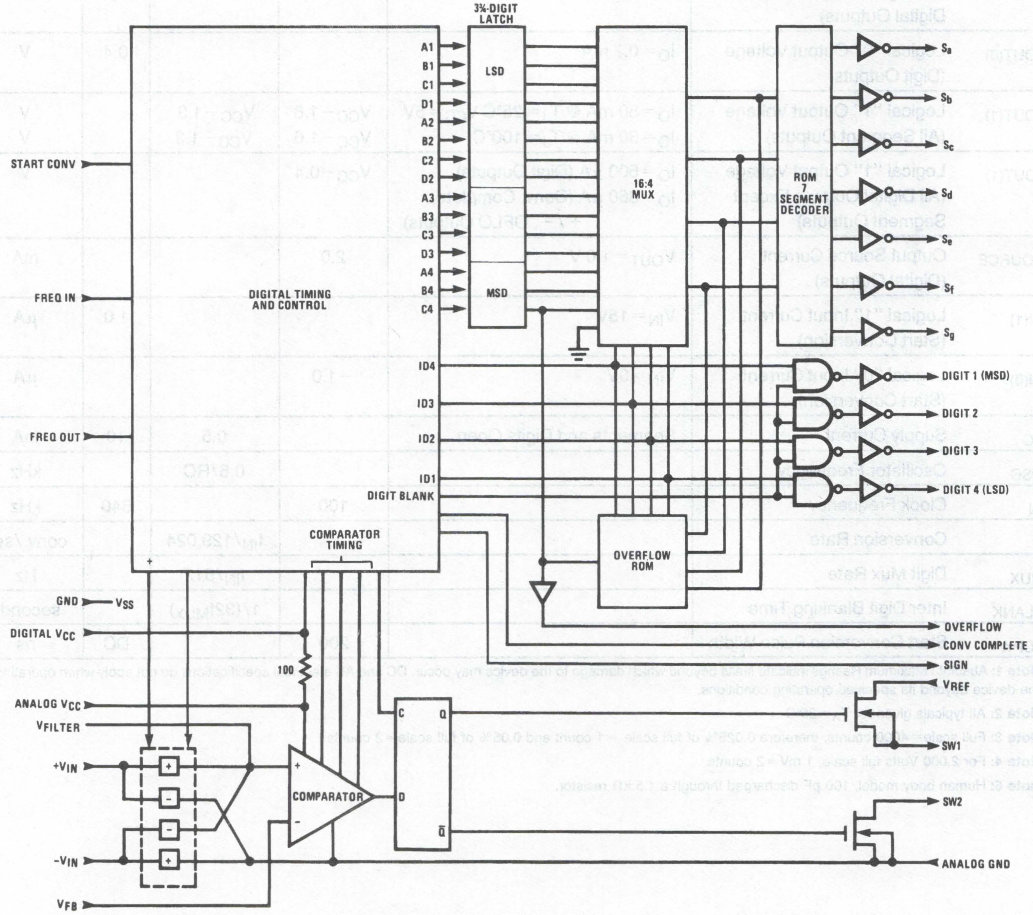
Electrical Characteristics (Continued)

$t_C = 2.5$ conversions/second, $0°C \leq T_A \leq +70°C$, unless otherwise specified.

Parameter	Conditions	Min	Typ^2	Max	Units
Non-Linearity of Output Reading	$V_{IN} = 0-2V$ Full Scale $V_{IN} = 0-200$ mV Full Scale	−0.05 −0.05	±0.025 ±0.025	±0.05 ±0.05	% full scale (Note 3)
Quantization Error		−1		+0	counts
Offset Error, $V_{IN} = 0V$		−0.5	+1.5	+3	mV (Note 4)
Rollover Error		−0		+0	counts
Analog Input Current ($V_{IN}+$, $V_{IN}-$)	$T_A = 25°C$	−5	±1	+5	nA

Block Diagram

ADD3701 3¾-Digit DVM


3¾-DIGIT LATCH
LSD
MSD
A1
B1
C1
D1
A2
B2
C2
D2
A3
B3
C3
D3
A4
B4
C4
START CONV
FREQ IN
DIGITAL TIMING AND CONTROL
ID4
ID3
ID2
ID1
DIGIT BLANK
FREQ OUT
COMPARATOR TIMING
+
GND
VSS
DIGITAL VCC
100
ANALOG VCC
VFILTER
+VIN
-VIN
VFB
+
−
COMPARATOR
C
Q
D
Q̄
16:4 MUX
ROM 7 SEGMENT DECODER
OVERFLOW ROM
Sa
Sb
Sc
Sd
Se
Sf
Sg
DIGIT 1 (MSD)
DIGIT 2
DIGIT 3
DIGIT 4 (LSD)
OVERFLOW
CONV COMPLETE
SIGN
VREF
SW1
SW2
ANALOG GND

TL/H/5682-2

Theory of Operation

A schematic for the analog loop is shown in *Figure 1*. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and Q outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500 V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000 V) and V_{FB} will charge toward 2 V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500 V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time V_{FB} will start discharging toward 0V with a time constant R_1C_1. When V_{FB} is less than 0.5 V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\frac{t_{ON}}{t_{ON}+t_{OFF}} = V_{REF}\text{ (duty cycle)}$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}\text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}\text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times \text{(clock)}$$

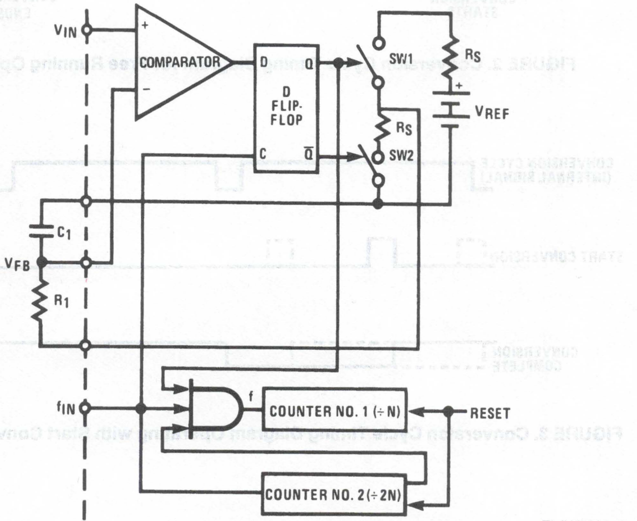
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{(count)} = \frac{f}{\text{(clock)}/N} = \frac{\text{(duty cycle)}\times\text{(clock)}}{\text{(clock)}/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3701 N = 4000.

Schematic Diagram



TL/H/5682–3

$$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$$

$$f = \text{(duty cycle)} \times f_{IN}$$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)}\times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE 1. Analog Loop Schematic Pulse Modulation A/D Converter

General Information

The timing diagram, shown in *Figure 2*, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to $129{,}024 \times 1/f_{IN}$.

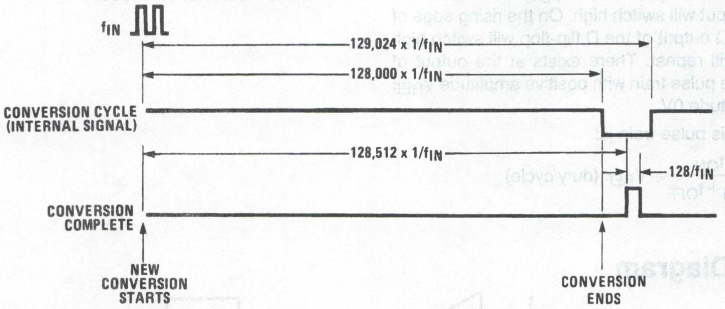
The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to $128 \times 1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way.

Internally the ADD3701 is always continuously converting the analog voltage present at its input. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

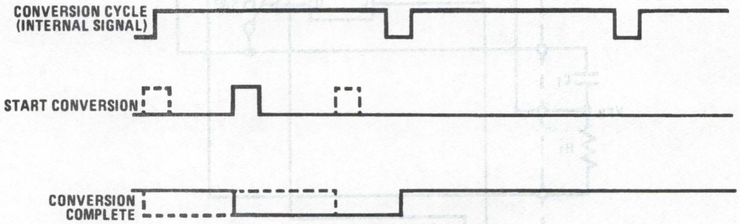
An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3*, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is $129{,}024 \times 1/f_{IN}$ and the minimum time is $512 \times 1/f_{IN}$.

Timing Waveforms


f_IN
129,024 x 1/f_IN
128,000 x 1/f_IN
CONVERSION CYCLE (INTERNAL SIGNAL)
128,512 x 1/f_IN
128/f_IN
CONVERSION COMPLETE
NEW CONVERSION STARTS
CONVERSION ENDS

TL/H/5682-4

FIGURE 2. Conversion Cycle Timing Diagram for Free Running Operation


CONVERSION CYCLE (INTERNAL SIGNAL)
START CONVERSION
CONVERSION COMPLETE

TL/H/5682-5

FIGURE 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3701 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3701 to minimize these problems but poor printed circuit layout can negate these features.

Figures 4, 5, and *6* show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

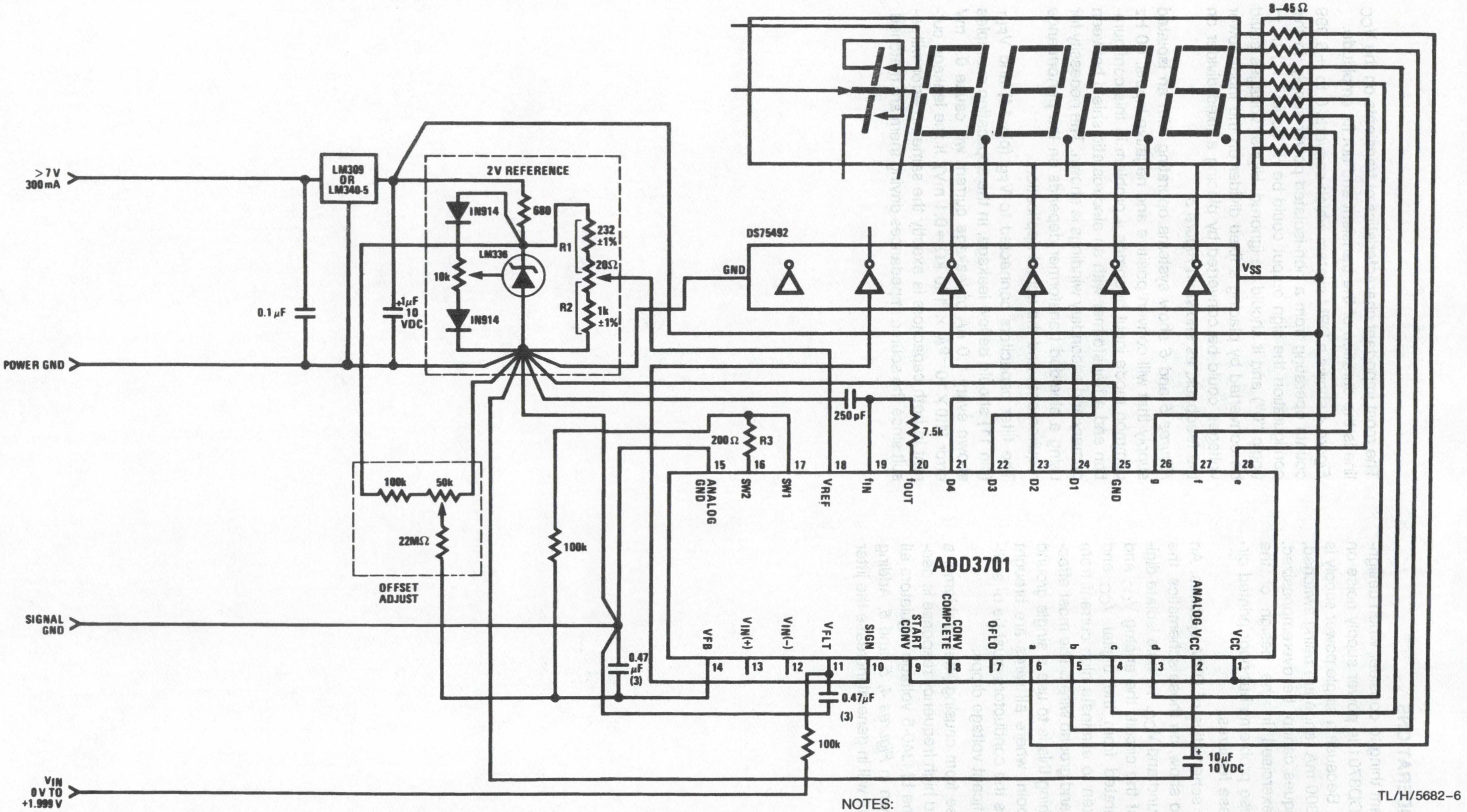
To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators all function well and are shown in *Figures 4, 5,* and *6.* Adding more filtering than is shown will in general increase the jitter rather than decrease it.

The most important characteristics of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0 to +3.999 counts operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or − (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in *Figure 5.*

Figures 5 and *6* show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0 nA of leakage current will cause 0.1 mV error ($1.0\times10^{-9}A \times 100\ k\Omega = 0.1\ mV$). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.

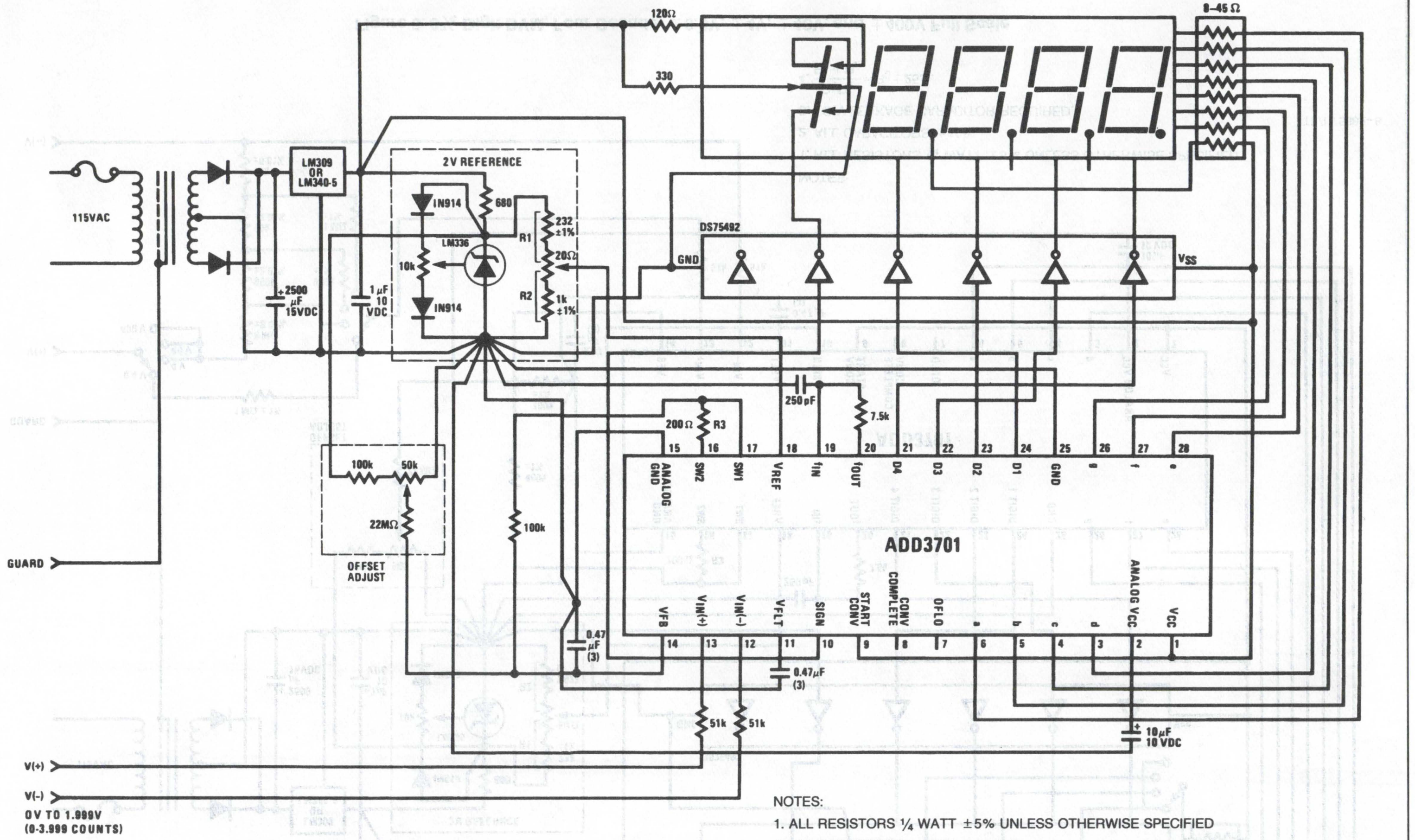

8–45 Ω
>7 V
300 mA
LM309
OR
LM340-5
2V REFERENCE
IN914
680
232
±1%
R1
20Ω
LM336
10k
R2
1k
±1%
0.1 µF
1µF
10
VDC
IN914
POWER GND
DS75492
GND
VSS
250 pF
7.5k
200 Ω
R3
15
16
17
18
19
20
21
22
23
24
25
26
27
28
ANALOG GND
SW2
SW1
VREF
fIN
fOUT
D4
D3
D2
D1
GND
g
f
e
100k
50k
22MΩ
OFFSET
ADJUST
100k
ADD3701
SIGNAL
GND
0.47
µF
(3)
VFB
VIN(+)
VIN(−)
VFLT
SIGN
START
CONV
CONV
COMPLETE
OFLO
a
b
c
d
ANALOG VCC
VCC
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0.47µF
(3)
100k
10µF
10 VDC
VIN
0 V TO
+1.999 V

TL/H/5682-6

NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED
2. ALL CAPACITORS ±10%
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1 + R_2} = R3 \pm 25\Omega$

Figure 4. 3¾-Digital DPM, +3.999 Count Full Scale


120Ω
330
8–45 Ω
115VAC
LM309
OR
LM340-5
2V REFERENCE
IN914
680
LM336
10k
IN914
232
±1%
R1
20Ω
R2
1k
±1%
+2500
μF
15VDC
1 μF
10
VDC
DS75492
GND
VSS
250 pF
7.5k
200 Ω
R3
100k
50k
22MΩ
OFFSET
ADJUST
100k
GUARD
15
16
17
18
19
20
21
22
23
24
25
26
27
28
ANALOG GND
SW2
SW1
VREF
fIN
fOUT
D4
D3
D2
D1
GND
g
f
e
ADD3701
VFB
VIN(+)
VIN(−)
VFLT
SIGN
START CONV
CONV COMPLETE
OFLO
a
b
c
d
ANALOG VCC
VCC
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0.47
μF
(3)
0.47μF
(3)
51k
51k
10μF
10 VDC
V(+)
V(−)
0V TO 1.999V
(0-3.999 COUNTS)

NOTES:

1. ALL RESISTORS ¼ WATT ±5% UNLESS OTHERWISE SPECIFIED
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$.

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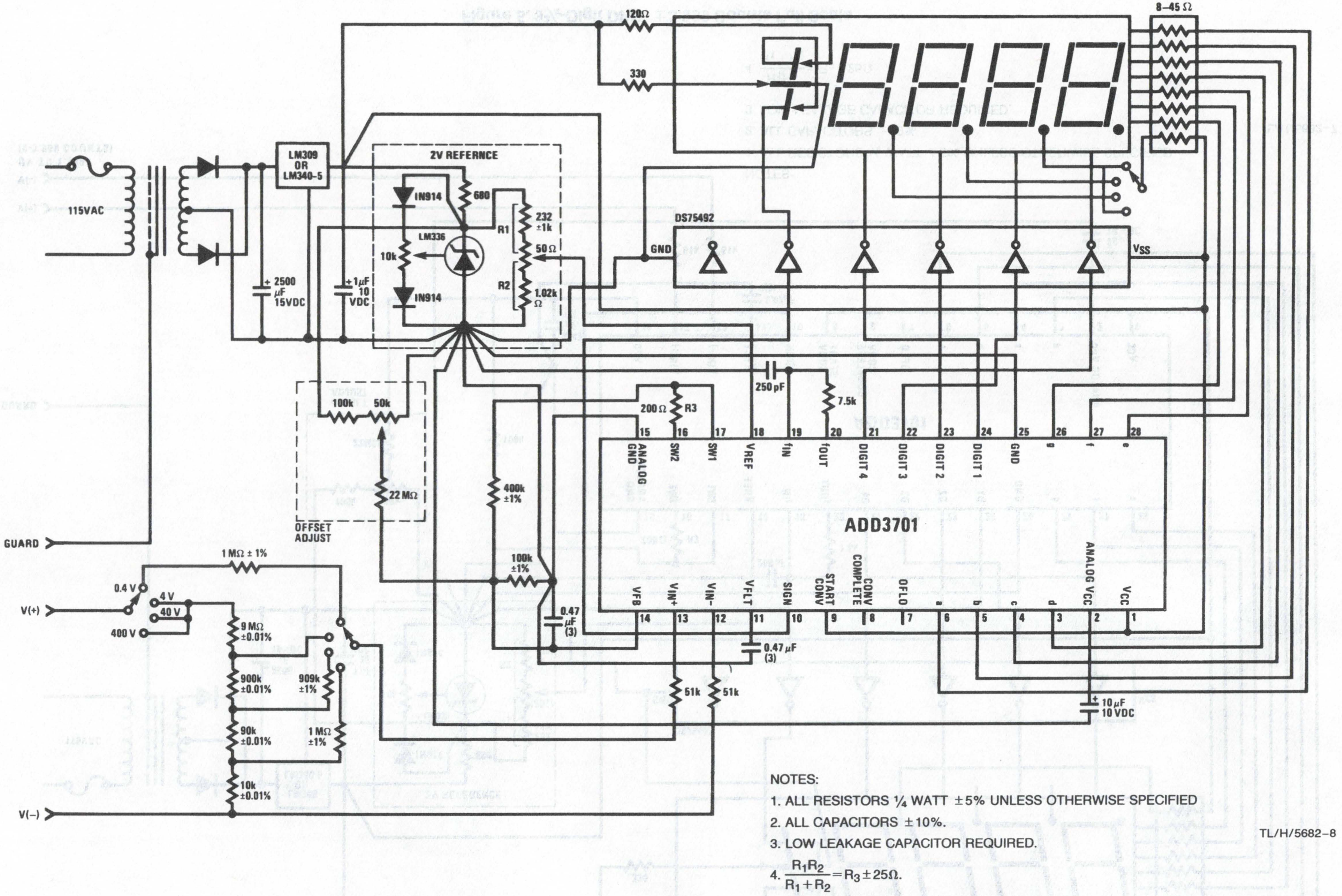
Figure 5. 3¾-Digit DPM, ±3.999 Counts Full Scale



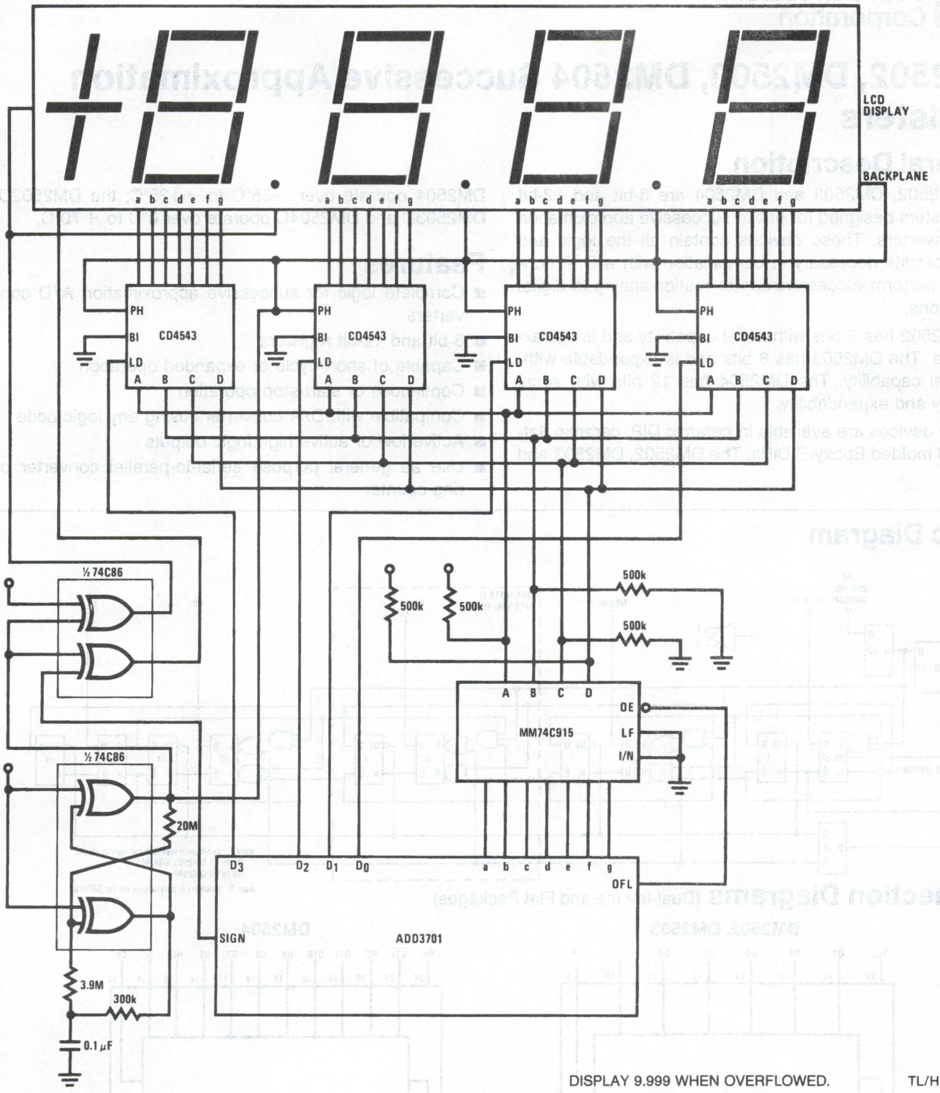
120Ω
330
8–45 Ω
LM309
OR
LM340-5
2V REFERNCE
IN914
680
LM336
10k
IN914
R1
232
±1k
50 Ω
R2
1.02k
Ω
115VAC
+ 2500
μF
15VDC
+1μF
10
VDC
DS75492
GND
VSS
250 pF
7.5k
200 Ω
R3
100k
50k
22 MΩ
OFFSET
ADJUST
400k
±1%
100k
±1%
0.47
μF
(3)
0.47 μF
(3)
51k
51k
+ 10 μF
10 VDC
GUARD
1 MΩ ± 1%
0.4 V
4 V
40 V
400 V
V(+)
V(–)
9 MΩ
±0.01%
900k
±0.01%
909k
±1%
90k
±0.01%
1 MΩ
±1%
10k
±0.01%
ADD3701
15 ANALOG GND
16 SW2
17 SW1
18 VREF
19 fIN
20 fOUT
21 DIGIT 4
22 DIGIT 3
23 DIGIT 2
24 DIGIT 1
25 GND
26 g
27 f
28 e
14 VFB
13 VIN+
12 VIN–
11 VFLT
10 SIGN
9 START CONV
8 CONV COMPLETE
7 OFLO
6 a
5 b
4 c
3 d
2 ANALOG VCC
1 VCC

NOTES:

1. ALL RESISTORS ¼ WATT ±5% UNLESS OTHERWISE SPECIFIED
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$.

TL/H/5682–8

Figure 6. 3¾-Digit DVM, Four Decade, ±0.4V, ±4V, ±40V, and ±400V Full Scale


LCD DISPLAY
BACKPLANE
a b c d e f g
PH
BI
LD
CD4543
A B C D
½ 74C86
20M
3.9M
300k
0.1 µF
500k
500k
500k
500k
MM74C915
A B C D
OE
LF
I/N
D3 D2 D1 D0
a b c d e f g
OFL
SIGN
ADD3701

DISPLAY 9.999 WHEN OVERFLOWED.
ALL DIGITS CAN ALSO BE BLANKED AT
OVERFLOW BY TYING OFL TO B1 ON THE
CD4543s.

TL/H/5682-9

Figure 7. ADD3701 Driving Liquid Crystal Display

National Semiconductor Corporation

DM2502, DM2503, DM2504 Successive Approximation Registers

General Description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary in combination with a D/A converter to perform successive approximation analog-to-digital conversions.

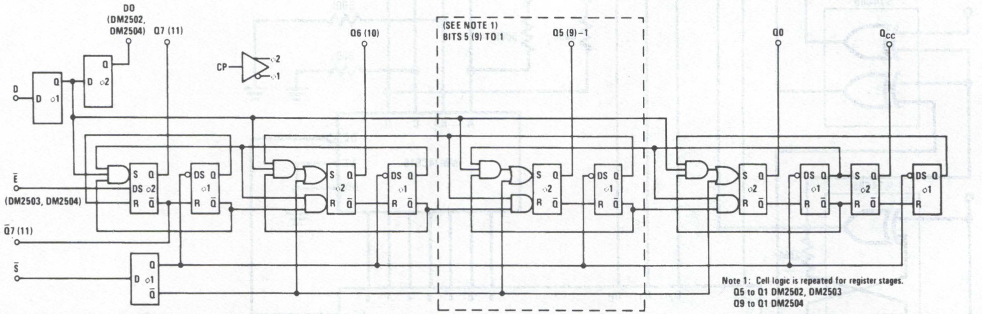
The DM2502 has 8 bits with serial capability and is not expandable. The DM2503 has 8 bits and is expandable without serial capability. The DM2504 has 12 bits with serial capability and expandability.

All three devices are available in ceramic DIP, ceramic flatpak, and molded Epoxy-B DIPs. The DM2502, DM2503 and DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.

Features

- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

Logic Diagram

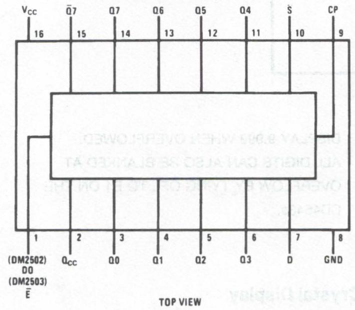

D0 (DM2502, DM2504)
Q7 (11)
Q6 (10)
(SEE NOTE 1) BITS 5 (9) TO 1
Q5 (9)−1
Q0
Q_{CC}
CP
φ2
φ1
D
Ē
(DM2503, DM2504)
Q̄7 (11)
S̄
S Q DS φ2 R Q̄
DS Q φ1 R Q̄
D φ1 Q Q̄

Note 1: Cell logic is repeated for register stages. Q5 to Q1 DM2502, DM2503 Q9 to Q1 DM2504

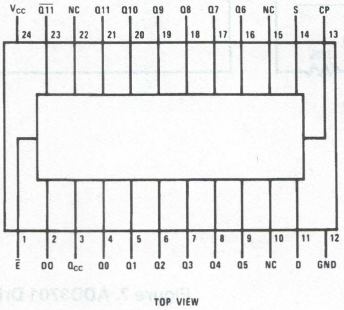
Note 2: Numbers in parentheses are for DM2504.

Connection Diagrams (Dual-In-Line and Flat Packages)

DM2502, DM2503


V_{CC} 16
Q̄7 15
Q7 14
Q6 13
Q5 12
Q4 11
S̄ 10
CP 9
1 (DM2502) D0 (DM2503) Ē
2 Q_{CC}
3 Q0
4 Q1
5 Q2
6 Q3
7 D
8 GND
TOP VIEW

DM2504


V_{CC} 24
Q̄11 23
NC 22
Q11 21
Q10 20
Q9 19
Q8 18
Q7 17
Q6 16
NC 15
S̄ 14
CP 13
1 Ē
2 D0
3 Q_{CC}
4 Q0
5 Q1
6 Q2
7 Q3
8 Q4
9 Q5
10 NC
11 D
12 GND
TOP VIEW

TL/F/5702–1

Order Number DM2502J, DM2502CJ, DM2503J or DM2503CJ
See NS Package J16A
Order Number DM2502CN or DM2503CN
See NS Package N16A
Order Number DM2502W, DM2502CW, DM2503W, or DM2503CW
See NS Package W16A

Order Number DM2504F or DM2504CJ
See NS Package F24D
Order Number DM2504J or DM2504CJ
See NS Package J24A
Order Number DM2504CN
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DM2502C, DM2503C, DM2504C	4.75	5.25	V
DM2502, DM2503, DM2504	4.5	5.5	V
Temperature, T_A			
DM2502C, DM2503C, DM2504C	0	+70	°C
DM2502, DM2503 DM2504	−55	+125	°C

Electrical Characteristics (Notes 2 and 3) $V_{CC}=5.0V$, $T_A=25°C$, $C_L=15$ pF, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Logical “1” Input Voltage (V_{IH})	$V_{CC}=$ Min	2.0			V
Logical “1” Input Current (I_{IH})	$V_{CC}=$ Max				
CP Input	$V_{IH}=2.4V$		6	40	μA
D, $\overline{E}$, $\overline{S}$ Inputs	$V_{IH}=2.4V$		6	80	μA
All Inputs	$V_{IH}=5.5V$			1.0	mA
Logical “0” Input Voltage (V_{IL})	$V_{CC}=$ Min			0.8	V
Logical “0” Input Current (I_{IL})	$V_{CC}=$ Max				
CP, $\overline{S}$ Inputs	$V_{IL}=0.4V$		−1.0	−1.6	mA
D, E Inputs	$V_{IL}=0.4V$		−1.0	−3.2	mA
Logical “1” Output Voltage (V_{OH})	$V_{CC}=$ Min, $I_{OH}=0.48$ mA	2.4	3.6		V
Output Short Circuit Current (Note 4) (I_{OS})	$V_{CC}=$ Max; $V_{OUT}=0.0V$; Output High; CP, D, $\overline{S}$, High; $\overline{E}$ Low	−10	−20	−45	mA
Logical “0” Output Voltage (V_{OL})	$V_{CC}=$ Min, $I_{OL}=9.6$ mA		0.2	0.4	V
Supply Current (I_{CC})	$V_{CC}=$ Max, All Outputs Low				
DM2502C			65	95	mA
DM2502			65	85	mA
DM2503C			60	90	mA
DM2503			60	80	mA
DM2504C			90	124	mA
DM2504			90	110	mA
Propagation Delay to a Logical “0” From CP to Any Output (t_{pd0})		10	18	28	ns
Propagation Delay to a Logical “0” From $\overline{E}$ to Q7 (Q11) Output (t_{pd0})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		16	24	ns
Propagation Delay to a Logical “1” From CP to Any Output (t_{pd1})		10	26	38	ns
Propagation Delay to a Logical “1” From $\overline{E}$ to Q7 (Q11) Output (t_{pd1})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		13	19	ns
Set-Up Time Data Input ($t_{s(D)}$)		−10	4	8	ns
Set-Up Time Start Input ($t_{s(\overline{S})}$)		0	9	16	ns
Minimum Low CP Width (t_{PWL})			30	42	ns
Minimum High CP Width (t_{PWH})			17	24	ns
Maximum Clock Frequency (f_{MAX})		15	21		MHz

Note 1: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM2502, DM2503 and DM2504, and across the 0°C to +70°C range for the DM2502C, DM2503C and DM2504C. All typicals are given for $V_{CC}=5.0V$ and $T_A=25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Application Information

OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ signal must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide nonoverlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator ½ full range + ½ LSB and using the complement of the MSB ($\overline{Q7}$ or $\overline{Q}11$) with a binary D/A converter. Offset binary is used in the same manner but with the MSB ($\overline{Q}7$ or $\overline{Q}11$). BCD D/A converters can be used with the addition of illegal code suppression logic.

ACTIVE HIGH OR ACTIVE LOW LOGIC

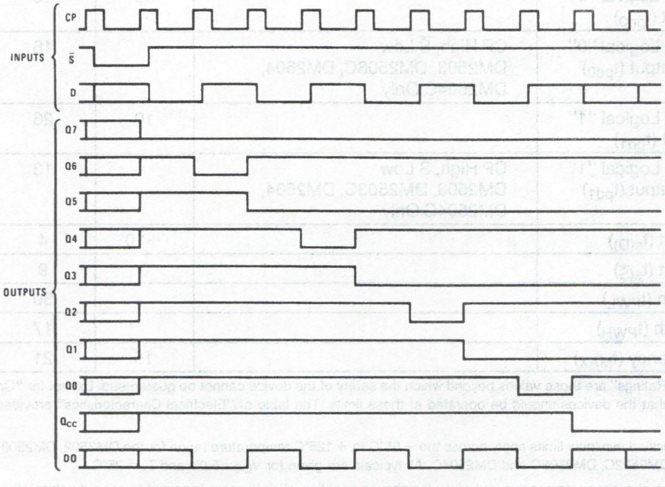
The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

Timing Diagram

DM2502, DM2503



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Application Information (Continued)

SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather then the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

COMPARATOR BIAS

To minimize the digital error below ±½ LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +½ LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −½ LSB.

Definition of Terms

CP: The clock input of the register.

D: The serial data input of the register.

DO: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_i i = 7 (11) to 0: The outputs of the register.

Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

Q7 (11): The true output of the MSB of the register.

$\overline{Q7}$ (11): The complement output of the MSB of the register.

$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

Truth Table

DM2502, DM2503

Time	Inputs			Outputs[1]									
t_n	D	$\overline{S}$	$\overline{E}$[2]	D0[3]	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

Note 1: Truth table for DM2504 is extended to include 12 outputs.

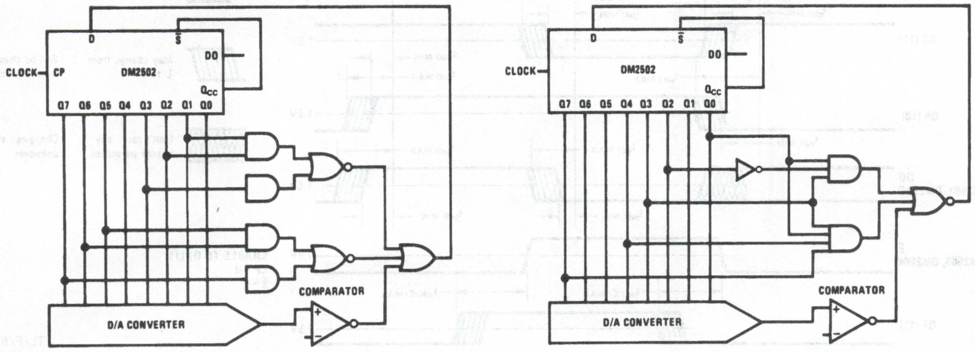
Note 2: Truth table for DM2502 does not include $\overline{E}$ column or last line in truth table shown.

Note 3: Truth table for DM2503 does not include D0 column.

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NC = No Change

Typical Applications

BCD Illegal Code Suppression



Active High

Active Low

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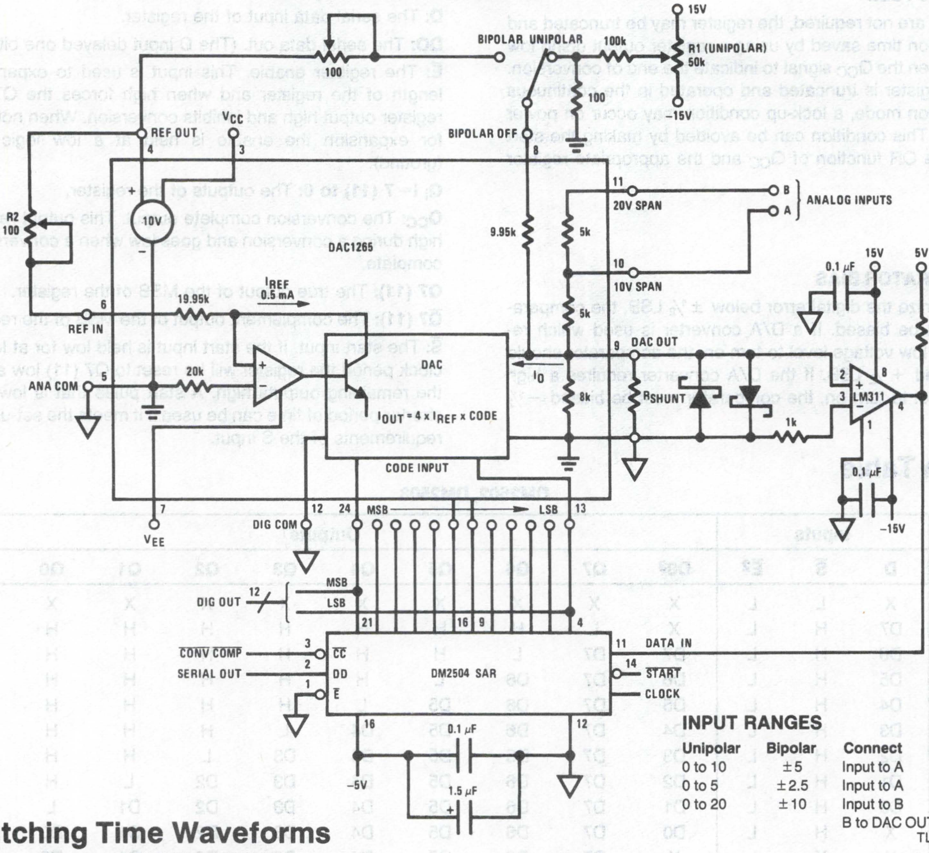
Typical Applications (Continued)

Fast Precision Analog-to-Digital Converter


15V
BIPOLAR UNIPOLAR
100k
R1 (UNIPOLAR)
50k
100
100
−15V
BIPOLAR OFF
8
V_{CC}
REF OUT
4
3
11
20V SPAN
B
A
ANALOG INPUTS
R2
100
10V
9.95k
5k
DAC1265
10
10V SPAN
15V
5V
0.1 µF
I_{REF}
0.5 mA
19.95k
6
REF IN
5k
1k
9
DAC OUT
20k
5
ANA COM
DAC
I_O
8k
R_{SHUNT}
2
3
8
LM311
4
1
1k
I_{OUT} = 4 × I_{REF} × CODE
CODE INPUT
0.1 µF
7
V_{EE}
12
24
MSB
LSB
13
DIG COM
−15V
12
DIG OUT
MSB
LSB
21
16
9
4
CONV COMP
SERIAL OUT
3
2
1
CC
DD
E
DM2504 SAR
11
DATA IN
14
START
CLOCK
16
12
0.1 µF
−5V
1.5 µF

INPUT RANGES

Unipolar	Bipolar	Connect	Equiv. DAC Z_{OUT}
0 to 10	±5	Input to A	2.36 kΩ
0 to 5	±2.5	Input to A	1.90 kΩ
0 to 20	±10	Input to B B to DAC OUT	3.08 kΩ

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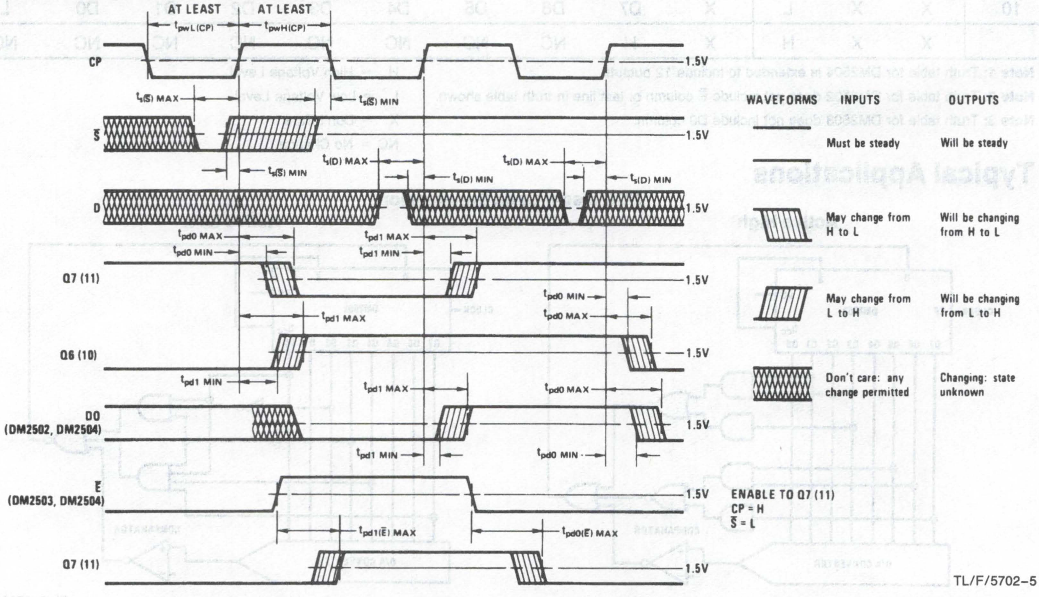
Switching Time Waveforms


AT LEAST
t_{pwL(CP)}
AT LEAST
t_{pwH(CP)}
CP
1.5V
t_{s(S)} MAX
t_{h(S)} MIN
S̄
1.5V
t_{s(S)} MIN
t_{s(D)} MAX
t_{s(D)} MIN
t_{s(D)} MAX
t_{s(D)} MIN
D
1.5V
t_{pd0} MAX
t_{pd0} MIN
t_{pd1} MAX
t_{pd1} MIN
Q7 (11)
1.5V
t_{pd0} MIN
t_{pd0} MAX
t_{pd1} MAX
Q6 (10)
1.5V
t_{pd1} MIN
t_{pd1} MAX
t_{pd0} MAX
DO
(DM2502, DM2504)
1.5V
t_{pd1} MIN
t_{pd0} MIN
E
(DM2503, DM2504)
1.5V
ENABLE TO Q7 (11)
CP = H
S̄ = L
t_{pd1(E)} MAX
t_{pd0(E)} MAX
Q7 (11)
1.5V
WAVEFORMS
INPUTS
OUTPUTS
Must be steady
Will be steady
May change from H to L
Will be changing from H to L
May change from L to H
Will be changing from L to H
Don't care: any change permitted
Changing: state unknown

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National Semiconductor Corporation

LM131A/LM131, LM231A/LM231, LM331A/LM331 Precision Voltage-to-Frequency Converters

General Description

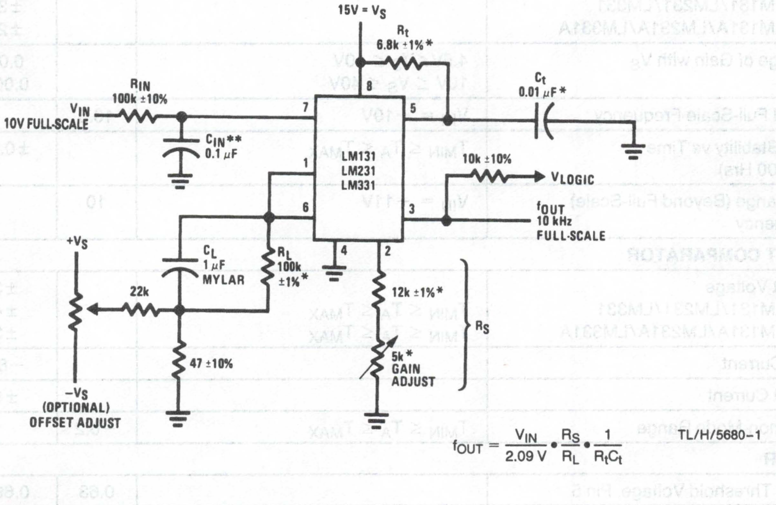
The LM131/LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM131A/LM231A/LM331A attains a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM131 is ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM131/LM231/LM331 utilizes a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100 kHz voltage-to-frequency conversion. And the output is capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against V_{CC}.

Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50 ppm/°C max
- Low power dissipation, 15 mW typical at 5V
- Wide dynamic range, 100 dB min at 10 kHz full scale frequency
- Wide range of full scale frequency, 1 Hz to 100 kHz
- Low cost

Typical Applications



$$f_{OUT} = \frac{V_{IN}}{2.09\text{ V}} \cdot \frac{R_S}{R_L} \cdot \frac{1}{R_t C_t}$$

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*Use stable components with low temperature coefficients. See Typical Applications section.

**0.1µF or 1µF, See "Principles of Operation."

FIGURE 1. Simple Stand-Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LM131A/LM131	**LM231A/LM231**	**LM331A/LM331**
Supply Voltage	40V	40V	40V
Output Short Circuit to Ground	Continuous	Continuous	Continuous
Output Short Circuit to V_{CC}	Continuous	Continuous	Continuous
Input Voltage	−0.2V to $+V_S$	−0.2V to $+V_S$	−0.2V to $+V_S$
	T_{MIN} T_{MAX}	**T_{MIN} T_{MAX}**	**T_{MIN} T_{MAX}**
Operating Ambient Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Power Dissipation (P_D at 25°C)			
and Thermal Resistance (θ_{jA})			
(H Package) P_D	670 mW	570 mW	570 mW
θ_{jA}	150°C/W	150°C/W	150°C/W
(N Package) P_D		500 mW	500 mW
θ_{jA}		155°C/W	155°C/W
Lead Temperature (Soldering, 10 sec.)			
Dual-In-Line Package (Plastic)	260°C	260°C	260°C
Metal Can Package (TO-5)	260°C	260°C	260°C
ESD Susceptibility (Note 4)	TBD V	TBD V	TBD V

Electrical Characteristics $T_A = 25°C$ unless otherwise specified (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
VFC Non-Linearity (Note 3)	$4.5V \leq V_S \leq 20V$		±0.003	±0.01	% Full-Scale
	$T_{MIN} \leq T_A \leq T_{MAX}$		±0.006	±0.02	% Full-Scale
VFC Non-Linearity In Circuit of *Figure 1*	$V_S = 15V$, f = 10 Hz to 11 kHz		±0.024	±0.14	%Full-Scale
Conversion Accuracy Scale Factor (Gain)	$V_{IN} = -10V$, $R_S = 14\ k\Omega$				
LM131, LM131A, LM231, LM231A		0.95	1.00	1.05	kHz/V
LM331, LM331A		0.90	1.00	1.10	kHz/V
Temperature Stability of Gain	$T_{MIN} \leq T_A \leq T_{MAX}$, $4.5V \leq V_S \leq 20V$				
LM131/LM231/LM331			±30	±150	ppm/°C
LM131A/LM231A/LM331A			±20	±50	ppm/°C
Change of Gain with V_S	$4.5V \leq V_S \leq 10V$		0.01	0.1	%/V
	$10V \leq V_S \leq 40V$		0.006	0.06	%/V
Rated Full-Scale Frequency	$V_{IN} = -10V$	10.0			kHz
Gain Stability vs Time (1000 Hrs)	$T_{MIN} \leq T_A \leq T_{MAX}$		±0.02		% Full-Scale
Overrange (Beyond Full-Scale) Frequency	$V_{IN} = -11V$	10			%
INPUT COMPARATOR					
Offset Voltage			±3	±10	mV
LM131/LM231/LM331	$T_{MIN} \leq T_A \leq T_{MAX}$		±4	±14	mV
LM131A/LM231A/LM331A	$T_{MIN} \leq T_A \leq T_{MAX}$		±3	±10	mV
Bias Current			−80	−300	nA
Offset Current			±8	±100	nA
Common-Mode Range	$T_{MIN} \leq T_A \leq T_{MAX}$	−0.2		$V_{CC}-2.0$	V
TIMER					
Timer Threshold Voltage, Pin 5		0.63	0.667	0.70	× V_S
Input Bias Current, Pin 5	$V_S = 15V$				
All Devices	$0V \leq V_{PIN\ 5} \leq 9.9V$		±10	±100	nA
LM131/LM231/LM331	$V_{PIN\ 5} = 10V$		200	1000	nA
LM131A/LM231A/LM331A	$V_{PIN\ 5} = 10V$		200	500	nA
$V_{SAT\ PIN\ 5}$ (Reset)	I = 5 mA		0.22	0.5	V

Electrical Characteristics $T_A = 25°C$ unless otherwise specified (Note 2) (Continued)

Parameter	Conditions	Min	Typ	Max	Units
CURRENT SOURCE (Pin 1)					
Output Current	$R_S = 14\ k\Omega$, $V_{PIN\ 1} = 0$				
LM131, LM131A, LM231, LM231A		126	135	144	μA
LM331, LM331A		116	136	156	μA
Change with Voltage	$0V \le V_{PIN\ 1} \le 10V$		0.2	1.0	μA
Current Source OFF Leakage					
LM131, LM131A			0.01	1.0	nA
LM231, LM231A, LM331, LM331A			0.02	10.0	nA
All Devices	$T_A = T_{MAX}$		2.0	50.0	nA
Operating Range of Current (Typical)			(10 to 500)		μA
REFERENCE VOLTAGE (Pin 2)					
LM131, LM131A, LM231, LM231A		1.76	1.89	2.02	V_{DC}
LM331, LM331A		1.70	1.89	2.08	V_{DC}
Stability vs Temperature			±60		ppm/°C
Stability vs Time, 1000 Hours			±0.1		%
LOGIC OUTPUT (Pin 3)					
V_{SAT}	$I = 5\ mA$		0.15	0.50	V
	$I = 3.2\ mA$ (2 TTL Loads), $T_{MIN} \le T_A \le T_{MAX}$		0.10	0.40	V
OFF Leakage			±0.05	1.0	μA
SUPPLY CURRENT					
LM131, LM131A, LM231, LM231A	$V_S = 5V$	2.0	3.0	4.0	mA
	$V_S = 40V$	2.5	4.0	6.0	mA
LM331, LM331A	$V_S = 5V$	1.5	3.0	6.0	mA
	$V_S = 40V$	2.0	4.0	8.0	mA

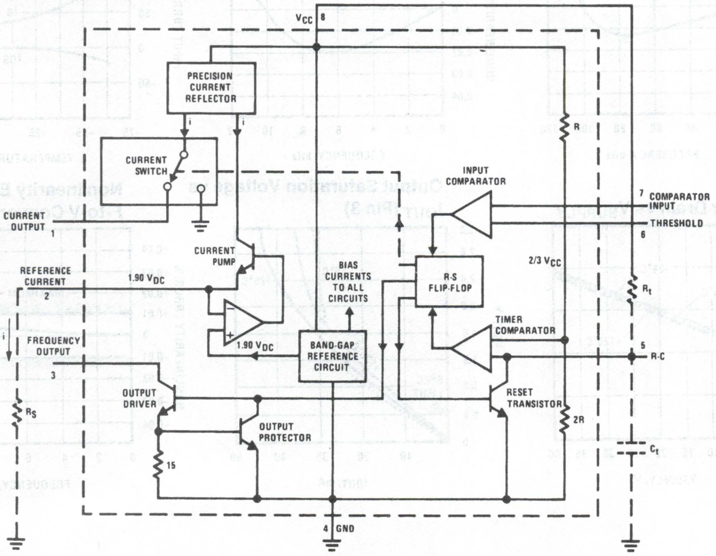
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All specifications apply in the circuit of *Figure 3*, with $4.0V \le V_S \le 40V$, unless otherwise noted.

Note 3: Nonlinearity is defined as the deviation of f_{OUT} from $V_{IN} \times (10\ kHz / -10\ V_{DC})$ when the circuit has been trimmed for zero error at 10 Hz and at 10 kHz, over the frequency range 1 Hz to 11 kHz. For the timing capacitor, C_T, use NPO ceramic, Teflon®, or polystyrene.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Block Diagram



V_{CC} 8
PRECISION CURRENT REFLECTOR
i
i
CURRENT SWITCH
CURRENT OUTPUT 1
REFERENCE CURRENT 2
i
FREQUENCY OUTPUT
3
R_S
1.90 V_{DC}
CURRENT PUMP
1.90 V_{DC}
BIAS CURRENTS TO ALL CIRCUITS
BAND-GAP REFERENCE CIRCUIT
OUTPUT DRIVER
OUTPUT PROTECTOR
15
INPUT COMPARATOR
R-S FLIP-FLOP
TIMER COMPARATOR
RESET TRANSISTOR
2R
R
2/3 V_{CC}
7 COMPARATOR INPUT
THRESHOLD 6
R_t
5
R-C
C_t
4 GND

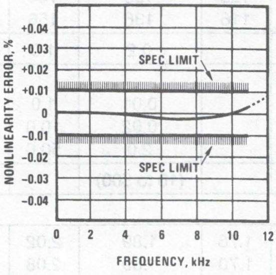
TL/H/5680–2

FIGURE 1a

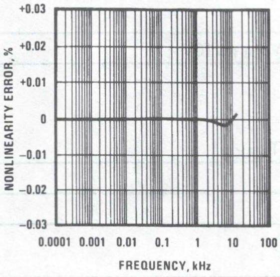
Typical Performance Characteristics

(All electrical characteristics apply for the circuit of *Figure 3*, unless otherwise noted.)

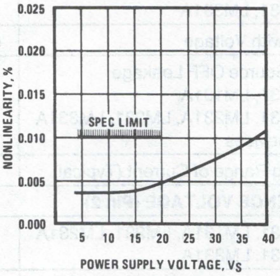
Nonlinearity Error, LM131 Family, as Precision V-to-F Converter (*Figure 3*)



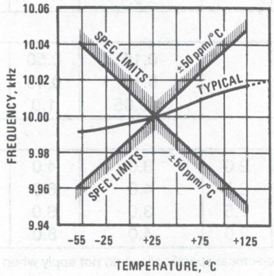
Nonlinearity Error, LM131 Family



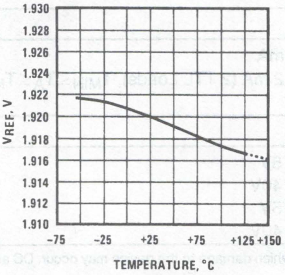
Nonlinearity vs Power Supply Voltage



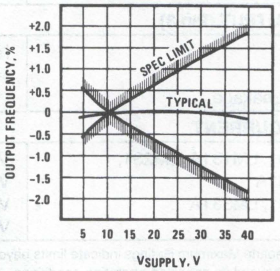
Frequency vs Temperature, LM131A



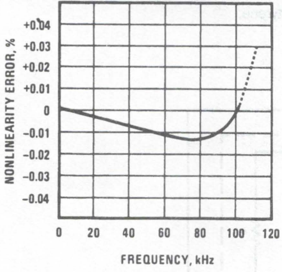
VREF vs Temperature, LM131A



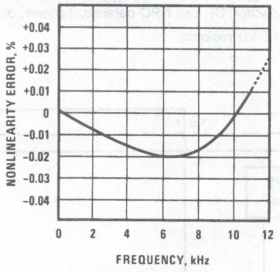
Output Frequency vs VSUPPLY



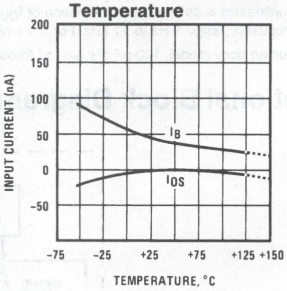
100 kHz Nonlinearity Error, LM131 Family (*Figure 4*)



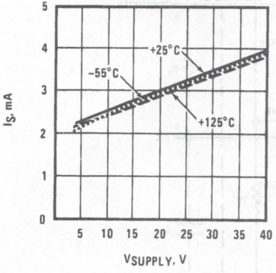
Nonlinearity Error, LM131 (*Figure 1*)



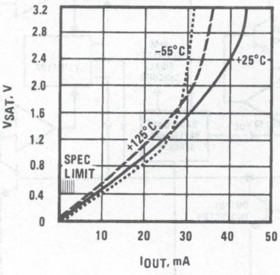
Input Current (Pins 6, 7) vs Temperature



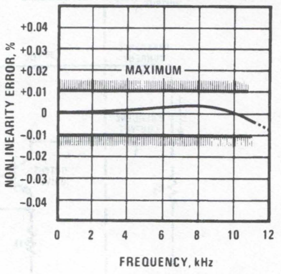
Power Drain vs VSUPPLY



Output Saturation Voltage vs IOUT (Pin 3)



Nonlinearity Error, Precision F-to-V Converter (*Figure 6*)



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Typical Applications (Continued)

PRINCIPLES OF OPERATION OF A SIMPLIFIED VOLTAGE-TO-FREQUENCY CONVERTER

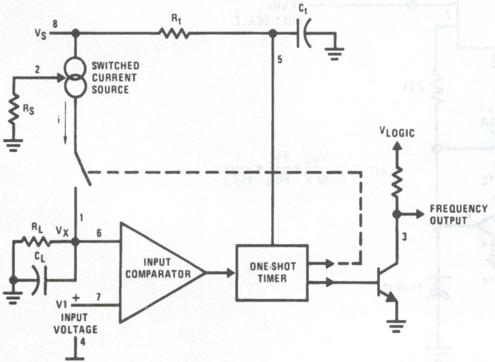
The LM131 is a monolithic circuit designed for accuracy and versatile operation when applied as a voltage-to-frequency (V-to-F) converter or as a frequency-to-voltage (F-to-V) converter. A simplified block diagram of the LM131 is shown in *Figure 2* and consists of a switched current source, input comparator, and 1-shot timer.

The operation of these blocks is best understood by going through the operating cycle of the basic V-to-F converter, *Figure 2*, which consists of the simplified block diagram of the LM131 and the various resistors and capacitors connected to it.

The voltage comparator compares a positive input voltage, V1, at pin 7 to the voltage, V_x, at pin 6. If V1 is greater, the comparator will trigger the 1-shot timer. The output of the timer will turn ON both the frequency output transistor and the switched current source for a period $t = 1.1\ R_tC_t$. During this period, the current i will flow out of the switched current source and provide a fixed amount of charge, $Q = i \times t$, into the capacitor, C_L. This will normally charge V_x up to a higher level than V1. At the end of the timing period, the current i will turn OFF, and the timer will reset itself.

Now there is no current flowing from pin 1, and the capacitor C_L will be gradually discharged by R_L until V_x falls to the level of V1. Then the comparator will trigger the timer and start another cycle.

The current flowing into C_L is exactly $I_{AVE} = i \times (1.1 \times R_tC_t) \times f$, and the current flowing out of C_L is exactly $V_x/R_L \cong V_{IN}/R_L$. If V_{IN} is doubled, the frequency will double to maintain this balance. Even a simple V-to-F converter can provide a frequency precisely proportional to its input voltage over a wide range of frequencies.



TL/H/5680-4

FIGURE 2. Simplified Block Diagram of Stand-Alone Voltage-to-Frequency Converter Showing LM131 and External Components

DETAIL OF OPERATION, FUNCTIONAL BLOCK DIAGRAM (*FIGURE 1a*)

The block diagram shows a band gap reference which provides a stable 1.9 V_{DC} output. This 1.9 V_{DC} is well regulated over a V_S range of 3.9V to 40V. It also has a flat, low temperature coefficient, and typically changes less than ½% over a 100°C temperature change.

The current pump circuit forces the voltage at pin 2 to be at 1.9V, and causes a current $i = 1.90V/R_S$ to flow. For $R_S = 14k$, $i = 135\ \mu A$. The precision current reflector provides a current equal to i to the current switch. The current switch switches the current to pin 1 or to ground depending on the state of the R_S flip-flop.

The timing function consists of an R_S flip-flop, and a timer comparator connected to the external R_tC_t network. When the input comparator detects a voltage at pin 7 higher than pin 6, it sets the R_S flip-flop which turns ON the current switch and the output driver transistor. When the voltage at pin 5 rises to ⅔ V_{CC}, the timer comparator causes the R_S flip-flop to reset. The reset transistor is then turned ON and the current switch is turned OFF.

However, if the input comparator still detects pin 7 higher than pin 6 when pin 5 crosses ⅔ V_{CC}, the flip-flop will not be reset, and the current at pin 1 will continue to flow, in its attempt to make the voltage at pin 6 higher than pin 7. This condition will usually apply under start-up conditions or in the case of an overload voltage at signal input. It should be noted that during this sort of overload, the output frequency will be 0; as soon as the signal is restored to the working range, the output frequency will be resumed.

The output driver transistor acts to saturate pin 3 with an ON resistance of about 50Ω. In case of overvoltage, the output current is actively limited to less than 50 mA.

The voltage at pin 2 is regulated at 1.90 V_{DC} for all values of i between 10 μA to 500 μA. It can be used as a voltage reference for other components, but care must be taken to ensure that current is not taken from it which could reduce the accuracy of the converter.

PRINCIPLES OF OPERATION OF BASIC VOLTAGE-TO-FREQUENCY CONVERTER (*FIGURE 1*)

The simple stand-alone V-to-F converter shown in *Figure 1* includes all the basic circuitry of *Figure 2* plus a few components for improved performance.

A resistor, $R_{IN} = 100\ k\Omega \pm 10\%$, has been added in the path to pin 7, so that the bias current at pin 7 (−80 nA typical) will cancel the effect of the bias current at pin 6 and help provide minimum frequency offset.

The resistance R_S at pin 2 is made up of a 12 kΩ fixed resistor plus a 5 kΩ (cermet, preferably) gain adjust rheostat. The function of this adjustment is to trim out the gain tolerance of the LM131, and the tolerance of R_t, R_L and C_t.

Typical Applications (Continued)

For best results, all the components should be stable low-temperature-coefficient components, such as metal-film resistors. The capacitor should have low dielectric absorption; depending on the temperature characteristics desired, NPO ceramic, polystyrene, Teflon or polypropylene are best suited.

A capacitor C_{IN} is added from pin 7 to ground to act as a filter for V_{IN}. A value of 0.01 μF to 0.1 μF will be adequate in most cases; however, in cases where better filtering is required, a 1 μF capacitor can be used. When the RC time constants are matched at pin 6 and pin 7, a voltage step at V_{IN} will cause a step change in f_{OUT}. If C_{IN} is much less than C_L, a step at V_{IN} may cause f_{OUT} to stop momentarily.

A 47Ω resistor, in series with the 1 μF C_L, is added to give hysteresis effect which helps the input comparator provide the excellent linearity (0.03% typical).

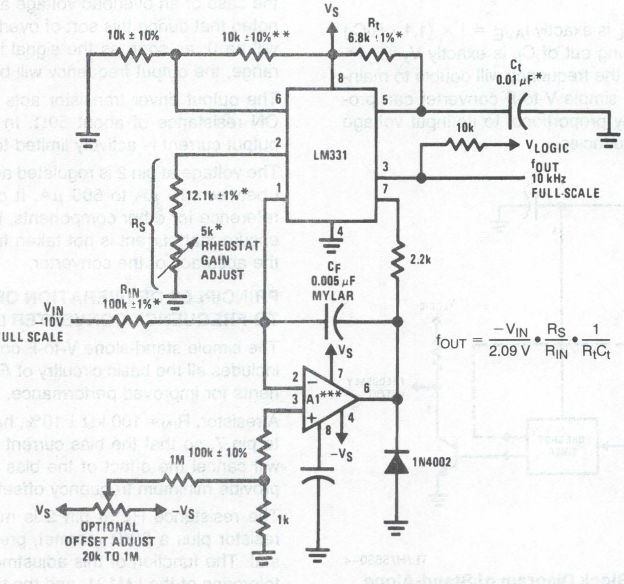
DETAIL OF OPERATION OF PRECISION V-TO-F CONVERTER (*FIGURE 3*)

In this circuit, integration is performed by using a conventional operational amplifier and feedback capacitor, C_F. When the integrator's output crosses the nominal threshold level at pin 6 of the LM131, the timing cycle is initiated.

The average current fed into the op amp's summing point (pin 2) is i × (1.1 R_tC_t) × f which is perfectly balanced with $-V_{IN}/R_{IN}$. In this circuit, the voltage offset of the LM131 input comparator does not affect the offset or accuracy of the V-to-F converter as it does in the stand-alone V-to-F converter; nor does the LM131 bias current or offset current. Instead, the offset voltage and offset current of the operational amplifier are the only limits on how small the signal can be accurately converted. Since op amps with voltage offset well below 1 mV and offset currents well below 2 nA are available at low cost, this circuit is recommended for best accuracy for small signals. This circuit also responds immediately to any change of input signal (which a stand-alone circuit does not) so that the output frequency will be an accurate representation of V_{IN}, as quickly as 2 output pulses' spacing can be measured.

In the precision mode, excellent linearity is obtained because the current source (pin 1) is always at ground potential and that voltage does not vary with V_{IN} or f_{OUT}. (In the stand-alone V-to-F converter, a major cause of non-linearity is the output impedance at pin 1 which causes i to change as a function of V_{IN}).

The circuit of *Figure 4* operates in the same way as *Figure 3*, but with the necessary changes for high speed operation.



TL/H/5680–5

*Use stable components with low temperature coefficients. See Typical Applications section.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

***Use low offset voltage and low offset current op amps for A1: recommended types LM108, LM308A, LF411A

FIGURE 3. Standard Test Circuit and Applications Circuit, Precision Voltage-to-Frequency Converter

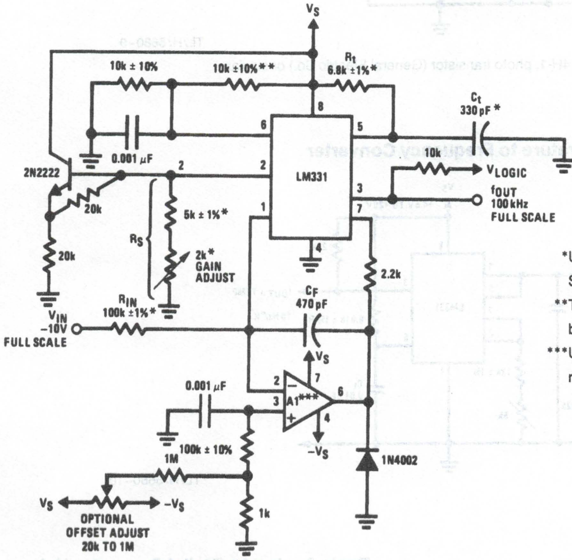
Typical Applications (Continued)

DETAILS OF OPERATION, FREQUENCY-TO-VOLTAGE CONVERTERS *(FIGURES 5 AND 6)*

In these applications, a pulse input at f_{IN} is differentiated by a C-R network and the negative-going edge at pin 6 causes the input comparator to trigger the timer circuit. Just as with a V-to-F converter, the average current flowing out of pin 1 is $I_{AVERAGE} = i \times (1.1\ R_tC_t) \times f$.

In the simple circuit of *FIGURE 5*, this current is filtered in the network $R_L = 100\ k\Omega$ and $1\ \mu F$. The ripple will be less than 10 mV peak, but the response will be slow, with a 0.1 second time constant, and settling of 0.7 second to 0.1% accuracy.

In the precision circuit, an operational amplifier provides a buffered output and also acts as a 2-pole filter. The ripple will be less than 5 mV peak for all frequencies above 1 kHz, and the response time will be much quicker than in *Figure 5*. However, for input frequencies below 200 Hz, this circuit will have worse ripple than *Figure 5*. The engineering of the filter time-constants to get adequate response and small enough ripple simply requires a study of the compromises to be made. Inherently, V-to-F converter response can be fast, but F-to-V response can not.



VS
10k ± 10%
10k ±10%**
Rt 6.8k ±1%*
Ct 330 pF *
8
6
5
0.001 µF
2N2222
2
LM331
10k
VLOGIC
fOUT 100 kHz FULL SCALE
3
1
7
20k
5k ± 1%*
RS
2k* GAIN ADJUST
20k
4
2.2k
RIN 100k ±1%*
VIN -10V FULL SCALE
CF 470 pF
VS
0.001 µF
A1***
100k ± 10%
1M
-VS
1N4002
VS
-VS
OPTIONAL OFFSET ADJUST 20k TO 1M
1k

*Use stable components with low temperature coefficients. See Typical Applications section.

**This resistor can be 5 kΩ or 10 kΩ for $V_S = 8V$ to 22V, but must be 10 kΩ for $V_S = 4.5V$ to 8V.

***Use low offset voltage and low offset current op amps for A1: recommended types LF411A or LF356.

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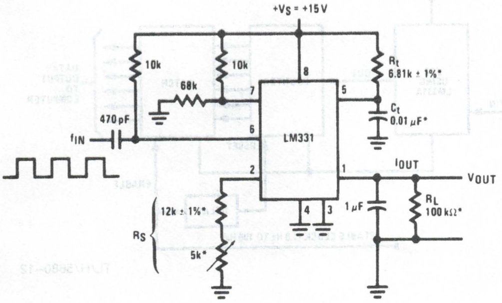
FIGURE 4. Precision Voltage-to-Frequency Converter, 100 kHz Full-Scale, ±0.03% Non-Linearity



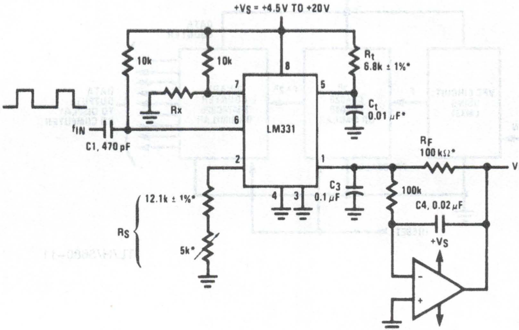
+VS = +15V
10k
10k
68k
8
Rt 6.81k ± 1%*
Ct 0.01 µF*
5
7
470 pF
fIN
6
LM331
IOUT
VOUT
2
1
12k ± 1%*
RS
5k*
4
3
1 µF
RL 100 kΩ*

TL/H/5680-7

$$V_{OUT} = f_{IN} \times 2.09V \times \frac{R_L}{R_S} \times (R_tC_t)$$

*Use stable components with low temperature coefficients.

FIGURE 5. Simple Frequency-to-Voltage Converter, 10 kHz Full-Scale, ±0.06% Non-Linearity



+VS = +4.5V TO +20V
10k
10k
8
Rt 6.8k ± 1%*
7
5
Rx
Ct 0.01 µF*
6
fIN
C1, 470 pF
LM331
RF 100 kΩ*
2
1
VOUT
C3 0.1 µF
12.1k ± 1%*
4
3
100k
C4, 0.02 µF
RS
5k*
+VS
-VS

TL/H/5680-8

$$V_{OUT} = -f_{IN} \times 2.09V \times \frac{R_F}{R_S} \times (R_tC_t)$$

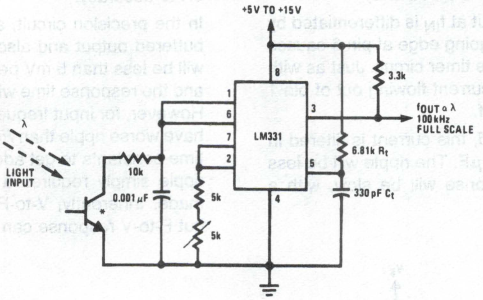
$$\text{SELECT } Rx = \frac{(V_S - 2V)}{0.2\ mA}$$

*Use stable components with low temperature coefficients.

FIGURE 6. Precision Frequency-to-Voltage Converter, 10 kHz Full-Scale with 2-Pole Filter, ±0.01% Non-Linearity Maximum

Typical Applications (Continued)

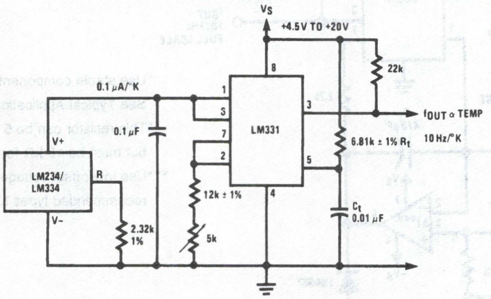
Light Intensity to Frequency Converter


+5V TO +15V
8
3.3k
1
6
7
2
3
5
4
LM331
λ
LIGHT INPUT
*
10k
0.001 µF
5k
5k
6.81k R_t
f_OUT ∝ λ
100 kHz
FULL SCALE
330 pF C_t

TL/H/5680-9

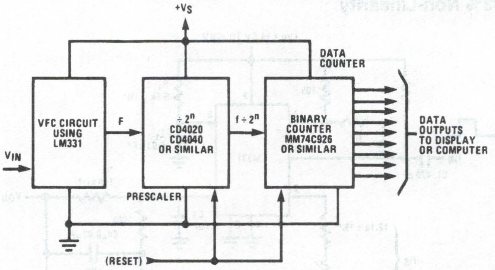
*L14F-1, L14G-1 or L14H-1, photo transistor (General Electric Co.) or similar

Temperature to Frequency Converter


V_S
+4.5V TO +20V
8
22k
0.1 µA/°K
1
3
LM331
7
2
5
4
0.1 µF
V+
LM234/LM334
R
V−
2.32k 1%
12k ± 1%
5k
6.81k ± 1% R_t
f_OUT ∝ TEMP
10 Hz/°K
C_t 0.01 µF

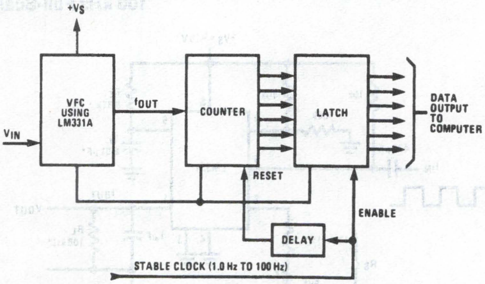
TL/H/5680-10

Long-Term Digital Integrator Using VFC


+V_S
DATA COUNTER
VFC CIRCUIT USING LM331
F
÷2^n CD4020 CD4040 OR SIMILAR
f ÷ 2^n
BINARY COUNTER MM74C926 OR SIMILAR
DATA OUTPUTS TO DISPLAY OR COMPUTER
V_IN
PRESCALER
(RESET)

TL/H/5680-11

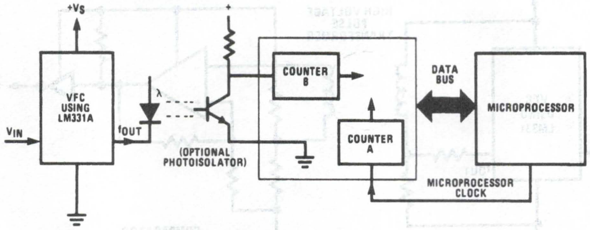
Basic Analog-to-Digital Converter Using Voltage-to-Frequency Converter


+V_S
VFC USING LM331A
f_OUT
COUNTER
LATCH
DATA OUTPUT TO COMPUTER
V_IN
RESET
ENABLE
DELAY
STABLE CLOCK (1.0 Hz TO 100 Hz)

TL/H/5680-12

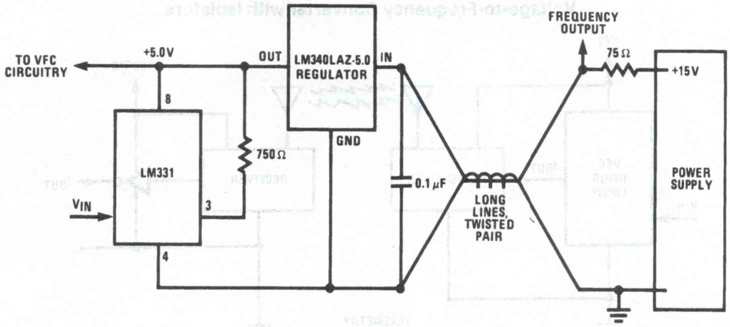
Typical Applications (Continued)

Analog-to-Digital Converter with Microprocessor


+VS
+
VFC
USING
LM331A
VIN
fOUT
λ
(OPTIONAL
PHOTOISOLATOR)
COUNTER
B
COUNTER
A
DATA
BUS
MICROPROCESSOR
MICROPROCESSOR
CLOCK

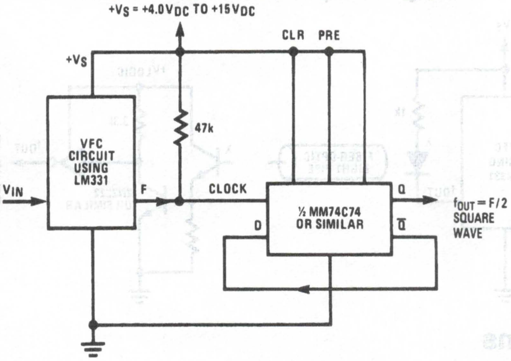
TL/H/5680–13

Remote Voltage-to-Frequency Converter with 2-Wire Transmitter and Receiver


TO VFC
CIRCUITRY
+5.0V
OUT
LM340LAZ-5.0
REGULATOR
IN
GND
FREQUENCY
OUTPUT
75 Ω
+15V
8
LM331
750 Ω
VIN
3
4
0.1 μF
LONG
LINES,
TWISTED
PAIR
POWER
SUPPLY

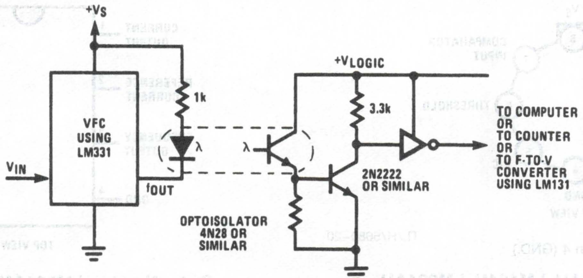
TL/H/5680–14

Voltage-to-Frequency Converter with Square-Wave Output Using ÷ 2 Flip-Flop


+VS = +4.0VDC TO +15VDC
CLR
PRE
+VS
VFC
CIRCUIT
USING
LM331
VIN
47k
F
CLOCK
Q
½ MM74C74
OR SIMILAR
D
Q̄
fOUT = F/2
SQUARE
WAVE

TL/H/5680–15

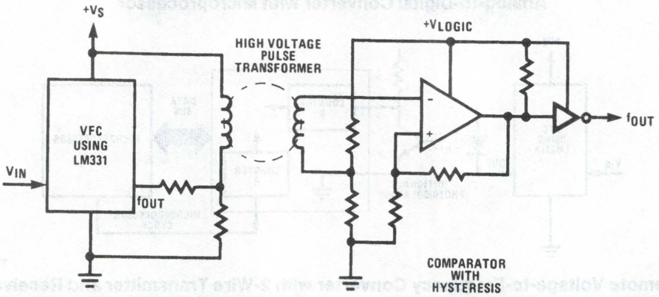
Voltage-to-Frequency Converter with Isolators


+VS
VFC
USING
LM331
VIN
fOUT
1k
λ
λ
OPTOISOLATOR
4N28 OR
SIMILAR
+VLOGIC
3.3k
2N2222
OR SIMILAR
TO COMPUTER
OR
TO COUNTER
OR
TO F-TO-V
CONVERTER
USING LM131

TL/H/5680–16

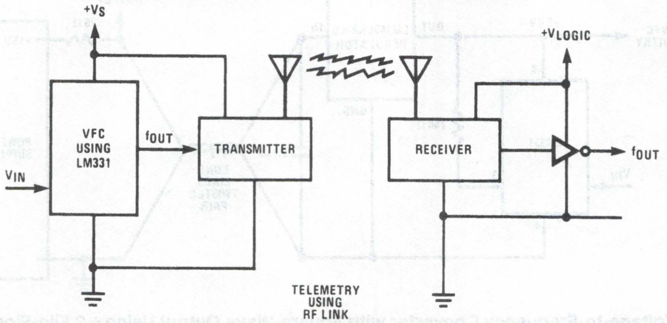
Typical Applications (Continued)

Voltage-to-Frequency Converter with Isolators


+VS
HIGH VOLTAGE PULSE TRANSFORMER
+VLOGIC
VFC USING LM331
VIN
fOUT
fOUT
COMPARATOR WITH HYSTERESIS

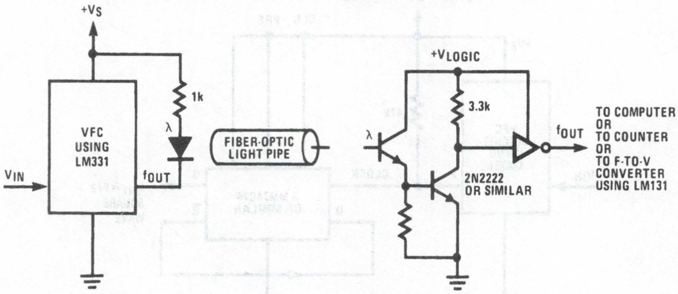
TL/H/5680–17

Voltage-to-Frequency Converter with Isolators


+VS
+VLOGIC
VFC USING LM331
VIN
fOUT
TRANSMITTER
RECEIVER
fOUT
TELEMETRY USING RF LINK

TL/H/5680–18

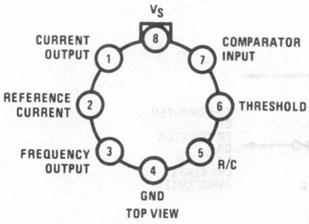
Voltage-to-Frequency Converter with Isolators


+VS
1k
λ
VFC USING LM331
VIN
fOUT
FIBER-OPTIC LIGHT PIPE
λ
+VLOGIC
3.3k
fOUT
2N2222 OR SIMILAR
TO COMPUTER OR TO COUNTER OR TO F-TO-V CONVERTER USING LM131

TL/H/5680–19

Connection Diagrams

Metal Can Package

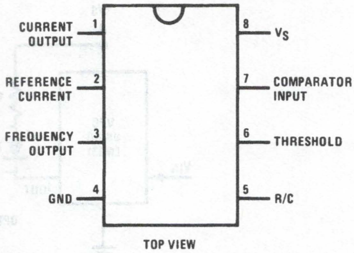

VS
8
CURRENT OUTPUT
1
COMPARATOR INPUT
7
REFERENCE CURRENT
2
THRESHOLD
6
FREQUENCY OUTPUT
3
R/C
5
4
GND
TOP VIEW

TL/H/5680–20

Note: Metal case is connected to pin 4 (GND.)

Order Number LM131AH, LM131H, LM231AH, LM231H, LM331AH or LM331H
See NS Package Number H08C

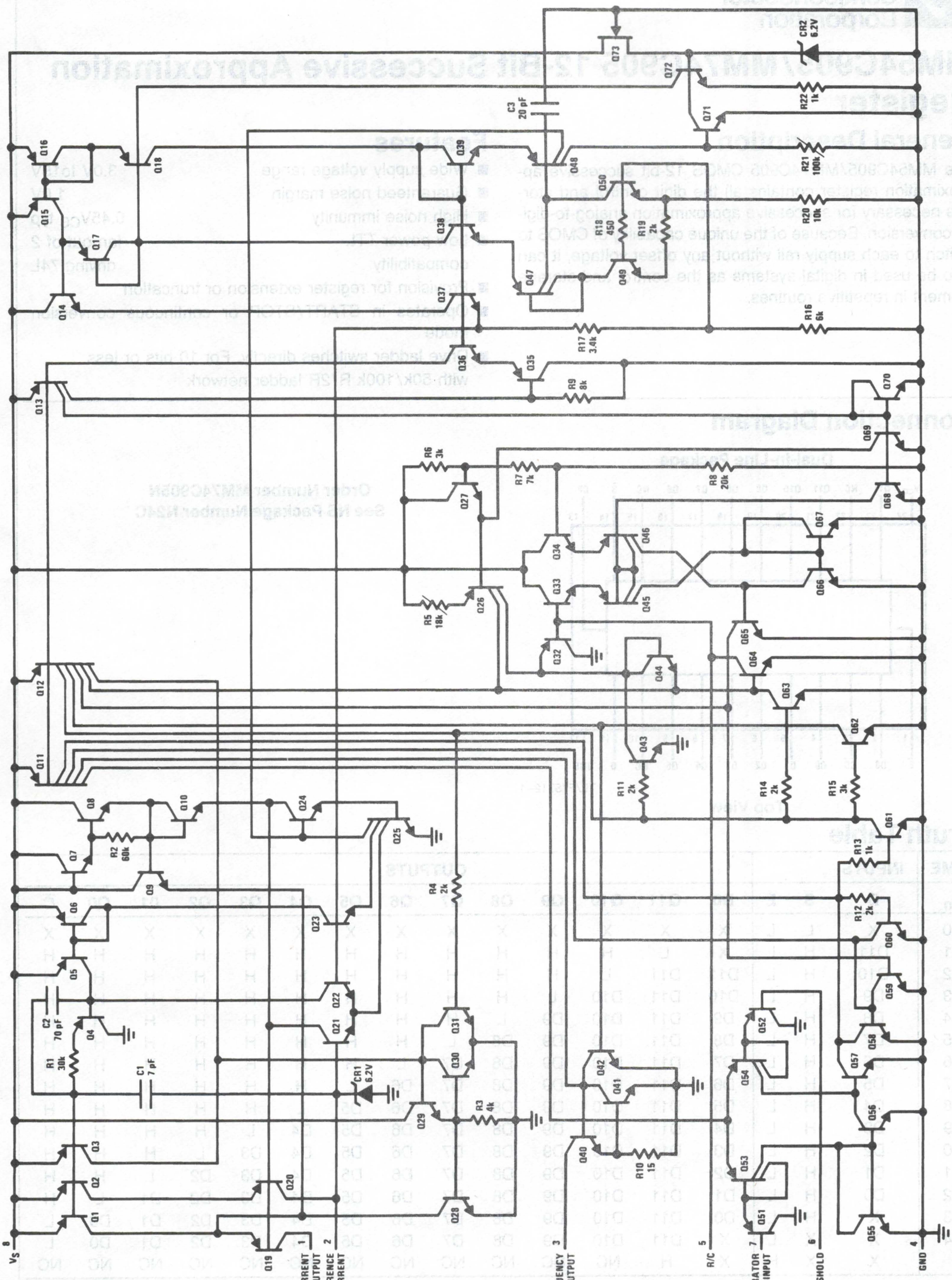
Dual-In-Line Package


CURRENT OUTPUT
1
8
VS
REFERENCE CURRENT
2
7
COMPARATOR INPUT
FREQUENCY OUTPUT
3
6
THRESHOLD
GND
4
5
R/C
TOP VIEW

TL/H/5680–21

Order Number LM231AN, LM231N, LM331AN, or LM331N
See NS Package Number N08E

Schematic Diagram


Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
Q37
Q38
Q39
Q40
Q41
Q42
Q43
Q44
Q45
Q46
Q47
Q48
Q49
Q50
Q51
Q52
Q53
Q54
Q55
Q56
Q57
Q58
Q59
Q60
Q61
Q62
Q63
Q64
Q65
Q66
Q67
Q68
Q69
Q70
Q71
Q72
Q73
R1 30k
R2 60k
R3 4k
R4 2k
R5 18k
R6 3k
R7 7k
R8 20k
R9 8k
R10 15
R11 2k
R12 2k
R13 1k
R14 2k
R15 3k
R16 6k
R17 3.4k
R18 450
R19 2k
R20 10k
R21 100k
R22 1k
C1 7 pF
C2 70 pF
C3 20 pF
CR1 6.2V
CR2 6.2V
8
V_S
1
CURRENT OUTPUT
2
REFERENCE CURRENT
3
FREQUENCY OUTPUT
5
R/C
7
COMPARATOR INPUT
6
THRESHOLD
4
GND

TL/H/5680-22

National
Semiconductor
Corporation

MM54C905/MM74C905 12-Bit Successive Approximation Register

General Description

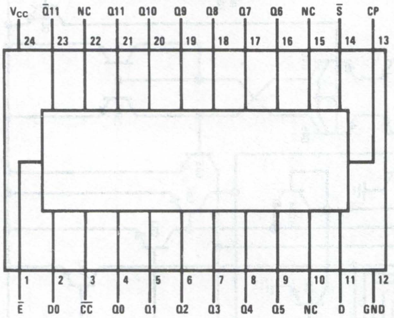
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

Features

- Wide supply voltage range 3.0V to15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

Connection Diagram

Dual-In-Line Package



TL/F/5712-1

Top View

Order Number MM74C905N
See NS Package Number N24C

Truth Table

TIME	INPUTS			OUTPUTS													
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	01	Q0	$\overline{C}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level
L = Low level
X = Don't care
NC = No change

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.3 to V_{CC} +0.3V
Operating Temperature Range	
MM74C905	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility (Note 4)	400V
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC}=5.0V$, $I_O=10\mu A$ $V_{CC}=10V$, $I_O=10\mu A$			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	µA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		µA
Supply Current (I_{CC})	$V_{CC}=15V$		0.05	300	µA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$) MM54C905 MM74C905	 $V_{CC}=4.5V$ $V_{CC}=4.75V$	 $V_{CC}-1.5$ $V_{CC}-1.5$			 V V
Logical "0" Input Voltage ($V_{IN(0)}$) MM54C905 MM74C905	 $V_{CC}=4.5V$ $V_{CC}=4.75V$			 0.8 0.8	 V V
Logical "1" Output Voltage ($V_{OUT(1)}$) MM54C905 MM74C905	 $V_{CC}=4.5V$, $I_O=-360\mu A$ $V_{CC}=4.75V$, $I_O=-360\mu A$	 2.4 2.4			 V V
Logical "0" Output Voltage ($V_{OUT(0)}$) MM54C905 MM74C905	 $V_{CC}=4.5V$, $I_O=360\mu A$ $V_{CC}=4.75V$, $I_O=360\mu A$			 0.4 0.4	 V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA
Q11–Q0 Outputs R_{SOURCE}	$V_{CC}=10V$ ±5% $V_{OUT}=V_{CC}-0.3V$ $T_A=25°C$	150		350	Ω
R_{SINK}	$V_{CC}=10V$ ±5% $V_{OUT}=0.3V$ $T_A=25°C$	80		230	Ω

AC Electrical Characteristics $T_A = 25°C, C_L = 50pF$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Propagation Delay Time From Clock	$V_{CC} = 5.0V$		200	350	ns
Input To Outputs (Q0–Q11)($t_{pd(Q)}$)	$V_{CC} = 10V$		80	150	ns
Propagation Delay Time From Clock	$V_{CC} = 5.0V$		180	325	ns
Input To D_O($t_{pd(D_O)}$)	$V_{CC} = 10V$		70	125	ns
Propagation Delay Time From Register	$V_{CC} = 5.0V$		190	350	ns
Enable ($\overline{E}$) To Output (Q11) ($t_{pd(\overline{E})}$)	$V_{CC} = 10V$		75	150	ns
Propagation Delay Time From Clock	$V_{CC} = 5.0V$		190	350	ns
To $\overline{CC}$ ($t_{pd(\overline{CC})}$)	$V_{CC} = 10V$		75	0.50	ns
Data Input Set-UpTime (t_{DS})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	80 30			ns ns
Start Input Set-Up Time (t_{SS})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	80 30			ns ns
Minimum Clock Pulse Width (t_{PWL}, t_{PWH})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	250 100	125 40		ns ns
Maximum Clock Rise and Fall Time (t_r, t_f)	$V_{CC} = 5.0V$ $V_{CC} = 10V$			15 5	µs µs
Maximum Clock Frequency (f_{MAX})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2 5	4 10		MHz MHz
Clock Input Capacitance (C_{CLK})	Clock Input (Note 2)		10		pF
Input Capacitance (C_{IN})	Any Other Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	(Note 3)		100		pF

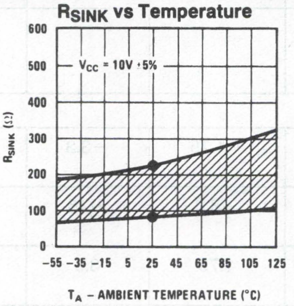
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

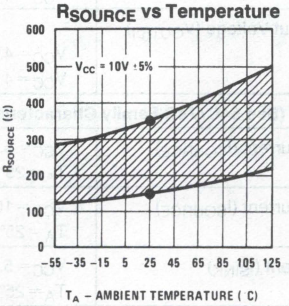
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics



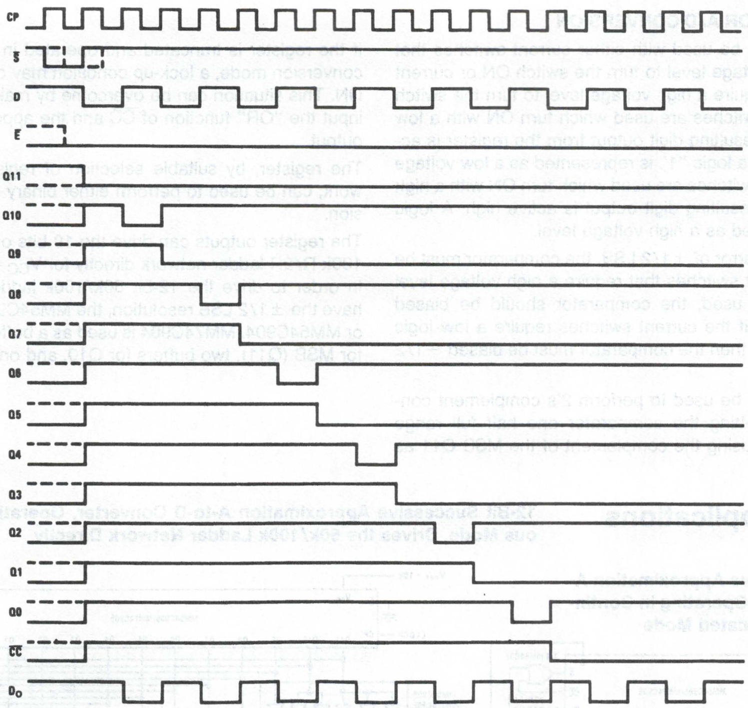
•These points are guaranteed by automatic testing



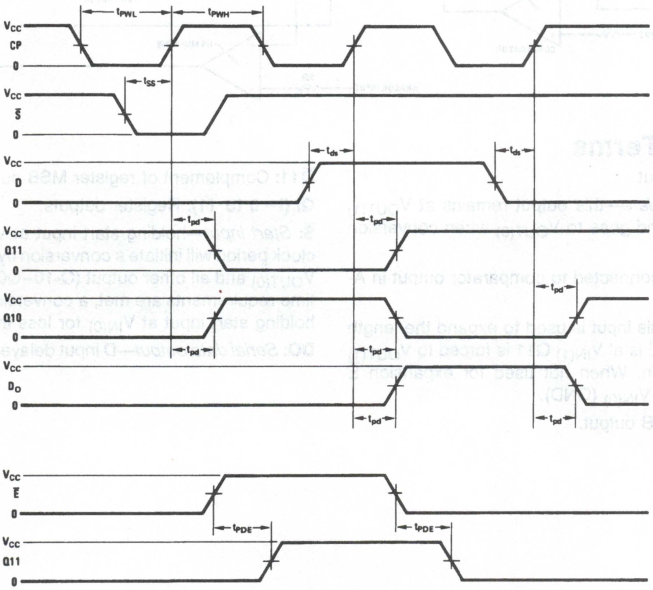
TL/F/5712-2

•These points are guaranteed by automatic testing.

Timing Diagram


CP
S̄
Ē
Q11
Q10
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
CC
D₀

Switching Time Waveforms


V_CC
CP
0
t_PWL
t_PWH
V_CC
S̄
0
t_SS
V_CC
D
0
t_ds
t_ds
V_CC
Q11
0
t_pd
t_pd
V_CC
Q10
0
t_pd
t_pd
V_CC
D₀
0
t_pd
t_pd
V_CC
Ē
0
t_PDE
t_PDE
V_CC
Q11
0

TL/F/5712-3

Typical Performance Characteristics

USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±1/2 LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased −1/2 LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range +1/2 LSB and using the complement of the MSB Q11 as the sign bit.

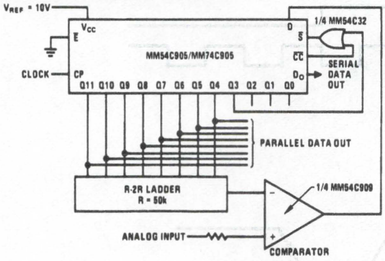
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

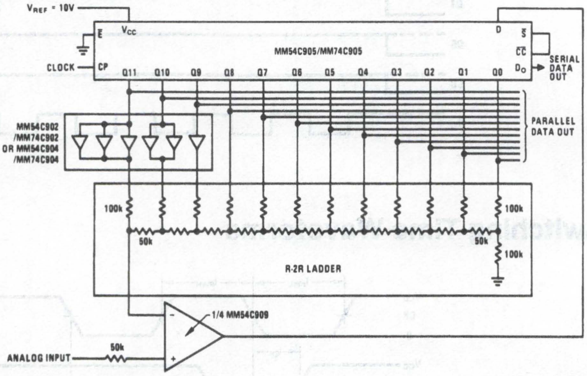
The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for $V_{CC} = 10V$ or higher. In order to drive the 12-bit 50k/100k ladder network and have the ±1/2 LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as a buffer, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

Typical Applications

12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode


VREF = 10V
VCC
E
D
S
1/4 MM54C32
MM54C905/MM74C905
CC
SERIAL DATA OUT
DO
CLOCK
CP
Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
PARALLEL DATA OUT
R-2R LADDER
R = 50k
1/4 MM54C909
ANALOG INPUT
COMPARATOR

12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly


VREF = 10V
E
VCC
D
S
MM54C905/MM74C905
CC
CLOCK
CP
Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
DO
SERIAL DATA OUT
PARALLEL DATA OUT
MM54C902 /MM74C902 OR MM54C904 /MM74C904
100k
100k
50k
50k
100k
R-2R LADDER
1/4 MM54C909
50k
ANALOG INPUT

TL/F/5712-4

Definition of Terms

CP: Register *clock* input.

$\overline{CC}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{Q}$11: Complement of register MSB output.

QI (I = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q-10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

Section 4

Digital-to-Analog Converters

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***Devices Not Covered In Last Publication**

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Definition of Terms
D/A Converters

Conversion Time: The time required for a complete measurement by an analog-to-digital converter.

DC Common-Mode Error: This specification applies to ADCs with differential inputs. It is the change in the output code that occurs when the analog voltages on the two inputs are changed by an equal amount. It is expressed in LSBs.

Differential Nonlinearity: Ideally, any two adjacent digital codes correspond to measured analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. For example, a DAC with a 1.5 LSB output change for a 1 LSB digital code change exhibits ½ LSB differential non-linearity. Differential non-linearity may be expressed in fractional bits or as a percentage of full scale. A differential non-linearity greater than 1 LSB will lead to a non-monotonic transfer function in a DAC and missing codes in an ADC.

Gain Error (Full Scale Error): For an ADC, the difference (usually expressed in LSBs) between the input voltage that should ideally produce a full scale output code and the actual input voltage that produces that code. For DACs, it is the difference between the output voltage (or current) with full scale input code and the ideal voltage (or current) that should exist with a full scale input code.

Gain Temperature Coefficient (Full Scale Temperature Coefficient): Change in gain error divided by change in temperature. Usually expressed in parts per million per degree Celsius (ppm/°C).

Integral Nonlinearity (Linearity Error): Worst case deviation from the line between the endpoints (zero and full scale). Can be expressed as a percentage of full scale or in fractions of an LSB.

LSB (Least-Significant Bit): In a binary coded system this is the bit that carries the smallest value or weight. Its value is the full scale voltage (or current) divided by 2^n, where n is the resolution of the converter.

Monotonicity: A monotonic function has a slope whose sign does not change. A monotonic DAC has an output that changes in the same direction (or remains constant) for each increase in the input code. The converse is true for decreasing codes.

MSB (Most Significant Bit): In a binary coded system this is the bit that has the largest value or weight. Its value is one half of full scale.

Multiplying DAC: In a sense, every DAC is a multiplying DAC since the output voltage (or current) is equal to the reference voltage times a constant determined by the digital input code divided by 2^n (n is the number of bits of resolution). In a two quadrant multiplying DAC the reference voltage or the digital input code can change the output voltage polarity. If both the reference voltage and the digital code change the output voltage polarity, four quadrant multiplication exists.

Offset Error (Zero Error): In a DAC, this is the output voltage that exists when the input digital code is set to give an ideal output of zero volts. In the case of an ADC, this is the difference between the ideal input voltage (½ LSB) and the actual input voltage that is needed to make the transition from zero to 1 LSB. All the digital codes in the transfer curve are offset by the same value. Many converters allow nulling of offset with an external potentiometer. Offset error is usually expressed in LSBs.

Power Supply Rejection (Power Supply Sensitivity): The sensitivity of a converter to changes in the dc power supply voltages.

Quantizing Error: The error inherent in all A/D conversions. Since even an "ideal" converter has finite resolution, any analog voltage that falls between two adjacent output codes will result in an output code that is inaccurate by up to ½ LSB.

Ratiometric Operation: Many A/D applications require a stable and accurate reference voltage against which the input voltage is compared. This approach results in an **absolute conversion**. Some applications, however, use transducers or other signal sources whose output voltages are proportional to some external reference. In these **ratiometric** applications, the reference for the signal source should be connected to the reference input of the converter. Thus, any variations in the source reference voltage will also change the converter reference voltage and produce an accurate conversion.

Resolution: The smallest analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in bits, where the number of analog levels is equal to 2^n. As an example, a 12-bit converter divides the analog signal into $2^{12} = 4096$ discrete voltage (or current) levels.

Settling Time: The time from a change in input code until a DAC's output signal remains within ± ½ LSB (or some other specified tolerance) of the final value.

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D/A Converter Selection Guide

Part No.	Resolution (Bits)	Linearity @ 25°C % (Max)	Settling Time (+½ LSB)	Supplies (V)	Temperature Range*			Package	Comments
					M	I	C		
ADC0852	8	0.19		5		•	•	8-Pin DIP	DAC, Comparator, Serial Input
ADC0854	8	0.19		5		•	•	14-Pin DIP	DAC, Comparator, Serial Input
DAC0800	8	0.19	100 ns	±5 to ±15	•		•	16-Pin DIP 16-Pin S.O.	High-Speed Multiplying
DAC0801	8	0.39	100 ns	±5 to ±15	•		•	16-Pin DIP 16-Pin S.O.	High-Speed Multiplying
DAC0802	8	0.10	100 ns	±5 to ±15	•		•	16-Pin DIP 16-Pin S.O.	High-Speed Multiplying
DAC0806	8	0.78	150 ns	±5 to ±15			•	16-Pin DIP 16-Pin S.O.	Multiplying
DAC0807	8	0.39	150 ns	±5 to ±15			•	16-Pin DIP 16-Pin S.O.	Multiplying
DAC0808	8	0.19	150 ns	±5 to ±15	•		•	16-Pin DIP 16-Pin S.O.	Multiplying
DAC0830	8	0.05	1 µs	5 to 15	•	•	•	20-Pin DIP 20-Pin S.O. 20-Pin PCC	µP Compatible 4-Quadrant Multiplying
DAC0831	8	0.10	1 µs	5 to 15			•	20-Pin DIP	µP Compatible 4-Quadrant Multiplying
DAC0832	8	0.20	1 µs	5 to 15		•	•	20-Pin DIP 20-Pin S.O. 20-Pin PCC	µP Compatible 4-Quadrant Multiplying
DAC1000	10	0.05	500 ns	5 to 15	•	•	•	24-Pin DIP	µP Compatible Double Buffered
DAC1001	10	0.1	500 ns	5 to 15		•	•	24-Pin DIP	µP Compatible Double Buffered
DAC1002	10	0.2	500 ns	5 to 15	•	•	•	24-Pin DIP	µP Compatible Double Buffered
DAC1006	10	0.05	500 ns	5 to 15	•	•	•	20-Pin DIP	µP Compatible Double Buffered
DAC1007	10	0.1	500 ns	5 to 15		•	•	20-Pin DIP	µP Compatible Double Buffered
DAC1008	10	0.2	500 ns	5 to 15	•		•	20-Pin DIP	µP Compatible Double Buffered

D/A Converter Selection Guide (Continued)

Part No.	Resolution (Bits)	Linearity @ 25°C % (Max)	Settling Time (+½ LSB)	Supplies (V)	Temperature Range*			Package	Comments
					M	I	C		
DAC1020	10	0.05	500 ns	5 to 15	●	●	●	16-Pin DIP	4-Quadrant Multiplying
DAC1021	10	0.1	500 ns	5 to 15	●	●	●	16-Pin DIP	4-Quadrant Multiplying
DAC1022	10	0.2	500 ns	5 to 15	●	●	●	16-Pin DIP	4-Quadrant Multiplying
DAC1208	12	0.012	1 μs	5 to 15		●	●	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1209	12	0.024	1 μs	5 to 15		●	●	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1210	12	0.05	1 μs	5 to 15		●	●	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1218	12	0.012	1 μs	5 to 15		●	●	18-Pin DIP	4-Quadrant Multiplying
DAC1219	12	0.024	1 μs	5 to 15		●	●	18-Pin DIP	4-Quadrant Multiplying
DAC1220	12	0.05	500 ns	5 to 15	●	●	●	18-Pin DIP	4-Quadrant Multiplying
DAC1221	12	0.1	500 ns	5 to 15			●	18-Pin DIP	4-Quadrant Multiplying
DAC1222	12	0.2	500 ns	5 to 15	●	●	●	18-Pin DIP	4-Quadrant Multiplying
DAC1230	12	0.012	1 μs	5 to 15		●	●	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1231	12	0.024	1 μs	5 to 15		●	●	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1232	12	0.05	1 μs	5 to 15		●	●	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1265A	12	0.006	200 ns	±15	●		●	24-Pin DIP	High-Speed
DAC1265	12	0.012	200 ns	±15	●		●	24-Pin DIP	High-Speed
DAC1266A	12	0.006	200 ns	±12 to ±15	●		●	24-Pin DIP	High-Speed
DAC1266	12	0.012	200 ns	±12 to ±15	●		●	24-Pin DIP	High-Speed

*Ambient temperature range for "M" is −55°C to +125°C, "I" is −25°C to +85°C or −40°C to +85°C, "C" 0°C to +70°C.

National Semiconductor Corporation

DAC0800/DAC0801/DAC0802 8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

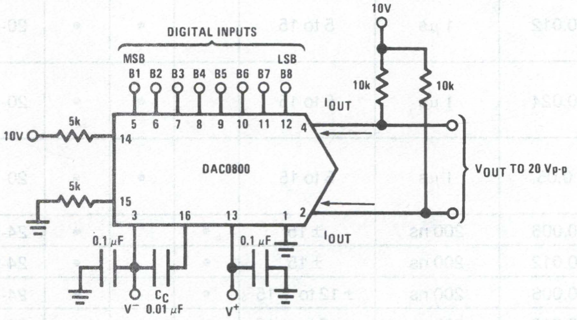
The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C, DAC0801C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, DAC-08E and DAC-08H, respectively.

Features

- Fast settling output current 100 ns
- Full scale error ±1 LSB
- Nonlinearity over temperature ±0.1%
- Full scale current drift ±10 ppm/°C
- High output compliance −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range ±4.5V to ±18V
- Low power consumption 33 mW at ±5V
- Low cost

Typical Applications



TL/H/5686–1

FIGURE 1. ±20 $V_{P\text{-}P}$ Output Digital-to-Analog Converter (Note 4)

Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A)*		N Package (N16A)*		SO Package (M16A)
±0.1% FS	$-55°C \le T_A \le +125°C$	DAC0802LJ	DAC-08AQ			
±0.1% FS	$0°C \le T_A \le +70°C$	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
±0.19% FS	$-55°C \le T_A \le +125°C$	DAC0800LJ	DAC-08Q			
±0.19% FS	$0°C \le T_A \le +70°C$	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM
±0.39% FS	$0°C \le T_A \le +70°C$	DAC0801LCJ	DAC-08CQ	DAC0801LCN	DAC-08CP	DAC0801LCM

*Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	±18V or 36V
Power Dissipation (Note 2)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs ($V_{S^-} = -15V$)	4.25 mA
ESD Susceptibility (Note 3)	TBD V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Conditions (Note 1)

	Min	Max	Units
Temperature (T_A)			
DAC0802L	−55	+125	°C
DAC0800L	−55	+125	°C
DAC0800LC	0	+70	°C
DAC0801LC	0	+70	°C
DAC0802LC	0	+70	°C

Electrical Characteristics

The following specifications apply for $V_S = \pm 15V$, $I_{REF} = 2$ mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802L/ DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19			±0.39	%FS
t_s	Settling Time	To ±½ LSB, All Bits Switched "ON" or "OFF", $T_A = 25°C$		100	135					100	150	ns
		DAC0800L					100	135				ns
		DAC0800LC					100	150				ns
tPLH, tPHL	Propagation Delay	$T_A = 25°C$										
	Each Bit			35	60		35	60		35	60	ns
	All Bits Switched			35	60		35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change <½ LSB, $R_{OUT} > 20$ MΩ Typ	−10		18	−10		18	−10		18	V
I_{FS4}	Full Scale Current	$V_{REF} = 10.000V$, R14 = 5.000 kΩ R15 = 5.000 kΩ, $T_A = 25°C$	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±1	±8.0		±2	±16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	$V^- = -5V$	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		$V^- = -8V$ to $-18V$	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels											
V_{IL}	Logic "0"	$V_{LC} = 0V$			0.8			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			2.0			V
	Logic Input Current	$V_{LC} = 0V$										
I_{IL}	Logic "0"	$-10V \le V_{IN} \le +0.8V$		−2.0	−10		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic "1"	$2V \le V_{IN} \le +18V$		0.002	10		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	$V^- = -15V$	−10		18	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	$V_S = \pm 15V$	−10		13.5	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate	*(Figure 12)*	4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$4.5V \le V^+ \le 18V$		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$		$-4.5V \le V^- \le 18V$ $I_{REF} = 1$ mA		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
	Power Supply Current	$V_S = \pm 5V$, $I_{REF} = 1$ mA										
I+				2.3	3.8		2.3	3.8		2.3	3.8	mA
I−				−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	mA
		$V_S = 5V$, $-15V$, $I_{REF} = 2$ mA										
I+				2.4	3.8		2.4	3.8		2.4	3.8	mA
I−				−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	mA
		$V_S = \pm 15V$, $I_{REF} = 2$ mA										
I+				2.5	3.8		2.5	3.8		2.5	3.8	mA
I−				−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	mA

Electrical Characteristics (Continued)

The following specifications apply for $V_S = \pm 15V$, $I_{REF} = 2\ mA$ and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802L/ DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
P_D	Power Dissipation	$\pm 5V$, $I_{REF} = 1\ mA$ $5V, -15V$, $I_{REF} = 2\ mA$ $\pm 15V$, $I_{REF} = 2\ mA$		33 108 135	48 136 174		33 108 135	48 136 174		33 108 135	48 136 174	mW mW mW

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

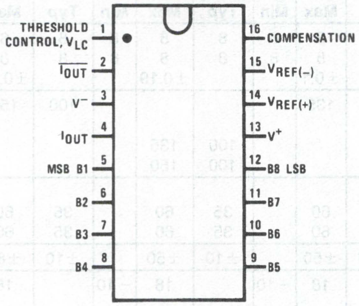
Note 2: The maximum junction temperature of the DAC0800, DAC0801 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the Dual-In-Line J package must be derated based on a thermal resistance of 100°C/W, junction-to-ambient, 175°C/W for the molded Dual-In-Line N package and 100°C/W for the Small Outline M package.

Note 3: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 4: Pin-out numbers for the DAC080X represent the Dual-In-Line package. The Small Outline package pin-out differs from the Dual-In-Line package.

Connection Diagrams

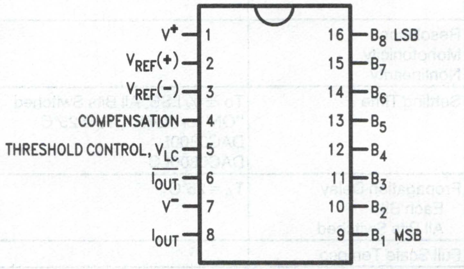
Dual-In-Line Package


1 THRESHOLD CONTROL, V_{LC}
2 $\overline{I_{OUT}}$
3 V−
4 I_{OUT}
5 MSB B1
6 B2
7 B3
8 B4
16 COMPENSATION
15 $V_{REF}(-)$
14 $V_{REF}(+)$
13 V+
12 B8 LSB
11 B7
10 B6
9 B5

TL/H/5686-13

Top View

Small Outline Package

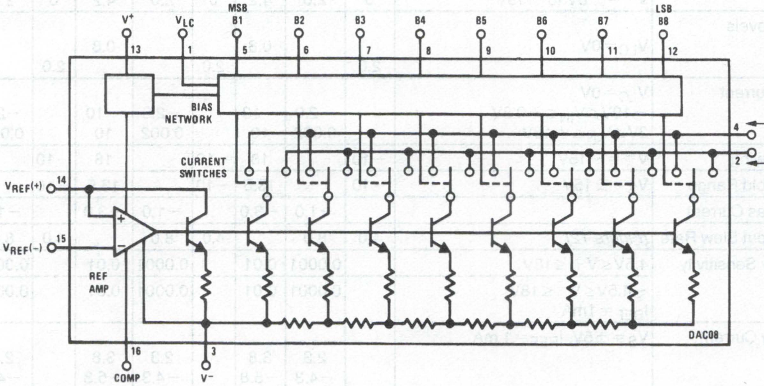

V+ 1
$V_{REF}(+)$ 2
$V_{REF}(-)$ 3
COMPENSATION 4
THRESHOLD CONTROL, V_{LC} 5
I_{OUT} 6
V− 7
$\overline{I_{OUT}}$ 8
16 B_8 LSB
15 B_7
14 B_6
13 B_5
12 B_4
11 B_3
10 B_2
9 B_1 MSB

TL/H/5686-14

Top View

See Ordering Information

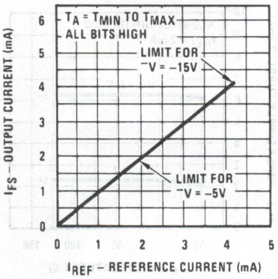
Block Diagram (Note 4)


V+ 13
V_{LC} 1
MSB B1 5
B2 6
B3 7
B4 8
B5 9
B6 10
B7 11
LSB B8 12
BIAS NETWORK
CURRENT SWITCHES
$V_{REF}(+)$ 14
$V_{REF}(-)$ 15
REF AMP
4 I_{OUT}
2 $\overline{I_{OUT}}$
16 COMP
3 V−
DAC08

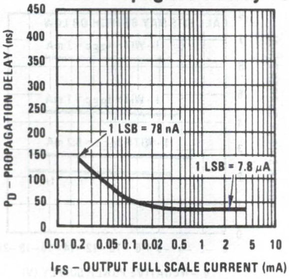
TL/H/5686-2

Typical Performance Characteristics

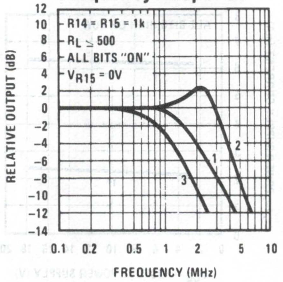
Full Scale Current vs Reference Current



LSB Propagation Delay Vs I_{FS}



Reference Input Frequency Response

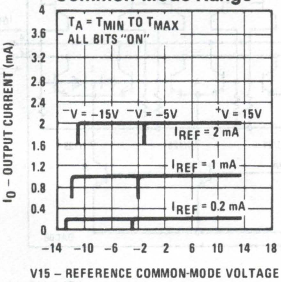


Curve 1: $C_C = 15$ pF, $V_{IN} = 2$ Vp-p centered at 1V.

Curve 2: $C_C = 15$ pF, $V_{IN} = 50$ mVp-p centered at 200 mV.

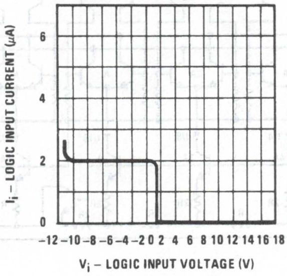
Curve 3: $C_C = 0$ pF, $V_{IN} = 100$ mVp-p at 0V and applied through 50 Ω connected to pin 14.2V applied to R14.

Reference Amp Common-Mode Range

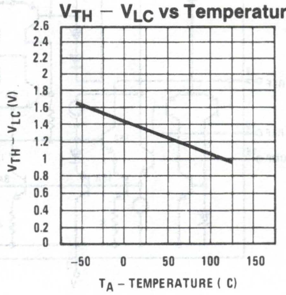


Note. Positive common-mode range is always (V+) − 1.5V

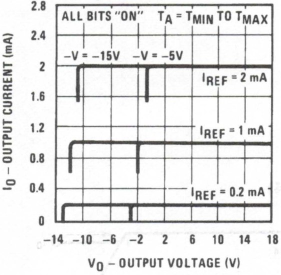
Logic Input Current vs Input Voltage



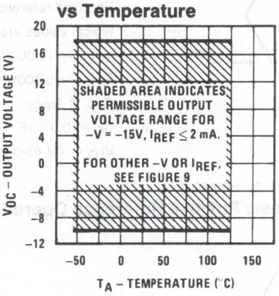
$V_{TH} - V_{LC}$ vs Temperature



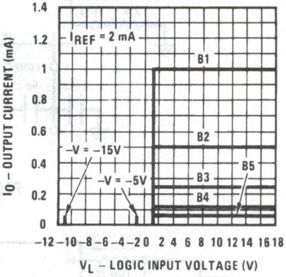
Output Current vs Output Voltage (Output Voltage Compliance)



Output Voltage Compliance vs Temperature



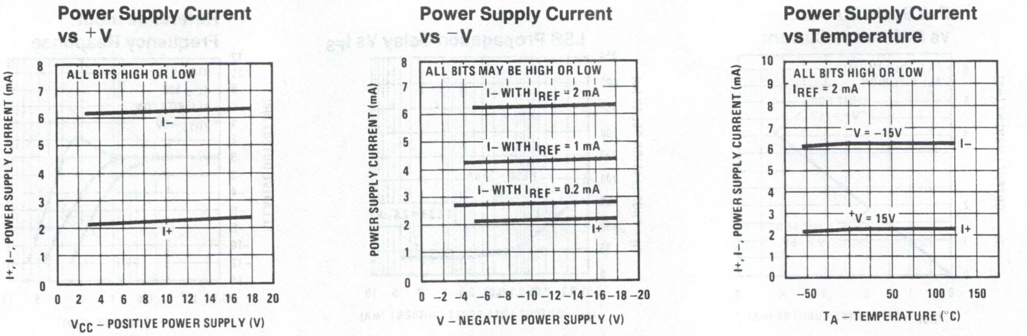
Bit Transfer Characteristics



TL/H/5686-3

Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

Typical Performance Characteristics (Continued)

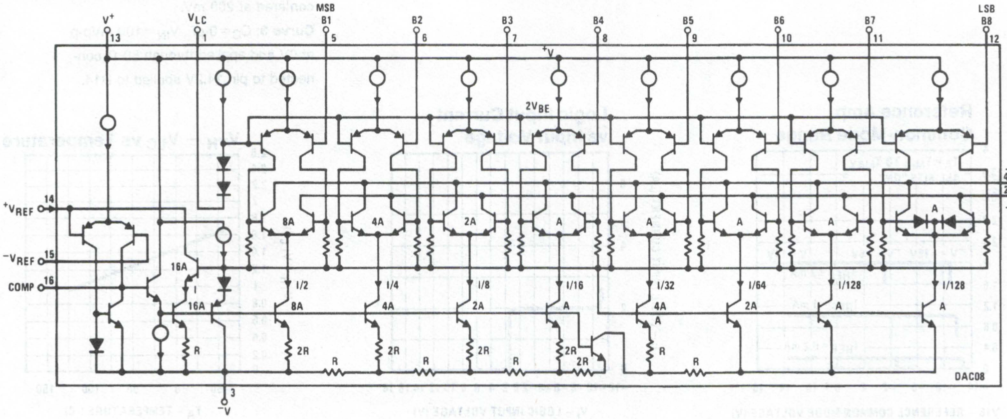

Power Supply Current vs +V

Power Supply Current vs −V

Power Supply Current vs Temperature

TL/H/5686-4

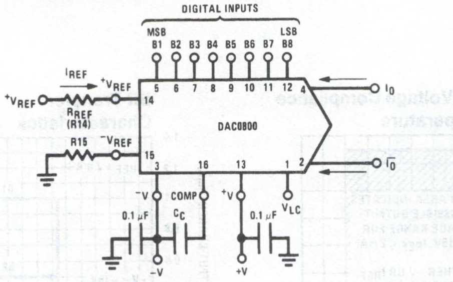
Equivalent Circuit


V+
13
VLC
1
MSB
B1
5
B2
6
B3
7
B4
8
B5
9
B6
10
B7
11
LSB
B8
12
+V
2VBE
IOUT
4
2
IOUT
+VREF
14
−VREF
15
COMP
16
16A
16A
8A
4A
2A
A
I/2
I/4
I/8
I/16
I/32
I/64
I/128
I/128
R
2R
DAC08
3
−V

TL/H/5686-15

FIGURE 2

Typical Applications (Continued)


DIGITAL INPUTS
MSB
B1 B2 B3 B4 B5 B6 B7 B8
LSB
5 6 7 8 9 10 11 12
4
I_O
I_{REF}
+VREF
+VREF
RREF
(R14)
14
R15
−VREF
15
DAC0800
3
16
13
1
2
$\overline{I_O}$
−V
COMP
CC
+V
VLC
0.1 µF
0.1 µF
−V
+V

$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation, typical values are:

$V_{REF} = 10.000V$

$R_{REF} = 5.000k$

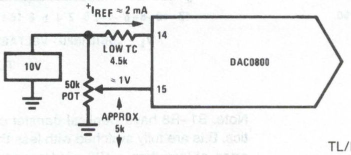
$R15 \approx R_{REF}$

$C_C = 0.01\ \mu F$

$V_{LC} = 0V$ (Ground)

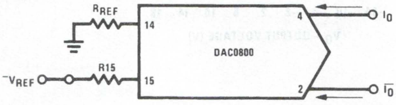
TL/H/5686-5

FIGURE 3. Basic Positive Reference Operation (Note 4)


$+I_{REF} \approx 2$ mA
14
10V
LOW TC
4.5k
≈ 1V
50k
POT
APPROX
5k
15
DAC0800

TL/H/5686-21

FIGURE 4. Recommended Full Scale Adjustment Circuit (Note 4)


RREF
14
DAC0800
4
I_O
−VREF
R15
15
2
$\overline{I_O}$

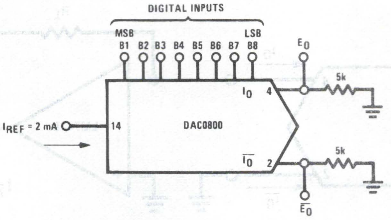
TL/H/5686-16

$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note. R_{REF} sets I_{FS}; R15 is for bias current cancellation

FIGURE 5. Basic Negative Reference Operation (Note 4)

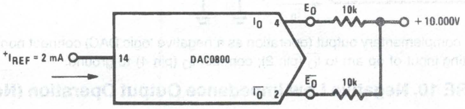
Typical Applications (Continued)


DIGITAL INPUTS
MSB
LSB
B1 B2 B3 B4 B5 B6 B7 B8
E_O
5k
I_O 4
I_{REF} = 2 mA
14
DAC0800
$\overline{I_O}$ 2
5k
$\overline{E_O}$

TL/H/5686-17

	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale − LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale + LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale − LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

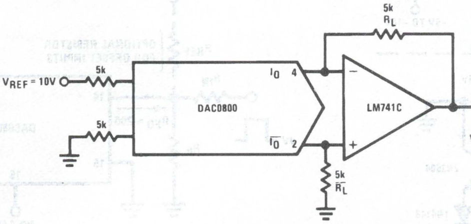
FIGURE 6. Basic Unipolar Negative Operation (Note 4)


E_O
10k
+10.000V
I_O 4
$^+I_{REF}$ = 2 mA
14
DAC0800
$\overline{E_O}$
10k
$\overline{I_O}$ 2

TL/H/5686-6

	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale − LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale − LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

FIGURE 7. Basic Bipolar Output Operation (Note 4)


5k
R_L
V_{REF} = 10V
5k
I_O 4
DAC0800
LM741C
5k
$\overline{I_O}$ 2
5k
$\overline{R_L}$

$E_O = V_{REF}\left(\frac{-255}{256} + \frac{2X}{256}\right)$

where X is the input code and

$R_L = \overline{R_L} = R_{REF}$

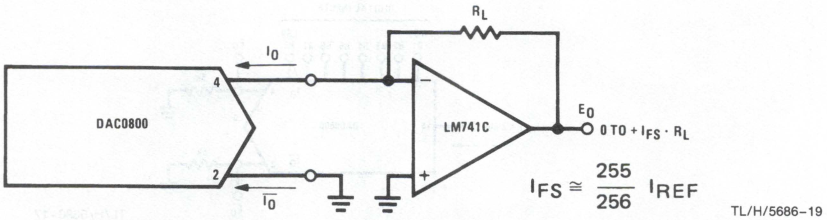
TL/H/5686-18

If $R_L = \overline{R_L}$ within ±0.05%, output is symmetrical about ground

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale − LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−)Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	−9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.960

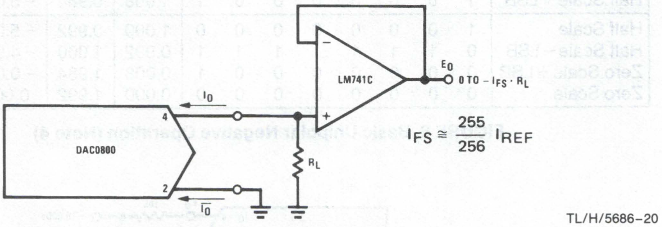
FIGURE 8. Symmetrical Offset Binary Operation (Note 4)

Typical Applications (Continued)


RL
IO
DAC0800
4
2
$\overline{I_O}$
LM741C
−
+
EO
0 TO + IFS · RL
$I_{FS} \cong \frac{255}{256} I_{REF}$
TL/H/5686–19

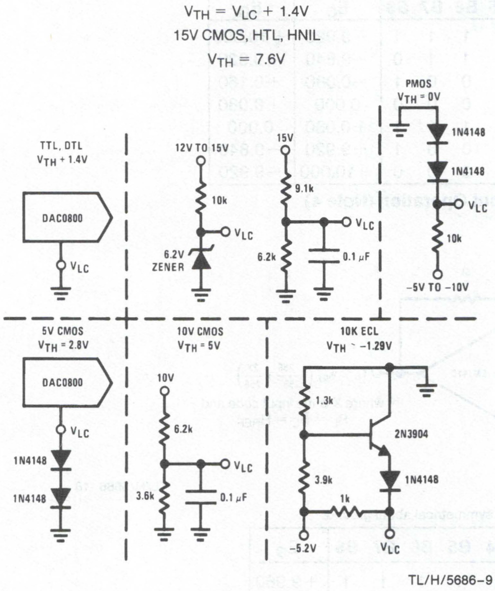
For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_O}$ (pin 2), connect I_O (pin 4) to ground.

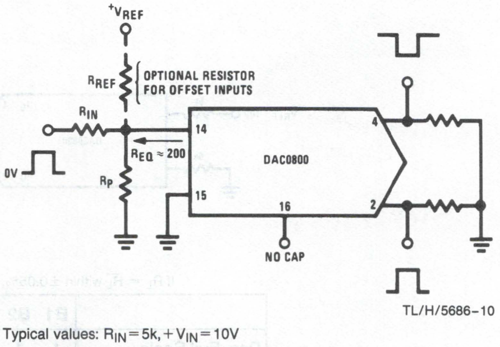
FIGURE 9. Positive Low Impedance Output Operation (Note 4)


LM741C
−
+
EO
0 TO − IFS · RL
IO
4
DAC0800
2
$\overline{I_O}$
RL
$I_{FS} \cong \frac{255}{256} I_{REF}$
TL/H/5686–20

For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to $\overline{I_O}$ (pin 2); connect I_O (pin 4) to ground.

FIGURE 10. Negative Low Impedance Output Operation (Note 4)


VTH = VLC + 1.4V
15V CMOS, HTL, HNIL
VTH = 7.6V
TTL, DTL
VTH + 1.4V
DAC0800
VLC
12V TO 15V
10k
VLC
6.2V ZENER
15V
9.1k
VLC
6.2k
0.1 μF
PMOS
VTH = 0V
1N4148
1N4148
VLC
10k
−5V TO −10V
5V CMOS
VTH = 2.8V
DAC0800
VLC
1N4148
1N4148
10V CMOS
VTH = 5V
10V
6.2k
VLC
3.6k
0.1 μF
10K ECL
VTH ~ −1.29V
1.3k
2N3904
3.9k
1N4148
1k
−5.2V
VLC
TL/H/5686–9


+VREF
RREF
OPTIONAL RESISTOR FOR OFFSET INPUTS
RIN
REQ ≈ 200
0V
RP
14
15
16
DAC0800
4
2
NO CAP
TL/H/5686–10

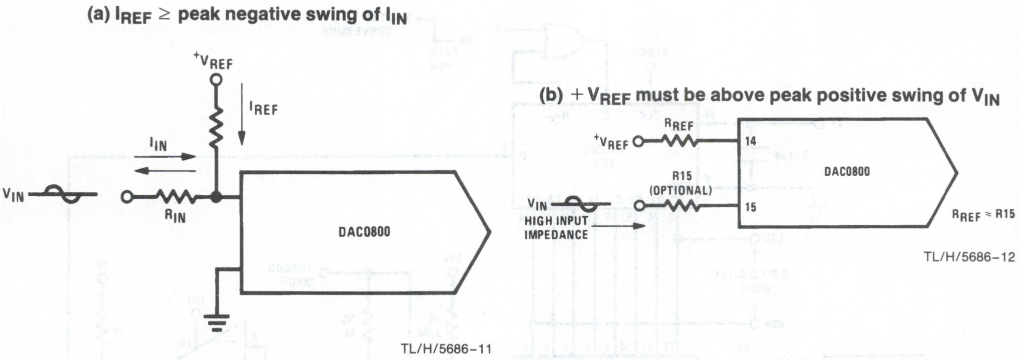
Typical values: $R_{IN} = 5k, +V_{IN} = 10V$

Note. Do not exceed negative logic input range of DAC.

FIGURE 11. Interfacing with Various Logic Families

FIGURE 12. Pulsed Reference Operation (Note 4)

Typical Applications (Continued)


(a) $I_{REF} \geq$ peak negative swing of I_{IN}

(b) $+V_{REF}$ must be above peak positive swing of V_{IN}

+VREF
IREF
IIN
VIN
RIN
DAC0800
TL/H/5686-11
RREF
+VREF
14
R15
(OPTIONAL)
VIN
HIGH INPUT
IMPEDANCE
15
DAC0800
RREF ≈ R15
TL/H/5686-12

FIGURE 13. Accommodating Bipolar References (Note 4)

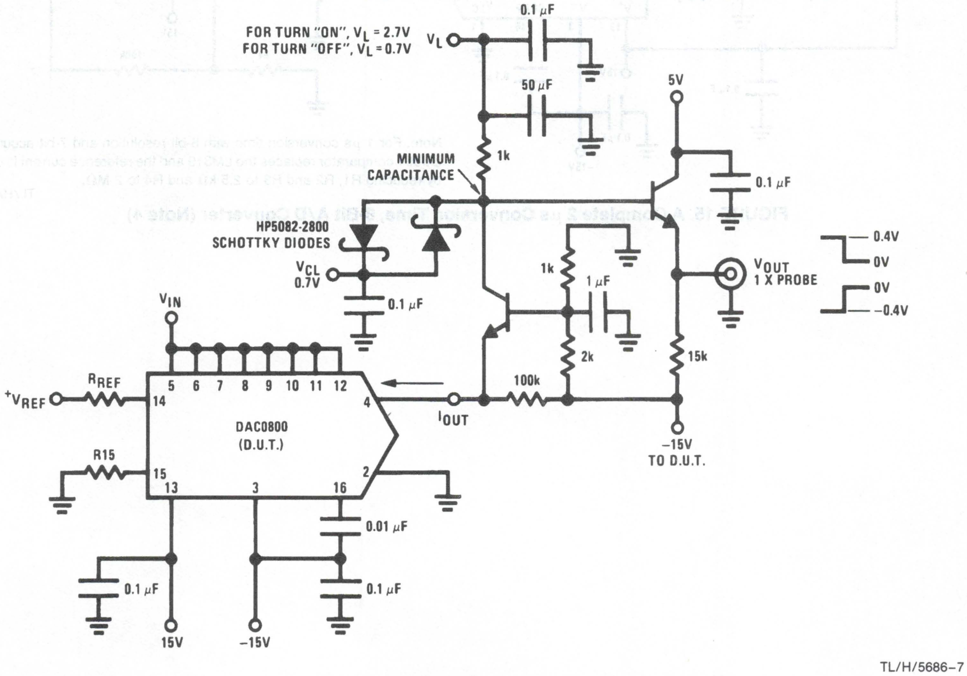
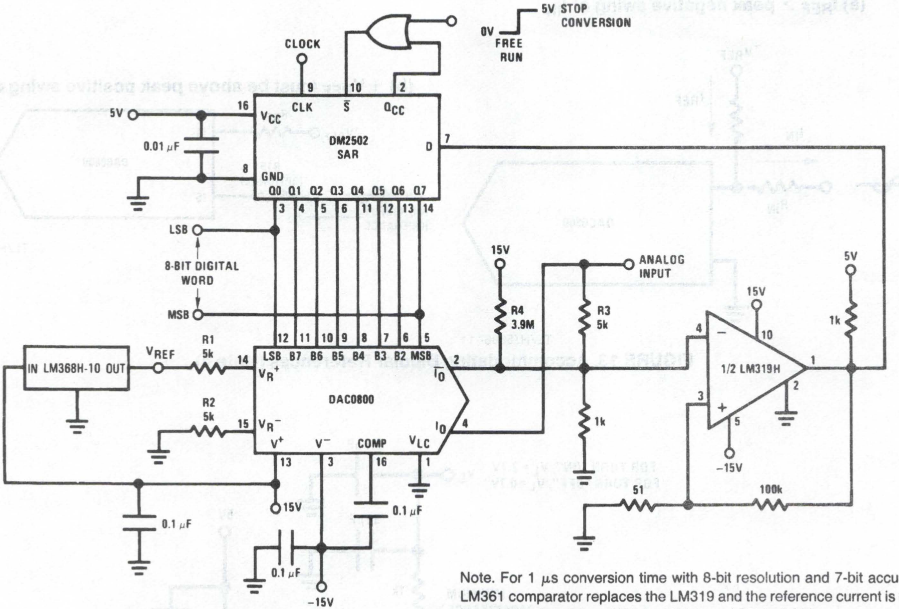

FOR TURN "ON", VL = 2.7V
FOR TURN "OFF", VL = 0.7V
VL
0.1 µF
50 µF
1k
MINIMUM
CAPACITANCE
HP5082-2800
SCHOTTKY DIODES
VCL
0.7V
0.1 µF
5V
0.1 µF
1k
1 µF
2k
100k
15k
VOUT
1 X PROBE
0.4V
0V
0V
−0.4V
−15V
TO D.U.T.
VIN
+VREF
RREF
14
R15
15
5
6
7
8
9
10
11
12
4
DAC0800
(D.U.T.)
IOUT
2
13
3
16
0.01 µF
0.1 µF
0.1 µF
15V
−15V
TL/H/5686-7

FIGURE 14. Settling Time Measurement (Note 4)

Typical Applications (Continued)


CLOCK
5V STOP CONVERSION
0V FREE RUN
5V
0.01 μF
16
VCC
8
GND
9
CLK
10
S̄
2
QCC
DM2502 SAR
D
7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
3 4 5 6 11 12 13 14
LSB
8-BIT DIGITAL WORD
MSB
15V
R4 3.9M
ANALOG INPUT
R3 5k
15V
5V
1k
4
10
1/2 LM319H
1
2
3
5
−15V
1k
12 11 10 9 8 7 6 5
LSB B7 B6 B5 B4 B3 B2 MSB
IN LM368H-10 OUT
VREF
R1 5k
14
VR+
DAC0800
Ī0
2
I0
4
R2 5k
15
VR−
V+
V−
COMP
VLC
13
3
16
1
15V
0.1 μF
0.1 μF
0.1 μF
−15V
51
100k

Note. For 1 μs conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 kΩ and R4 to 2 MΩ.

TL/H/5686-8

FIGURE 15. A Complete 2 μs Conversion Time, 8-Bit A/D Converter (Note 4)

National Semiconductor Corporation

DAC0808, DAC0807, DAC0806 8-Bit D/A Converters

General Description

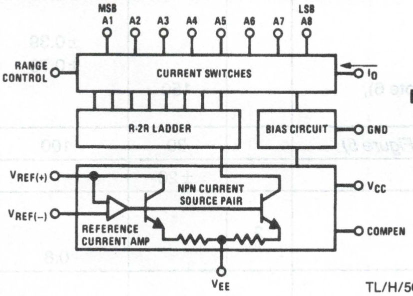
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/ 256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

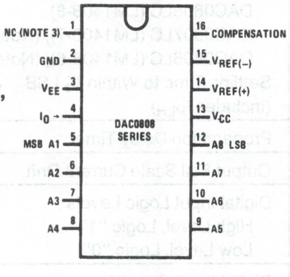
- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams


MSB
A1
A2
A3
A4
A5
A6
A7
LSB
A8
RANGE CONTROL
CURRENT SWITCHES
I_O
R-2R LADDER
BIAS CIRCUIT
GND
$V_{REF(+)}$
$V_{REF(-)}$
NPN CURRENT SOURCE PAIR
REFERENCE CURRENT AMP
V_{CC}
COMPEN
V_{EE}

TL/H/5687–1

Dual-In-Line Package

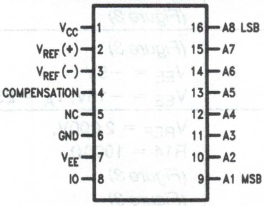

NC (NOTE 3) 1
GND 2
V_{EE} 3
I_O 4
MSB A1 5
A2 6
A3 7
A4 8
9 A5
10 A6
11 A7
12 A8 LSB
13 V_{CC}
14 $V_{REF(+)}$
15 $V_{REF(-)}$
16 COMPENSATION
DAC0808 SERIES

TOP VIEW

TL/H/5687–2

Order Number DAC0808, DAC0807, or DAC0806
See NS Package Number J16A, M16A or N16A

Small-Outline Package


V_{CC} 1
V_{REF} (+) 2
V_{REF} (−) 3
COMPENSATION 4
NC 5
GND 6
V_{EE} 7
IO 8
9 A1 MSB
10 A2
11 A3
12 A4
13 A5
14 A6
15 A7
16 A8 LSB

Top View

TL/H/5687–13

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS				
		J PACKAGE (J16A)*		N PACKAGE (N16A)*		SO PACKAGE (M16A)
8-bit	$-55°C \leq T_A \leq +125°C$	DAC0808LJ	MC1508L8			
8-bit	$0°C \leq T_A \leq +75°C$	DAC0808LCJ	MC1408L8	DAC0808LCN	MC1408P8	DAC0808LCM
7-bit	$0°C \leq T_A \leq +75°C$	DAC0807LCJ	MC1408L7	DAC0807LCN	MC1408P7	DAC0807LCM
6-bit	$0°C \leq T_A \leq +75°C$	DAC0806LCJ	MC1408L6	DAC0806LCN	MC1408P6	DAC0806LCM

***Note.** Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	$+18\ V_{DC}$
V_{EE}	$-18\ V_{DC}$
Digital Input Voltage, V5–V12	$-10\ V_{DC}$ to $+18\ V_{DC}$
Applied Output Voltage, V_O	$-11\ V_{DC}$ to $+18\ V_{DC}$
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 3)	1000 mW
ESD Susceptibility (Note 4)	TBD
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
DAC0808L	$-55°C \leq T_A \leq +125°C$
DAC0808LC Series	$0 \leq T_A \leq +75°C$

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = $-15\ V_{DC}$, $V_{REF}/R14$ = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
	DAC0808L (LM1508-8), DAC0808LC (LM1408-8)				±0.19	%
	DAC0807LC (LM1408-7), (Note 5)				±0.39	%
	DAC0806LC (LM1408-6), (Note 5)				±0.78	%
	Settling Time to Within ½ LSB (Includes t_{PLH})	T_A = 25°C (Note 6), *(Figure 5)*		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 3)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 3)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 3)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω, *(Figure 3)*	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 3)*		0	4	μA
	Output Voltage Compliance (Note 2)	$E_r \leq 0.19\%$, T_A = 25°C				
	V_{EE} = −5V, I_{REF} = 1 mA				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}

Electrical Characteristics (Continued)

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SRI_{REF}	Reference Current Slew Rate	*(Figure 6)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	−5V ≤ V_{EE} ≤ −16.5V		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	*(Figure 3)*				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Range control is not required.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maixmum Ratings, whichever is lower. For this device, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

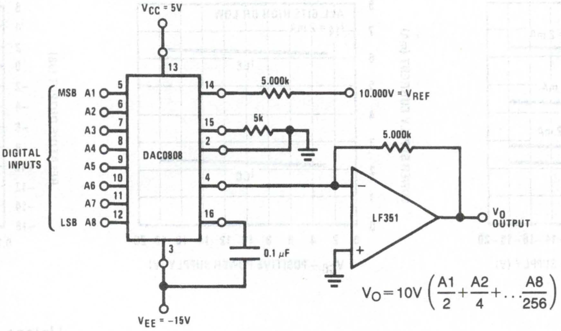
Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: All current switches are tested to guarantee at least 50% of rated current.

Note 6: All bits switched.

Note 7: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application



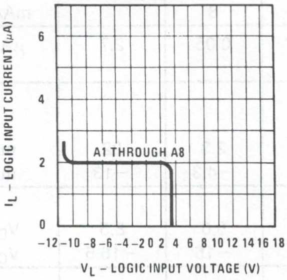
TL/H/5687-3

FIGURE 1. +10V Output Digital to Analog Converter (Note 7)

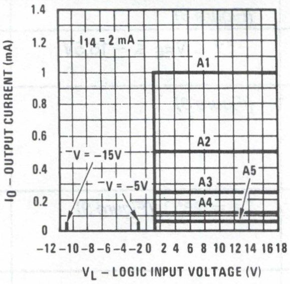
Typical Performance Characteristics

V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

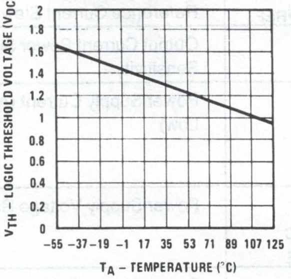
Logic Input Current vs Input Voltage



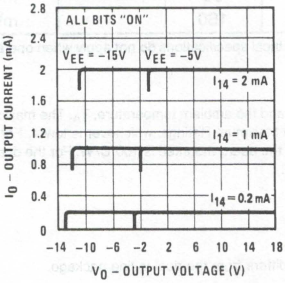
Bit Transfer Characteristics



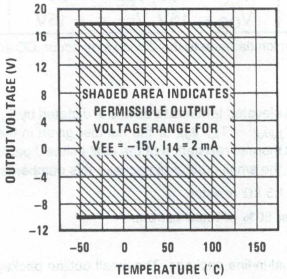
Logic Threshold Voltage vs Temperature



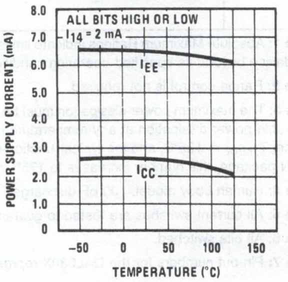
Output Current vs Output Voltage (Output Voltage Compliance)



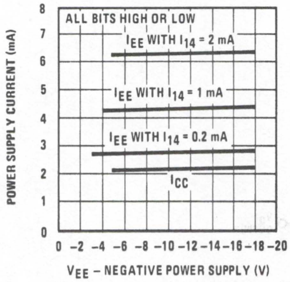
Output Voltage Compliance vs Temperature



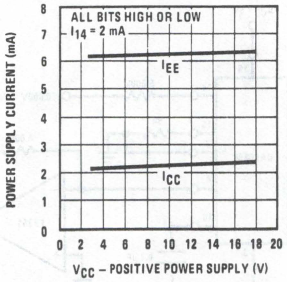
Typical Power Supply Current vs Temperature



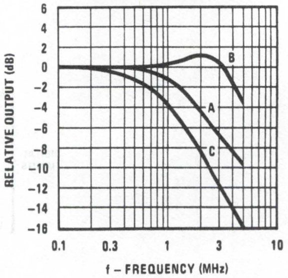
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



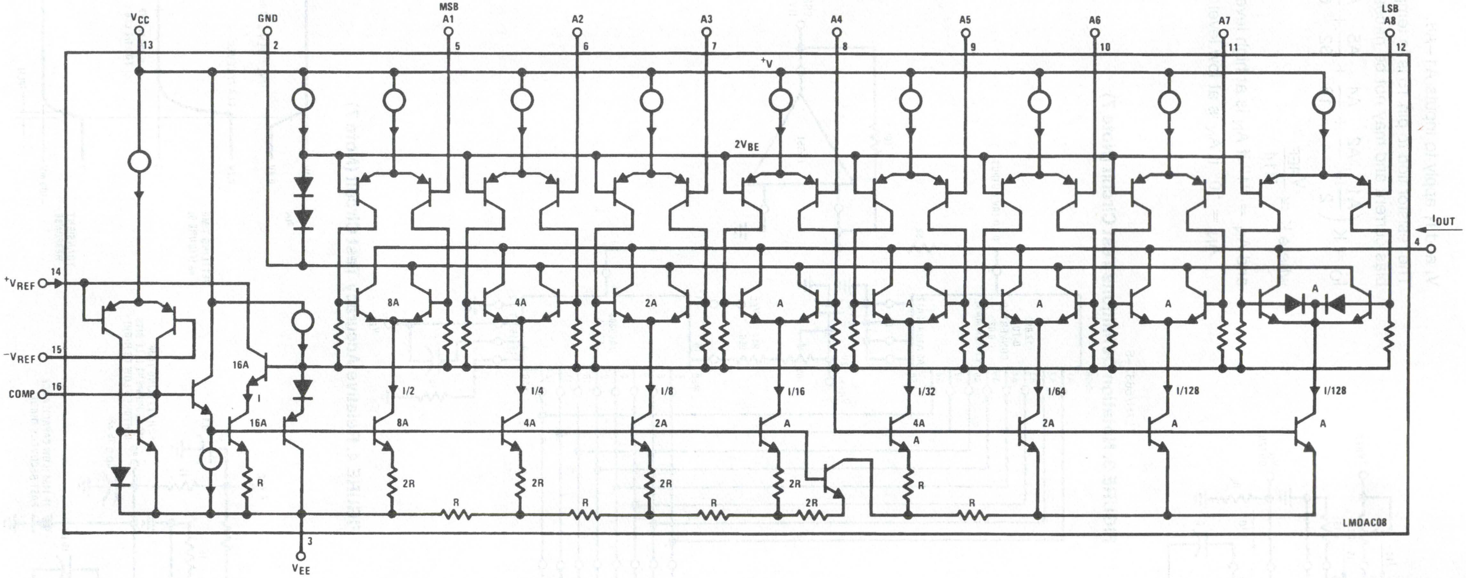
TL/H/5687–5

Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground.

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

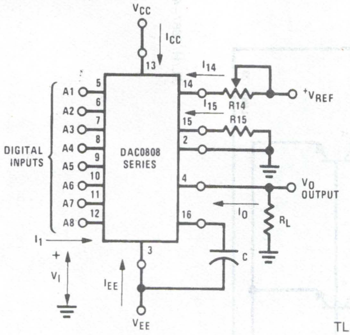
Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.


VCC
13
GND
2
MSB
A1
5
A2
6
A3
7
A4
8
A5
9
A6
10
A7
11
LSB
A8
12
+V
2VBE
IOUT
4
+VREF
14
−VREF
15
COMP
16
16A
I
16A
8A
4A
2A
A
A
A
A
A
1/2
1/4
1/8
1/16
1/32
1/64
1/128
1/128
8A
4A
2A
A
4A
A
2A
A
A
R
2R
2R
2R
2R
2R
R
R
R
R
R
VEE
3
LMDAC08

TL/H/5687–4

FIGURE 2. Equivalent Circuit of the DAC0808 Series (Note 7)

Test Circuits


V_CC
I_CC
13
I_14
14
+V_REF
I_15
R14
15
R15
2
DIGITAL INPUTS
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
DAC0808 SERIES
4
V_O OUTPUT
I_O
R_L
16
C
I_1
+
V_I
I_EE
3
V_EE

V_I and I_1 apply to inputs A1–A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

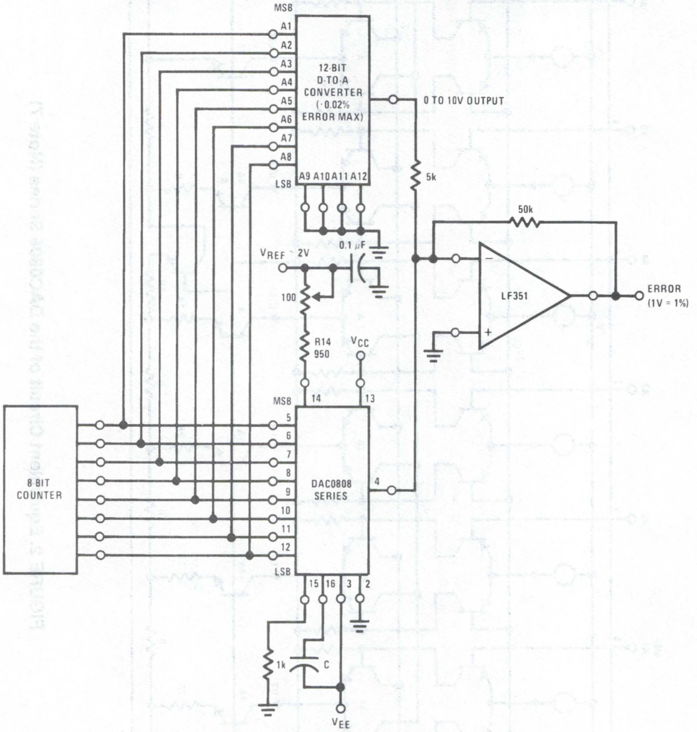
where $K \cong \dfrac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level

A_N = "0" if A_N is at low level

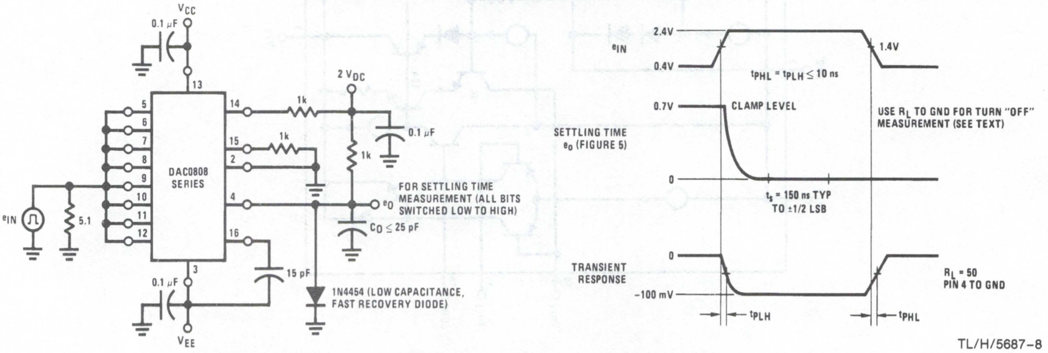
TL/H/5687–6

FIGURE 3. Notation Definitions Test Circuit (Note 7)


MSB
A1
A2
A3
A4
A5
A6
A7
A8
LSB
12-BIT D-TO-A CONVERTER (±0.02% ERROR MAX)
A9 A10 A11 A12
0 TO 10V OUTPUT
5k
50k
0.1 µF
V_REF ≈ 2V
100
R14 950
V_CC
LF351
ERROR (1V = 1%)
MSB
14
13
5
6
7
8
9
10
11
12
LSB
8-BIT COUNTER
DAC0808 SERIES
4
15
16
3
2
1k
C
V_EE

TL/H/5687–7

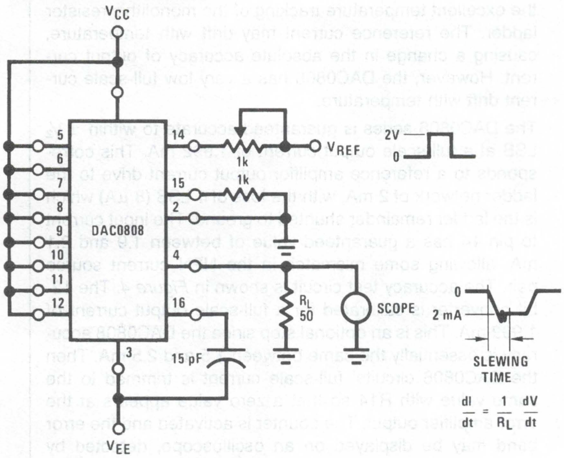
FIGURE 4. Relative Accuracy Test Circuit (Note 7)


V_CC
0.1 µF
13
5
6
7
8
9
10
11
12
DAC0808 SERIES
14
15
2
4
16
3
e_IN
5.1
0.1 µF
V_EE
2 V_DC
1k
1k
1k
0.1 µF
FOR SETTLING TIME MEASUREMENT (ALL BITS SWITCHED LOW TO HIGH)
e_O
C_O ≤ 25 pF
15 pF
1N4454 (LOW CAPACITANCE, FAST RECOVERY DIODE)
2.4V
0.4V
e_IN
1.4V
t_PHL = t_PLH ≤ 10 ns
0.7V
CLAMP LEVEL
USE R_L TO GND FOR TURN "OFF" MEASUREMENT (SEE TEXT)
SETTLING TIME e_0 (FIGURE 5)
0
t_s = 150 ns TYP TO ±1/2 LSB
TRANSIENT RESPONSE
0
−100 mV
R_L = 50 PIN 4 TO GND
t_PLH
t_PHL

TL/H/5687–8

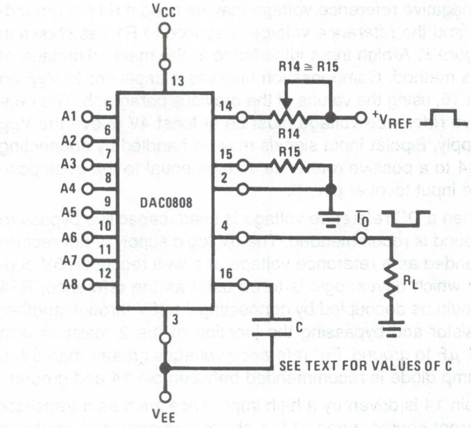
FIGURE 5. Transient Response and Settling Time (Note 7)

Test Circuits (Continued)


VCC
5
6
7
8
9
10
11
12
DAC0808
14
15
2
4
16
3
1k
1k
R15
VREF
2V
0
RL
50
SCOPE
0
2 mA
SLEWING
TIME
15 pF
VEE
$\frac{dI}{dt} = \frac{1}{R_L}\frac{dV}{dt}$

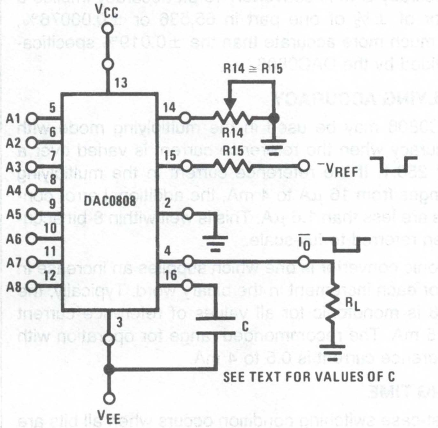
TL/H/5687–9

FIGURE 6. Reference Current Slew Rate Measurement (Note 7)


VCC
13
R14 ≥ R15
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
DAC0808
14
15
2
4
16
3
R14
R15
+VREF
I0
RL
C
SEE TEXT FOR VALUES OF C
VEE

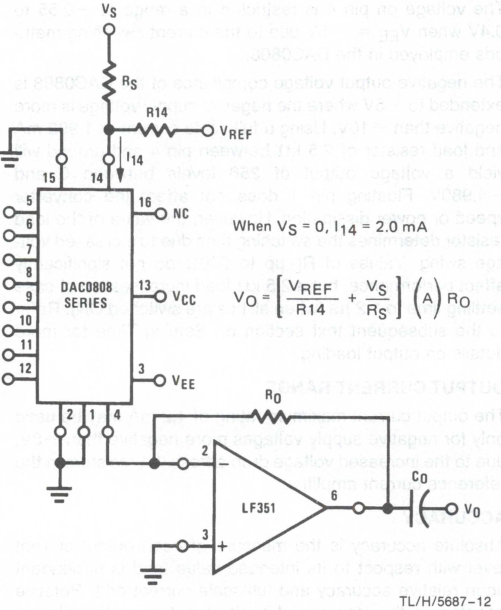
TL/H/5687–10

FIGURE 7. Positive V_{REF} (Note 7)


VCC
13
R14 ≥ R15
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
DAC0808
14
15
2
4
16
3
R14
R15
−VREF
I0
RL
C
SEE TEXT FOR VALUES OF C
VEE

TL/H/5687–11

FIGURE 8. Negative V_{REF} (Note 7)


VS
RS
R14
VREF
I14
15
14
16
NC
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
DAC0808 SERIES
13
VCC
3
VEE
2
1
4
RO
LF351
2
3
6
CO
VO
When $V_S = 0$, $I_{14} = 2.0$ mA
$V_O = \left[\frac{V_{REF}}{R14} + \frac{V_S}{R_S}\right](A) R_O$

TL/H/5687–12

FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit (Note 7)

Application Hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input currrent, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

Application Hints (Continued)

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.55 to 0.4V when $V_{EE} = -5V$ due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −8V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±½ LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±½ of one part in 65,536 or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within ±½ LSB, for 8-bit accuracy, and 100 ns to ½ LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

National Semiconductor Corporation

DAC0830/DAC0831/DAC0832 8-Bit μP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z80®, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DACs (MICRO-DAC™). For applications demanding higher resolution, the DAC1000 series (10-bits) and the DAC1208 and DAC1230 (12-bits) are available alternatives.

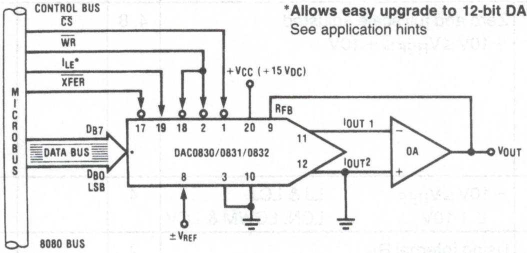
Features

- Double-buffered, single-buffered or flow-through digital data inputs
- Easy interchange and pin-compatible with 12-bit DAC1230 series
- Direct interface to all popular microprocessors
- Linearity specified with zero and full scale adjust only—NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates "STAND ALONE" (without μP) if desired
- Available in 20-pin small-outline or molded chip carrier package

Key Specifications

■ Current settling time	1 μs
■ Resolution	8 bits
■ Linearity (guaranteed over temp.)	8, 9, or 10 bits
■ Gain Tempco	0.0002% FS/°C
■ Low power dissipation	20 mW
■ Single power supply	5 to 15 V_{DC}

Typical Application

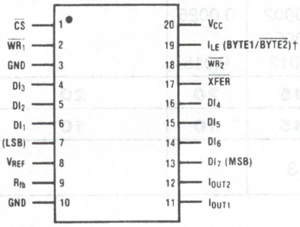

CONTROL BUS
CS
WR
ILE*
XFER
MICROBUS
8080 BUS
DB7
DATA BUS
DB0 LSB
17
19
18
2
1
20
9
11
12
8
3
10
DAC0830/0831/0832
+VCC (+15 VDC)
RFB
IOUT 1
IOUT2
OA
VOUT
±VREF

***Allows easy upgrade to 12-bit DAC1230,**
See application hints

TL/H/5608–1

Connection Diagrams (Top Views)

Dual-In-Line and Small-Outline Packages


CS 1
WR1 2
GND 3
DI3 4
DI2 5
DI1 6
DI0 (LSB) 7
VREF 8
Rfb 9
GND 10
20 VCC
19 ILE (BYTE1/BYTE2)†
18 WR2
17 XFER
16 DI4
15 DI5
14 DI6
13 DI7 (MSB)
12 IOUT2
11 IOUT1

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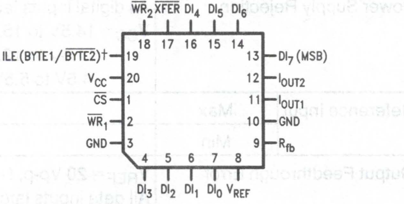
†This is necessary for the 12-bit DAC1230 series to permit interchanging from an 8-bit to a 12-bit DAC with **No PC board changes** and no software changes, See applications section.

Molded Chip Carrier Package


WR2 18
XFER 17
DI4 16
DI5 15
DI6 14
ILE (BYTE1/BYTE2)† 19
VCC 20
CS 1
WR1 2
GND 3
13 DI7 (MSB)
12 IOUT2
11 IOUT1
10 GND
9 Rfb
DI3 4
DI2 5
DI1 6
DI0 7
VREF 8

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$ (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
ESD Susceptability (Note 14)	800V
Lead Temperature (soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Conditions

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
Part numbers with 'LCN' suffix	0°C to +70°C
Part numbers with 'LCWM' suffix	0°C to +70°C
Part numbers with 'LCV' suffix	0°C to +70°C
Part numbers with 'LCJ' suffix	−40°C to +85°C
Part numbers with 'LJ' suffix	−55°C to +125°C
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics $V_{REF} = 10.000\ V_{DC}$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	$V_{CC} = 4.75\ V_{DC}$ $V_{CC} = 15.75\ V_{DC}$		$V_{CC} = 5\ V_{DC} \pm 5\%$ $V_{CC} = 12\ V_{DC} \pm 5\%$ to $15\ V_{DC} \pm 5\%$	Limit Units
			Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER CHARACTERISTICS						
Resolution			8	8	**8**	bits
Linearity Error Max	Zero and full scale adjusted $-10V \le V_{REF} \le +10V$	4, 8				
DAC0830LJ & LCJ				**0.05**	**0.05**	% FSR
DAC0832LJ & LCJ				**0.2**	**0.2**	% FSR
DAC0830LCN, LCWM & LCV				0.05	**0.05**	% FSR
DAC0831LCN				0.1	**0.1**	% FSR
DAC0832LCN, LCWM & LCV				0.2	**0.2**	% FSR
Differential Nonlinearity Max	Zero and full scale adjusted $-10V \le V_{REF} \le +10V$	4, 8				
DAC0830LJ & LCJ				**0.1**	**0.1**	% FSR
DAC0832LJ & LCJ				**0.4**	**0.4**	% FSR
DAC0830LCN, LCWM & LCV				0.1	**0.1**	% FSR
DAC0831LCN				0.2	**0.2**	% FSR
DAC0832LCN, LCWM & LCV				0.4	**0.4**	% FSR
Monotonicity	$-10V \le V_{REF} \le +10V$ LJ & LCJ	4		**8**	**8**	bits
	LCN, LCWM & LCV			8	**8**	bits
Gain Error Max	Using Internal R_{fb} $-10V \le V_{REF} \le +10V$	7	±0.2	±1	**±1**	% FS
Gain Error Tempco Max	Using internal R_{fb}		**0.0002**		**0.0006**	% FS/°C
Power Supply Rejection	All digital inputs latched high $V_{CC} = 14.5V$ to $15.5V$ 11.5V to 12.5V 4.5V to 5.5V		 0.0002 0.0006 0.013	 0.0025 0.015		% FSR/V
Reference Input Max			**15**	**20**	**20**	kΩ
Reference Input Min			**15**	**10**	**10**	kΩ
Output Feedthrough Error	$V_{REF} = 20$ Vp-p, f = 100 kHz All data inputs latched low		3			mVp-p

Electrical Characteristics

V_{REF} = 10.000 V_{DC} unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits T_A = 25°C. (Continued)

Parameter		Conditions		See Note	V_{CC} = 4.75 V_{DC} V_{CC} = 15.75 V_{DC}		V_{CC} = 5 V_{DC} ±5% V_{CC} = 12 V_{DC} ±5% to 15 V_{DC} ±5%	Limit Units
					Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER CHARACTERISTICS (Continued)								
Output Leakage Current Max	I_{OUT1}	All data inputs latched low	LJ & LCJ	10		**100**	**100**	nA
			LCN, LCWM & LCV			50	**100**	
	I_{OUT2}	All data inputs latched high	LJ & LCJ			**100**	**100**	nA
			LCN, LCWM & LCV			50	**100**	
Output Capacitance	I_{OUT1}	All data inputs latched low			45			pF
	I_{OUT2}				115			
	I_{OUT1}	All data inputs latched high			130			pF
	I_{OUT2}				30			
DIGITAL AND DC CHARACTERISTICS								
Digital Input Voltages	Max	Logic Low	LJ 4.75V			**0.6**		V_{DC}
			LJ 15.75V			**0.8**		
			LCJ 4.75V			**0.7**		
			LCJ 15.75V			**0.8**		
			LCN, LCWM, LCV			0.95	**0.8**	
	Min	Logic High	LJ & LCJ			**2.0**	**2.0**	V_{DC}
			LCN, LCWM, LCV			1.9	**2.0**	
Digital Input Currents	Max	Digital inputs <0.8V	LJ & LCJ		−50	**−200**	**−200**	μA
			LCN, LCWM, LCV			−160	**−200**	μA
		Digital inputs >2.0V	LJ & LCJ		0.1	**+10**	**+10**	μA
			LCN, LCWM, LCV			+8	**+10**	μA
Supply Current Drain	Max		LJ & LCJ		1.2	**3.5**	**3.5**	mA
			LCN, LCWM, LCV			1.7	**2.0**	

Electrical Characteristics $V_{REF} = 10.000\ V_{DC}$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits $T_A = 25°C$. (Continued)

Symbol	Parameter	Conditions	See Note	$V_{CC} = 15.75\ V_{DC}$		$V_{CC} = 12\ V_{DC} \pm 5\%$ to $15\ V_{DC} \pm 5\%$	$V_{CC} = 4.75\ V_{DC}$		$V_{CC} = 5\ V_{DC} \pm 5\%$	Limit Units
				Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
AC CHARACTERISTICS										
t_S	Current Setting Time	$V_{IL} = 0V$, $V_{IH} = 5V$		1.0			1.0			µs
t_W	Write and XFER Pulse Width Min	$V_{IL} = 0V$, $V_{IH} = 5V$	11 9	100	250 **320**	**320**	375	600 **900**	**900**	ns
t_{DS}	Data Setup Time Min	$V_{IL} = 0V$, $V_{IH} = 5V$	9	100	250 **320**	**320**	375	600 **900**	**900**	
t_{DH}	Data Hold Time Min	$V_{IL} = 0V$, $V_{IH} = 5V$	9		30 **30**			50 **50**		
t_{CS}	Control Setup Time Min	$V_{IL} = 0V$, $V_{IH} = 5V$	9	110	250 **320**	**320**	600	900 **1100**	**1100**	
t_{CH}	Control Hold Time Min	$V_{IL} = 0V$, $V_{IH} = 5V$	9	0	0 **0**	**10**	0	0 **0**		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$ (plastic) or 150°C (ceramic), and the typical junction-to-ambient thermal resistance of the J package when board mounted is 80°C/W. For the N package, this number increases to 100°C/W and for the V package this number is 120°C/W.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm 1\ V_{DC}$.

Note 8: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC0830 is "0.05% of FSR (MAX)". This guarantees that after performing a zero and full scale adjustment (see Sections 2.5 and 2.6), the plot of the 256 analog voltage outputs will each be within $0.05\% \times V_{REF}$ of a straight line which passes through zero and full scale.

Note 9: Boldface tested limits apply to the LJ and LCJ suffix parts only.

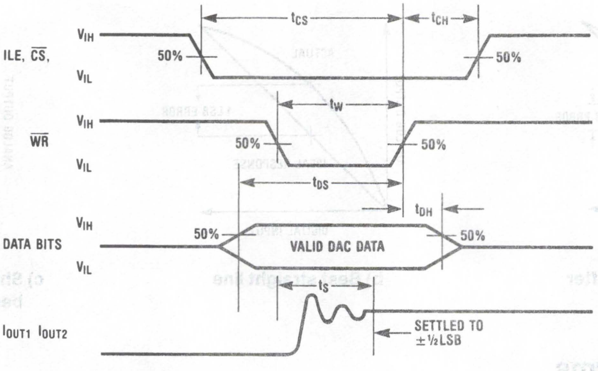
Note 10: A 100nA leakage current with $R_{fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(100 \times 10^{-9} \times 20 \times 10^3) \times 100/10$ which is 0.02% of FS.

Note 11: The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 12: Typicals are at 25°C and represent most likely parametric norm.

Note 13: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Switching Waveform



TL/H/5608-2

Definition of Package Pinouts

Control Signals (All control signals level actuated)

$\overline{\text{CS}}$: **Chip Select** (active low). The $\overline{\text{CS}}$ in combination with ILE will enable $\overline{\text{WR}}_1$.

ILE: **Input Latch Enable** (active high). The ILE in combination with $\overline{\text{CS}}$ enables $\overline{\text{WR}}_1$.

$\overline{\text{WR}}_1$: **Write 1.** The active low $\overline{\text{WR}}_1$ is used to load the digital input data bits (DI) into the input latch. The data in the input latch is latched when $\overline{\text{WR}}_1$ is high. To update the input latch—$\overline{\text{CS}}$ and $\overline{\text{WR}}_1$ must be low while ILE is high.

$\overline{\text{WR}}_2$: **Write 2** (active low). This signal, in combination with $\overline{\text{XFER}}$, causes the 8-bit data which is available in the input latch to transfer to the DAC register.

$\overline{\text{XFER}}$: **Transfer control signal** (active low). The $\overline{\text{XFER}}$ will enable $\overline{\text{WR}}_2$.

Other Pin Functions

DI_0-DI_7: **Digital Inputs.** DI_0 is the least significant bit (LSB) and DI_7 is the most significant bit (MSB).

I_{OUT1}: **DAC Current Output 1.** I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in DAC register.

I_{OUT2}: **DAC Current Output 2.** I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1}+I_{OUT2}=$ constant (I full scale for a fixed reference voltage).

R_{fb}: **Feedback Resistor.** The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: **Reference Voltage Input.** This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of +10 to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: **Digital Supply Voltage.** This is the power supply pin for the part. V_{CC} can be from +5 to +15V_{DC}. Operation is optimum for +15V_{DC}.

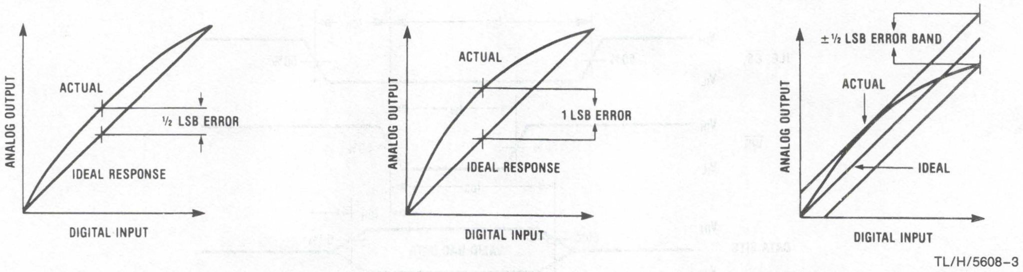
GND: The pin 10 voltage must be at the same ground potential as I_{OUT1} and I_{OUT2} for current switching applications. Any difference of potential (V_{OS} pin 10) will result in a linearity change of

$$\frac{V_{OS}\text{ pin 10}}{3V_{REF}}$$

For example, if V_{REF} = 10V and pin 10 is 9mV offset from I_{OUT1} and I_{OUT2} the linearity change will be 0.03%.

Pin 3 can be offset ±100mV with no linearity change, but the logic input threshold will shift.

Linearity Error



a) End point test after zero and fs adj.

b) Best straight line

c) Shifting fs adj. to pass best straight line test

Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC0830 has 2^8 or 256 steps and therefore has 8-bit resolution.

Linearity Error: Linearity Error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic*. It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity "end point test" (a) and the "best straight line" test (b,c) used by other suppliers are illustrated above. The "end point test" greatly simplifies the adjustment procedure by eliminating the need for multiple iterations of checking the linearity and then adjusting full scale until the linearity is met. The "end point test" guarantees that linearity is met after a single full scale adjust. (One adjustment vs. multiple iterations of the adjustment.) The "end point test" uses a standard zero and F.S. adjustment procedure and is a much more stringent test for DAC linearity.

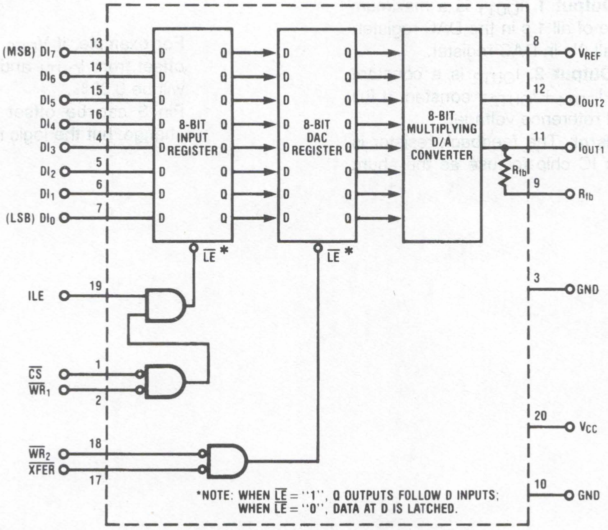
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within ±½LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC0830 series, full-scale is $V_{REF} - 1LSB$. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 39mV = 9.961V$. Full-scale error is adjustable to zero.

Differential Nonlinearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential nonlinearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. An 8-bit DAC which is monotonic to 8 bits simply means that increasing digital input codes will produce an increasing analog output.

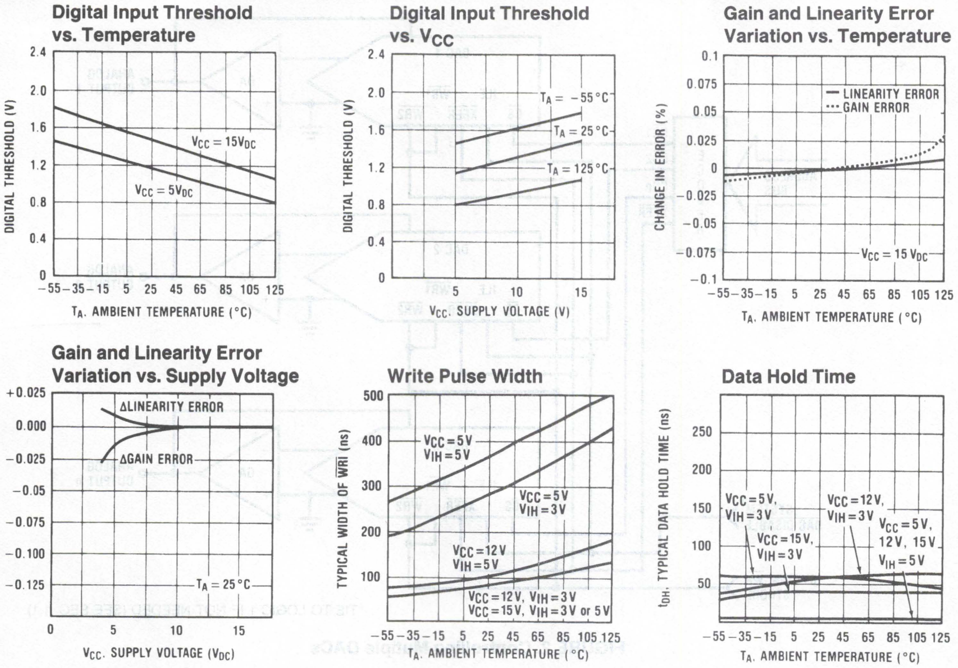


*NOTE: WHEN $\overline{LE}$ = "1", Q OUTPUTS FOLLOW D INPUTS;
WHEN $\overline{LE}$ = "0", DATA AT D IS LATCHED.

TL/H/5608–4

FIGURE 1. DAC0830 Functional Diagram

Typical Performance Characteristics



TL/H/5608–5

DAC0830 Series Application Hints

These DAC's are the industry's first microprocessor compatible, double-buffered 8-bit multiplying D to A converters. Double-buffering allows the utmost application flexibility from a digital control point of view. This 20-pin device is also pin for pin compatible (with one exception) with the DAC1230, a 12-bit MICRO-DAC. In the event that a system's analog output resolution and accuracy must be upgraded, substituting the DAC1230 can be easily accomplished. By tying address bit A_0 to the ILE pin, a two-byte μP write instruction (double precision) which automatically increments the address for the second byte write (starting with A_0 = "1") can be used. This allows either an 8-bit or the 12-bit part to be used with no hardware or software changes. For the simplest 8-bit application, this pin should be tied to V_{CC} (also see other uses in section 1.1).

Analog signal control versatility is provided by a precision R-2R ladder network which allows full 4-quadrant multiplication of a wide range bipolar reference voltage by an applied digital word.

1.0 DIGITAL CONSIDERATIONS

A most unique characteristic of these DAC's is that the 8-bit digital input byte is double-buffered. This means that the data must transfer through two independently controlled 8-bit latching registers before being applied to the R-2R ladder network to change the analog output. The addition of a second register allows two useful control features. First, any DAC in a system can simultaneously hold the current DAC data in one register (DAC register) and the next data word in the second register (input register) to allow fast updating of the DAC output on demand. Second, and probably more important, double-buffering allows any number of DAC's in a system to be updated to their new analog output levels simultaneously via a common strobe signal.

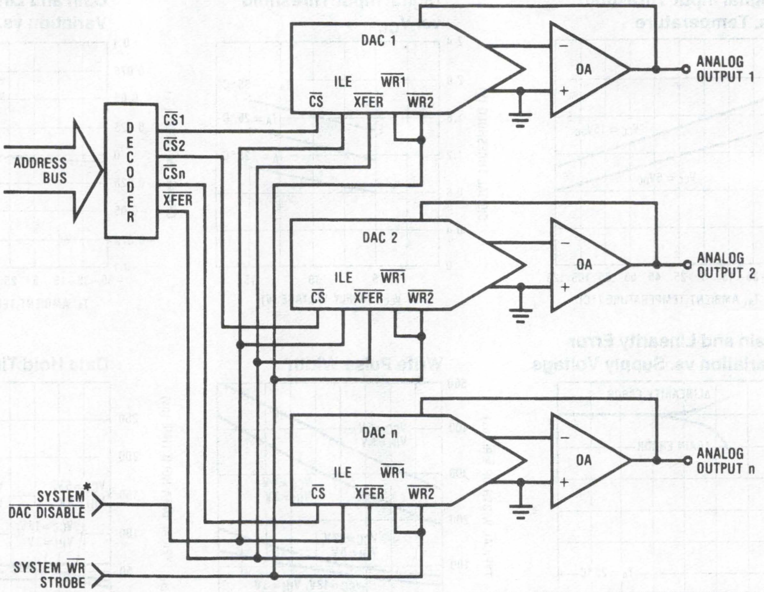
The timing requirements and logic level convention of the register control signals have been designed to minimize or eliminate external interfacing logic when applied to most popular microprocessors and development systems. It is easy to think of these converters as 8-bit "write-only" memory locations that provide an analog output quantity. All inputs to these DAC's meet TTL voltage level specs and can also be driven directly with high voltage CMOS logic in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. If any of the digital inputs are inadvertantly left floating, the DAC interprets the pin as a logic "1".

1.1 Double-Buffered Operation

Updating the analog output of these DAC's in a double-buffered manner is basically a two step or double write operation. In a microprocessor system two unique system addresses must be decoded, one for the input latch controlled by the $\overline{CS}$ pin and a second for the DAC latch which is controlled by the $\overline{XFER}$ line. If more than one DAC is being driven, *Figure 2*, the $\overline{CS}$ line of each DAC would typically be decoded individually, but all of the converters could share a common $\overline{XFER}$ address to allow simultaneous updating of any number of DAC's. The timing for this operation is shown, *Figure 3*.

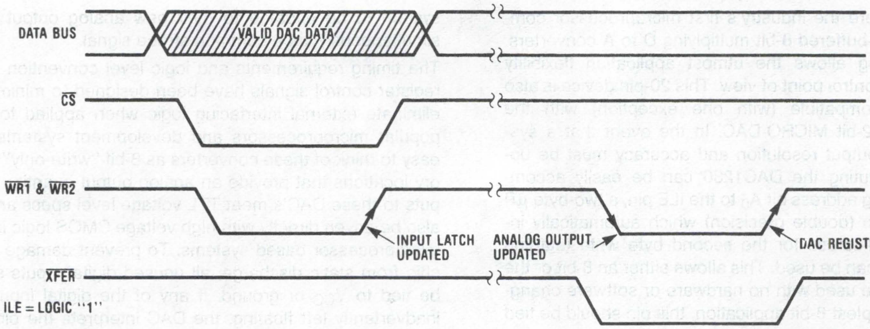
It is important to note that the analog outputs that will change after a simultaneous transfer are those from the DAC's whose input register had been modified prior to the $\overline{XFER}$ command.

DAC0830 Series Application Hints (Continued)


DAC 1
ILE
WR1
CS
XFER
WR2
OA
ANALOG OUTPUT 1
ADDRESS BUS
DECODER
CS1
CS2
CSn
XFER
DAC 2
ANALOG OUTPUT 2
DAC n
ANALOG OUTPUT n
SYSTEM* DAC DISABLE
SYSTEM WR STROBE

*TIE TO LOGIC 1 IF NOT NEEDED (SEE SEC. 1.1).

FIGURE 2. Controlling Mutiple DACs


DATA BUS
VALID DAC DATA
CS
WR1 & WR2
INPUT LATCH UPDATED
ANALOG OUTPUT UPDATED
DAC REGISTER LATCHED
XFER
ILE = LOGIC "1"

TL/H/5608–6

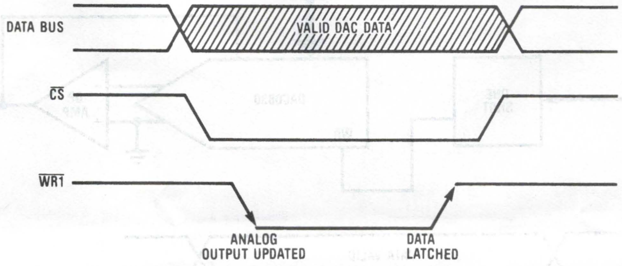
FIGURE 3

The ILE pin is an active high chip select which can be decoded from the address bus as a qualifier for the normal $\overline{CS}$ signal generated during a write operation. This can be used to provide a higher degree of decoding unique control signals for a particular DAC, and thereby create a more efficient addressing scheme.

Another useful application of the ILE pin of each DAC in a multiple DAC system is to tie these inputs together and use this as a control line that can effectively "freeze" the outputs of all the DAC's at their present value. Pulling this line low latches the input register and prevents new data from being written to the DAC. This can be particularly useful in multiprocessing systems to allow a processor other than the one controlling the DAC's to take over control of the data bus and control lines. If this second system were to use the same addresses as those decoded for DAC control (but for a different purpose) the ILE function would prevent the DAC's from being erroneously altered.

In a "Stand-Alone" system the control signals are generated by discrete logic. In this case double-buffering can be controlled by simply taking $\overline{CS}$ and $\overline{XFER}$ to a logic "0", ILE to a logic "1" and pulling $\overline{WR_1}$ low to load data to the input latch. Pulling $\overline{WR_2}$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.

DAC0830 Series Application Hints (Continued)



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ILE = LOGIC "1"; $\overline{\text{WR2}}$ and $\overline{\text{XFER}}$ GROUNDED

FIGURE 4

1.2 Single-Buffered Operation

In a microprocessor controlled system where maximum data throughput to the DAC is of primary concern, or when only one DAC of several needs to be updated at a time, a single-buffered configuration can be used. One of the two internal registers allows the data to flow through and the other register will serve as the data latch.

Digital signal feedthrough (see Section 1.5) is minimized if the input register is used as the data latch. Timing for this mode is shown in *Figure 4*.

Single-buffering in a "stand-alone" system is achieved by strobing $\overline{\text{WR}}_1$ low to update the DAC with $\overline{\text{CS}}$, $\overline{\text{WR}}_2$ and $\overline{\text{XFER}}$ grounded and ILE tied high.

1.3 Flow-Through Operation

Though primarily designed to provide microprocessor interface compatibility, the MICRO-DAC's can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in applications where the DAC is used in a continuous feedback control loop and is driven by a binary up-down counter, or in function generation circuits where a ROM is continuously providing DAC data.

Simply grounding $\overline{\text{CS}}$, $\overline{\text{WR}}_1$, $\overline{\text{WR}}_2$, and $\overline{\text{XFER}}$ and tying ILE high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.4 Control Signal Timing

When interfacing these MICRO-DAC to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{\text{WR}}$ strobe pulse width which is specified as 900 ns for all valid operating conditions of supply voltage and ambient temperature, but typically a pulse width of only 180ns is adequate if $V_{CC} = 15V_{DC}$. A second consideration is that the guaranteed minimum data hold time of 50ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{\text{CS}}$) $\overline{\text{WR}}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{\text{WR}}$ pulse-width. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{\text{WR}}$ pin of the DAC. This is illustrated in *Figure 5* for an exemplary system which provides a 250ns $\overline{\text{WR}}$ strobe time with a data hold time of less than 10ns.

The proper data set-up time prior to the latching edge (LO to HI transition) of the $\overline{\text{WR}}$ strobe, is insured if the $\overline{\text{WR}}$ pulse-width is within spec and the data is valid on the bus for the duration of the DAC $\overline{\text{WR}}$ strobe.

1.5 Digital Signal Feedthrough

When data is latched in the internal registers, but the digital inputs are changing state, a narrow spike of current may flow out of the current output terminals. This spike is caused by the rapid switching of internal logic gates that are responding to the input changes.

There are several recommendations to minimize this effect. When latching data in the DAC, always use the input register as the latch. Second, reducing the V_{CC} supply for the DAC from +15V to +5V offers a factor of 5 improvement in the magnitude of the feedthrough, but at the expense of internal logic switching speed. Finally, increasing C_C (*Figure 8*) to a value consistent with the actual circuit bandwidth requirements can provide a substantial damping effect on any output spikes.

DAC0830 Series Application Hints (Continued)

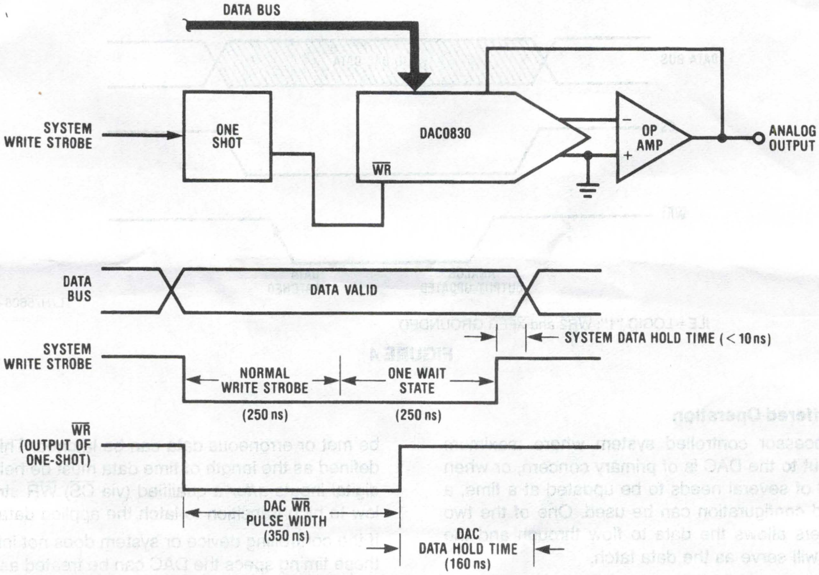

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FIGURE 5. Accommodating a High Speed System

2.0 ANALOG CONSIDERATIONS

The fundamental purpose of any D to A converter is to provide an accurate analog output quantity which is representative of the applied digital word. In the case of the DAC0830, the output, I_{OUT1}, is a current directly proportional to the product of the applied reference voltage and the digital input word. For application versatility, a second output, I_{OUT2}, is provided as a current directly proportional to the complement of the digital input. Basically:

$$I_{OUT1} = \frac{V_{REF}}{15\ k\Omega} \times \frac{\text{Digital Input}}{256};$$

$$I_{OUT2} = \frac{V_{REF}}{15\ k\Omega} \times \frac{255 - \text{Digital Input}}{256}$$

where the digital input is the decimal (base 10) equivalent of the applied 8-bit binary word (0 to 255), V_{REF} is the voltage at pin 8 and 15 kΩ is the nominal value of the internal resistance, R, of the R-2R ladder network (discussed in Section 2.1).

Several factors external to the DAC itself must be considered to maintain analog accuracy and are covered in subsequent sections.

2.1 The Current Switching R-2R Ladder

The analog circuitry, *Figure 6*, consists of a silicon-chromium (SiCr or Si-chrome) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there are no parasitic diode problems with the ladder (as there may be with diffused resistors) so the reference voltage, V_{REF}, can range −10V to +10V even if V_{CC} for the device is $5V_{DC}$.

The digital input code to the DAC simply controls the position of the SPDT current switches and steers the available ladder current to either I_{OUT1} or I_{OUT2} as determined by the logic input level ("1" or "0") respectively, as shown in *Figure 6*. The MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

2.2 Basic Unipolar Output Voltage

To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential ($0V_{DC}$) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in *Figure 7*.

The inverting input of the op amp is a "virtual ground" created by the feedback from its output through the internal 15 kΩ resistor, R_{fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage source or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than or equal to the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry.

Always use the internal R_{fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

DAC0830 Series Application Hints (Continued)

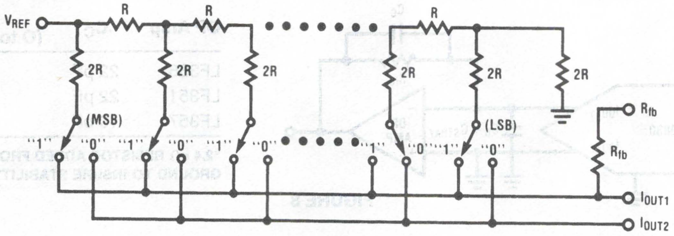


FIGURE 6

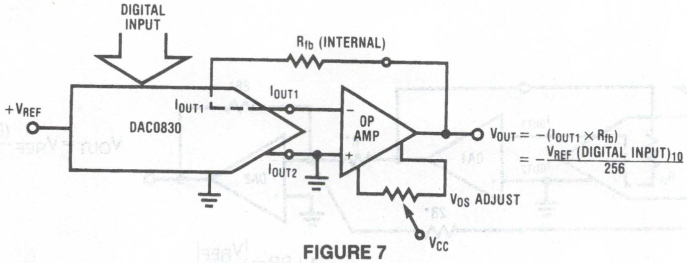


FIGURE 7

TL/H/5608-9

2.3 Op Amp Considerations

The op amp used in *Figure 7* should have offset voltage nulling capability (See Section 2.5).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET op amps are highly recommended for use with these DACs because of their very low input current.

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in *Figure 8*, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

Finally, the output voltage swing of the amplifier must be greater than V_{REF} to allow reaching the full scale output voltage. Depending on the loading on the output of the amplifier and the available op amp supply voltages (only ±12 volts in many development systems), a reference voltage less than 10 volts may be necessary to obtain the full analog output voltage range.

2.4 Bipolar Output Voltage with a Fixed Reference

The addition of a second op amp to the previous circuitry can be used to generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word and allows two-quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication: $\pm V_{REF} \times \pm \text{Digital Code} = \pm V_{OUT}$. This circuit is shown in *Figure 9*.

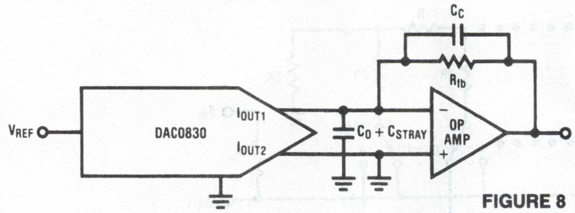
This configuration features several improvements over existing circuits for bipolar outputs with other multiplying DACs. Only the offset voltage of amplifier 1 has to be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp (although a constant output voltage error) has no effect on linearity. It should be nulled only if absolute output accuracy is required. Finally, the values of the resistors around the second amplifier do not have to match the internal DAC resistors, they need only to match and temperature track each other. A thin film 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. These resistors are matched to 0.1% and exhibit only 5 ppm/°C resistance tracking temperature coefficient. Two of the four available 10 kΩ resistors can be paralleled to form R in *Figure 9* and the other two can be used independently as the resistances labeled 2R.

2.5 Zero Adjustment

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near $0V_{DC}$ as possible. This is accomplished for the typical DAC — op amp connection (*Figure 7*) by shorting out R_{fb}, the amplifier feedback resistor, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all one's for I_{OUT2}). The short around R_{fb} is then removed and the converter is zero adjusted.

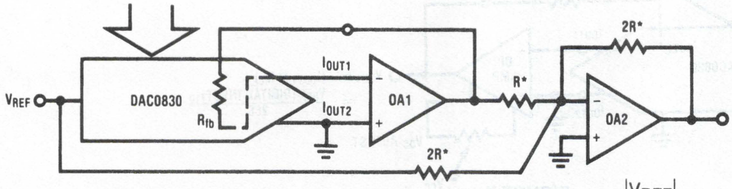
DAC0830 Series Application Hints (Continued)



OP Amp	C_C	t_s (O to Full Scale)
LF356	22 pF	4 µs
LF351	22 pF	5 µs
LF357*	10 pF	2 µs

***2.4 kΩ RESISTOR ADDED FROM − INPUT TO GROUND TO INSURE STABILITY**

FIGURE 8



$$V_{OUT} = V_{REF}\,\frac{(\text{DIGITAL CODE} - 128)}{128}$$

$$1\ \text{LSB} = \frac{|V_{REF}|}{128}$$

***THESE RESISTORS ARE AVAILABLE FROM BECKMAN INSTRUMENTS, INC. AS THEIR PART NO. 694-3-R10K-D**

TL/H/5608-10

Input Code	IDEAL V_{OUT}	
MSB ……….LSB	$+V_{REF}$	$-V_{REF}$
1 1 1 1 1 1 1 1	$V_{REF} - 1$ LSB	$-\|V_{REF}\| + 1$ LSB
1 1 0 0 0 0 0 0	$V_{REF}/2$	$-\|V_{REF}\|/2$
1 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1	-1 LSB	$+1$ LSB
0 0 1 1 1 1 1 1	$-\frac{\|V_{REF}\|}{2} - 1$ LSB	$\frac{\|V_{REF}\|}{2} + 1$ LSB
0 0 0 0 0 0 0 0	$-\|V_{REF}\|$	$+\|V_{REF}\|$

FIGURE 9

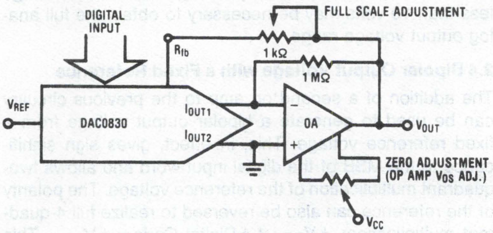
2.6 Full-Scale Adjustment

In the case where the matching of R_{fb} to the R value of the R-2R ladder (typically ±0.2%) is insufficient for full-scale accuracy in a particular application, the V_{REF} voltage can be adjusted or an external resistor and potentiometer can be added as shown in *Figure 10* to provide a full-scale adjustment.

The temperature coefficients of the resistors used for this adjustment are an important concern. To prevent degradation of the gain error temperature coefficient by the external resistors, their temperature coefficients ideally would have to match that of the internal DAC resistors, which is a highly impractical constraint. For the values shown in *Figure 10*, if the resistor and the potentiometer each had a temperature coefficient of ±100 ppm/°C maximum, the overall gain error temperature coefficent would be degraded a maximum of 0.0025%/°C for an adjustment pot setting of less than 3% of R_{fb}.

2.7 Using the DAC0830 in a Voltage Switching Configuration

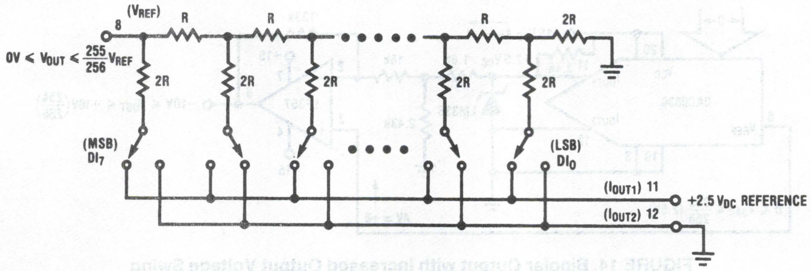
The R-2R ladder can also be operated as a voltage switching network. In this mode the ladder is used in an inverted manner from the standard current switching configuration. The reference voltage is connected to one of the current output terminals (I_{OUT1} for true binary digital control, I_{OUT2} is for complementary binary) and the output voltage is taken from the normal V_{REF} pin. The converter output is now a voltage in the range from 0V to 255/256 V_{REF} as a function of the applied digital code as shown in *Figure 11*.



TL/H/5608-11

FIGURE 10. Adding Full-Scale Adjustment

DAC0830 Series Application Hints (Continued)

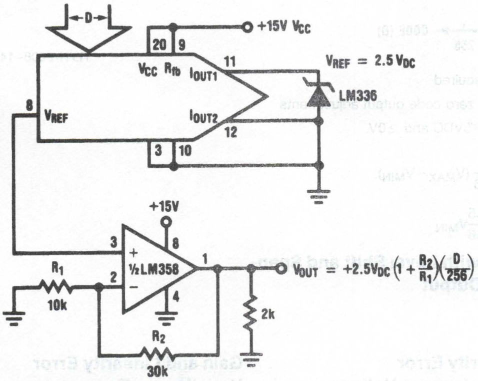

(VREF)
8
R
R
R
2R
0V ≤ VOUT ≤ 255/256 VREF
2R
2R
2R
2R
2R
(MSB)
DI7
(LSB)
DI0
(IOUT1) 11
+2.5 VDC REFERENCE
(IOUT2) 12

TL/H/5608–12

FIGURE 11. Voltage Mode Switching

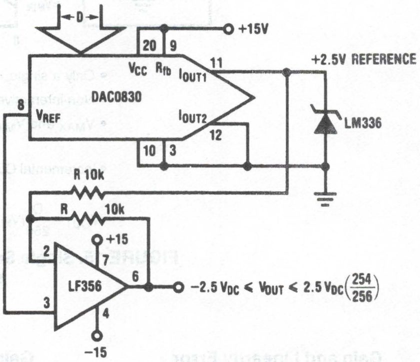
This configuration offers several useful application advantages. Since the output is a voltage, an external op amp is not necessarily required but the output impedance of the DAC is fairly high (equal to the specified reference input resistance of 10 kΩ to 20 kΩ) so an op amp may be used for buffering purposes. Some of the advantages of this mode are illustrated in *Figures 12, 13, 14* and *15*.

There are two important things to keep in mind when using this DAC in the voltage switching mode. The applied reference voltage must be positive since there are internal parasitic diodes from ground to the I_{OUT1} and I_{OUT2} terminals which would turn on if the applied reference went negative. There is also a dependence of conversion linearity and gain error on the voltage difference between V_{CC} and the voltage applied to the normal current output terminals. This is a result of the voltage drive requirements of the ladder switches. To ensure that all 8 switches turn on sufficiently (so as not to add significant resistance to any leg of the ladder and thereby introduce additional linearity and gain errors) it is recommended that the applied reference voltage be kept less than $+5V_{DC}$ and V_{CC} be at least 9V more positive than V_{REF}. These restrictions ensure less than 0.1% linearity and gain error change. *Figures 16, 17* and *18* characterize the effects of bringing V_{REF} and V_{CC} closer together as well as typical temperature performance of this voltage switching configuration.


D
+15V VCC
20
9
VCC
Rfb
IOUT1
11
VREF = 2.5 VDC
LM336
8
VREF
IOUT2
12
3
10
+15V
3
8
1/2LM358
1
VOUT = +2.5VDC (1 + R2/R1)(D/256)
R1
10k
2
4
2k
R2
30k

- Voltage switching mode eliminates output signal inversion and therefore a need for a negative power supply.
- Zero code output voltage is limited by the low level output saturation voltage of the op amp. The 2 kΩ pull-down resistor helps to reduce this voltage.
- V_{OS} of the op amp has no effect on DAC linearity.

FIGURE 12. Single Supply DAC


D
+15V
20
9
VCC
Rfb
IOUT1
11
+2.5V REFERENCE
DAC0830
8
VREF
IOUT2
12
LM336
10
3
R 10k
R
10k
+15
2
7
LF356
6
−2.5 VDC ≤ VOUT ≤ 2.5 VDC (254/256)
3
4
−15

TL/H/5608–13

- $V_{OUT} = 2.5V \left(\frac{D}{128} - 1\right)$
- Slewing and settling time for a full scale output change is ≈ 1.8 µs

FIGURE 13. Obtaining a Bipolar Output from a Fixed Reference with a Single Op Amp

DAC0830 Series Application Hints (Continued)

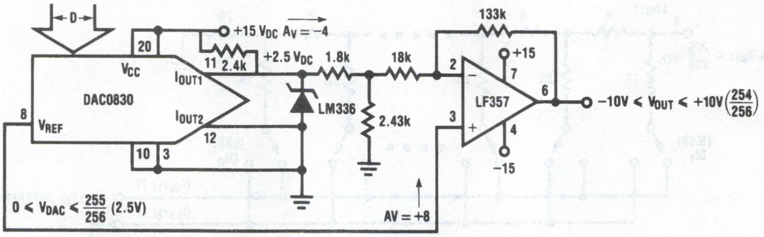
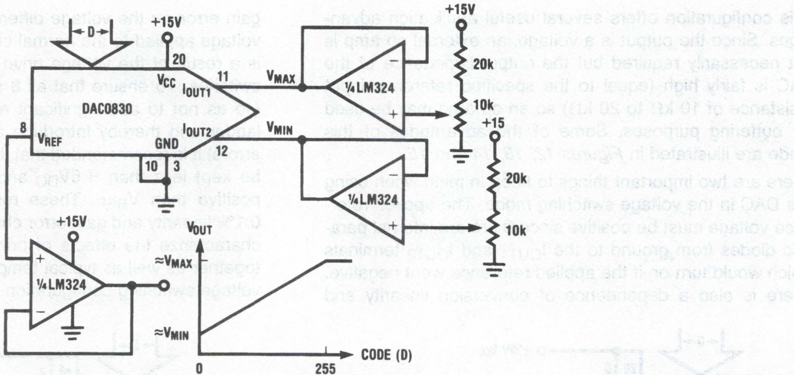

D
20
V_{CC}
DAC0830
I_{OUT1}
I_{OUT2}
8
V_{REF}
10
3
+15 V_{DC}
$A_V = -4$
11
2.4k
+2.5 V_{DC}
1.8k
LM336
12
18k
2.43k
133k
2
3
+15
7
LF357
6
4
−15
$-10V \leq V_{OUT} \leq +10V\left(\frac{254}{256}\right)$
$0 < V_{DAC} < \frac{255}{256}$ (2.5V)
AV = +8

FIGURE 14. Bipolar Output with Increased Output Voltage Swing


+15V
20
11
V_{CC}
I_{OUT1}
DAC0830
8
V_{REF}
I_{OUT2}
GND
12
10
3
V_{MAX}
V_{MIN}
+15V
¼LM324
20k
10k
+15
20k
¼LM324
10k
+15V
¼LM324
V_{OUT}
$\approx V_{MAX}$
$\approx V_{MIN}$
0
255
CODE (D)
TL/H/5608–14

- Only a single +15V supply required
- Non-interactive full-scale and zero code output adjustments
- V_{MAX} and V_{MIN} must be $\leq +5VDC$ and $\geq 0V$.
- Incremental Output Step $= \frac{1}{256}(V_{MAX} - V_{MIN})$.
- $V_{OUT} = \frac{D}{256}(V_{MAX} - V_{MIN}) + \frac{255}{256}V_{MIN}$

FIGURE 15. Single Supply DAC with Level Shift and Span-Adjustable Output

Gain and Linearity Error Variation vs. Supply Voltage

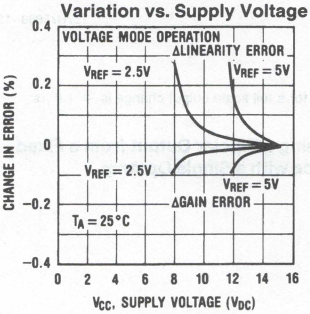


FIGURE 16

Gain and Linearity Error Variation vs. Reference Voltage

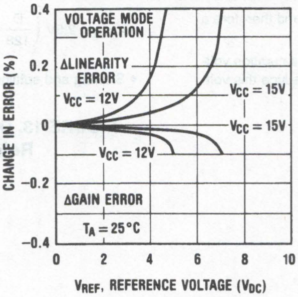
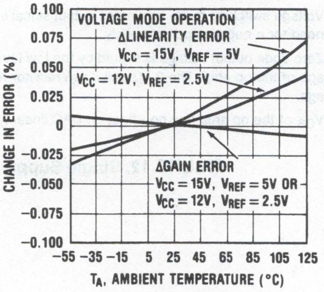


FIGURE 17

Note: For these curves, V_{REF} is the voltage applied to pin 11 (I_{OUT1}) with pin 12 (I_{OUT2}) grounded.

Gain and Linearity Error Variation vs. Temperature



TL/H/5608–15

FIGURE 18

DAC0830 Series Application Hints (Continued)

2.8 Miscellaneous Application Hints

These converters are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to static discharge.

Conversion accuracy is only as good as the applied reference voltage so providing a stable source over time and temperature changes is an important factor to consider.

A "good" ground is most desirable. A single point ground distribution technique for analog signals and supply returns keeps other devices in a system from affecting the output of the DACs.

During power-up supply voltage sequencing, the −15V (or −12V) supply of the op amp may appear first. This will cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is internally clamped to one diode drop below ground.

Careful circuit construction with minimization of lead lengths around the analog circuitry, is a primary concern. Good high frequency supply decoupling will aid in preventing inadvertant noise from appearing on the analog output.

Overall noise reduction and reference stability is of particular concern when using the higher accuracy versions, the DAC0830 and DAC0831, or their advantages are wasted.

3.0 GENERAL APPLICATION IDEAS

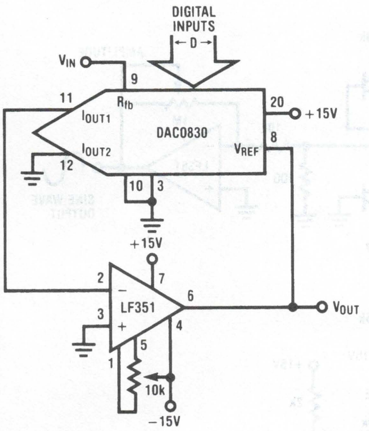
The connections for the control pins of the digital input registers are purposely omitted. Any of the control formats discussed in Section 1 of the accompanying text will work with any of the circuits shown. The method used depends on the overall system provisions and requirements.

The digital input code is referred to as D and represents the decimal equivalent value of the 8-bit binary input, for example:

Binary Input								
Pin 13 MSB							**Pin 7 LSB**	**D Decimal Equivalent**
1	1	1	1	1	1	1	1	255
1	0	0	0	0	0	0	0	128
0	0	0	1	0	0	0	0	16
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0

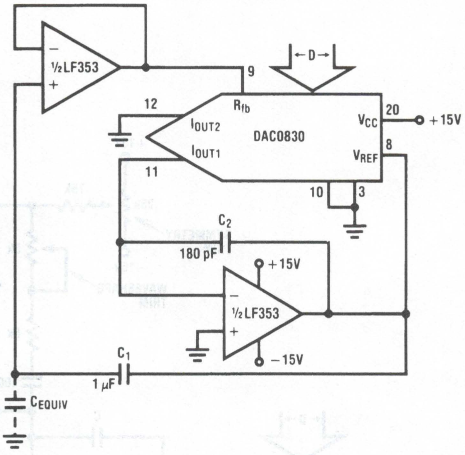
Applications

DAC Controlled Amplifier (Volume Control)



- $V_{OUT} = \frac{-V_{IN}(256)}{D}$
- When D=0, the amplifier will go open loop and the output will saturate.
- Feedback impedance from the −input to the output varies from 15 kΩ to ∞ as the input code changes from full-scale to zero.

Capacitance Multiplier

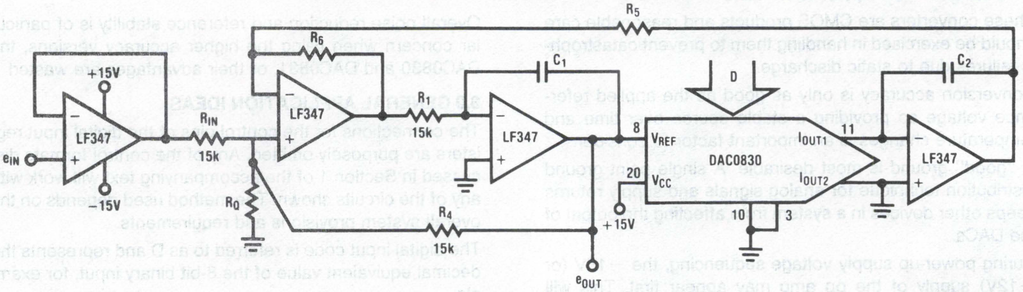


TL/H/5608-16

- $C_{EQUIV} = C_1\left(1+\frac{256}{D}\right)$
- Maximum voltage across the equivalent capacitance is limited to $\frac{V_{O\,MAX}\,(\text{op amp})}{1+\frac{256}{D}}$
- C_2 is used to improve settling time of op amp.

Applications (Continued)

Variable f_O, Variable Q_O, Constant BW Bandpass Filter



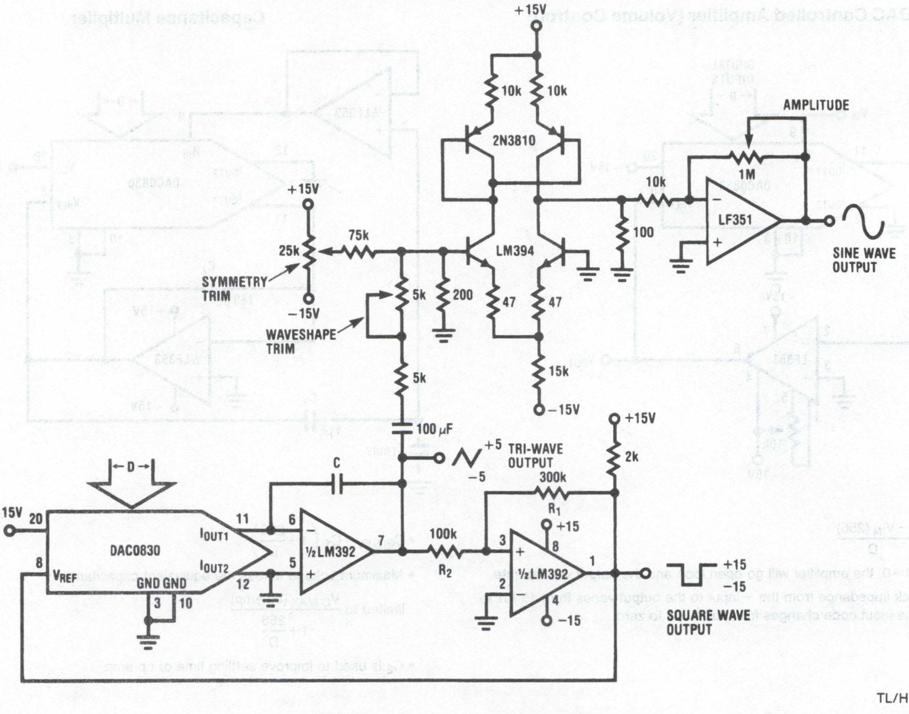
R5
R6
C1
C2
+15V
D
−
LF347
+
R1
15k
RIN
15k
eIN
−15V
RQ
R4
15k
8
VREF
DAC0830
20
VCC
+15V
11
IOUT1
IOUT2
10
3
LF347
eOUT

TL/H/5608–17

- $f_O = \dfrac{\sqrt{\dfrac{KD}{256}}}{2\pi R_1 C}$; $Q_O = \sqrt{\dfrac{KD}{256}}\,\dfrac{(2R_Q + R_1)}{R_Q(K + 1)}$; $3dbBW = \dfrac{R_Q(K + 1)}{2\pi R_1 C(2R_Q + R_1)}$

  where $C_1 = C_2 = C$; $K = \dfrac{R_6}{R_5}$ and R_1 = R of DAC = 15k
- $H_O = 1$ for $R_{IN} = R_4 = R_1$
- Range of f_O and Q is ≈ 16 to 1 for circuit shown. The range can be extended to 255 to 1 by replacing R_1 with a second DAC0830 driven by the same digital input word.
- Maximum $f_O \times Q$ product should be ≤200 kHz.

DAC Controlled Function Generator



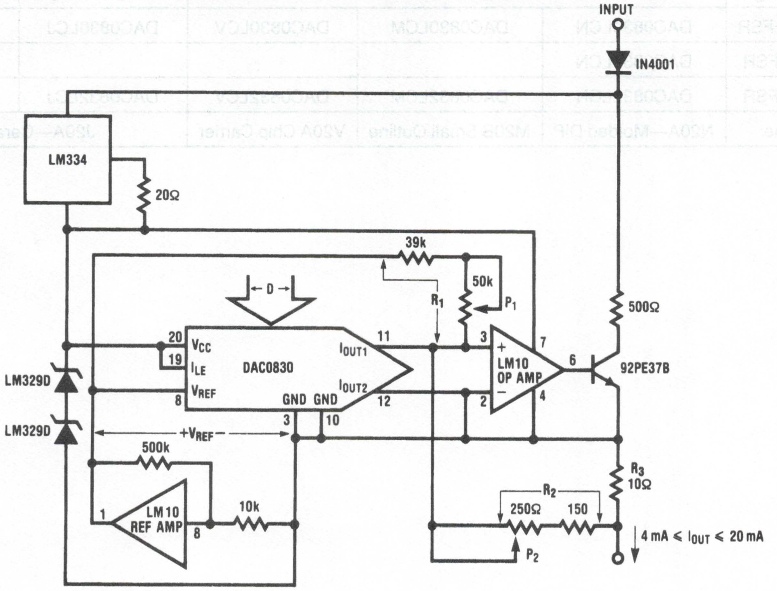
+15V
10k
10k
2N3810
AMPLITUDE
1M
10k
100
−
LF351
+
SINE WAVE OUTPUT
+15V
25k
75k
SYMMETRY TRIM
−15V
LM394
5k
200
47
47
WAVESHAPE TRIM
5k
15k
−15V
100 µF
+5
−5
TRI-WAVE OUTPUT
+15V
2k
300k
R1
C
D
+15V
20
DAC0830
8
VREF
11
IOUT1
IOUT2
12
GND GND
3
10
6
5
½LM392
7
100k
R2
3
8
+15
2
½LM392
1
−15
+15
−15
SQUARE WAVE OUTPUT

TL/H/5608–18

- DAC controls the frequency of sine, square, and triangle outputs.
- $f = \dfrac{D}{256(20k)C}$ for $V_{OMAX} = V_{OMIN}$ of square wave output and $R_1 = 3\,R_2$.
- 255 to 1 linear frequency range; oscillator stops with D = 0
- Trim symmetry and wave-shape for minimum sine wave distortion.

Applications (Continued)

Two Terminal Floating 4 to 20 mA Current Loop Controller

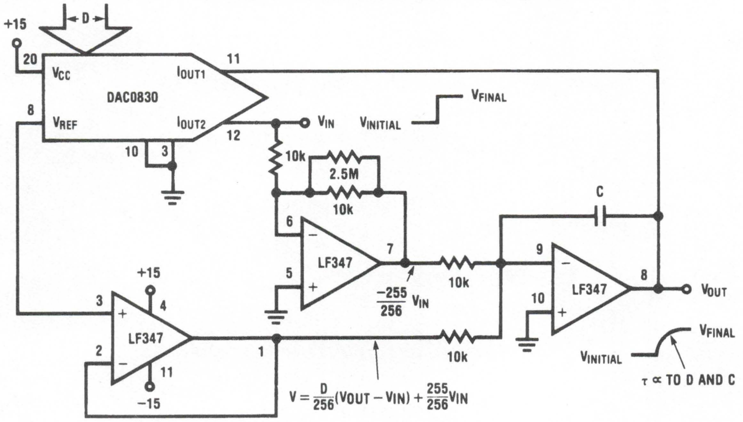

INPUT
IN4001
LM334
20Ω
39k
50k
R1
P1
← D →
500Ω
20
19
8
VCC
ILE
VREF
DAC0830
IOUT1
IOUT2
GND GND
3
10
11
12
3
7
6
2
4
LM10
OP AMP
92PE37B
LM329D
LM329D
+VREF
500k
1
LM10
REF AMP
8
10k
R3
10Ω
R2
250Ω
150
P2
4 mA ≤ IOUT ≤ 20 mA

TL/H/5608-19

$$I_{OUT} = V_{REF}\left[\frac{1}{R_1} + \frac{D}{256\,R_{fb}}\right]\left[1 + \frac{R_2}{R_3}\right]$$

- DAC0830 linearly controls the current flow from the input terminal to the output terminal to be 4 mA (for D=0) to 19.94 mA (for D=255).
- Circuit operates with a terminal voltage differential of 16V to 55V.
- P_2 adjusts the magnitude of the output current and P_1 adjusts the zero to full scale range of output current.
- Digital inputs can be supplied from a processor using opto isolators on each input or the DAC latches can flow-through (connect control lines to pins 3 and 10 of the DAC) and the input data can be set by SPST toggle switches to ground (pins 3 and 10).

DAC Controlled Exponential Time Response


+15
← D →
20
VCC
DAC0830
IOUT1
11
8
VREF
IOUT2
12
10
3
VIN
VINITIAL
VFINAL
10k
2.5M
10k
C
6
5
LF347
7
−255/256 VIN
10k
9
10
LF347
8
VOUT
+15
3
4
LF347
2
11
−15
1
10k
V = D/256(VOUT − VIN) + 255/256 VIN
VFINAL
VINITIAL
τ ∝ TO D AND C

TL/H/5608-20

- Output responds exponentially to input changes and automatically stops when $V_{OUT} = V_{IN}$
- Output time constant is directly proportional to the DAC input code and capacitor C
- Input voltage must be positive (See section 2.7)

Ordering Information

Temperature Range		0°C to +70°			−40°C to +85°C	−55°C to +125°C
Non Linearity	0.05% FSR	DAC0830LCN	DAC0830LCM	DAC0830LCV	DAC0830LCJ	DAC0830LJ
	0.1% FSR	DAC0831LCN				
	0.2% FSR	DAC0832LCN	DAC0832LCM	DAC0832LCV	DAC0832LCJ	DAC0832LJ
Package Outline		N20A—Molded DIP	M20B Small Outline	V20A Chip Carrier	J20A—Ceramic DIP	

National Semiconductor Corporation

DAC1000, DAC1001, DAC1002, DAC1006, DAC1007, DAC1008 μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1000/1/2 and DAC1006/7/8 are advanced CMOS/Si-Cr 10-, 9- and 8-bit accurate multiplying DACs which are designed to interface directly with the 8080, 8048, 8085, Z-80 and other popular microprocessors. These DACs appear as a memory location or an I/O port to the μP and no interfacing logic is needed.

These devices, combined with an external amplifier and voltage reference, can be used as standard D/A converters; and they are very attractive for multiplying applications (such as digitally controlled gain blocks) since their linearity error is essentially independent of the voltage reference. They become equally attractive in audio signal processing equipment as audio gain controls or as programmable attenuators which marry high quality audio signal processing to digitally based systems under microprocessor control.

All of these DACs are double buffered. They can load all 10 bits or two 8-bit bytes and the data format can be either right justified or left justified. The analog section of these DACs is essentially the same as that of the DAC1020.

The DAC1000 series are the 10-bit members of a family of microprocessor-compatible DAC's (MICRO-DAC™'s). For applications requiring other resolutions, the DAC0830 series (8 bits) and the DAC1208 and DAC1230 (12 bits) are available alternatives.

Part #	Accuracy (bits)	Pin	Description
DAC1000	10	24	Has all logic features
DAC1001	9		
DAC1002	8		
DAC1006	10	20	For left-justified data
DAC1007	9		
DAC1008	8		

Features

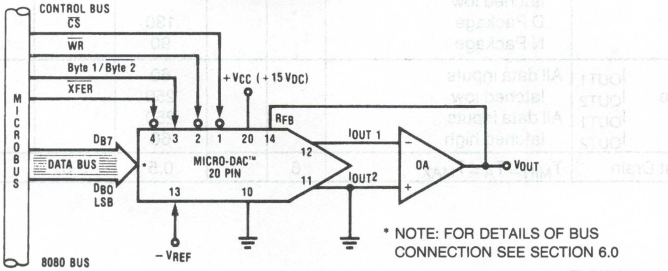
- Uses easy to adjust END POINT specs, NOT BEST STRAIGHT LINE FIT
- Low power consumption
- Direct interface to all popular microprocessors.
- Integrated thin film on CMOS structure
- Double-buffered, single-buffered or flow through digital data inputs.
- Loads two 8-bit bytes or a single 10-bit word.
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold).
- Works with ±10V reference—full 4-quadrant multiplication.
- Operates STAND ALONE (without μP) if desired.
- Available in 0.3″ standard 20-pin and 0.6″ 24-pin package.
- Differential non-linearity selection available as special order.

Key Specifications

■ Output Current Settling Time	500 ns
■ Resolution	10 bits
■ Linearity	10, 9, and 8 bits (guaranteed over temp.)
■ Gain Tempco	−0.0003% of FS/°C
■ Low Power Dissipation (including ladder)	20 mW
■ Single Power Supply	5 to 15 V_{DC}

Typical Application

DAC1006/1007/1008



* NOTE: FOR DETAILS OF BUS CONNECTION SEE SECTION 6.0

TL/H/5688-1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$ (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
ESD Susceptibility (Note 11)	800V
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
Part numbers with 'LCN' suffix	0°C to 70°C
Part numbers with 'LCJ' suffix	−40°C to +85°C
Part numbers with 'LJ' suffix	−55°C to +125°C
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

Tested at $V_{CC} = 4.75\ V_{DC}$ and $15.75\ V_{DC}$, $T_A = 25°C$, $V_{REF} = 10.000\ V_{DC}$ unless otherwise noted

Parameter	Conditions	See Note	$V_{CC} = 12V_{DC} \pm 5\%$ to $15V_{DC} \pm 5\%$			$V_{CC} = 5V_{DC} \pm 5\%$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Resolution					10			10	bits
Linearity Error	Endpoint adjust only	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC1000 and 1006				0.05			0.05	% of FSR
	DAC1001 and 1007				0.1			0.1	% of FSR
	DAC1002 and 1008				0.2			0.2	% of FSR
Differential Nonlinearity	Endpoint adjust only	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC1000 and 1006				0.1			0.1	% of FSR
	DAC1001 and 1007				0.2			0.2	% of FSR
	DAC1002 and 1008				0.4			0.4	% of FSR
Monotonicity	$T_{MIN} < T_A < T_{MAX}$	4,6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC1000 and 1006		10			10			bits
	DAC1001 and 1007		9			9			bits
	DAC1002 and 1008		8			8			bits
Gain Error	Using internal R_{fb} $-10V \le V_{REF} \le +10V$	5	−1.0	±0.3	1.0	−1.0	±0.3	1.0	% of FS
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$ Using internal R_{fb}	6 9		−0.0003	−0.001		−0.0006	−0.002	% of FS/°C
Power Supply Rejection	All digital inputs latched high								
	$V_{CC} = 14.5V$ to $15.5V$			0.003	0.008				% FSR/V
	11.5V to 12.5V			0.004	0.010				% FSR/V
	4.75V to 5.25V						0.033	0.10	% FSR/V
Reference Input Resistance			10	15	20	10	15	20	kΩ
Output Feedthrough Error	$V_{REF} = 20V_{p\text{-}p}$, $f = 100$ kHz All data inputs latched low								
	D Package			130			130		$mV_{p\text{-}p}$
	N Package			90			90		$mV_{p\text{-}p}$
Output Capacitance I_{OUT1}	All data inputs latched low			60			60		pF
I_{OUT2}				250			250		pF
I_{OUT1}	All data inputs latched high			250			250		pF
I_{OUT2}				60			60		pF
Supply Current Drain	$T_{MIN} \le T_A \le T_{MAX}$	6		0.5	3.5		0.5	3.5	mA

Electrical Characteristics

Tested at V_{CC} = 4.75 V_{DC} and 15.75 V_{DC}, T_A = 25°C, V_{REF} = 10.000 V_{DC} unless otherwise noted (Continued)

Parameter	Conditions	See Note	$V_{CC}=12V_{DC}\pm5\%$ to $15V_{DC}\pm5\%$			$V_{CC}=5V_{DC}\pm5\%$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current I_{OUT1}	$T_{MIN}\leq T_A\leq T_{MAX}$ All data inputs latched low	6 10			200			200	nA
I_{OUT2}	All data inputs latched high				200			200	nA
Digital Input Voltages	$T_{MIN}\leq T_A\leq T_{MAX}$	6							
	Low level								
	LJ suffix				0.8			0.6	V_{DC}
	LCJ, LCN suffix				0.8, 0.8			0.7, 0.8	V_{DC}
	High level (all parts)		2.0			2.0			V_{DC}
Digital Input Currents	$T_{MIN}\leq T_A\leq T_{MAX}$	6							
	Digital inputs <0.8V			−40	−150		−40	−150	μA_{DC}
	Digital inputs >2.0V			1.0	+10		1.0	+10	μA_{DC}
Current Settling Time t_S	$V_{IL}=0V$, $V_{IH}=5V$			500			500		ns
Write and $\overline{XFER}$ Pulse Width t_W	$V_{IL}=0V$, $V_{IH}=5V$, $T_A=25°C$	8	150	60		320	200		ns
	$T_{MIN}\leq T_A\leq T_{MAX}$	9	320	100		500	250		ns
Data Set Up Time t_{DS}	$V_{IL}=0V$, $V_{IH}=5V$, $T_A=25°C$	9	150	80		320	170		ns
	$T_{MIN}\leq T_A\leq T_{MAX}$		320	120		500	250		ns
Data Hold Time t_{DH}	$V_{IL}=OV$, $V_{IH}=5V$ $T_A=25°C$	9	200	100		320	220		ns
	$T_{MIN}\leq T_A\leq T_{MAX}$		250	120		500	320		ns
Control Set Up Time t_{CS}	$V_{IL}=0V$, $V_{IL}=5V$, $T_A=25°C$	9	150	60		320	180		ns
	$T_{MIN}\leq T_A\leq T_{MAX}$		320	100		500	260		ns
Control Hold Time t_{CH}	$V_{IL}=0V$, $V_{IH}=5V$, $T_A=25°C$	9	10	0		10	0		ns
	$T_{MIN}\leq T_A\leq T_{MAX}$		10	0		10	0		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS}\div V_{REF}$. For example, if $V_{REF}=10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF}=\pm10$ V_{DC} and $V_{REF}=\pm1$ V_{DC}.

Note 6: $T_{MIN}=0°C$ and $T_{MAX}=70°C$ for "LCN" suffix parts.

$T_{MIN}=-40°C$ and $T_{MAX}=85°C$ for "LCJ" suffix parts.

$T_{MIN}=55°C$ and $T_{MAX}=125°C$ for "LJ" suffix parts.

Note 7: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC1000 is "0.05% of FSR (MAX)." This guarantees that after performing a zero and full scale adjustment (See Sections 2.5 and 2.6), the plot of the 1024 analog voltage outputs will each be within $0.05\%\times V_{REF}$ of a straight line which passes through zero and full scale.

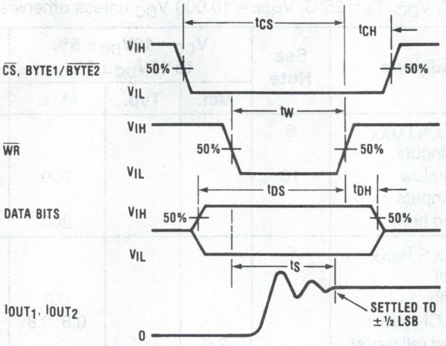
Note 8: This specification implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 9: Guaranteed by design but not tested.

Note 10: A 200 nA leakage current with $R_{fb}=20K$ and $V_{REF}=10V$ corresponds to a zero error of $(200\times10^{-9}\times20\times10^3)\times100\div10$ which is 0.04% of FS.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

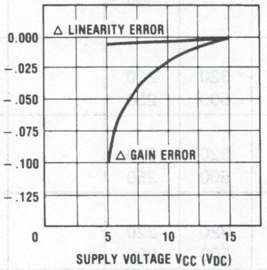
Switching Waveforms


CS, BYTE1/BYTE2
WR
DATA BITS
IOUT1, IOUT2
VIH
VIL
50%
tCS
tCH
tW
tDS
tDH
tS
FS
0
SETTLED TO ± ½ LSB

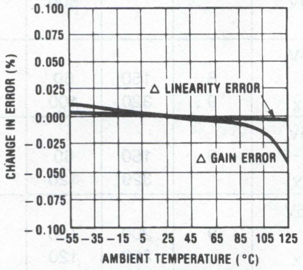
TL/H/5688-2

Typical Performance Characteristics

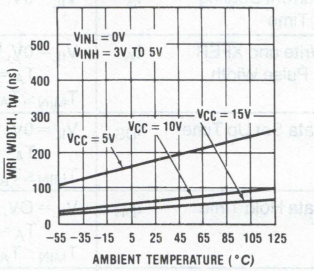
Errors vs. Supply Voltage



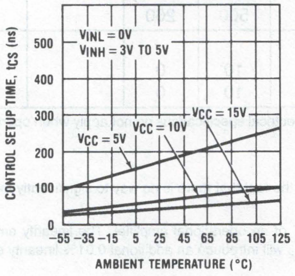
Errors vs. Temperature



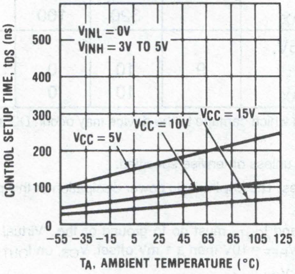
Write Width, t_W



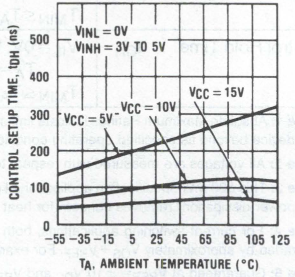
Control Setup Time, t_{CS}



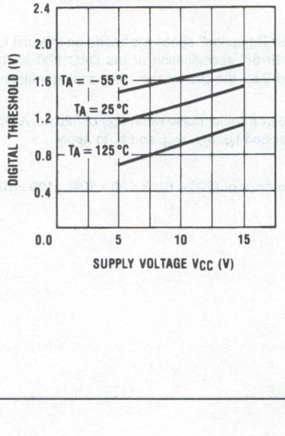
Data Setup Time, t_{DS}



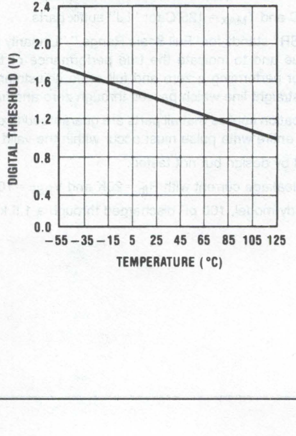
Data Hold Time, t_{DH}



Digital Threshold vs. Supply Voltage



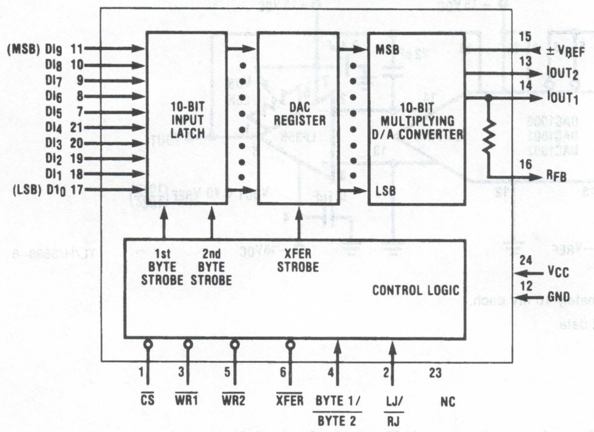
Digital Input Threshold vs. Temperature



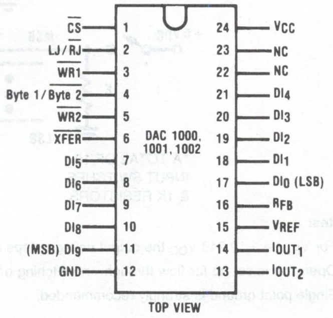
TL/H/5688-3

Block and Connection Diagrams

DAC1000/1001/1002 (24-Pin Parts)

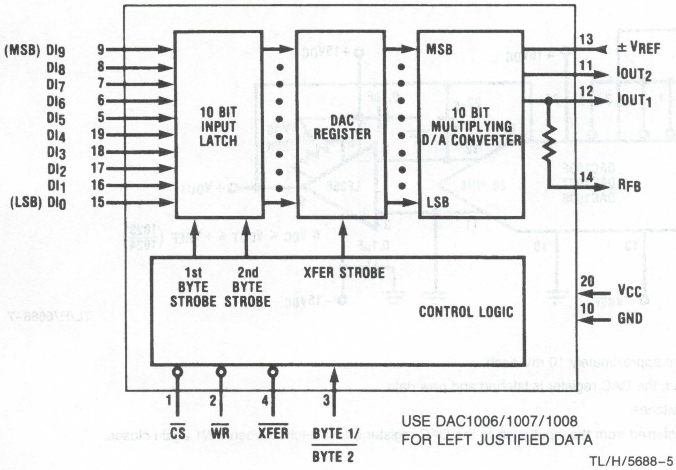

(MSB) DI9 11
DI8 10
DI7 9
DI6 8
DI5 7
DI4 21
DI3 20
DI2 19
DI1 18
(LSB) DI0 17
10-BIT INPUT LATCH
DAC REGISTER
MSB
LSB
10-BIT MULTIPLYING D/A CONVERTER
15 ±VREF
13 IOUT2
14 IOUT1
16 RFB
1st BYTE STROBE
2nd BYTE STROBE
XFER STROBE
CONTROL LOGIC
24 VCC
12 GND
1 CS
3 WR1
5 WR2
6 XFER
4 BYTE 1/BYTE 2
2 LJ/RJ
23 NC

DAC1000/1001/1002
(24-Pin Parts)
Dual-In-Line Package


CS 1
LJ/RJ 2
WR1 3
Byte 1/Byte 2 4
WR2 5
XFER 6
DI5 7
DI6 8
DI7 9
DI8 10
(MSB) DI9 11
GND 12
24 VCC
23 NC
22 NC
21 DI4
20 DI3
19 DI2
18 DI1
17 DI0 (LSB)
16 RFB
15 VREF
14 IOUT1
13 IOUT2
DAC 1000, 1001, 1002
TOP VIEW

TL/H/5688-4

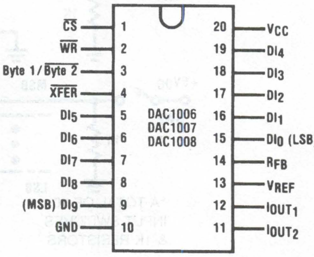
DAC1006/1007/1008 (20-Pin Parts)


(MSB) DI9 9
DI8 8
DI7 7
DI6 6
DI5 5
DI4 19
DI3 18
DI2 17
DI1 16
(LSB) DI0 15
10 BIT INPUT LATCH
DAC REGISTER
MSB
LSB
10 BIT MULTIPLYING D/A CONVERTER
13 ±VREF
11 IOUT2
12 IOUT1
14 RFB
1st BYTE STROBE
2nd BYTE STROBE
XFER STROBE
CONTROL LOGIC
20 VCC
10 GND
1 CS
2 WR
4 XFER
3 BYTE 1/BYTE 2

USE DAC1006/1007/1008 FOR LEFT JUSTIFIED DATA

TL/H/5688-5

DAC1006/1007/1008
(20-Pin Parts)
Dual-In-Line Package

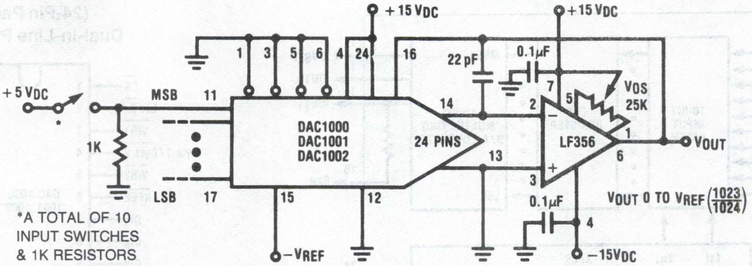

CS 1
WR 2
Byte 1/Byte 2 3
XFER 4
DI5 5
DI6 6
DI7 7
DI8 8
(MSB) DI9 9
GND 10
20 VCC
19 DI4
18 DI3
17 DI2
16 DI1
15 DI0 (LSB)
14 RFB
13 VREF
12 IOUT1
11 IOUT2
DAC1006 DAC1007 DAC1008

TL/H/5688-28

Top View

See Ordering Information

DAC1000/1001/1002—Simple Hookup for a "Quick Look"


+15 VDC
+15 VDC
1
3
5
6
4
24
16
22 pF
0.1μF
7
VOS
25K
+5 VDC
MSB
11
14
2
5
*
1K
DAC1000
DAC1001
DAC1002
24 PINS
LF356
1
VOUT
13
6
3
LSB
17
15
12
0.1μF
4
VOUT 0 TO VREF (1023/1024)
*A TOTAL OF 10
INPUT SWITCHES
& 1K RESISTORS
−VREF
−15VDC

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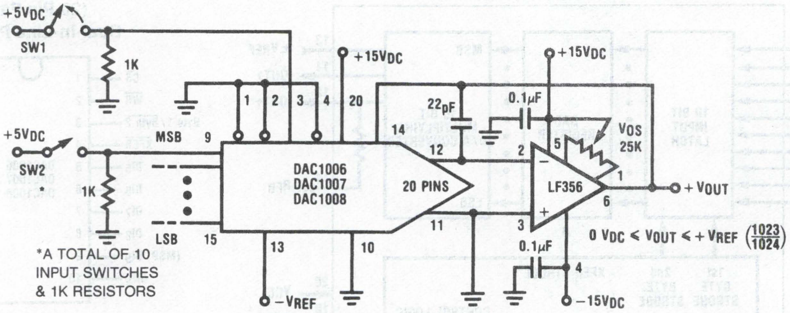
Notes:

1. For $V_{REF} = -10.240$ V_{DC} the output voltage steps are approximately 10 mV each.
2. Operation is set up for flow through—no latching of digital input data.
3. Single point ground is strongly recommended.

DAC1006/1007/1008—Simple Hookup for a "Quick Look"


+5VDC
SW1
1K
+15VDC
+15VDC
1
2
3
4
20
22pF
0.1μF
+5VDC
MSB
9
14
VOS
25K
SW2
12
2
5
*
1K
DAC1006
DAC1007
DAC1008
20 PINS
LF356
1
+VOUT
6
11
3
LSB
15
13
10
0 VDC ≤ VOUT ≤ +VREF (1023/1024)
0.1μF
4
*A TOTAL OF 10
INPUT SWITCHES
& 1K RESISTORS
−VREF
−15VDC

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Notes:

1. For $V_{REF} = -10.240$ V_{DC} the output voltage steps are approximately 10 mV each.
2. SW1 is a normally closed switch. While SW1 is closed, the DAC register is latched and new data can be loaded into the input latch via the 10 SW2 switches.

When SW1 is momentarily opened the new data is transferred from the input latch to the DAC register and is latched when SW1 again closes.

1.0 DEFINITION OF PACKAGE PINOUTS

1.1 Control Signals (All control signals are level actuated.)

$\overline{\text{CS}}$: Chip Select — active low, it will enable $\overline{\text{WR}}$ (DAC1003–1008) or WR_1 (DAC1000–1002).

$\overline{\text{WR}}$ or $\overline{\text{WR}_1}$: Write — The active low $\overline{\text{WR}}$ (or $\overline{\text{WR}_1}$ — DAC1000-1002) is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{\text{WR}}$ (or $\overline{\text{WR}_1}$) is high. The 10-bit input latch is split into two latches; one holds 8 bits and the other holds 2 bits. The Byte1/$\overline{\text{Byte2}}$ control pin is used to select both input latches when Byte1/$\overline{\text{Byte2}}$ = 1 or to overwrite the 2-bit input latch when in the low state.

$\overline{\text{WR}_2}$: Extra Write (DAC1000–1002) — The active low $\overline{\text{WR}_2}$ is used to load the data from the input latch to the DAC register while $\overline{\text{XFER}}$ is low. The data in the DAC register is latched when WR_2 is high.

Byte1/$\overline{\text{Byte2}}$: Byte Sequence Control — When this control is high, all ten locations of the input latch are enabled. When low, only two locations of the input latch are enabled and these two locations are overwritten on the second byte write. On the DAC1006, 1007, and 1008, the Byte1/$\overline{\text{Byte2}}$ must be low to transfer the 10-bit data in the input latch to the DAC register.

$\overline{\text{XFER}}$: Transfer Control Signal, active low — This signal, in combination with others, is used to transfer the 10-bit data which is available in the input latch to the DAC register — see timing diagrams.

LJ/$\overline{\text{RJ}}$: Left Justify/Right Justify (DAC1000–1002) — When LJ/$\overline{\text{RJ}}$ is high the part is set up for left justified (fractional) data format. (DAC1006–1008 have this done internally.) When LJ/$\overline{\text{RJ}}$ is low, the part is set up for right justified (integer) data.

1.2 Other Pin Functions

DI_i (i = 0 to 9): Digital Inputs — DI_0 is the least significant bit (LSB) and DI_9 is the most significant bit (MSB).

I_{OUT1}: DAC Current Output 1 — I_{OUT1} is a maximum for a digital input code of all 1s and is zero for a digital input code of all 0s.

I_{OUT2}: DAC Current Output 2 — I_{OUT2} is a constant minus I_{OUT1}, or

$$I_{OUT1} + I_{OUT2} = \frac{1023\ V_{REF}}{1024\ R}$$

where R ≅ 15 kΩ.

R_{FB}: Feedback Resistor — This is provided on the IC chip for use as the shunt feedback resistor when an external op amp is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) because it matches the resistors used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input — This is the connection for the external precision voltage source which drives the R-2R ladder. V_{REF} can range from −10 to +10 volts. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage — This is the power supply pin for the part. V_{CC} can be from +5 to +15 V_{DC}. Operation is optimum for +15V. The input threshold voltages are nearly independent of V_{CC}. (See Typical Performance Characteristics and Description in Section 3.0, T^2L compatible logic inputs.)

GND: Ground — the ground pin for the part.

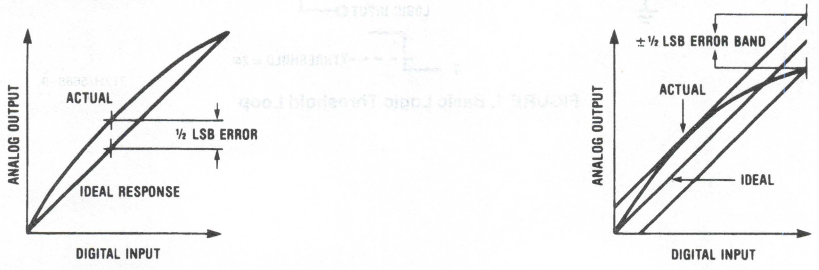
1.3 Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC1000 has 2^{10} or 1024 steps and therefore has 10-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the "best straight line" test (b) used by other suppliers are illustrated below. The "best straight line" requires a special zero and FS adjustment for each part, which is almost impossible for user to determine. The "end point test" uses a standard zero and FS adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output (which is the worst case).



a. End Point Test After Zero and FS Adj.

b. Best Straight Line

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Settling Time: Settling time is the time required from a code transition until the DAC output reaches within ±½ LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1000 series, full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = -10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 9.8mV = 9.9902V$. Full-scale error is adjustable to zero.

Monotonicity: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 10-bit DAC with 10-bit monotonicity will produce an increasing analog output when all 10 digital inputs are exercised. A 10-bit DAC with 9-bit monotonicity will be monotonic when only the most significant 9 bits are exercised. Similarly, 8-bit monotonicity is guaranteed when only the most significant 8 bits are exercised.

2.0 DOUBLE BUFFERING

These DACs are double-buffered, microprocessor compatible versions of the DAC1020 10-bit multiplying DAC. The addition of the buffers for the digital input data not only allows for storage of this data, but also provides a way to assemble the 10-bit input data word from two write cycles when using an 8-bit data bus. Thus, the next data update for the DAC output can be made with the complete new set of 10-bit data. Further, the double buffering allows many DACs in a system to store current data and also the next data. The updating of the new data for each DAC is also not time critical. When all DACs are updated, a common strobe signal can then be used to cause all DACs to switch to their new analog output levels.

3.0 TTL COMPATIBLE LOGIC INPUTS

To guarantee TTL voltage compatibility of the logic inputs, a novel bipolar (NPN) regulator circuit is used. This makes the input logic thresholds equal to the forward drop of two diodes (and also matches the temperature variation) as occurs naturally in TTL. The basic circuit is shown in *Figure 1*. A curve of digital input threshold as a function of power supply voltage is shown in the Typical Performance Characteristics section.

4.0 APPLICATION HINTS

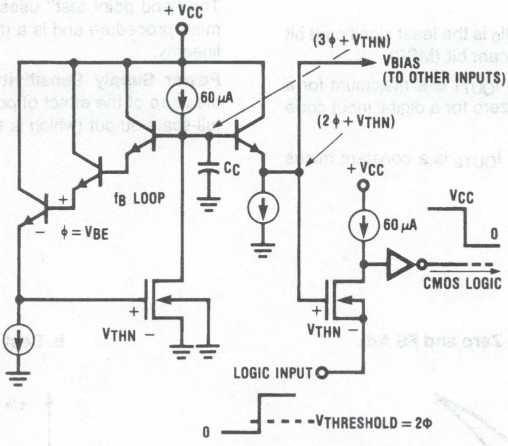
The DC stability of the V_{REF} source is the most important factor to maintain accuracy of the DAC over time and temperature changes. A good single point ground for the analog signals is next in importance.

These MICRO-DAC converters are CMOS products and reasonable care should be exercised in handling them prior to final mounting on a PC board. The digital inputs are protected, but permanent damage may occur if the part is subjected to high electrostatic fields. Store unused parts in conductive foam or anti-static rails.

4.1 Power Supply Sequencing & Decoupling

Some IC amplifiers draw excessive current from the Analog inputs to V− when the supplies are first turned on. To prevent damage to the DAC — an external Schottky diode connected from I_{OUT1} or I_{OUT2} to ground may be required to prevent destructive currents in I_{OUT1} or I_{OUT2}. If an LM741 or LF356 is used — these diodes are not required.

The standard power supply decoupling capacitors which are used for the op amp are adequate for the DAC.



TL/H/5688-9

FIGURE 1. Basic Logic Threshold Loop

4.2 Op Amp Bias Current & Input Leads

The op amp bias current (I_B) CAN CAUSE DC ERRORS. BI-FET™ op amps have very low bias current, and therefore the error introduced is negligible. BI-FET op amps are strongly recommended for these DACs.

The distance from the I_{OUT1} pin of the DAC to the inverting input of the op amp should be kept as short as possible to prevent inadvertent noise pickup.

5.0 ANALOG APPLICATIONS

The analog section of these DACs uses an R-2R ladder which can be operated both in the current switching mode and in the voltage switching mode.

The major product changes (compared with the DAC1020) have been made in the digital functioning of the DAC. The analog functioning is reviewed here for completeness. For additional analog applications, such as multipliers, attenuators, digitally controlled amplifiers and low frequency sine wave oscillators, refer to the DAC1020 data sheet. Some basic circuit ideas are presented in this section in addition to complete applications circuits.

5.1 Operation in Current Switching Mode

The analog circuitry, *Figure 2*, consists of a silicon-chromium (Si-Cr) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there is no parasitic diode connected to the V_{REF} pin as would exist if diffused resistors were used. The reference voltage input (V_{REF}) can therefore range from −10V to +10V.

The digital input code to the DAC simply controls the position of the SPDT current switches, SW0 to SW9. A logical 1 digital input causes the current switch to steer the available ladder current to the I_{OUT1} output pin. These MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

5.1.1 Providing a Unipolar Output Voltage with the DAC in the Current Switching Mode

A voltage output is provided by making use of an external op amp as a current-to-voltage converter. The idea is to use the internal feedback resistor, R_{FB}, from the output of the op amp to the inverting (−) input. Now, when current is entered at this inverting input, the feedback action of the op amp keeps that input at ground potential. This causes the applied input current to be diverted to the feedback resistor. The output voltage of the op amp is forced to a voltage given by:

$$V_{OUT} = -(I_{OUT1} \times R_{FB})$$

Notice that the sign of the output voltage depends on the direction of current flow through the feedback resistor.

In current switching mode applications, both current output pins (I_{OUT1} and I_{OUT2}) should be operated at 0 V_{DC}. This is accomplished as shown in *Figure 3*. The capacitor, C_C, is used to compensate for the output capacitance of the DAC and the input capacitance of the op amp. The required feedback resistor, R_{FB}, is available on the chip (one end is internally tied to I_{OUT1}) and must be used since an external resistor will not provide the needed matching and temperature tracking. This circuit can therefore be simplified as

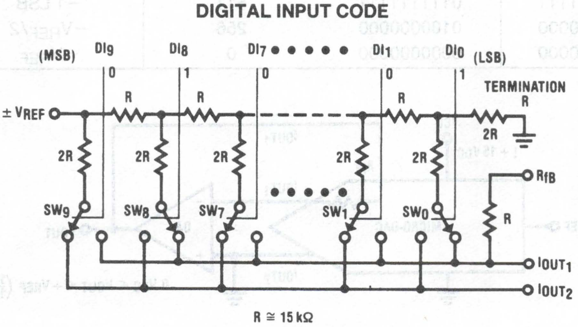


FIGURE 2. Current Mode Switching

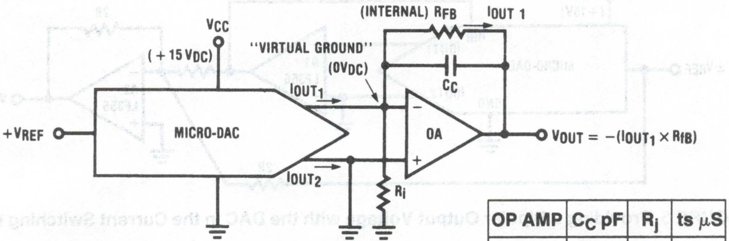


FIGURE 3. Converting I_{OUT} to V_{OUT}

OP AMP	C_C pF	R_i	ts μS
LF356	22	∞	3
LF351	24	∞	4
LF357	10	2.4k	1.5

shown in *Figure 4*, where the sign of the reference voltage has been changed to provide a positive output voltage. Note that the output current, I_{OUT1}, now flows through the R_{FB} pin.

5.1.2 Providing a Bipolar Output Voltage with the DAC in the Current Switching Mode

The addition of a second op amp to the circuit of *Figure 4* can be used to generate a bipolar output voltage from a fixed reference voltage *Figure 5*. This, in effect, gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize the full four-quadrant multiplication.

The applied digital word is offset binary which includes a code to output zero volts without the need of a large valued resistor common to existing bipolar multiplying DAC circuits. Offset binary code can be derived from 2's complement data (most common for signed processor arithmetic) by inverting the state of the MSB in either software or hardware. After doing this the output then responds in accordance to the following expression:

$$V_O = V_{REF} \times \frac{D}{512}$$

where V_{REF} can be positive or negative and D is the signed decimal equivalent of the 2's complement processor data. ($-512 \leq D \leq +511$ or $1000000000 \leq D \leq 0111111111$). If the applied digital input is interpreted as the decimal equivalent of a true binary word, V_{OUT} can be found by:

$$V_O = V_{REF}\left(\frac{D-512}{512}\right) \qquad 0 \leq D \leq 1023$$

With this configuration, only the offset voltage of amplifier 1 need be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp has no effect on linearity. It presents a constant output voltage error and should be nulled only if absolute accuracy is needed. Another advantage of this configuration is that the values of the external resistors required do not have to match the value of the internal DAC resistors; they need only to match and temperature track each other.

A thin film 4 resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. Two of the four available 10 kΩ resistor can be paralleled to form R in *Figure 5* and the other two can be used separately as the resistors labeled 2R.

Operation is summarized in the table below:

2's Comp. (Decimal)	2's Comp. (Binary)	Applied Digital Input	Applied True Binary (Decimal)	V_{OUT}	
				$+V_{REF}$	$-V_{REF}$
+511	0111111111	1111111111	1023	$V_{REF} - 1$ LSB	$-\lvert V_{REF}\rvert + 1$ LSB
+256	0100000000	1100000000	768	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
0	0000000000	1000000000	512	0	0
−1	1111111111	0111111111	511	−1 LSB	+1 LSB
−256	1100000000	0100000000	256	$-V_{REF}/2$	$+\lvert V_{REF}\rvert/2$
−512	1000000000	0000000000	0	$-V_{REF}$	$+\lvert V_{REF}\rvert$

with: $1\ \text{LSB} = \frac{\lvert V_{REF}\rvert}{512}$

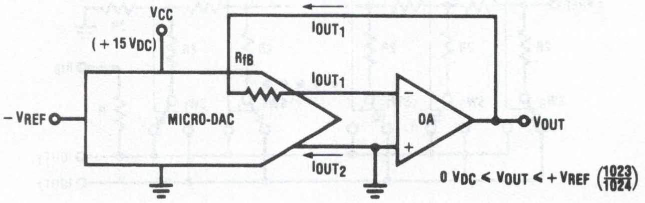


FIGURE 4. Providing a Unipolar Output Voltage

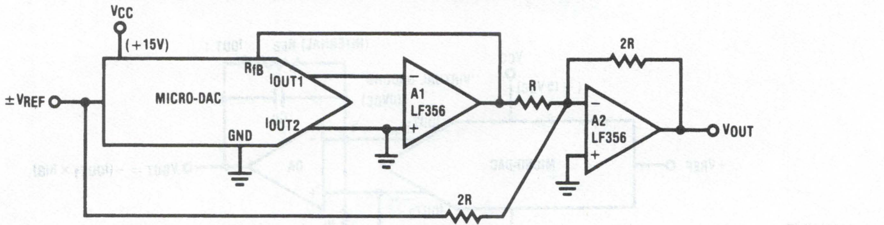


FIGURE 5. Providing a Bipolar Output Voltage with the DAC in the Current Switching Mode

5.2 Analog Operation in the Voltage Switching Mode

Some useful application circuits result if the R-2R ladder is operated in the voltage switching mode. There are two very important things to remember when using the DAC in the voltage mode. The reference voltage (+V) must always be positive since there are parasitic diodes to ground on the I_{OUT1} pin which would turn on if the reference voltage went negative. To maintain a degradation of linearity less than ±0.005%, keep $+V \leq 3\ V_{DC}$ and V_{CC} at least 10V more positive than +V. *Figures 6* and *7* show these errors for the voltage switching mode. This operation appears unusual, since a reference voltage (+V) is applied to the I_{OUT1} pin and the voltage output is the V_{REF} pin. This basic idea is shown in *Figure 8*.

This V_{OUT} range can be scaled by use of a non-inverting gain stage as shown in *Figure 9*.

Notice that this is unipolar operation since all voltages are positive. A bipolar output voltage can be obtained by using a single op amp as shown in *Figure 10*. For a digital input code of all zeros, the output voltage from the V_{REF} pin is zero volts. The external op amp now has a single input of +V and is operating with a gain of −1 to this input. The output of the op amp therefore will be at −V for a digital input of all zeros. As the digital code increases, the output voltage at the V_{REF} pin increases.

Notice that the gain of the op amp to voltages which are applied to the (+) input is +2 and the gain to voltages which are applied to the input resistor, R, is −1. The output voltage of the op amp depends on both of these inputs and is given by:

$$V_{OUT} = (+V)(-1) + V_{REF}(+2)$$

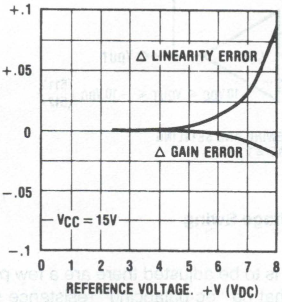


FIGURE 6

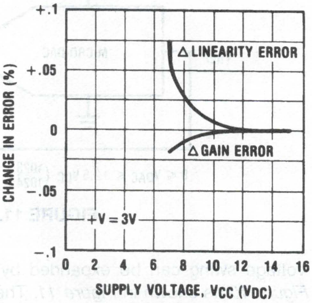


FIGURE 7

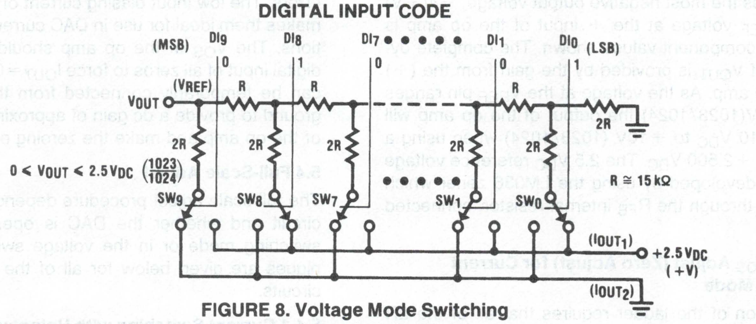

DIGITAL INPUT CODE
(MSB)
DI9
DI8
DI7
DI1
DI0
(LSB)
0
1
0
1
0
1
(VREF)
VOUT
R
R
R
2R
2R
2R
2R
2R
2R
0 < VOUT < 2.5VDC (1023/1024)
R ≅ 15 kΩ
SW9
SW8
SW7
SW1
SW0
(IOUT1)
+2.5VDC
(+V)
(IOUT2)

FIGURE 8. Voltage Mode Switching

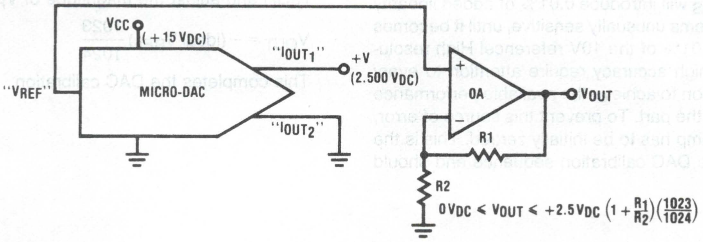

VCC
(+15 VDC)
"IOUT1"
+V
(2.500 VDC)
"VREF"
MICRO-DAC
"IOUT2"
+
−
OA
VOUT
R1
R2
0 VDC ≤ VOUT ≤ +2.5VDC (1 + R1/R2)(1023/1024)

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FIGURE 9. Amplifying the Voltage Mode Output (Single Supply Operation)

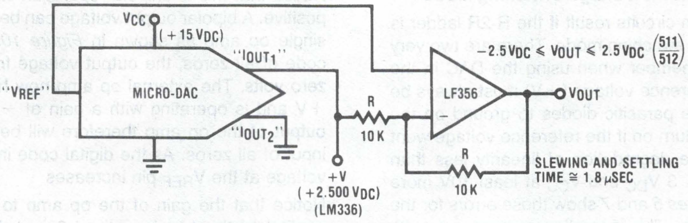
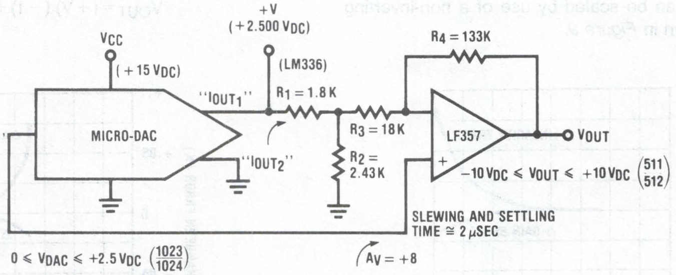


FIGURE 10. Providing a Bipolar Output Voltage with a Single Op Amp



TL/H/5688–13

FIGURE 11. Increasing the Output Voltage Swing

The output voltage swing can be expanded by adding 2 resistors to *Figure 10* as shown in *Figure 11*. These added resistors are used to attenuate the +V voltage. The overall gain, $A_V(-)$, from the +V terminal to the output of the op amp determines the most negative output voltage, $-4(+V)$ (when the V_{REF} voltage at the + input of the op amp is zero) with the component values shown. The complete dynamic range of V_{OUT} is provided by the gain from the (+) input of the op amp. As the voltage at the V_{REF} pin ranges from 0V to $+V(1023/1024)$ the output of the op amp will range from $-10\ V_{DC}$ to $+10V\ (1023/1024)$ when using a +V voltage of $+2.500\ V_{DC}$. The $2.5\ V_{DC}$ reference voltage can be easily developed by using the LM336 zener which can be biased through the R_{FB} internal resistor, connected to V_{CC}.

5.3 Op Amp V_{OS} Adjust (Zero Adjust) for Current Switching Mode

Proper operation of the ladder requires that all of the 2R legs always go to exactly $0\ V_{DC}$ (ground). Therefore offset voltage, V_{OS}, of the external op amp cannot be tolerated as every millivolt of V_{OS} will introduce 0.01% of added linearity error. At first this seems unusually sensitive, until it becomes clear the 1 mV is 0.01% of the 10V reference! High resolution converters of high accuracy require attention to every detail in an application to achieve the available performance which is inherent in the part. To prevent this source of error, the V_{OS} of the op amp has to be initially zeroed. This is the "zero adjust" of the DAC calibration sequence and should be done first.

If the V_{OS} is to be adjusted there are a few points to consider. Note that no "dc balancing" resistance should be used in the grounded positive input lead of the op amp. This resistance and the input current of the op amp can also create errors. The low input biasing current of the BI-FET op amps makes them ideal for use in DAC current to voltage applications. The V_{OS} of the op amp should be adjusted with a digital input of all zeros to force $I_{OUT} = 0$ mA. A 1 kΩ resistor can be temporarily connected from the inverting input to ground to provide a dc gain of approximately 15 to the V_{OS} of the op amp and make the zeroing easier to sense.

5.4 Full-Scale Adjust

The full-scale adjust procedure depends on the application circuit and whether the DAC is operated in the current switching mode or in the voltage switching mode. Techniques are given below for all of the possible application circuits.

5.4.1 Current Switching with Unipolar Output Voltage

After doing a "zero adjust," set all of the digital input levels HIGH and adjust the magnitude of V_{REF} for

$$V_{OUT} = -(\text{ideal } V_{REF})\,\frac{1023}{1024}$$

This completes the DAC calibration.

5.4.2 Current Switching with Bipolar Output Voltage

The circuit of *Figure 12* shows the 3 adjustments needed. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) and then trim "zero adj." for zero volts at the inverting input (pin 2) of 0A1. Next, with a code of all zeros still applied, adjust "−FS adj.", the reference voltage, for $V_{OUT} = \pm|(\text{ideal } V_{REF})|$. The sign of the output voltage will be opposite that of the applied reference.

Finally, set all of the digital inputs HIGH and adjust "+FS adj." for $V_{OUT} = V_{REF}$ (511/512). The sign of the output at this time will be the same as that of the reference voltage. The addition of the 200Ω resistor in series with the V_{REF} pin of the DAC is to force the circuit gain error from the DAC to be negative. This insures that adding resistance to R_{fb}, with the 500Ω pot, will always compensate the gain error of the DAC.

5.4.3 Voltage Switching with a Unipolar Output Voltage

Refer to the circuit of *Figure 13* and set all digital inputs LOW. Trim the "zero adj." for $V_{OUT} = 0\ V_{DC} \pm 1$ mV. Then set all digital inputs HIGH and trim the "FS Adj." for:

$$V_{OUT} = (+V)\left(1 + \frac{R_1}{R_2}\right)\frac{1023}{1024}$$

5.4.4 Voltage Switching with a Bipolar Output Voltage

Refer to *Figure 14* and set all digital inputs LOW. Trim the "−FS Adj." for $V_{OUT} = -2.5\ V_{DC}$. Then set all digital inputs HIGH and trim the "+FS Adj." for $V_{OUT} = +2.5$ (511/512) V_{DC}. Test the zero by setting the MS digital input HIGH and all the rest LOW. Adjust V_{OS} of amp #3, if necessary, and recheck the full-scale values.

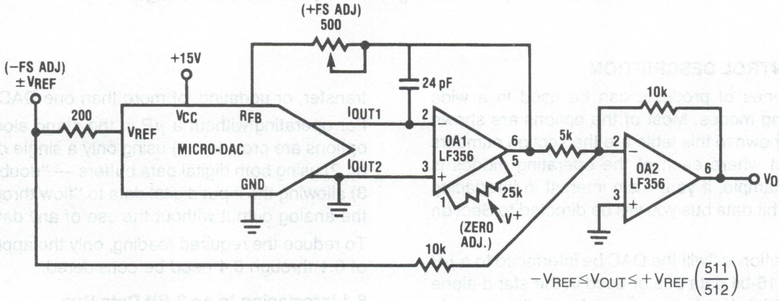

(+FS ADJ)
500
(−FS ADJ)
±VREF
+15V
24 pF
10k
200
VCC
RFB
IOUT1
VREF
MICRO-DAC
IOUT2
GND
2
3
OA1
LF356
6
5
1
25k
V+
(ZERO ADJ.)
5k
2
3
OA2
LF356
6
VOUT
10k
$-V_{REF} \le V_{OUT} \le +V_{REF}\left(\frac{511}{512}\right)$

FIGURE 12. Full Scale Adjust — Current Switching with Bipolar Output Voltage

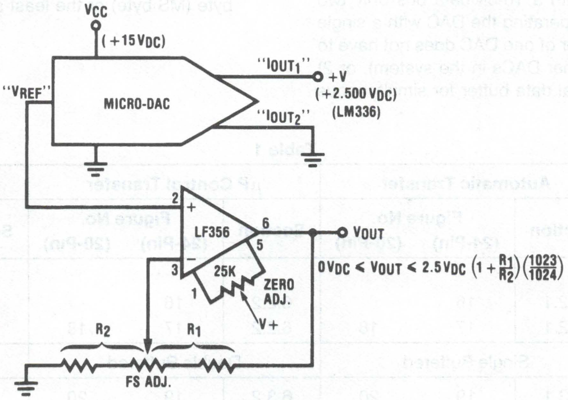

VCC
(+15VDC)
"IOUT1"
+V
(+2.500 VDC)
(LM336)
"VREF"
MICRO-DAC
"IOUT2"
2
3
LF356
6
5
1
25K
ZERO ADJ.
V+
VOUT
$0V_{DC} < V_{OUT} < 2.5V_{DC}\left(1 + \frac{R_1}{R_2}\right)\left(\frac{1023}{1024}\right)$
R2
R1
FS ADJ.

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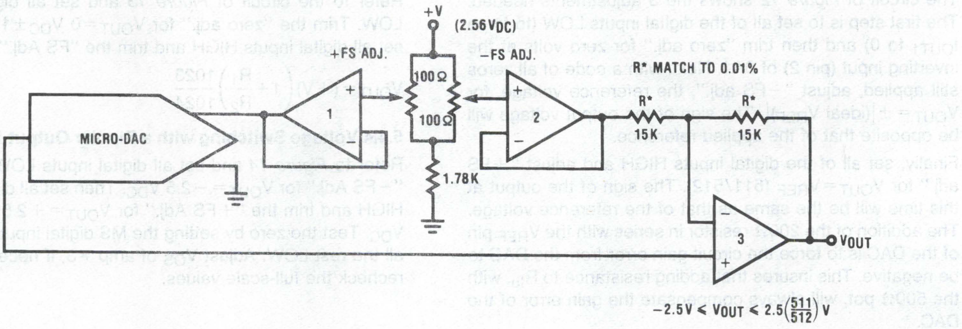
FIGURE 13. Full Scale Adjust — Voltage Switching with a Unipolar Output Voltage



TL/H/5688-15

FIGURE 14. Voltage Switching with a Bipolar Output Voltage

6.0 DIGITAL CONTROL DESCRIPTION

The DAC1000 series of products can be used in a wide variety of operating modes. Most of the options are shown in Table 1. Also shown in this table are the section numbers of this data sheet where each of the operating modes is discussed. For example, if your main interest in interfacing to a µP with an 8-bit data bus you will be directed to Section 6.1.0.

The first consideration is "will the DAC be interfaced to a µP with an 8-bit or a 16-bit data bus or used in the stand-alone mode?" For the 8-bit data bus, a second selection is made on how the 2nd digital data buffer (the DAC Latch) is updated by a transfer from the 1st digital data buffer (the Input Latch). Three options are provided: 1) an automatic transfer when the 2nd data byte is written to the DAC, 2) a transfer which is under the control of the µP and can include more than one DAC in a simultaneous transfer, or 3) a transfer which is under the control of external logic. Further, the data format can be either left justified or right justified.

When interfacing to a µP with a 16-bit data bus only two selections are available: 1) operating the DAC with a single digital data buffer (the transfer of one DAC does not have to be synchronized with any other DACs in the system), or 2) operating with a double digital data buffer for simultaneous transfer, or updating, of more than one DAC.

For operating without a µP in the stand alone mode, three options are provided: 1) using only a single digital data buffer, 2) using both digital data buffers — "double buffered," or 3) allowing the input digital data to "flow through" to provide the analog output without the use of any data latches.

To reduce the required reading, only the applicable sections of 6.1 through 6.4 need be considered.

6.1 Interfacing to an 8-Bit Data Bus

Transferring 10 bits of data over an 8-bit bus requires two write cycles and provides four possible combinations which depend upon two basic data format and protocol decisions:

1. Is the data to be left justified (considered as fractional binary data with the binary point to the left) or right justified (considered as binary weighted data with the binary point to the right)?
2. Which byte will be transferred first, the most significant byte (MS byte) or the least significant byte (LS byte)?

Table 1

Operating Mode	Automatic Transfer			µP Control Transfer			External Transfer		
Data Bus	**Section**	**Figure No. (24-Pin)**	**(20-Pin)**	**Section**	**Figure No. (24-Pin)**	**(20-Pin)**	**Section**	**Figure No. (24-Pin)**	**(20-Pin)**
8-Bit Data Bus (6.1.0)									
Right Justified (6.1.1)	6.2.1	16		6.2.2	16		6.2.3	16	
Left Justified (6.1.2)	6.2.1	17	18	6.2.2	17	18	6.2.3	17	18
16-Bit Data Bus (6.3.0)	Single Buffered			Double Buffered			Flow Through		
	6.3.1	19	20	6.3.2	19	20	Not Applicable		
Stand Alone (6.4.0)	Single Buffered			Double Buffered			Flow Through		
	6.4.1	19	20	6.4.2	19	20	6.4.3	19	NA

These data possibilities are shown in *Figure 15.* Note that the justification of data depends on how the 10-bit data word is located within the 16-bit data source (CPU) register. In either case, there is a surplus of 6 bits and these are shown as "don't care" terms ("×") in this figure.

All of these DACs load 10 bits on the 1st write cycle. A particular set of 2 bits is then overwritten on the 2nd write cycle, depending on the justification of the data. This requires the 1st write cycle to contain the LS or L0 Byte data group for all right justified data options. For all left justified data options, the 1st write cycle must contain the MS or Hi Byte data group.

6.1.1 Providing for Optional Data Format

The DAC1000/1/2 (24-pin parts) can be used for either data formatting by tying the LJ/$\overline{\text{RJ}}$ pin either high or low, respectively. A simplified logic diagram which shows the external connections to the data bus and the internal functions of both of the data buffer registers (Input Latch and DAC Register) is shown in *Figure 16* for the right justified data operation. *Figure 17* is for left justified data.

6.1.2 For Left Justified Data

For applications which require left justified data, DAC1006–1008 (20-pin parts) can be used. A simplified logic diagram which shows the external connections to the data bus and the internal functions of both of the data buffer registers (Input Latch and DAC Register) is shown in *Figure 18.* These parts require the MS or Hi Byte data group to be transferred on the 1st write cycle.

6.2 Controlling Data Transfer for an 8-Bit Data Bus

Three operating modes are possible for controlling the transfer of data from the Input Latch to the DAC Register, where it will update the analog output voltage. The simplest is the automatic transfer mode, which causes the data transfer to occur at the time of the 2nd write cycle. This is recommended when the exact timing of the changes of the DAC analog output are not critical. This typically happens where each DAC is operating individually in a system and the analog updating of one DAC is not required to be synchronized to any other DAC. For synchronized DAC updating, two options are provided: μP control via a common $\overline{\text{XFER}}$ strobe or external update timing control via an external strobe. The details of these options are now shown.

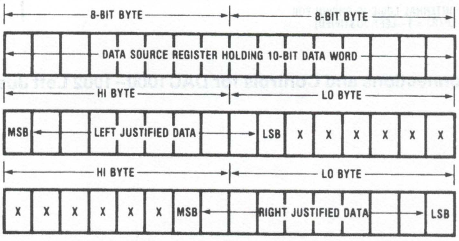

8-BIT BYTE
8-BIT BYTE
DATA SOURCE REGISTER HOLDING 10-BIT DATA WORD
HI BYTE
LO BYTE
MSB
LEFT JUSTIFIED DATA
LSB
X
HI BYTE
LO BYTE
X
MSB
RIGHT JUSTIFIED DATA
LSB

FIGURE 15. Fitting a 10-Bit Data Word into 16 Available Bit Locations

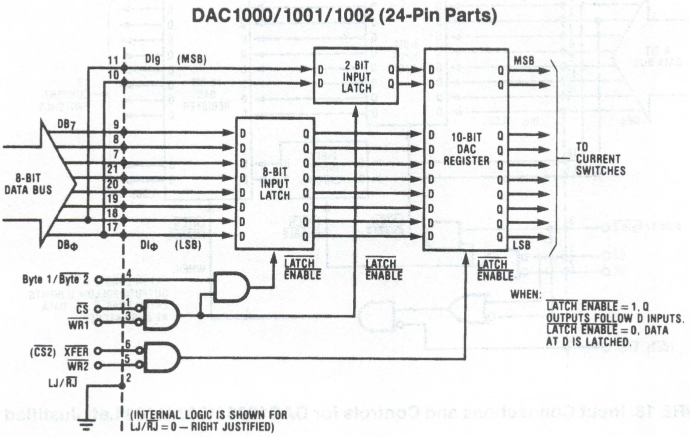

DAC1000/1001/1002 (24-Pin Parts)
DI9 (MSB)
DI0 (LSB)
11
10
9
8
7
21
20
19
18
17
DB7
DB0
8-BIT DATA BUS
2 BIT INPUT LATCH
8-BIT INPUT LATCH
10-BIT DAC REGISTER
D
Q
MSB
LSB
TO CURRENT SWITCHES
LATCH ENABLE
Byte 1/$\overline{\text{Byte 2}}$
$\overline{\text{CS}}$
$\overline{\text{WR1}}$
($\overline{\text{CS2}}$) $\overline{\text{XFER}}$
$\overline{\text{WR2}}$
LJ/$\overline{\text{RJ}}$
4
1
3
6
5
2
WHEN:
LATCH ENABLE = 1, Q OUTPUTS FOLLOW D INPUTS.
LATCH ENABLE = 0, DATA AT D IS LATCHED.
(INTERNAL LOGIC IS SHOWN FOR LJ/$\overline{\text{RJ}}$ = 0 — RIGHT JUSTIFIED)

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FIGURE 16. Input Connections and Controls for DAC1000–1002 Right Justified Data Option

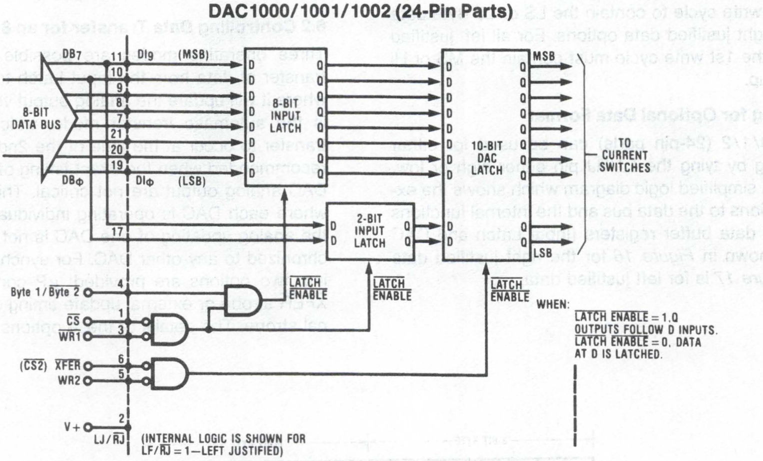
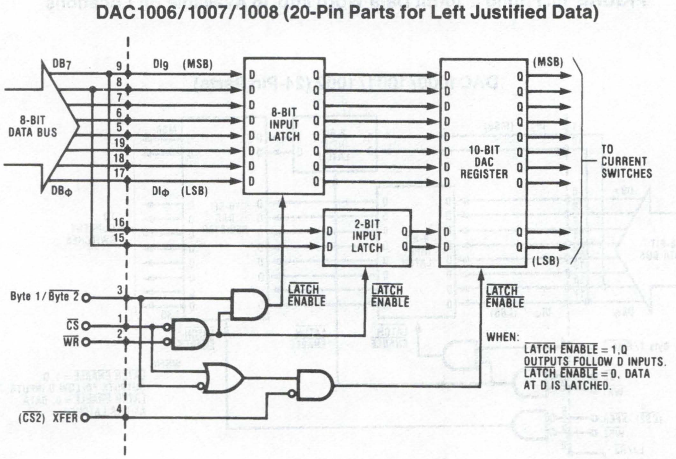

DAC1000/1001/1002 (24-Pin Parts)
8-BIT DATA BUS
DB7
DBφ
DI9 (MSB)
DIφ (LSB)
11
10
9
8
7
21
20
19
17
8-BIT INPUT LATCH
2-BIT INPUT LATCH
10-BIT DAC LATCH
MSB
LSB
TO CURRENT SWITCHES
LATCH ENABLE
Byte 1/Byte 2
CS
WR1
(CS2) XFER
WR2
V+
LJ/RJ
4
1
3
6
5
2
WHEN:
LATCH ENABLE = 1, Q OUTPUTS FOLLOW D INPUTS.
LATCH ENABLE = 0, DATA AT D IS LATCHED.
(INTERNAL LOGIC IS SHOWN FOR LF/RJ = 1—LEFT JUSTIFIED)

FIGURE 17. Input Connections and Controls for DAC1000–1002 Left Justified Data Option

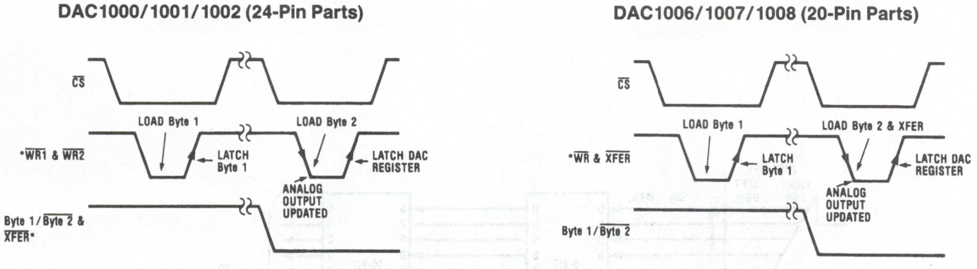

DAC1006/1007/1008 (20-Pin Parts for Left Justified Data)
8-BIT DATA BUS
DB7
DBφ
DI9 (MSB)
DIφ (LSB)
9
8
7
6
5
19
18
17
16
15
8-BIT INPUT LATCH
2-BIT INPUT LATCH
10-BIT DAC REGISTER
(MSB)
(LSB)
TO CURRENT SWITCHES
LATCH ENABLE
Byte 1/Byte 2
CS
WR
(CS2) XFER
3
1
2
4
WHEN:
LATCH ENABLE = 1, Q OUTPUTS FOLLOW D INPUTS.
LATCH ENABLE = 0, DATA AT D IS LATCHED.

TL/H/5688-17

FIGURE 18. Input Connections and Controls for DAC1006/1007/1008 Left Justified Data

6.2.1 Automatic Transfer

This makes use of a double byte (double precision) write. The first byte (8 bits) is strobed into the input latch and the second byte causes a simultaneous strobe of the two remaining bits into the input latch and also the transfer of the complete 10-bit word from the input latch to the DAC register. This is shown in the following timing diagrams; the point in time where the analog output is updated is also indicated on these diagrams.


DAC1000/1001/1002 (24-Pin Parts)

DAC1006/1007/1008 (20-Pin Parts)

CS
LOAD Byte 1
LOAD Byte 2
*WR1 & WR2
LATCH Byte 1
LATCH DAC REGISTER
ANALOG OUTPUT UPDATED
Byte 1/Byte 2 & XFER*
CS
LOAD Byte 1
LOAD Byte 2 & XFER
*WR & XFER
LATCH Byte 1
LATCH DAC REGISTER
ANALOG OUTPUT UPDATED
Byte 1/Byte 2

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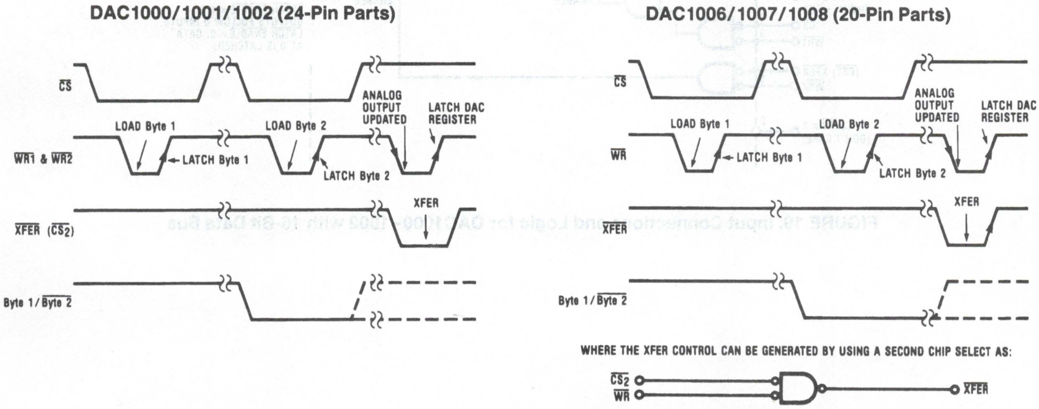
*SIGNIFIES CONTROL INPUTS WHICH ARE DRIVEN IN PARALLEL

6.2.2 Transfer Using μP Write Stroke

The input latch is loaded with the first two write strobes. The $\overline{\text{XFER}}$ signal is provided by external logic, as shown below, to cause the transfer to be accomplished on a third write strobe. This is shown in the following diagrams:


DAC1000/1001/1002 (24-Pin Parts)

DAC1006/1007/1008 (20-Pin Parts)

CS
LOAD Byte 1
LOAD Byte 2
ANALOG OUTPUT UPDATED
LATCH DAC REGISTER
WR1 & WR2
LATCH Byte 1
LATCH Byte 2
XFER (CS2)
XFER
Byte 1/Byte 2
CS
LOAD Byte 1
LOAD Byte 2
ANALOG OUTPUT UPDATED
LATCH DAC REGISTER
WR
LATCH Byte 1
LATCH Byte 2
XFER
XFER
Byte 1/Byte 2
CS2
WR
XFER

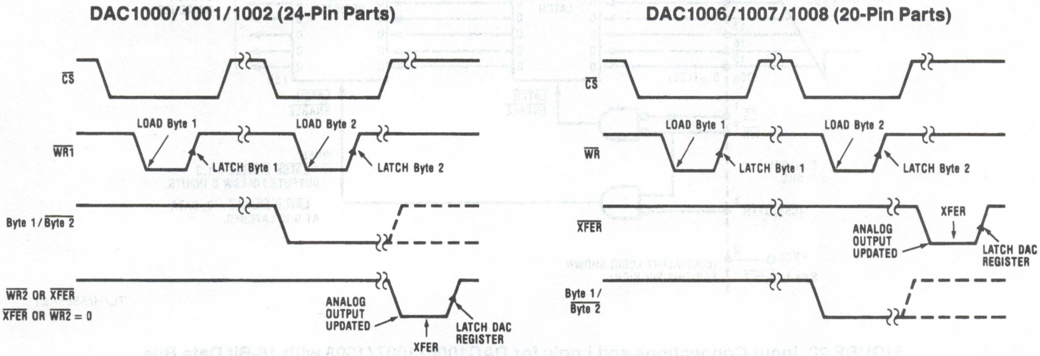
WHERE THE XFER CONTROL CAN BE GENERATED BY USING A SECOND CHIP SELECT AS:

AND THE BYTE CONTROL CAN BE DERIVED FROM THE ADDRESS BUS SIGNALS.

TL/H/5688–19

6.2.3 Transfer Using an External Strobe

This is similar to the previous operation except the $\overline{\text{XFER}}$ signal is not provided by the μP. The timing diagram for this is:


DAC1000/1001/1002 (24-Pin Parts)

DAC1006/1007/1008 (20-Pin Parts)

CS
LOAD Byte 1
LOAD Byte 2
WR1
LATCH Byte 1
LATCH Byte 2
Byte 1/Byte 2
WR2 OR XFER
XFER OR WR2 = 0
ANALOG OUTPUT UPDATED
XFER
LATCH DAC REGISTER
CS
LOAD Byte 1
LOAD Byte 2
WR
LATCH Byte 1
LATCH Byte 2
XFER
XFER
ANALOG OUTPUT UPDATED
LATCH DAC REGISTER
Byte 1/Byte 2

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6.3 Interfacing to a 16-Bit Data Bus

The interface to a 16-bit data bus is easily handled by connecting to 10 of the available bus lines. This allows a wiring selected right justified or left justified data format. This is shown in the connection diagrams of *Figures 19* and *20*, where the use of DB6 to DB15 gives left justified data operation. Note that any part number can be used and the Byte1/$\overline{\text{Byte2}}$ control should be wired Hi.

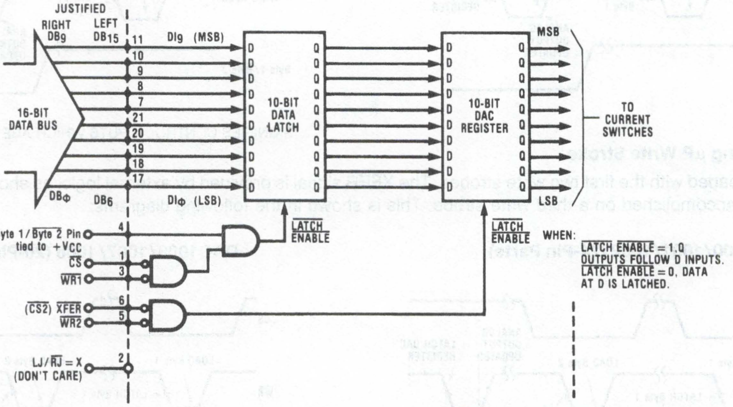
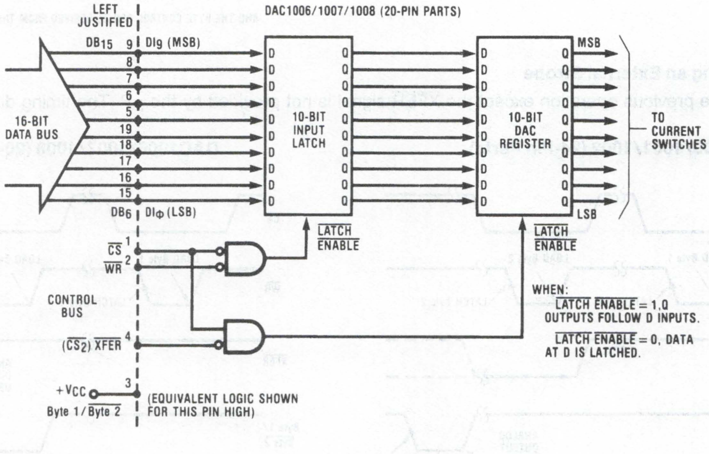

JUSTIFIED
RIGHT
LEFT
DB9
DB15
11
10
9
8
7
21
20
19
18
17
DI9 (MSB)
16-BIT DATA BUS
DBΦ
DB6
DIΦ (LSB)
D
Q
10-BIT DATA LATCH
10-BIT DAC REGISTER
MSB
LSB
TO CURRENT SWITCHES
LATCH ENABLE
LATCH ENABLE
Byte 1/Byte 2 Pin tied to +VCC
4
CS
1
WR1
3
(CS2) XFER
6
WR2
5
LJ/RJ = X (DON'T CARE)
2
WHEN:
LATCH ENABLE = 1, Q OUTPUTS FOLLOW D INPUTS.
LATCH ENABLE = 0, DATA AT D IS LATCHED.

FIGURE 19. Input Connections and Logic for DAC1000–1002 with 16-Bit Data Bus


LEFT JUSTIFIED
DAC1006/1007/1008 (20-PIN PARTS)
DB15
9
8
7
6
5
19
18
17
16
15
DB6
DI9 (MSB)
DIΦ (LSB)
16-BIT DATA BUS
D
Q
10-BIT INPUT LATCH
10-BIT DAC REGISTER
MSB
LSB
TO CURRENT SWITCHES
LATCH ENABLE
LATCH ENABLE
CS
1
WR
2
CONTROL BUS
(CS2) XFER
4
+VCC
3
Byte 1/Byte 2
(EQUIVALENT LOGIC SHOWN FOR THIS PIN HIGH)
WHEN:
LATCH ENABLE = 1, Q OUTPUTS FOLLOW D INPUTS.
LATCH ENABLE = 0, DATA AT D IS LATCHED.

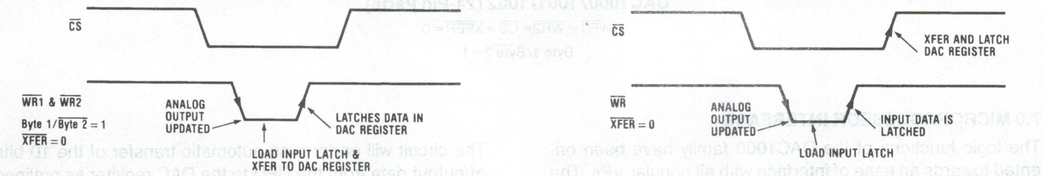
TL/H/5688–21

FIGURE 20. Input Connections and Logic for DAC1006/1007/1008 with 16-Bit Data Bus

Three operating modes are possible: flow through, single buffered, or double buffered. The timing diagrams for these are shown below:

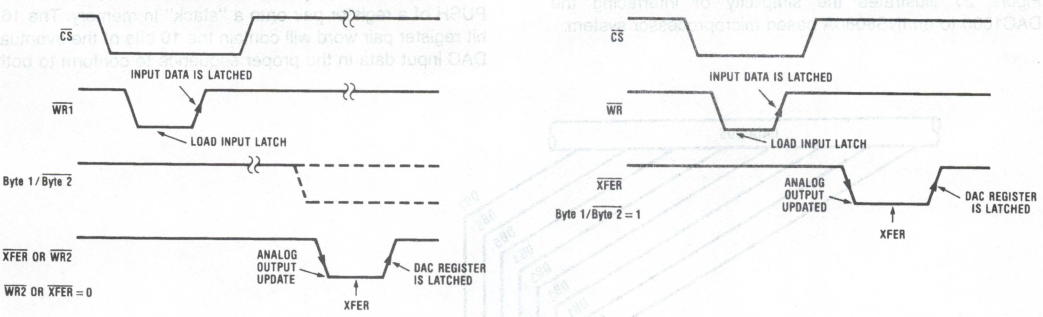
6.3.1 Single Buffered

DAC1000/1001/1002 (24-Pin Parts) DAC1006/1007/1008 (20-Pin Parts)


CS
WR1 & WR2
Byte 1/Byte 2 = 1
XFER = 0
ANALOG OUTPUT UPDATED
LATCHES DATA IN DAC REGISTER
LOAD INPUT LATCH & XFER TO DAC REGISTER
CS
XFER AND LATCH DAC REGISTER
WR
XFER = 0
ANALOG OUTPUT UPDATED
INPUT DATA IS LATCHED
LOAD INPUT LATCH

6.3.2 Double Buffered

DAC 1000/1001/1002 (24-Pin Parts) DAC1006/1007/1008 (20-Pin Parts)


CS
INPUT DATA IS LATCHED
WR1
LOAD INPUT LATCH
Byte 1/Byte 2
XFER OR WR2
WR2 OR XFER = 0
ANALOG OUTPUT UPDATE
DAC REGISTER IS LATCHED
XFER
CS
INPUT DATA IS LATCHED
WR
LOAD INPUT LATCH
XFER
Byte 1/Byte 2 = 1
ANALOG OUTPUT UPDATED
DAC REGISTER IS LATCHED
XFER

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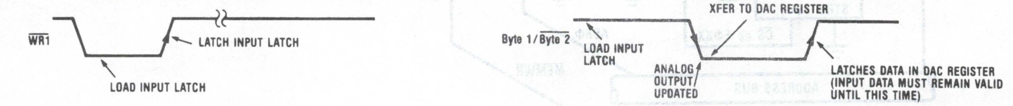
6.4 Stand Alone Operation

For applications for a DAC which are not under μP control (stand alone) there are two basic operating modes, single buffered and double buffered. The timing diagrams for these are shown below:

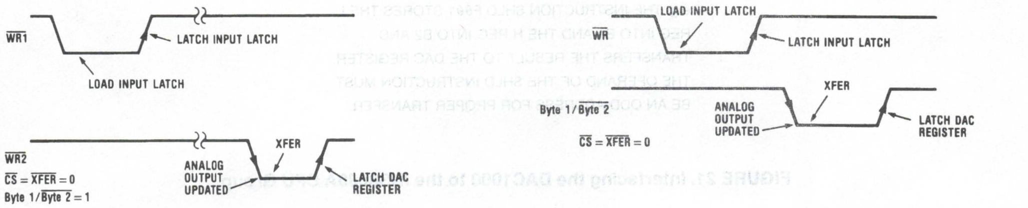
6.4.1 Single Buffered

DAC1000/1001/1002 (24-Pin Parts) DAC1006/1007/1008 (20-Pin Parts)


WR1
LATCH INPUT LATCH
LOAD INPUT LATCH
XFER TO DAC REGISTER
Byte 1/Byte 2
LOAD INPUT LATCH
ANALOG OUTPUT/ UPDATED
LATCHES DATA IN DAC REGISTER (INPUT DATA MUST REMAIN VALID UNTIL THIS TIME)

6.4.2 Double Buffered

DAC1000/1001/1002 (24-Pin Parts) DAC1006/1007/1008 (20-Pin Parts)*


WR1
LATCH INPUT LATCH
LOAD INPUT LATCH
WR2
CS = XFER = 0
Byte 1/Byte 2 = 1
XFER
ANALOG OUTPUT UPDATED
LATCH DAC REGISTER
LOAD INPUT LATCH
WR
LATCH INPUT LATCH
XFER
Byte 1/Byte 2
CS = XFER = 0
ANALOG OUTPUT UPDATED
LATCH DAC REGISTER

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*For a connection diagram of this operating mode use *Figure 18* for the Logic and *Figure 20* for the Data Input connections.

6.4.3 Flow Through

This operating mode causes the 10-bit input word to directly create the DAC output without any latching involved.

DAC1000/1001/1002 (24-Pin Parts)

$\overline{\text{WR1}} = \overline{\text{WR2}} = \overline{\text{CS}} = \overline{\text{XFER}} = 0$

Byte 1/$\overline{\text{Byte 2}} = 1$

7.0 MICROPROCESSOR INTERFACE

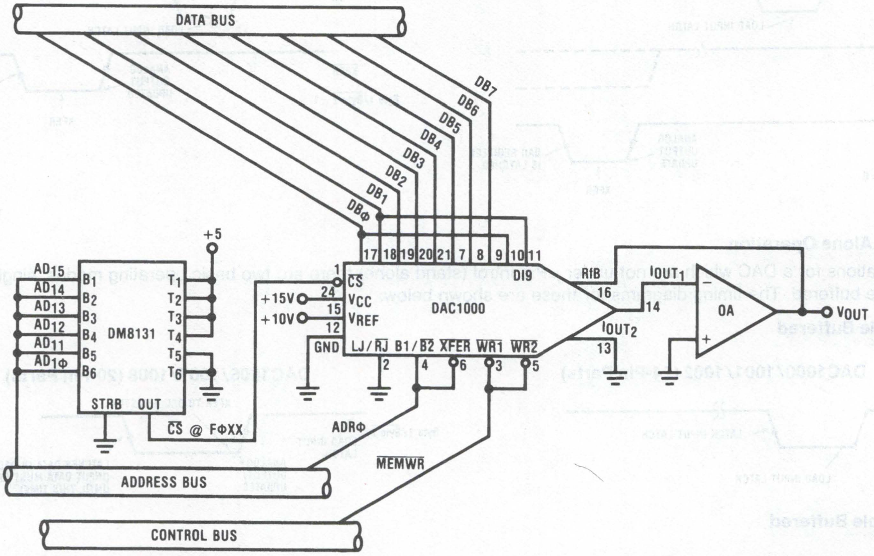
The logic functions of the DAC1000 family have been oriented towards an ease of interface with all popular μPs. The following sections discuss in detail a few useful interface schemes.

7.1 DAC1001/1/2 to INS8080A Interface

Figure 21 illustrates the simplicity of interfacing the DAC1000 to an INS8080A based microprocessor system.

The circuit will perform an automatic transfer of the 10 bits of output data from the CPU to the DAC register as outlined in Section 6.2.1, "Controlling Data Transfer for an 8-Bit Data Bus."

Since a double byte write is necessary to control the DAC with the INS8080A, a possible instruction to achieve this is a PUSH of a register pair onto a "stack" in memory. The 16-bit register pair word will contain the 10 bits of the eventual DAC input data in the proper sequence to conform to both


DATA BUS
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBΦ
+5
17
18
19
20
21
7
8
9
10
11
DI9
AD15
AD14
AD13
AD12
AD11
AD10
B1
B2
B3
B4
B5
B6
DM8131
T1
T2
T3
T4
T5
T6
STRB
OUT
CS @ FΦXX
1
CS
+15V
24
VCC
+10V
15
VREF
12
GND
LJ/RJ
B1/B2
XFER
WR1
WR2
DAC1000
2
4
6
3
5
RfB
16
IOUT1
14
IOUT2
13
OA
VOUT
ADRΦ
MEMWR
ADDRESS BUS
CONTROL BUS

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NOTE: DOUBLE BYTE STORES CAN BE USED.
e.g. THE INSTRUCTION SHLD FΦΦ1 STORES THE L REG INTO B1 AND THE H REG INTO B2 AND TRANSFERS THE RESULT TO THE DAC REGISTER. THE OPERAND OF THE SHLD INSTRUCTION MUST BE AN ODD ADDRESS FOR PROPER TRANSFER.

FIGURE 21. Interfacing the DAC1000 to the INS8080A CPU Group

the requirements of the DAC (with regard to right or left justified data) and the implementation of the PUSH instruction which will output the higher order byte of the register pair (i.e., register B of the BC pair) first. The DAC will actually appear as a two-byte "stack" in memory to the CPU. The auto-decrementing of the stack pointer during a PUSH allows using address bit 0 of the stack pointer as the Byte1/$\overline{\text{Byte2}}$ and $\overline{\text{XFER}}$ strobes if bit 0 of the stack pointer address −1, (SP−1), is a "1" as presented to the DAC. Additional address decoding by the DM8131 will generate a unique DAC chip select (CS) and synchronize this CS to the two memory write strobes of the PUSH instruction.

To reset the stack pointer so new data may be output to the same DAC, a POP instruction followed by instructions to insure that proper data is in the DAC data register pair before it is "PUSHED" to the DAC should be executed, as the POP instruction will arbitrarily alter the contents of a register pair.

Another double byte write instruction is Store H and L Direct (SHLD), where the HL register pair would temporarily contain the DAC data and the two sequential addresses for the DAC are specified by the instruction op code. The auto incrementing of the DAC address by the SHLD instruction permits the same simple scheme of using address bit 0 to generate the byte number and transfer strobes.

7.2 DAC1000 to MC6820/1 PIA Interface

In *Figure 22* the DAC1000 is interfaced to an M6800 system through an MC6820/1 Peripheral Interface Adapter (PIA). In this case the CS pin of the DAC is grounded since the PIA is already mapped in the 6800 system memory space and no decoding is necessary. Furthermore, by using both Ports A and B of the PIA the 10-bit data transfer, assumed right justified again in two 8-bit bytes, is greatly simplified. The HIGH byte is loaded into Output Register A (ORA) of the PIA, and the LOW byte is loaded into ORB. The 10-bit data transfer to the DAC and the corresponding analog output change occur simultaneously upon CB2 going LOW under program control. The 10-bit data word in the DAC register will be latched (and hence V_{OUT} will be fixed) when CB2 is brought back HIGH.

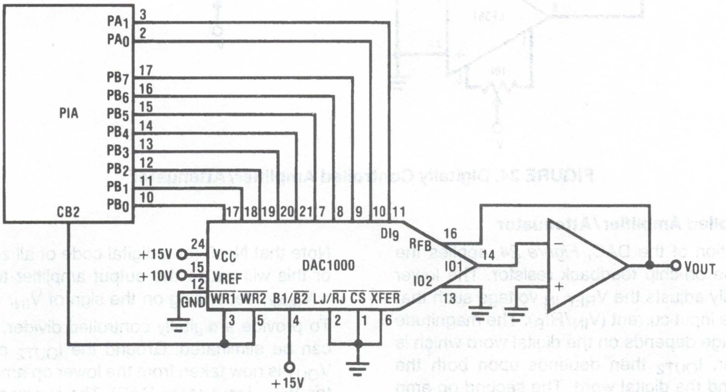
If both output ports of the PIA are not available, it is possible to interface the DAC1000 through a single port without much effort. However, additional logic at the CB2(or CA2) lines or access to some of the 6800 system control lines will be required.

7.3 Noise Considerations

A typical digital/microprocessor bus environment is a tremendous potential source of high frequency noise which can be coupled to sensitive analog circuitry. The fast edges of the data and address bus signals generate frequency components of 10's of megahertz and can cause noise spikes to appear at the DAC output. These noise spikes occur when the data bus changes state or when data is transferred between the latches of the device.

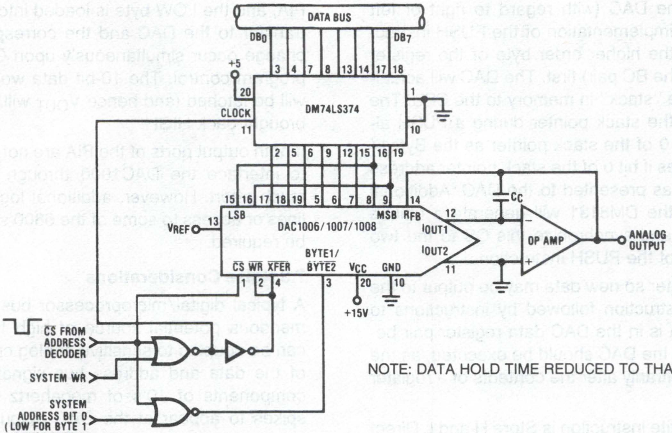
In low frequency or DC applications, low pass filtering can reduce these noise spikes. This is accomplished by overcompensating the DAC output amplifier by increasing the value of the feedback capacitor (C_C in *Figure 3*).

In applications requiring a fast transient response from the DAC and op amp, filtering may not be feasible. Adding a latch, DM74LS374, as shown in *Figure 23* isolates the device from the data bus, thus eliminating noise spikes that occur every time the data bus changes state. Another method for eliminating noise spikes is to add a sample and hold after the DAC op amp. This also has the advantage of eliminating noise spikes when changing digital codes.



TL/H/5688–25

FIGURE 22. DAC1000 to MC6820/1 PIA Interface


DATA BUS
DB0
DB7
+5
3 4 7 8 13 14 17 18
20
1
CLOCK
DM74LS374
11
10
2 5 6 9 12 15 16 19
15 16 17 18 19 5 6 7 8 9 14
LSB
MSB RFB
12
CC
VREF
13
DAC1006/1007/1008
IOUT1
IOUT2
OP AMP
ANALOG OUTPUT
11
BYTE1/ BYTE2
CS WR XFER
VCC GND
1 2 17
3
20 10
+15V
CS FROM ADDRESS DECODER
SYSTEM WR
SYSTEM ADDRESS BIT 0 (LOW FOR BYTE 1 HIGH FOR BYTE 2)

NOTE: DATA HOLD TIME REDUCED TO THAT OF DM74LS374 (≈10 ns)

FIGURE 23. Isolating Data Bus from DAC Circuitry to Eliminate Digital Noise Coupling

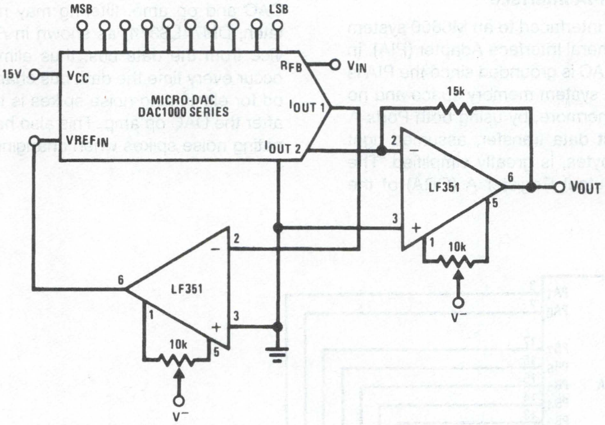

MSB
LSB
15V
VCC
RFB
VIN
15k
MICRO-DAC DAC1000 SERIES
IOUT 1
VREFIN
IOUT 2
2
6
LF351
VOUT
5
3
1
10k
V−
2
6
LF351
1
3
10k
5
V−

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FIGURE 24. Digitally Controlled Amplifier/Attenuator

7.4 Digitally Controlled Amplifier/Attenuator

An unusual application of the DAC, *Figure 24*, applies the input voltage via the on-chip feedback resistor. The lower op amp automatically adjusts the $V_{REF\ IN}$ voltage such that I_{OUT1} is equal to the input current (V_{IN}/Rf_B). The magnitude of this $V_{REF\ IN}$ voltage depends on the digital word which is in the DAC register. I_{OUT2} then depends upon both the magnitude of V_{IN} and the digital word. The second op amp converts I_{OUT2} to a voltage, V_{OUT}, which is given by:

$$V_{OUT} = V_{IN}\left(\frac{1023-N}{N}\right), \text{ where } 0<N\leq 1023.$$

Note that N = 0 (or a digital code of all zeros) is not allowed or this will cause the output amplifier to saturate at either $\pm V_{MAX}$, depending on the sign of V_{IN}.

To provide a digitally controlled divider, the output op amp can be eliminated. Ground the I_{OUT2} pin of the DAC and V_{OUT} is now taken from the lower op amp (which also drives the V_{REF} input of the DAC). The expression for V_{OUT} is now given by

$$V_{OUT} = -\frac{V_{IN}}{M} \text{ where M = Digital input (expressed as a fractional binary number).}$$

$$0<M<1.$$

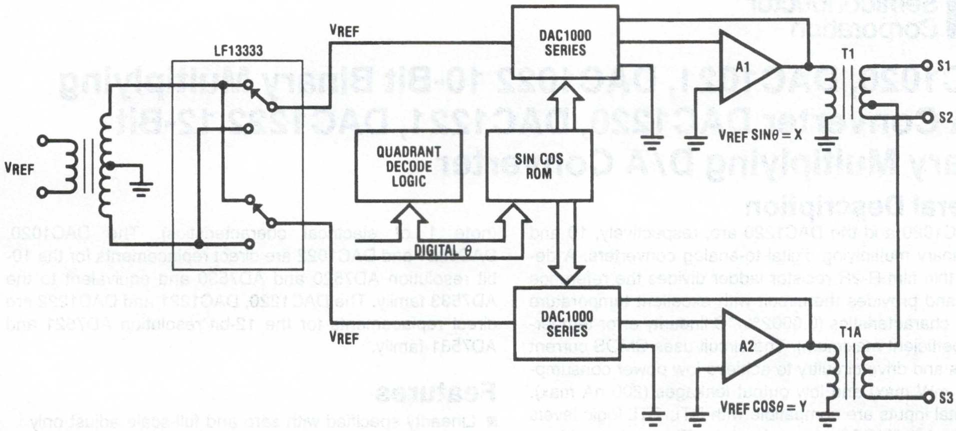
VREF
LF13333
VREF
DAC1000 SERIES
A1
T1
S1
S2
VREF SINθ = X
QUADRANT DECODE LOGIC
SIN COS ROM
DIGITAL θ
DAC1000 SERIES
VREF
A2
T1A
S3
VREF COSθ = Y

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FIGURE 25. Digital to Synchro Converter

Ordering Information

1. All Logic Features — 24-pin package.

Accuracy	Temperature Range		
	−40°C to +85°C	−55°C to +125°C	0° to +70°C
0.05% (10-bit) 0.10% (9-bit) 0.20% (8-bit)	DAC1000LCJ DAC1002LCJ	DAC1000LJ DAC1002LJ	DAC 1000LCN DAC1001LCN DAC1002LCN
Package Outline	J24A	J24A	N24A

2. For Left Justified Data — 20-pin package.

Accuracy	Temperature Range		
	−40°C to +85°C	−55°C to +125°C	0° to +70°C
0.05% (10-bit) 0.10% (9-bit) 0.20% (8-bit)	DAC1006LCJ DAC1008LCJ	DAC1006LJ DAC1008LJ	DAC1006LCN DAC1007LCN DAC1008LCN
Package Outline	J20A	J20A	N20A

National Semiconductor Corporation

DAC1020, DAC1021, DAC1022 10-Bit Binary Multiplying D/A Converter DAC1220, DAC1221, DAC1222 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1020 and the DAC1220 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.0002%/°C linearity error temperature coefficient maximum). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low output leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference. All inputs are protected from damage due to static discharge by diode clamps to V+ and ground.

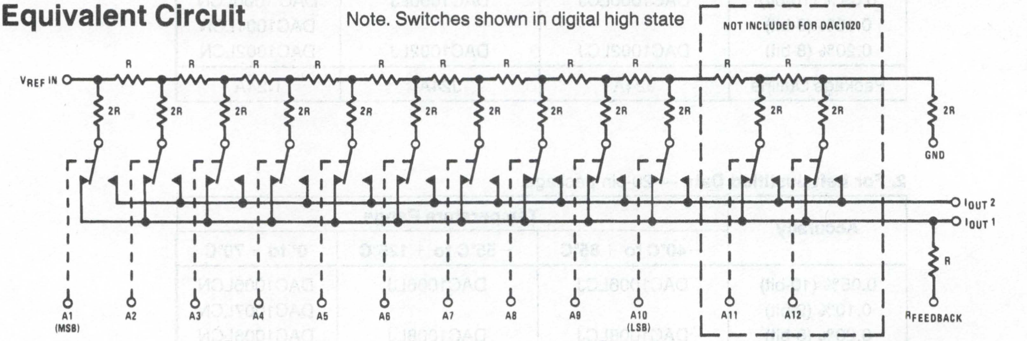
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity guaranteed over temperature (note 1 of electrical characteristics). The DAC1020, DAC1021 and DAC1022 are direct replacements for the 10-bit resolution AD7520 and AD7530 and equivalent to the AD7533 family. The DAC1220, DAC1221 and DAC1222 are direct replacements for the 12-bit resolution AD7521 and AD7531 family.

Features

- Linearity specified with zero and full-scale adjust only
- Non-linearity guaranteed over temperature
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq 25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—500 ns typ
- Low feedthrough error—½ LSB @100 kHz typ

Equivalent Circuit

Note. Switches shown in digital high state



TL/H/5689-1

Ordering Information

10-BIT D/A CONVERTERS

Temperature Range		0°C to 70°C		−40°C to +85°C		−55°C to +125°C	
Non-Linearity	0.05%	DAC1020LCN	AD7520LN,AD7530LN	DAC1020LCJ	AD7520LD,AD7530LD	DAC1020LJ	AD7520UD
	0.10%	DAC1021LCN	AD7520KN,AD7530KN	DAC1021LCJ	AD7520KD,AD7530KD	DAC1021LJ	AD7520TD
	0.20%	DAC1022LCN	AD7520JN,AD7530JN	DAC1022LCJ	AD7520JD,AD7530JD	DAC1022LJ	AD7520SD
Package Outline		N16A		J16A		J16A	

12-BIT D/A CONVERTERS

Temperature Range		0°C to 70°C		−40°C to +85°C		−55°C to +125°C	
Non-Linearity	0.05%	DAC1220LCN	AD7521LN,AD7531LN	DAC1220LCJ	AD7521LD,AD7531LD	DAC1220LJ	AD7521UD
	0.10%	DAC1221LCN	AD7521KN,AD7531KN				
	0.20%	DAC1222LCN	AD7521JN,AD7531JN	DAC1222LCJ	AD7521JD,AD7531JD	DAC1222LJ	AD7521SD
Package Outline		N18A		J18A		J18A	

Note. Devices may be ordered by either part number.

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V^+ to Gnd	17V
V_{REF} to Gnd	±25V
Digital Input Voltage Range	V^+ to Gnd
DC Voltage at Pin 1 or Pin 2 (Note 3)	−100 mV to V^+
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
ESD Susceptibility (Note 4)	800V

Operating Ratings

	Min	Max	Units
Temperature (T_A)			
DAC1020LJ, DAC1021LJ	−55	+125	°C
DAC1022LJ, DAC1220LJ	−55	+125	°C
DAC1222LJ	−55	+125	°C
DAC1020LCJ, DAC1021LCJ	−40	+85	°C
DAC1022LCJ, DAC1220LCJ	−40	+85	°C
DAC1222LCJ	−40	+85	°C
DAC1020LCN, DAC1021LCN	0	+70	°C
DAC1022LCN, DAC1220LCN	0	+70	°C
DAC1221LCN, DAC1222LCN	0	+70	°C

Electrical Characteristics ($V^+ = 15V$, $V_{REF} = 10.000V$, $T_A = 25°C$ unless otherwise specified)

Parameter	Conditions	DAC1020, DAC1021, DAC1022			DAC1220, DAC1221, DAC1222			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		10			12			Bits
Linearity Error	$T_{MIN} < T_A < T_{MAX}$, $-10V < V_{REF} < +10V$, (Note 1) End Point Adjustment Only (See Linearity Error in Definition of Terms)							
10-Bit Parts	DAC1020, DAC1220			0.05			0.05	% FSR
9-Bit Parts	DAC1021, DAC1221			0.10			0.10	% FSR
8-Bit Parts	DAC1022, DAC1222			0.20			0.20	% FSR
Linearity Error Tempco	$-10V \leq V_{REF} \leq +10V$, (Notes 1 and 2)			0.0002			0.0002	% FS/°C
Full-Scale Error	$-10V \leq V_{REF} \leq +10V$, (Notes 1 and 2)		0.3	1.0		0.3	1.0	% FS
Full-Scale Error Tempco	$T_{MIN} < T_A < T_{MAX}$, (Note 2)			0.001			0.001	% FS/°C
Output Leakage Current	$T_{MIN} \leq T_A \leq T_{MAX}$							
$I_{OUT\ 1}$	All Digital Inputs Low			200			200	nA
$I_{OUT\ 2}$	All Digital Inputs High			200			200	nA
Power Supply Sensitivity	All Digital Inputs High, $14V \leq V^+ \leq 16V$, (Note 2), *(Figure 2)*		0.005			0.005		% FS/V
V_{REF} Input Resistance		10	15	20	10	15	20	kΩ
Full-Scale Current Settling Time	$R_L = 100\Omega$ from 0 to 99. 95% FS All Digital Inputs Switched Simultaneously		500			500		ns
V_{REF} Feedthrough	All Digital Inputs Low, $V_{REF} = 20$ Vp-p @ 100 kHz			10			10	mVp-p
	J Package (Note 4)		6	9		6	9	mVp-p
	N Package		2	5		2	5	mVp-p
Output Capacitance								
$I_{OUT\ 1}$	All Digital Inputs Low		40			40		pF
	All Digital Inputs High		200			200		pF
$I_{OUT\ 2}$	All Digital Inputs Low		200			200		pF
	All Digital Inputs High		40			40		pF

Electrical Characteristics ($V^+ = 15V$, $V_{REF} = 10.000V$, $T_A = 25°C$ unless otherwise specified) (Continued)

Parameter	Conditions	DAC1020, DAC1021, DAC1022 Min	DAC1020, DAC1021, DAC1022 Typ	DAC1020, DAC1021, DAC1022 Max	DAC1220, DAC1221, DAC1222 Min	DAC1220, DAC1221, DAC1222 Typ	DAC1220, DAC1221, DAC1222 Max	Units
Digital Input	*(Figure 1)*							
Low Threshold	$T_{MIN}<T_A<T_{MAX}$			0.8			0.8	V
High Threshold	$T_{MIN}<T_A<T_{MAX}$	2.4			2.4			V
Digital Input Current	$T_{MIN} \le T_A \le T_{MAX}$							
	Digital Input High		1	100		1	100	μA
	Digital Input Low		−50	−200		−50	−200	μA
Supply Current	All Digital Inputs High		0.2	1.6		0.2	1.6	mA
	All Digital Inputs Low		0.6	2		0.6	2	mA
Operating Power Supply Range	*(Figures 1 and 2)*	5		15	5		15	V

Note 1: $V_{REF} = \pm 10V$ and $V_{REF} = \pm 1V$. A linearity error temperature coefficient of 0.0002% FS for a 45°C rise only guarantees 0.009% maximum change in linearity error. For instance, if the linearity error at 25°C is 0.045% FS it could increase to 0.054% at 70°C and the DAC will be no longer a 10-bit part. Note, however, that the linearity error is specified over the device full temperature range which is a more stringent specification since *it includes* the linearity error temperature coefficient.

Note 2: Using internal feedback resistor as shown in *Figure 3*.

Note 3: Both $I_{OUT\ 1}$ and $I_{OUT\ 2}$ must go to ground or the virtual ground of an operational amplifier. If $V_{REF} = 10V$, every millivolt offset between $I_{OUT\ 1}$ or $I_{OUT\ 2}$, 0.005% linearity error will be introduced.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 6: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temepature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the J18 package when board mounted is 85°C/W. For the J16 package, this number increases to 90°C/W, for the N18 package, θ_{JA} is 120°C/W, and for the N16 this number is 125°C/W.

Typical Performance Characteristics

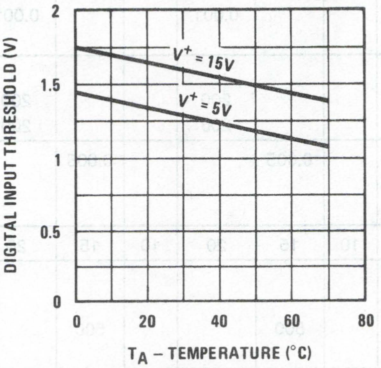
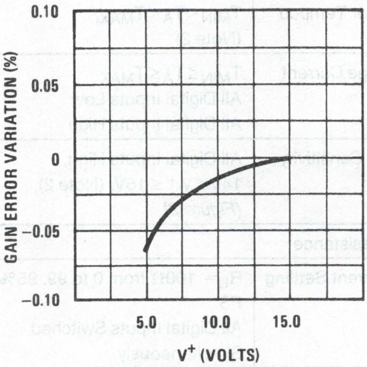


FIGURE 1. Digital Input Threshold vs Ambient Temperature



TL/H/5689-2

FIGURE 2. Gain Error Variation vs V^+

Typical Applications

The following applications are also valid for 12-bit systems using the DAC1220 and 2 additional digital inputs.

Operational Amplifier Bias Current (*Figure 3*)

The op amp bias current, I_b, flows through the 15k internal feedback resistor. BI-FET op amps have low I_b and, therefore, the 15k × I_b error they introduce is negligible; they are strongly recommended for the DAC1020 applications.

V_{OS} Considerations

The output impedance, R_{OUT}, of the DAC is modulated by the digital input code which causes a modulation of the operational amplifier output offset. It is therefore recommended to adjust the op amp V_{OS}. R_{OUT} is ~15k if more than 4 digital inputs are high; R_{OUT} is ~45k if a single digital input is high, and R_{OUT} approaches infinity if all inputs are low.

Operational Amplifier V_{OS} Adjust (*Figure 3*)

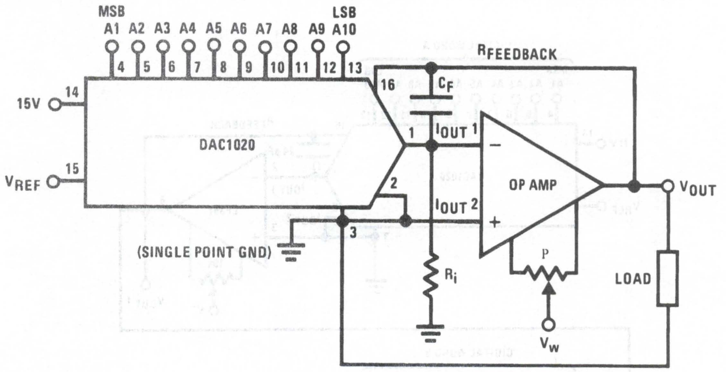
Connect all digital inputs, A1–A10, to ground and adjust the potentiometer to bring the op amp V_{OUT} pin to within ±1 mV from ground potential. If V_{REF} is less than 10V, a finer V_{OS} adjustment is required. It is helpful to increase the resolution of the V_{OS} adjust procedure by connecting a 1 kΩ resistor between the inverting input of the op amp to ground. After V_{OS} has been adjusted, remove the 1 kΩ.

Full-Scale Adjust (*Figure 4*)

Switch high all the digital inputs, A1–A10, and measure the op amp output voltage. Use a 500Ω potentiometer, as shown, to bring $\|V_{OUT}\|$ to a voltage equal to $V_{REF} \times 1023/1024$.

SELECTING AND COMPENSATING THE OPERATIONAL AMPLIFIER

Op Amp Family	C_F	R_i	P	V_W	Circuit Settling Time, t_s	Circuit Small Signal BW
LF357	10 pF	2.4k	25k	V^+	1.5 μs	1M
LF356	22 pF	∞	25k	V^+	3 μs	0.5M
LF351	24 pF	∞	10k	V^-	4 μs	0.5M
LM741	0	∞	10k	V^-	40 μs	200 kHz



TL/H/5689-3

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

$$-10V \le V_{REF} \le 10V$$

$$0 \le V_{OUT} \le -\frac{1023}{1024} V_{REF}$$

where A_N = 1 if the A_N digital input is high

A_N = 0 if the A_N digital input is low

FIGURE 3. Basic Connection: Unipolar or 2-Quadrant Multiplying Configuration (Digital Attenuator)

Typical Applications (Continued)

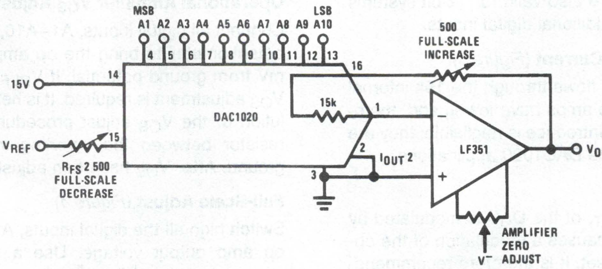

MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
500
FULL-SCALE
INCREASE
16
14
15V
15k
DAC1020
1
15
VREF
RFS 2 500
FULL-SCALE
DECREASE
2
IOUT 2
3
LF351
VOUT
AMPLIFIER
ZERO
ADJUST
V−

FIGURE 4. Full-Scale Adjust

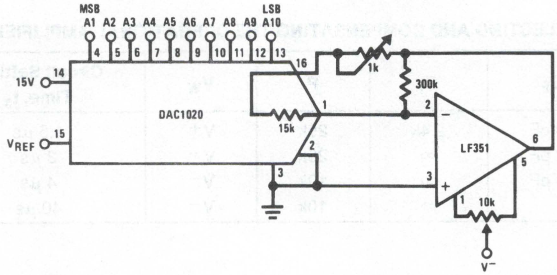
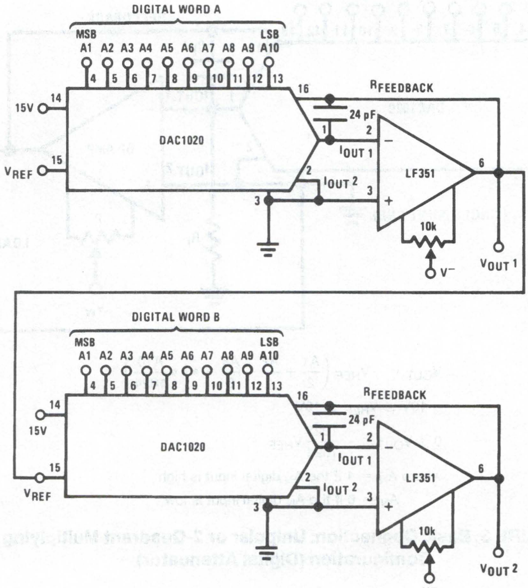

MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
16
1k
14
15V
300k
DAC1020
2
1
15k
6
LF351
15
VREF
2
5
3
3
1
10k
V−

FIGURE 5. Alternate Full-Scale Adjust: (Allows Increasing or Decreasing the Gain)


DIGITAL WORD A
MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
16
RFEEDBACK
14
15V
24 pF
DAC1020
1
2
IOUT 1
15
VREF
2
IOUT 2
6
LF351
3
3
10k
V−
VOUT 1
DIGITAL WORD B
MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
16
RFEEDBACK
14
15V
24 pF
DAC1020
1
2
IOUT 1
15
VREF
2
IOUT 2
6
LF351
3
3
10k
V−
VOUT 2

TL/H/5689-4

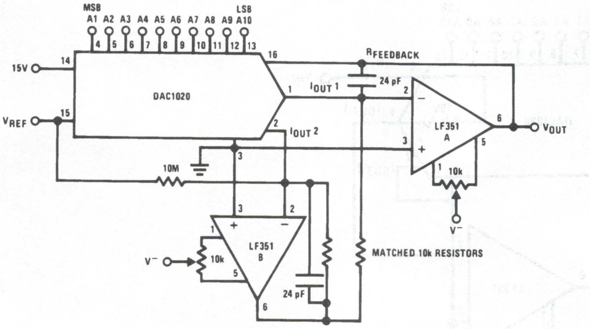
$$V_{OUT\,1} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

$$V_{OUT2} = V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right) \times \left(\frac{B1}{2} + \frac{B2}{4} + \frac{B3}{8} + \cdots \frac{B10}{1024}\right)$$

where V_{REF} can be an AC signal

FIGURE 6. Precision Analog-to-Digital Multiplier

Typical Applications (Continued)


MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
15V
14
16
$R_{FEEDBACK}$
DAC1020
V_{REF}
15
1
$I_{OUT\,1}$
24 pF
2
LF351
A
6
V_{OUT}
2
$I_{OUT\,2}$
3
5
10M
3
1
10k
V^-
3
2
1
LF351
B
V^-
10k
5
6
24 pF
MATCHED 10k RESISTORS

TL/H/5689-5

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \bullet\bullet\bullet + \frac{A10}{1024} - \frac{1}{1024}\right)$$

where: AN = +1 if A_N input is high

AN = −1 if A_N input is low

COMPLEMENTARY OFFSET BINARY (BIPOLAR) OPERATION

DIGITAL INPUT	V_{OUT}
0 0 0 0 0 0 0 0 0 0	$+V_{REF}$
0 0 0 0 0 0 0 0 0 1	$V_{REF} \times 1022/1024$
0 1 1 1 1 1 1 1 1 1	$V_{REF} \times 2/1024$
1 0 0 0 0 0 0 0 0 0	0
1 0 0 0 0 0 0 0 0 1	$-V_{REF} \times 2/1024$
1 1 1 1 1 1 1 1 1 1	$-V_{REF}$ (1022/1024)

Note that:

- $I_{OUT\,1} + I_{OUT\,2} = \frac{V_{REF}}{R_{LADDER}} \times \left(\frac{1023}{1024}\right)$
- By doubling the output range we get half the resolution
- The 10M resistor, adds a 1 LSB "thump", to allow full offset binary operation where the output reaches zero for the half-scale code. If symmetrical output excursions are required, omit the 10M resistor.

FIGURE 7. Bipolar 4-Quadrant Multiplying Configuration

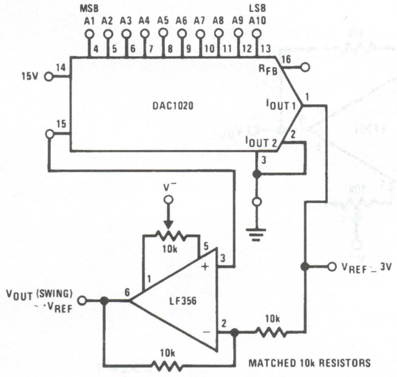
Operational Amplifiers V_{OS} Adjust (*Figure 7*)

a) Switch all the digital inputs high; adjust the V_{OS} potentiometer of op amp B to bring its output to a value equal to $-(V_{REF}/1024)$ (V).

b) Switch the MSB high and the remaining digital inputs low. Adjust the V_{OS} potentiometer of op amp A, to bring its output value to within a 1 mV from ground potential. For $V_{REF} < 10V$, a finer adjust is necessary, as already mentioned in the previous application.

Gain Adjust (Full-Scale Adjust)

Assuming that the external 10k resistors are matched to better than 0.1%, the gain adjust of the circuit is the same with the one previously discussed.


MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
15V
14
R_{FB}
16
DAC1020
$I_{OUT\,1}$
1
15
$I_{OUT\,2}$
2
3
V^-
10k
5
3
1
$V_{REF} \geq 3V$
V_{OUT} (SWING) ≈ $\pm V_{REF}$
6
LF356
2
10k
10k
MATCHED 10k RESISTORS

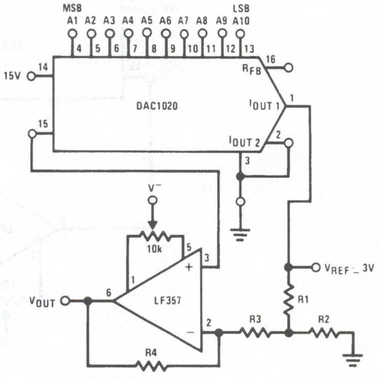
TRUE OFFSET BINARY OPERATION

DIGITAL INPUT	V_{OUT}
1 1 1 1 1 1 1 1 1 1	$V_{REF} \times 1022/1024$
1 0 0 0 0 0 0 0 0 0	0
0 0 0 0 0 0 0 0 0 0	$-V_{REF}$

$t_s = 1.8\ \mu s$

use LM336 for a voltage reference

FIGURE 8. Bipolar Configuration with a Single Op Amp


MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
15V
14
R_{FB}
16
DAC1020
$I_{OUT\,1}$
1
15
$I_{OUT\,2}$
2
3
V^-
10k
5
3
1
$V_{REF} \geq 3V$
R1
V_{OUT}
6
LF357
2
R3
R2
R4

TL/H/5689-6

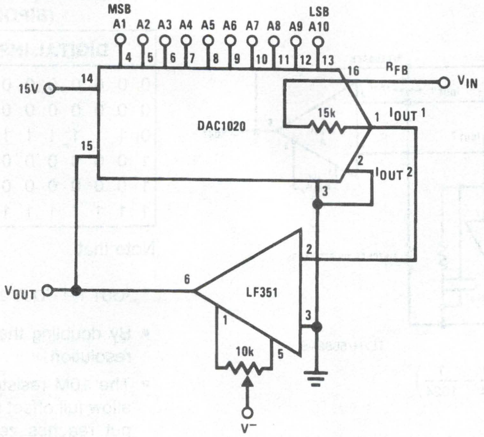
- $R4 = (2A_V^- - 1)\,R,\ \frac{R2}{R1} = \frac{A_V^-}{A_V^- - 1},$

  $R3 + R1 \| R2 = R;\ A_V^- = \frac{V_{OUT(PEAK)}}{V_{REF}},\ R = 20k$
- Example: $V_{REF} = 2V$, V_{OUT} (swing) $\cong \pm 10V$: $A_V^- = 5V$

  Then $R4 = 9R$, $R1 = 0.8\ R2$. If $R1 = 0.2R$ then $R2 = 0.25R$, $R3 = 0.64R$

FIGURE 9. Bipolar Configuration with Increased Output Swing

Typical Applications (Continued)

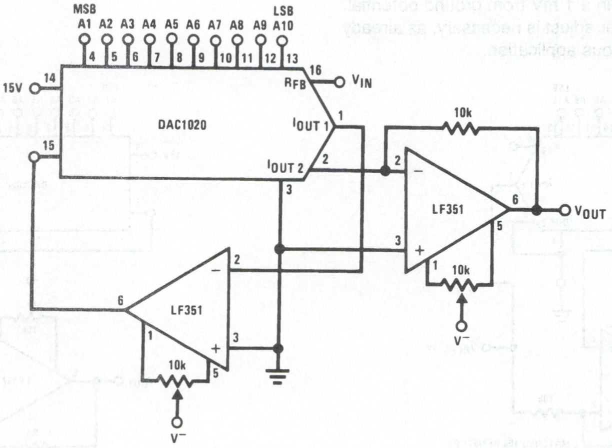

MSB
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
LSB
4
5
6
7
8
9
10
11
12
13
16
RFB
VIN
15V
14
DAC1020
15k
1
IOUT 1
15
2
IOUT 2
3
2
VOUT
6
LF351
1
3
10k
5
V−

$$V_{OUT} = \frac{-V_{REF}}{\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right)}$$

where: V_{REF} can be an AC signal

- By connecting the DAC in the feedback loop of an operational amplifier a linear digitally control gain block can be realized
- Note that with all digital inputs low, the gain of the amplifier is infinity, that is, the op amp will saturate. In other words, we cannot divide the V_{REF} by zero!

FIGURE 10. Analog-to-Digital Divider (or Digitally Gain Controlled Amplifier)


MSB
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
LSB
4
5
6
7
8
9
10
11
12
13
16
RFB
VIN
15V
14
DAC1020
IOUT 1
1
15
IOUT 2
2
3
10k
2
−
LF351
6
VOUT
5
3
+
1
10k
V−
2
−
6
LF351
1
3
+
10k
5
V−
TL/H/5689-7

$$V_{OUT} = V_{REF}\left[\frac{\frac{\overline{A1}}{2} + \frac{\overline{A2}}{4} + \ldots + \frac{\overline{A10}}{1024}}{\frac{A1}{2} + \frac{A2}{4} + \ldots + \frac{A10}{1024}}\right] \text{ or } V_{OUT} = V_{REF}\left(\frac{1023 - N}{N}\right)$$

where: $0 \le N \le 1023$

$N = 0$ for A_N = all zeros

$N = 1$ for $A10 = 1$, $A1–A9 = 0$

.

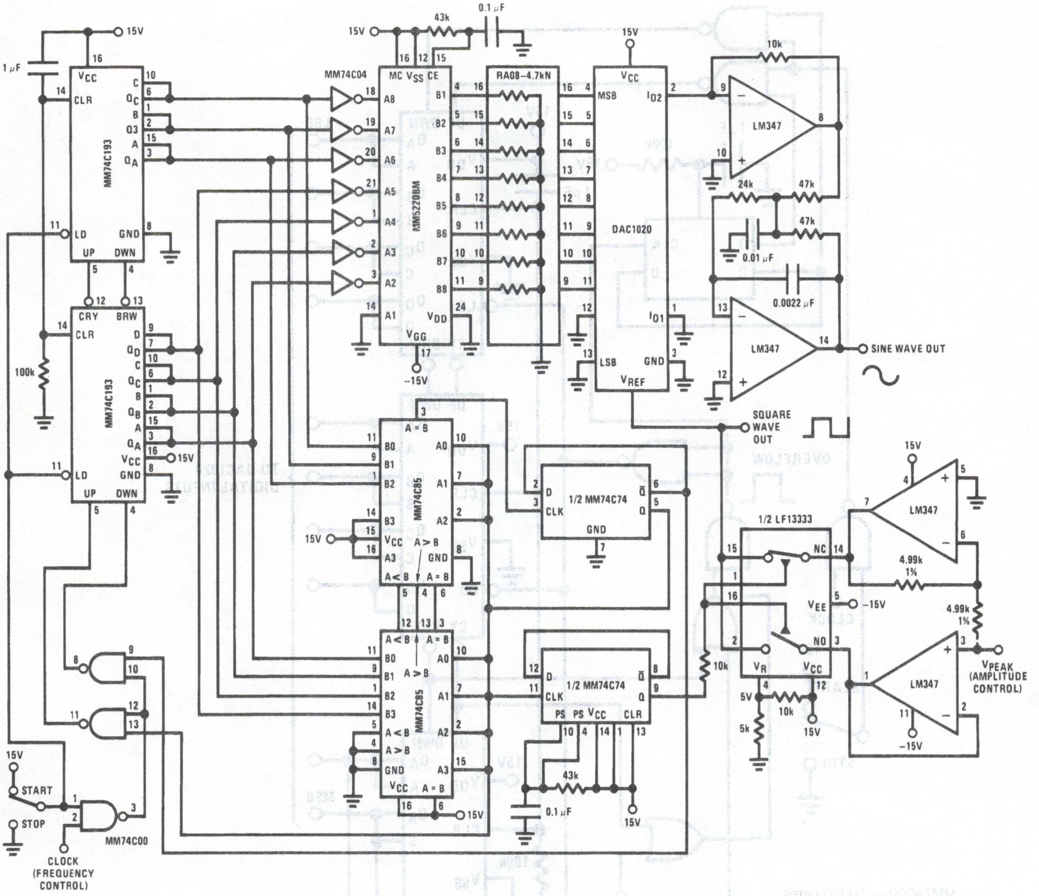
.

.

$N = 1023$ for A_N = all 1's

FIGURE 11. Digitally controlled Amplifier-Attenuator

Typical Applications (Continued)

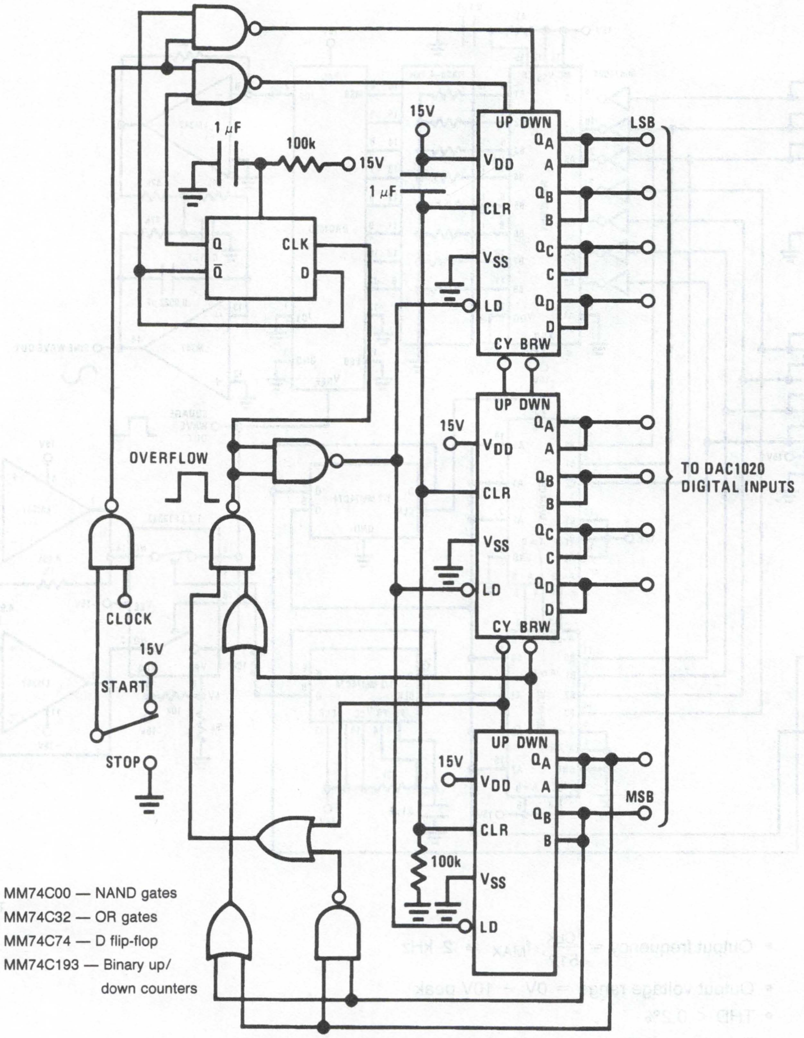

15V
1 μF
16
14
VCC
CLR
C
QC
B
Q3
A
QA
MM74C193
11
LD
GND
UP
DWN
5
4
12
13
CRY
BRW
CLR
D
QD
C
QC
B
QB
A
QA
VCC
GND
15V
100k
MM74C193
5
4
43k
0.1 μF
MM74C04
MC VSS CE
A8
A7
A6
A5
A4
A3
A2
A1
B1
B2
B3
B4
B5
B6
B7
B8
MM5220BM
VGG
VDD
-15V
RA08-4.7kN
VCC
MSB
IO2
IO1
DAC1020
LSB
GND
VREF
10k
LM347
24k
47k
47k
0.01 μF
0.0022 μF
LM347
SINE WAVE OUT
SQUARE WAVE OUT
A = B
B0
B1
B2
B3
VCC
A3
A < B
A0
A1
A2
A > B
GND
A = B
MM74C85
1/2 MM74C74
D
CLK
Q̄
Q
GND
A < B
A = B
B0
B1
B2
B3
A < B
A > B
GND
VCC
A0
A1
A2
A3
A = B
MM74C85
1/2 MM74C74
D
CLK
PS
PS
VCC
CLR
Q̄
Q
43k
0.1 μF
1/2 LF13333
NC
VEE
-15V
NO
VR
VCC
10k
5V
10k
5k
LM347
4.99k 1%
4.99k 1%
LM347
VPEAK (AMPLITUDE CONTROL)
-15V
START
STOP
MM74C00
CLOCK (FREQUENCY CONTROL)

TL/H/5689-8

- Output frequency $= \frac{f_{CLK}}{512}$; $f_{MAX} \cong 2$ kHz
- Output voltage range = 0V – 10V peak
- THD < 0.2%
- Excellent amplitude and frequency stability with temperature
- Low pass filter shown has a 1 kHz corner (for output frequencies below 10 Hz, filter corner should be reduced)
- Any periodic function can be implemented by modifying the contents of the look up table ROM
- No start up problems

FIGURE 12. Precision Low Frequency Sine Wave Oscillator Using Sine Look-Up ROM

Typical Applications (Continued)


1 µF
100k
15V
15V
1 µF
Q
Q̄
CLK
D
UP DWN
VDD
CLR
VSS
LD
QA
A
QB
B
QC
C
QD
D
CY BRW
LSB
15V
OVERFLOW
CLOCK
15V
START
STOP
15V
100k
MSB
TO DAC1020 DIGITAL INPUTS
MM74C00 — NAND gates
MM74C32 — OR gates
MM74C74 — D flip-flop
MM74C193 — Binary up/ down counters

TL/H/5689-9

- Binary up/down counter digitally "ramps" the DAC output
- Can stop counting at any desired 10-bit input code
- Senses up or down count overflow and automatically reverses direction of count

FIGURE 13. A Useful Digital Input Code Generator for DAC Attenuator or Amplifier Circuits

Definition of Terms

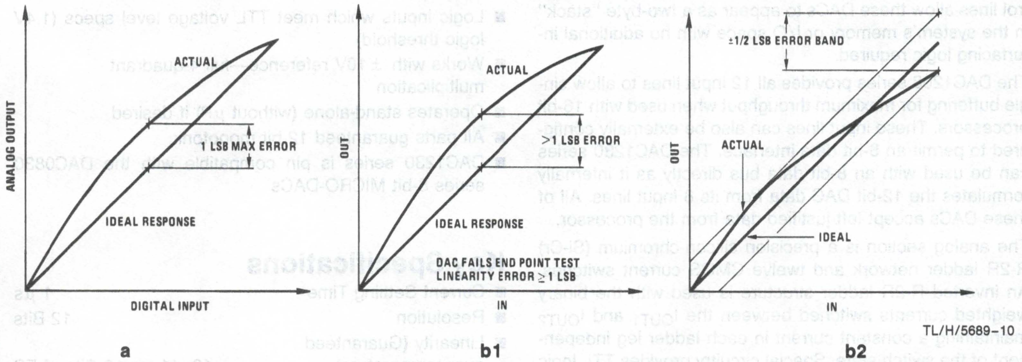
Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the D/A output. It is directly related to the number of switches or bits within the D/A. For example, the DAC1020 has 2^{10} or 1024 steps while the DAC1220 has 2^{12} or 4096 steps. Therefore, the DAC1020 has 10-bit resolution, while the DAC1220 has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from *a straight line passing through the endpoints of the D/A transfer characteristic.* It is measured after calibrating for zero (see V_{OS} adjust in typical applications) and full-scale. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time: Full-scale settling time requires a zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the D/A output reaches within ±½ LSB of final output value.

Full-Scale Error: Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1020 full-scale is $V_{REF}-1$ LSB. For $V_{REF}=10V$ and unipolar operation, $V_{FULL\text{-}SCALE}=10.0000V-9.8\ mV=9.9902V$. Full-scale error is adjustable to zero as shown in *Figure 5*.

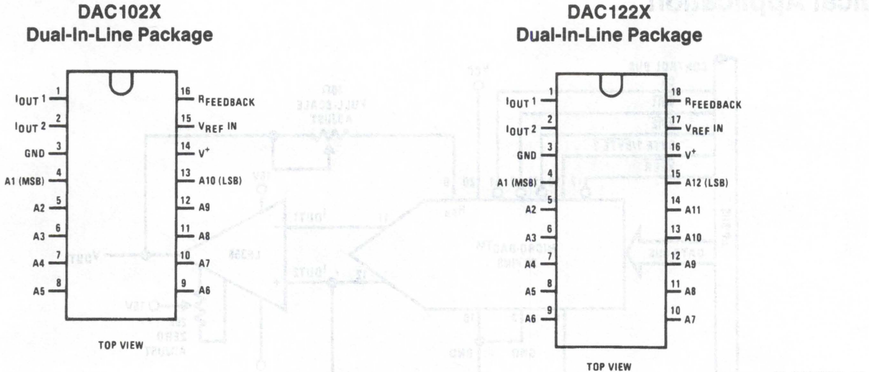


(a) End point test after zero and full-scale adjust. The DAC has 1 LSB linearity error.

(b) By shifting the full-scale calibration on of the DAC of *Figure (b1)* we could pass the "best straight line" (b2) test and meet the ±½ linearity error specification.

Note. (a), (b1) and (b2) above illustrate the difference between "end point" National's linearity test (a) and "best straight line" test. Note that both devices in (a) and (b2) meet the ±½ LSB linearity error specification but the end point test is a more "real life" way of characterizing the DAC.

Connection Diagrams


DAC102X
Dual-In-Line Package
$I_{OUT}1$ 1
$I_{OUT}2$ 2
GND 3
A1 (MSB) 4
A2 5
A3 6
A4 7
A5 8
9 A6
10 A7
11 A8
12 A9
13 A10 (LSB)
14 V+
15 V_{REF} IN
16 $R_{FEEDBACK}$
TOP VIEW
DAC122X
Dual-In-Line Package
$I_{OUT}1$ 1
$I_{OUT}2$ 2
GND 3
A1 (MSB) 4
A2 5
A3 6
A4 7
A5 8
A6 9
10 A7
11 A8
12 A9
13 A10
14 A11
15 A12 (LSB)
16 V+
17 V_{REF} IN
18 $R_{FEEDBACK}$
TOP VIEW
TL/H/5689-11

National
Semiconductor
Corporation

MICRO-DAC™ DAC1208, DAC1209, DAC1210, DAC1230, DAC1231, DAC1232 12-Bit, µP Compatible, Double-Buffered D to A Converters

General Description

The DAC1208 and the DAC1230 series are 12-bit multiplying D to A converters designed to interface directly with a wide variety of microprocessors (8080, 8048, 8085, Z-80, etc.). Double buffering input registers and associated control lines allow these DACs to appear as a two-byte "stack" in the system's memory or I/O space with no additional interfacing logic required.

The DAC1208 series provides all 12 input lines to allow single buffering for maximum throughput when used with 16-bit processors. These input lines can also be externally configured to permit an 8-bit data interface. The DAC1230 series can be used with an 8-bit data bus directly as it internally formulates the 12-bit DAC data from its 8 input lines. All of these DACs accept left-justified data from the processor.

The analog section is a precision silicon-chromium (Si-Cr) R-2R ladder network and twelve CMOS current switches. An inverted R-2R ladder structure is used with the binary weighted currents switched between the I_{OUT1} and I_{OUT2} maintaining a constant current in each ladder leg independent of the switch state. Special circuitry provides TTL logic input voltage level compatibility.

The DAC1208 series and DAC1230 series are the 12-bit members of a family of microprocessor compatible DACs (MICRO-DACs™). For applications requiring other resolutions, the DAC1000 series for 10-bit and DAC0830 series for 8-bit are available alternatives.

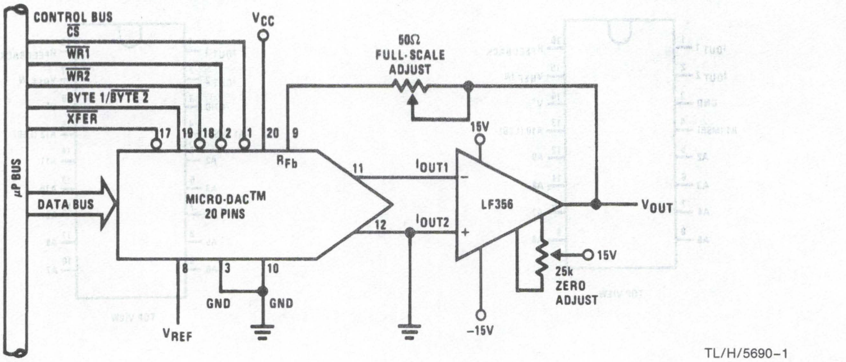
Features

- Linearity specified with zero and full-scale adjust only
- Direct interface to all popular microprocessors
- Double-buffered, single-buffered or flow through digital data inputs
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- Operates stand-alone (without µP) if desired
- All parts guaranteed 12-bit monotonic
- DAC1230 series is pin compatible with the DAC0830 series 8-bit MICRO-DACs

Key Specifications

■ Current Settling Time	1 µs
■ Resolution	12 Bits
■ Linearity (Guaranteed over temperature)	10, 11, or 12 Bits of FS
■ Gain Tempco	1.3 ppm/°C
■ Low Power Dissipation	20 mW
■ Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



TL/H/5690–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$ (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
ESD Susceptability	800V

Operating Conditions

Lead Temperature (Soldering, 10 seconds)	300°C
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
DAC1208LCJ, DAC1209LCJ, DAC1210LCJ, DAC1230LCJ, DAC1231LCJ, DAC1232LCJ	$-40°C \leq T_A \leq +85°C$
DAC1208LCJ-1, DAC1209LCJ-1, DAC1210LCJ-1, DAC1230LCJ-1, DAC1231LCJ-1, DAC1232LCJ-1	$0°C \leq T_A \leq +70°C$
Range of V_{CC}	4.75 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

$V_{REF} = 10.000$ V_{DC}, $V_{CC} = 11.4$ V_{DC} to 15.75 V_{DC} unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 13);** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	Notes	Typ (Note 10)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
Resolution			12	**12**	**12**	Bits
Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted DAC1208, DAC1230 DAC1209, DAC1231 DAC1210, DAC1232	4, 7, 13		 **0.012** **0.024** **0.050**	 **0.012** **0.024** **0.05**	 % of FSR % of FSR % of FSR
Differential Non-Linearity	Zero and Full-Scale Adjusted DAC1208, DAC1230 DAC1209, DAC1231 DAC1210, DAC1232	4, 7, 13		 **0.018** **0.024** **0.050**	 **0.018** **0.024** **0.05**	 % of FSR % of FSR % of FSR
Monotonicity		4	12	**12**	**12**	Bits
Gain Error (Min)	Using Internal R_{Fb} $V_{ref} = \pm 10V, \pm 1V$	7	−0.1	0.0		% of FSR
Gain Error (Max)		7	−0.1	−0.2		% of FSR
Gain Error Tempco		7	±1.3		**±6.0**	ppm of FS/°C
Power Supply Rejection	All Digital Inputs Latched High	7	±3.0	±30		ppm of FSR/V
Reference Input Resistance (Min)		13	15	**10**	**10**	kΩ
Reference Input Resistance (Max)			15	**20**	**20**	
Output Feedthrough Error	$V_{REF} = 20$ Vp-p, f = 100 kHz All Data Inputs Latched Low	9	3.0			mVp-p
Output Capacitance	All Data Inputs Latched High I_{OUT1} All Data Inputs Latched High I_{OUT2} All Data Inputs Latched Low I_{OUT1} All Data Inputs Latched Low I_{OUT2}				200 70 70 200	pF pF pF pF
Supply Current Drain		13		2.0	**2.5**	mA
Output Leakage Current I_{OUT1}	All Data Inputs Latched Low	11, 13	0.1	**15**	**15**	nA
I_{OUT2}	All Data Inputs Latched High	11, 13	0.1	**15**	**15**	nA
Digital Input Threshold	Low Threshold High Threshold	13 13		**0.8** **2.2**	**0.8** **2.2**	V_{DC} V_{DC}
Digital Input Currents	Digital Inputs <0.8V Digital Inputs >2.2V	13 13		**−200** **10**	**−200** **10**	μA_{DC} μA_{DC}

Electrical Characteristics (Continued)

V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 13);** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	See Note	Typ (Note 10)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
AC CHARACTERISTICS							
t_S	Current Setting Time	V_{IL} = 0V, V_{IH} = 5V		1.0			µs
t_W	Write and XFER Pulse Width Min.	V_{IL} = 0V, V_{IH} = 5V	8	50		320 **320**	ns
t_{DS}	Data Setup Time Min.	V_{IL} = 0V, V_{IH} = 5V		70		320 **320**	
t_{DH}	Data Hold Time Min.	V_{IL} = 0V, V_{IH} = 5V		30		90 **90**	
t_{CS}	Control Setup Time Min.	V_{IL} = 0V, V_{IH} = 5V		60		320 **320**	
t_{CH}	Control Hold Time Min.	V_{IL} = 0V, V_{IH} = 5V		0		10	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if V_{REF} = 10V then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels. Guaranteed for V_{CC} = 11.4V to 15.75V and V_{REF} = −10V to +10V.

Note 7: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1208 is 0.012% of FSR(max). This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% × V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR(parts per million of full-scale range) and ppm of FS(parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. In this instance, 1 ppm of FSR = $V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ±6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from −40°C to +85°C of $\pm(6)(V_{REF}/10^6)(125°C)$ or $\pm 0.75\ (10^{-3})\ V_{REF}$ which is $\pm 0.075\%$ of V_{REF}.

Note 8: This spec implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH} and t_S to apply.

Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 10: Typicals are at 25°C and represent the most likely parametric norm.

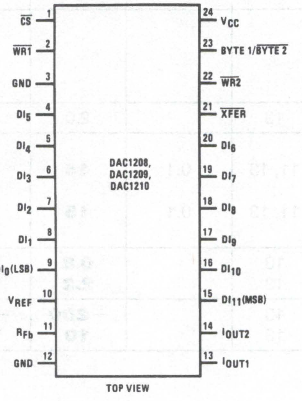
Note 11: A 10 nA leakage current with R_{Fb} = 20k and V_{REF} = 10V corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

Note 12: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

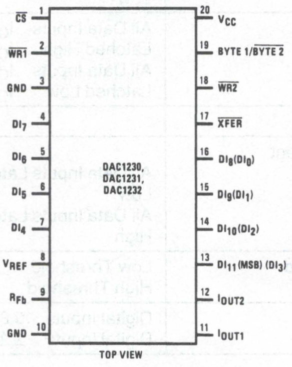
Note 13: Tested limit for −1 suffix parts applies only at 25°C.

Connection Diagrams

Dual-In-Line Package



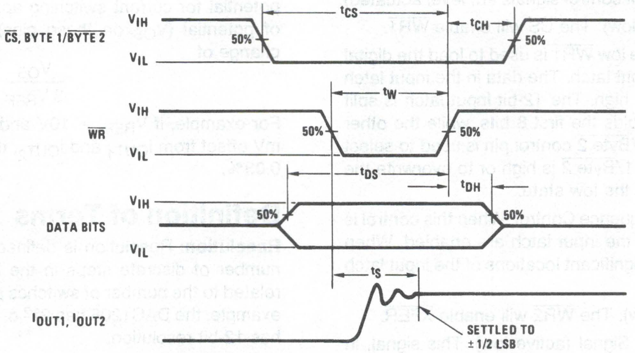
Dual-In-Line Package



TL/H/5690–2

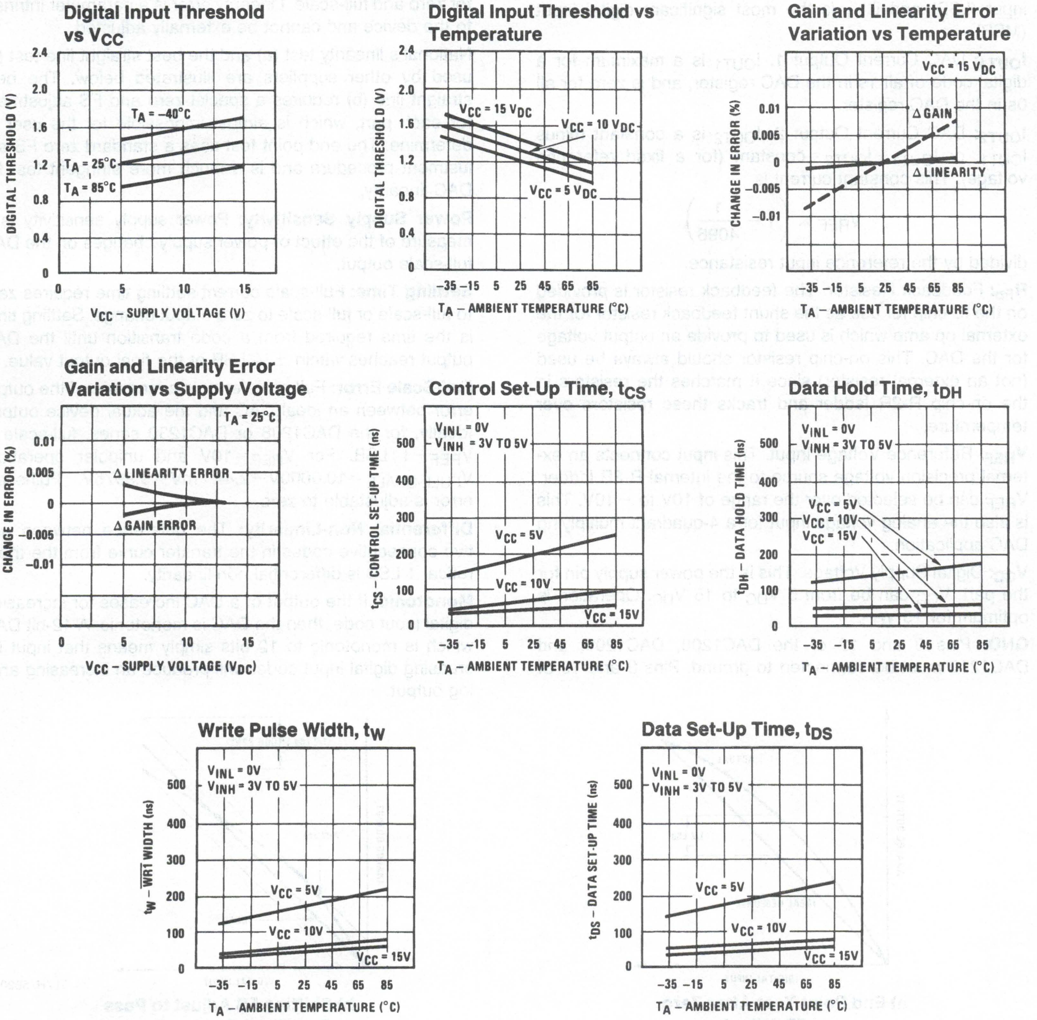
See Ordering Information

Switching Waveforms


CS, BYTE 1/BYTE 2
WR
DATA BITS
IOUT1, IOUT2
VIH
VIL
50%
tCS
tCH
tW
tDS
tDH
tS
SETTLED TO ± 1/2 LSB

TL/H/5690-3

Typical Performance Characteristics



TL/H/5690-4

Definition of Package Pinouts

CONTROL SIGNALS (all control signals are level actuated)

$\overline{\text{CS}}$: Chip Select (active low). The $\overline{\text{CS}}$ will enable $\overline{\text{WR1}}$.

$\overline{\text{WR1}}$: Write 1. The active low $\overline{\text{WR1}}$ is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{\text{WR1}}$ is high. The 12-bit input latch is split into two latches. One holds the first 8 bits, while the other holds 4 bits. The Byte 1/$\overline{\text{Byte 2}}$ control pin is used to select both latches when Byte 1/$\overline{\text{Byte 2}}$ is high or to overwrite the 4-bit input latch when in the low state.

Byte 1/$\overline{\text{Byte 2}}$: Byte Sequence Control. When this control is high, all 12 locations of the input latch are enabled. When low, only the four least significant locations of the input latch are enabled.

$\overline{\text{WR2}}$: Write 2 (active low). The $\overline{\text{WR2}}$ will enable $\overline{\text{XFER}}$.

$\overline{\text{XFER}}$: Transfer Control Signal (active low). This signal, in combination with $\overline{\text{WR2}}$, causes the 12-bit data which is available in the input latches to transfer to the DAC register.

DI_0 to DI_{11}: Digital Inputs. DI_0 is the least significant digital input (LSB) and DI_{11} is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital code of all 1s in the DAC register, and is zero for all 0s in the DAC register.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1}+I_{OUT2}=\text{constant}$ (for a fixed reference voltage). This constant current is

$$V_{REF} \times \left(1 - \frac{1}{4096}\right)$$

divided by the reference input resistance.

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Pins 3 and 12 of the DAC1208, DAC1209, and DAC1210 must be connected to ground. Pins 3 and 10 of the DAC1230, DAC1231, and DAC1232 must be connected to ground. It is important that I_{OUT_1} and I_{OUT_2} are at ground potential for current switching applications. Any difference of potential (V_{OS} on these pins) will result in a linearity change of

$$\frac{V_{OS}}{3\,V_{REF}}$$

For example, if $V_{REF} = 10V$ and these ground pins are 9 mV offset from I_{OUT_1} and I_{OUT_2}, the linearity change will be 0.03%.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1208 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

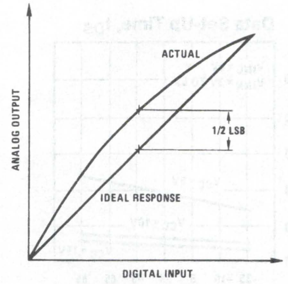
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ±½ LSB of the final output value.

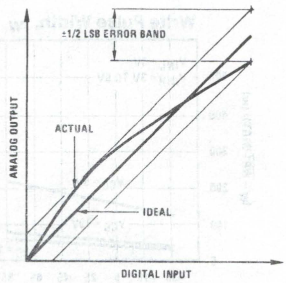
Full-Scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1208 or DAC1230 series, full-scale is $V_{REF}-1$ LSB. For $V_{REF}=10V$ and unipolar operation, $V_{FULL\text{-}SCALE}=10.0000V-2.44\ mV=9.9976V$. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End Point Test After Zero and FS Adjust



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b) Shifting FS Adjust to Pass Best Straight Line Test

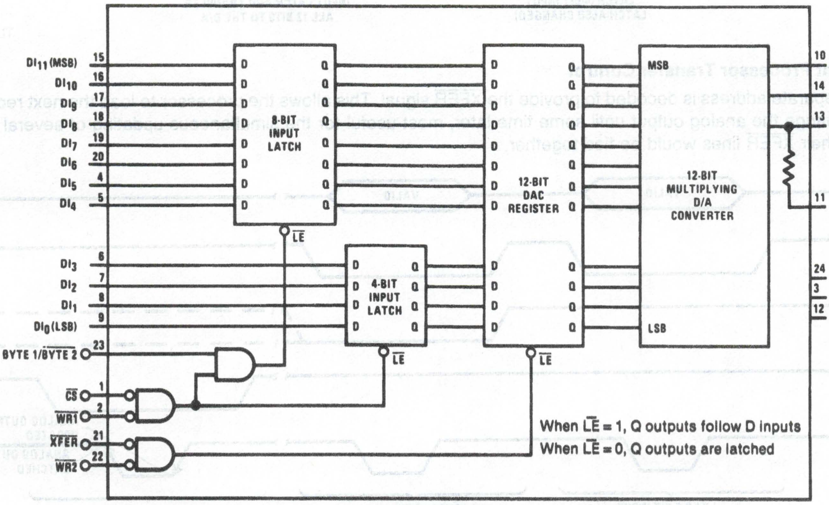
Application Hints

1.0 DIGITAL INTERFACE

These DACs are designed to provide all of the necessary digital input circuitry to permit a direct interface to a wide variety of microprocessor systems. The timing and logic level convention of the input control signals allow the DACs to be treated as a typical memory device or I/O peripheral with no external logic required in most systems. Essentially these DACs can be mapped as a two-byte stack in memory (or I/O space) to receive their 12 bits of input data in two successive 8-bit data writing sequences. The DAC1230 series is intended for use in systems with an 8-bit data bus. The DAC1208 series provides all 12 digital input lines which can be externally configured to be controlled from an 8-bit bus or can be driven directly from a 16-bit data bus.

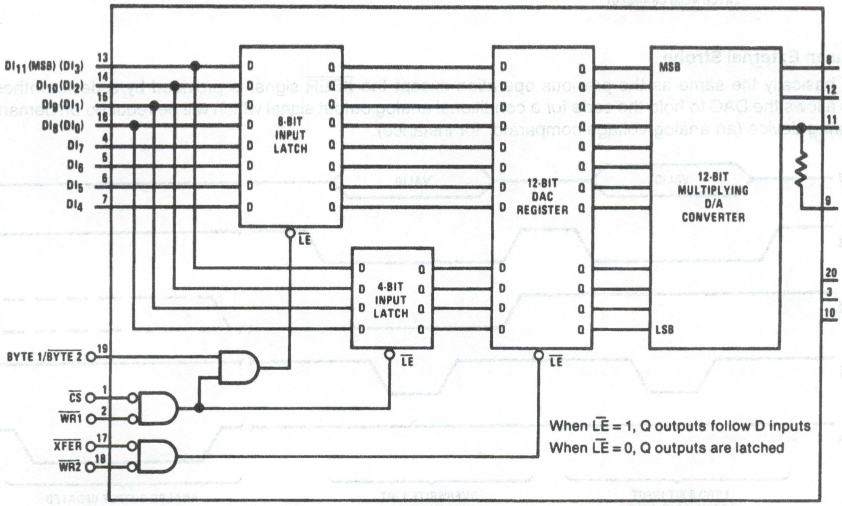
All of the digital inputs to these DACs contain a unique threshold regulator circuit to maintain TTL voltage level compatibility independent of the applied V_{CC} to the DAC. Any input can also be driven from higher voltage CMOS logic levels in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. As a troubleshooting aid, if any digital input is inadvertently left floating, the DAC will interpret the pin as a logic "1".

Double buffered digital inputs allow the DAC to internally format the 12-bit word used to set the current switching R-2R ladder network (see section 2.0) from two 8-bit data write cycles. *Figures 1* and *2* show the internal data registers and their controlling logic circuitry. The timing diagrams for updating the DAC output are shown in sections 1.1, 1.2 and 1.3 for three possible control modes. The method used depends strictly upon the particular application.



DI11 (MSB)
DI10
DI9
DI8
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0 (LSB)
BYTE 1/BYTE 2
CS
WR1
XFER
WR2
15
16
17
18
19
20
4
5
6
7
8
9
23
1
2
21
22
8-BIT INPUT LATCH
4-BIT INPUT LATCH
12-BIT DAC REGISTER
12-BIT MULTIPLYING D/A CONVERTER
D
Q
LE
MSB
LSB
10
VREF
14
IOUT2
13
IOUT1
11
RFb
24
VCC
3
GND
12
GND
When LE = 1, Q outputs follow D inputs
When LE = 0, Q outputs are latched

FIGURE 1. DAC1208, DAC1209, DAC1210 Functional Diagram



DI11 (MSB) (DI3)
DI10 (DI2)
DI9 (DI1)
DI8 (DI0)
DI7
DI6
DI5
DI4
BYTE 1/BYTE 2
CS
WR1
XFER
WR2
13
14
15
16
4
5
6
7
19
1
2
17
18
8-BIT INPUT LATCH
4-BIT INPUT LATCH
12-BIT DAC REGISTER
12-BIT MULTIPLYING D/A CONVERTER
D
Q
LE
MSB
LSB
8
VREF
12
IOUT2
11
IOUT1
9
RFb
20
VCC
3
GND
10
GND
When LE = 1, Q outputs follow D inputs
When LE = 0, Q outputs are latched

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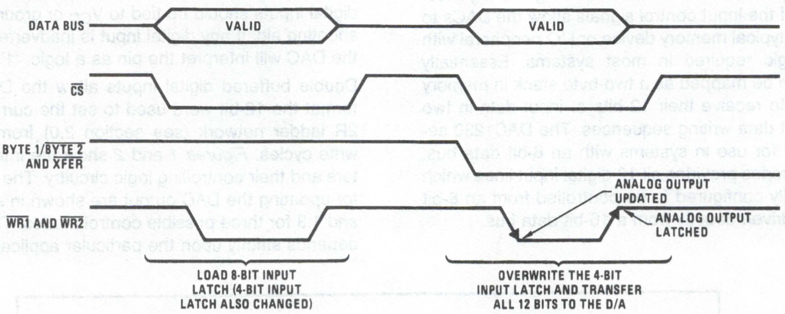
FIGURE 2. DAC1230, DAC1231, DAC1232 Functional Diagram

Application Hints (Continued)

1.1 Automatic Transfer

The 12-bit DAC word is automatically transferred to the DAC register and the R-2R ladder when the second write (the 4 LSBs of the data) occurs.


DATA BUS
VALID
VALID
$\overline{\text{CS}}$
BYTE 1/$\overline{\text{BYTE 2}}$ AND XFER
$\overline{\text{WR1}}$ AND $\overline{\text{WR2}}$
ANALOG OUTPUT UPDATED
ANALOG OUTPUT LATCHED
LOAD 8-BIT INPUT LATCH (4-BIT INPUT LATCH ALSO CHANGED)
OVERWRITE THE 4-BIT INPUT LATCH AND TRANSFER ALL 12 BITS TO THE D/A

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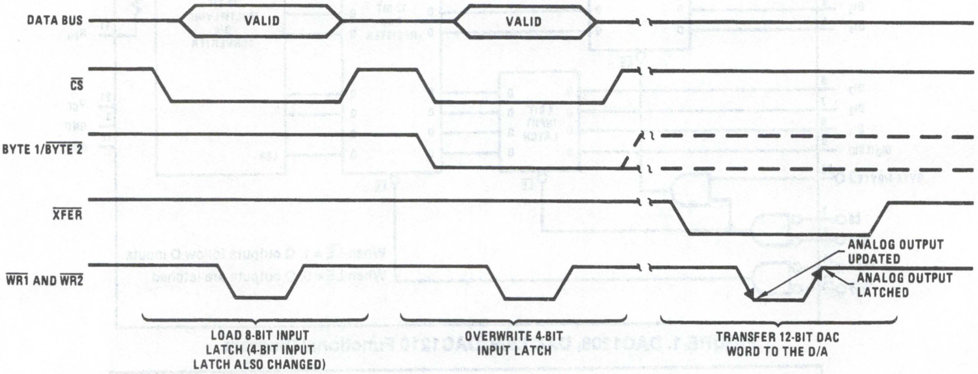
1.2 Independent Processor Transfer Control

In this case a separate address is decoded to provide the $\overline{\text{XFER}}$ signal. This allows the processor to load the next required DAC word but not change the analog output until some time later, most useful for the simultaneous updating of several DACs in a system where their $\overline{\text{XFER}}$ lines would be tied together.


DATA BUS
VALID
VALID
$\overline{\text{CS}}$
BYTE 1/$\overline{\text{BYTE 2}}$
$\overline{\text{XFER}}$
$\overline{\text{WR1}}$ AND $\overline{\text{WR2}}$
ANALOG OUTPUT UPDATED
ANALOG OUTPUT LATCHED
LOAD 8-BIT INPUT LATCH (4-BIT INPUT LATCH ALSO CHANGED)
OVERWRITE 4-BIT INPUT LATCH
TRANSFER 12-BIT DAC WORD TO THE D/A

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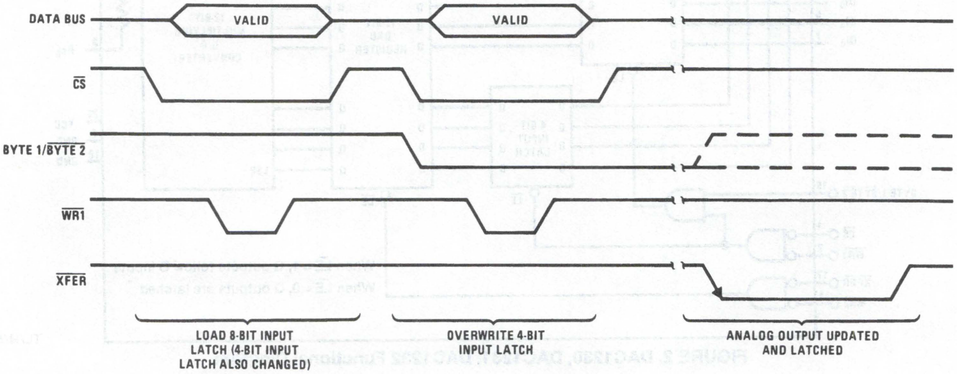
1.3 Transfer via an External Strobe

This method is basically the same as the previous operation except the $\overline{\text{XFER}}$ signal is provided by a device other than the processor. This allows the DAC to hold the code for a conditional analog output signal which will be required on demand from an external monitoring device (an analog voltage comparator for instance).


DATA BUS
VALID
VALID
$\overline{\text{CS}}$
BYTE 1/$\overline{\text{BYTE 2}}$
$\overline{\text{WR1}}$
$\overline{\text{XFER}}$
LOAD 8-BIT INPUT LATCH (4-BIT INPUT LATCH ALSO CHANGED)
OVERWRITE 4-BIT INPUT LATCH
ANALOG OUTPUT UPDATED AND LATCHED

$\overline{\text{WR2}}$ tied to a logic low (0V)

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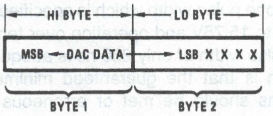
Application Hints (Continued)

1.4 Left-Justified Data Format

It is important to realize that the input registers of these DACs are arranged to accept a left-justified data word from the microprocessor with the most significant 8 bits coming first (Byte 1) and the lower 4 bits second. Left justification simply means that the binary point is assumed to be located to the left of the most significant bit. *Figure 3* shows how the 12 bits of DAC data should be arranged in 2 8-bit registers of an 8-bit processor before being written to the DAC.


HI BYTE
LO BYTE
MSB ← DAC DATA → LSB X X X X
BYTE 1
BYTE 2

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X = don't care

FIGURE 3. Left-Justified Data Format

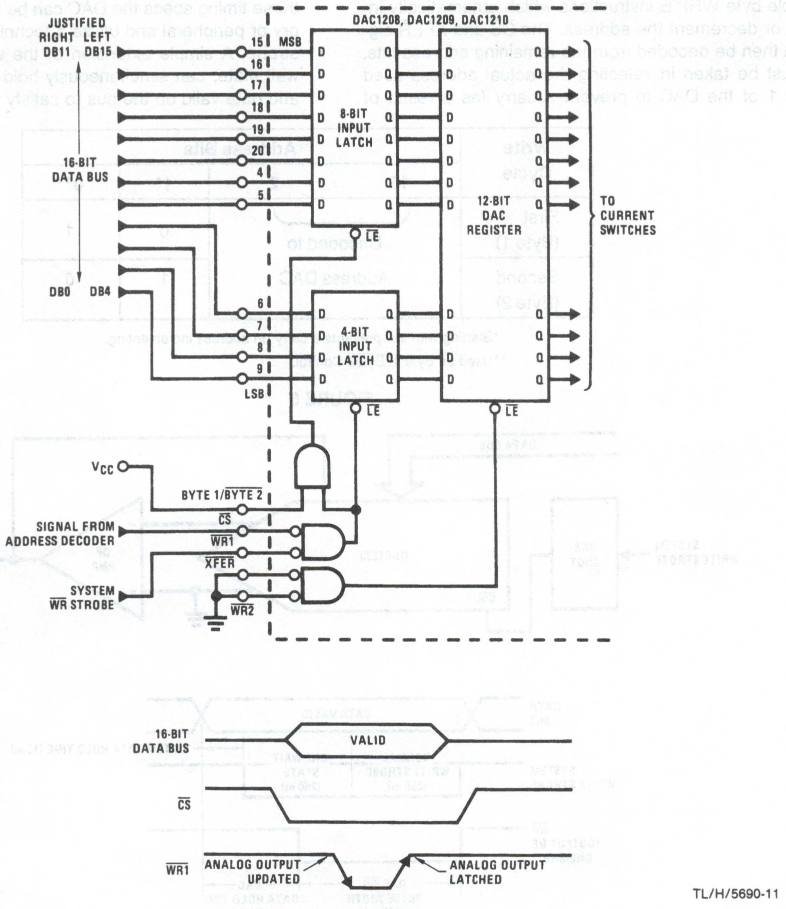
1.5 16-Bit Data Bus Interface

The DAC1208 series provides all 12 digital input lines to permit a direct parallel interface to a 16-bit data bus. In this instance, double buffering is not always necessary (unless a simultaneous updating of several DACs or a data transfer via an external strobe is desired) so the 12-bit DAC register can be wired to flow-through whereby its Q outputs always reflect the state of its D inputs. The external connections required and the timing diagram for this single buffered application are shown in *Figure 4.* Note that either left or right-justified data from the processor can be accommodated with a 16-bit data bus.

1.6 Flow-Through Operation

Through primarily designed to provide microprocessor interface compatibility, the MICRO-DACs can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in appli-

Interface Timing


DAC1208, DAC1209, DAC1210
JUSTIFIED
RIGHT LEFT
DB11 DB15
16-BIT DATA BUS
DB0 DB4
15 MSB
16
17
18
19
20
4
5
6
7
8
9
LSB
8-BIT INPUT LATCH
4-BIT INPUT LATCH
12-BIT DAC REGISTER
D
Q
LE
TO CURRENT SWITCHES
VCC
BYTE 1/BYTE 2
CS
WR1
XFER
WR2
SIGNAL FROM ADDRESS DECODER
SYSTEM WR STROBE
16-BIT DATA BUS
VALID
CS
WR1
ANALOG OUTPUT UPDATED
ANALOG OUTPUT LATCHED

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$\overline{\text{XFER}}$ and $\overline{\text{WR2}}$ grounded; Byte 1/$\overline{\text{Byte 2}}$ tied to V_{CC}.

FIGURE 4. 16-Bit Data Bus Interface for the DAC1208 Series

Application Hints (Continued)

cations where the DAC is used in a continuous feedback control loop and is driven by a binary up/down counter, or in function generation circuits where a ROM is continuously providing DAC data.

Only the DAC1208, DAC1209, DAC1210 devices can have all 12 inputs flow-through. Simply grounding $\overline{\text{CS}}$, $\overline{\text{WR1}}$, $\overline{\text{WR2}}$ and $\overline{\text{XFER}}$ and tying Byte 1/$\overline{\text{Byte 2}}$ high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.7 Address Decoding Tips

It is possible to map the MICRO-DACs into system ROM space to allow more efficient use of existing address decoding hardware. The DAC in effect can share the same addresses of any number of ROM locations. The ROM outputs will only be enabled by a READ of its address (gated by the system READ strobe) and the DAC will only accept data that is written to the same address (gated by the system WRITE strobe).

The Byte 1/$\overline{\text{Byte 2}}$ control function can easily be generated by the processor's least significant address bit (A0) by placing the DAC at two consecutive address locations and utilizing double-byte WRITE instructions which automatically increment or decrement the address. The $\overline{\text{CS}}$ and $\overline{\text{XFER}}$ signals can then be decoded from the remaining address bits. Care must be taken in selecting the actual address used for Byte 1 of the DAC to prevent a carry (as a result of incrementing the address for Byte 2) from propagating through the address word and changing any of the bits decoded for $\overline{\text{CS}}$ or $\overline{\text{XFER}}$. *Figure 5* shows how to prevent this effect.

The same problem can occur from a borrow when an auto-decremented address is used; but only if the processor's address outputs are inverted before being decoded.

1.8 Control Signal Timing

When interfacing these MICRO-DACs to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{\text{WR}}$ strobe pulse width which is specified as 320 ns for V_{CC} = 11.4V to 15.75V and operation over temperature, but typically a pulse width of only 250 ns is adequate. A second consideration is that the guaranteed minimum data hold time of 90 ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{\text{CS}}$) $\overline{\text{WR}}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{\text{WR}}$ pulse

Write Cycle	Address Bits 15 … 2	1*	0**
First (Byte 1)	Decoded to Address DAC	0	1
Second (Byte 2)		1	0

*Starting with a 0 prevents a carry on address incrementing.

**Used as Byte 1/$\overline{\text{Byte2}}$ Control.

FIGURE 5

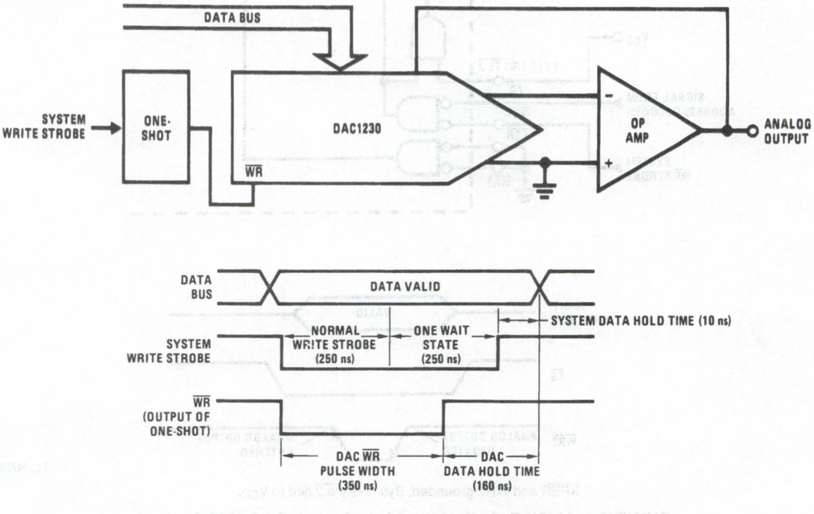
DATA BUS
SYSTEM WRITE STROBE
ONE-SHOT
DAC1230
$\overline{\text{WR}}$
−
+
OP AMP
ANALOG OUTPUT
DATA BUS
DATA VALID
SYSTEM DATA HOLD TIME (10 ns)
NORMAL WRITE STROBE (250 ns)
ONE WAIT STATE (250 ns)
SYSTEM WRITE STROBE
$\overline{\text{WR}}$ (OUTPUT OF ONE-SHOT)
DAC $\overline{\text{WR}}$ PULSE WIDTH (350 ns)
DAC DATA HOLD TIME (160 ns)

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FIGURE 6. Accommodating a High Speed System

Application Hints (Continued)

width. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{\text{WR}}$ pin of the DAC. This is illustrated in *Figure 6* for an exemplary system which provides a 250 ns $\overline{\text{WR}}$ strobe time with a data hold time of only 10 ns.

The proper data set-up time prior to the latching edge (low to high transition) of the $\overline{\text{WR}}$ strobe, is insured if the $\overline{\text{WR}}$ pulse width is within spec and the data is valid on the bus for the duration of the DAC $\overline{\text{WR}}$ strobe.

1.9 Digital Signal Feedthrough

A typical microprocessor is a tremendous potential source of high frequency noise which can be coupled to sensitive analog circuitry. The fast edges of the data and address bus signals generate frequency components of 10's of megahertz and may cause fast transients to appear at the DAC output, even when data is latched internally.

In low frequency or DC applications, low pass filtering can reduce the magnitude of any fast transients. This is most easily accomplished by over-compensating the DAC output amplifier by increasing the value of its feedback capacitor.

In applications requiring a fast output response from the DAC and op amp, filtering may not be feasible. In this event, digital signals can be completely isolated from the DAC circuitry, by the use of a DM74LS374 latch, until a valid $\overline{\text{CS}}$ signal is applied to update the DAC. This is shown in *Figure 7*.

A single TRI-STATE® data buffer such as the DM81LS95 can be used to isolate any number of DACs in a system. *Figure 8* shows this isolating circuitry and decoding hardware for a multiple DAC analog output card. Pull-up resistors are used on the buffer outputs to limit the impedance at the DAC digital inputs when the card is not selected. A unique feature of this card is that the DAC $\overline{\text{XFER}}$ strobes are controlled by the data bus. This allows a very flexible update of any combination of analog outputs via a transfer word which would contain a zero in the bit position assigned to any of the DACs required to change to a new output value.

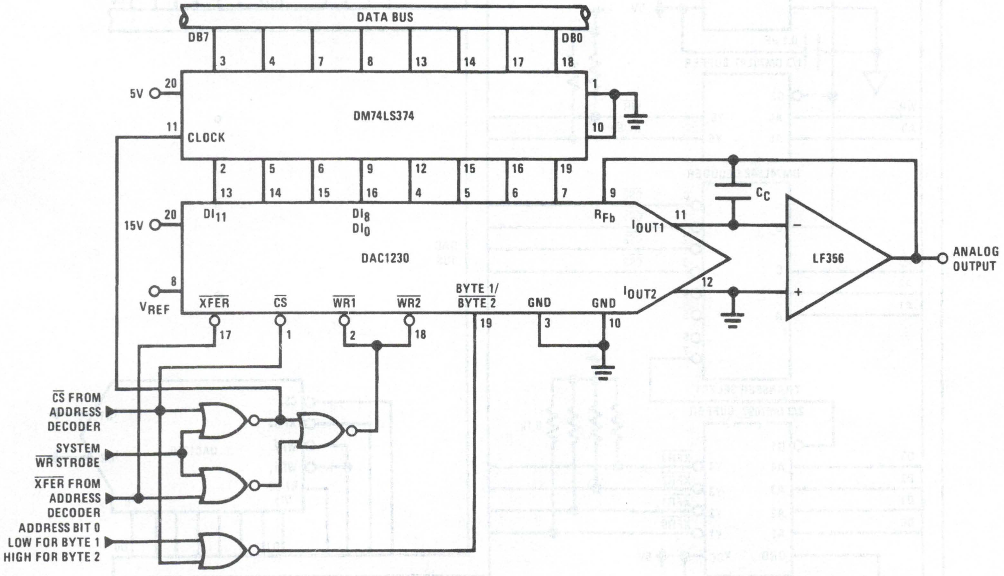
DATA BUS
DB7
DB0
3
4
7
8
13
14
17
18
5V
20
1
DM74LS374
11
CLOCK
10
2
5
6
9
12
15
16
19
13
14
15
16
4
5
6
7
9
15V
20
DI11
DI8
DI0
RFb
IOUT1
11
CC
DAC1230
LF356
ANALOG OUTPUT
8
VREF
XFER
CS
WR1
WR2
BYTE 1/BYTE 2
GND
GND
IOUT2
12
17
1
2
18
19
3
10
CS FROM ADDRESS DECODER
SYSTEM WR STROBE
XFER FROM ADDRESS DECODER
ADDRESS BIT 0 LOW FOR BYTE 1 HIGH FOR BYTE 2

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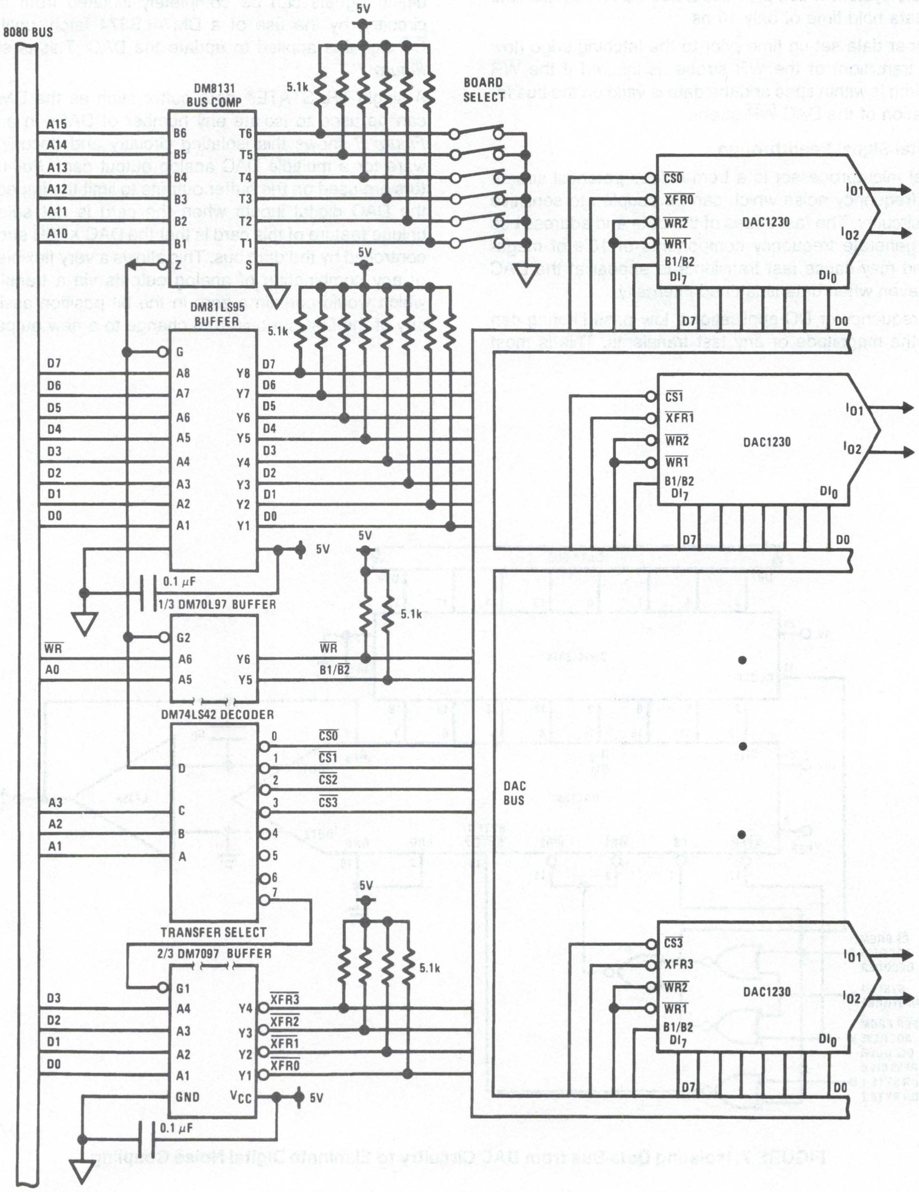
FIGURE 7. Isolating Data Bus from DAC Circuitry to Eliminate Digital Noise Coupling

Application Hints (Continued)


8080 BUS
5V
5.1k
DM8131
BUS COMP
BOARD
SELECT
A15
A14
A13
A12
A11
A10
B6
B5
B4
B3
B2
B1
Z
T6
T5
T4
T3
T2
T1
S
DM81LS95
BUFFER
G
D7
D6
D5
D4
D3
D2
D1
D0
A8
A7
A6
A5
A4
A3
A2
A1
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
0.1 µF
1/3 DM70L97 BUFFER
G2
WR
A0
B1/B2
DM74LS42 DECODER
CS0
CS1
CS2
CS3
0
1
2
3
4
5
6
7
D
C
B
A
TRANSFER SELECT
2/3 DM7097 BUFFER
G1
XFR3
XFR2
XFR1
XFR0
GND
VCC
DAC1230
CS0
XFR0
WR2
WR1
B1/B2
DI7
DI0
IO1
IO2
D7
D0
CS1
XFR1
CS3
XFR3
DAC
BUS

TL/H/5690-14

FIGURE 8. TRI-STATE® Buffers Isolate the Data and Control Lines from the DACs. A Transfer Word Provides a Flexible Update.

Application Hints (Continued)

2.0 ANALOG APPLICATIONS

The analog output signal for these DACs is derived from a conventional R-2R current switching ladder network. A detailed description of this network can be found on the DAC1000 series data sheet. Basically, output I_{OUT1} provides a current directly proportional to the product of the applied reference voltage and the digital input word. A second output, I_{OUT2} will be a current proportional to the complement of the digital input. Specifically:

$$I_{OUT1} = \frac{V_{REF}}{R} \times \frac{D}{4096},$$

$$I_{OUT2} = \frac{V_{REF}}{R} \times \frac{4095 - D}{4096}$$

where D is the decimal equivalent of the applied 12-bit binary word (ranging from 0 to 4095), V_{REF} is the voltage applied to the V_{REF} terminal and R is the internal resistance of the R-2R ladder. R is nominally 15 kΩ.

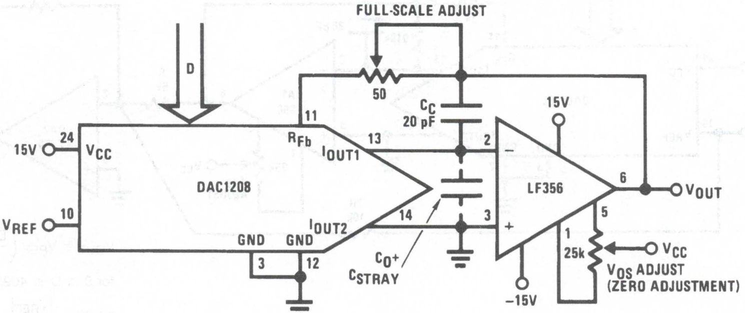
2.1 Obtaining a Unipolar Output Voltage

To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential (0 V_{DC}) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in *Figure 9*.

The inverting input of the op amp is a virtual ground created by the feedback from its output through the internal 15 kΩ resistor, R_{Fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{Fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{Fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage source or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry. Always use the internal R_{Fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET™ op amps are highly recommended for use with these DACs because of their very low input current.



TL/H/5690-15

$$V_{OUT} = -(I_{OUT1} \times R_{Fb})$$
$$= \frac{-V_{REF}(D)}{4096}$$
$$\text{for } 0 \leq D \leq 4095$$

FIGURE 9. Unipolar Output Configuration

Application Hints (Continued)

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{Fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in *Figure 9*, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

2.1.1 Zero and Full-Scale Adjustments

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

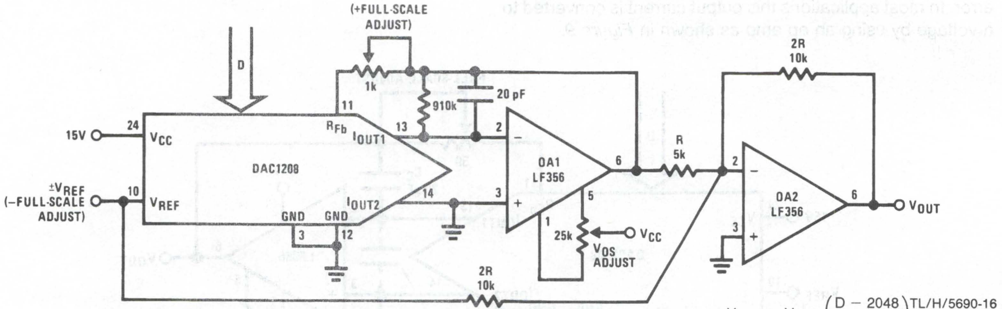
The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near 0 V_{DC} as possible. This is accomplished by shorting out R_{Fb}, the amplifier feedback resistor, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all ones for I_{OUT2}). The short around R_{Fb} is then removed and the converter is zero adjusted.

A unique feature of this series of DACs is that the full-scale or gain error is guaranteed to be negative. The gain error specification is a measure of how close the value of the internal feedback resistor, R_{Fb}, matches the R-2R ladder resistors. A negative gain error indicates that R_{Fb} is a smaller resistance value than it should be. To adjust this gain error, some resistance must always be added in series with R_{Fb}. The 50Ω potentiometer shown is sufficient to adjust the worst-case gain error for these devices.

2.2 Bipolar Output Voltage from a Fixed Reference

The addition of a second op amp to the unipolar circuit can generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication. This circuit is shown in *Figure 10*.

This configuration features several improvements over existing circuits for a bipolar output shown with other multiplying DACs. Only the offset voltage of amplifier 1 affects the linearity of the DAC. The offset voltage error of the second op amp (although a constant output error) has no effect on linearity. In addition, this configuration offers a non-interactive positive and negative full-scale calibration procedure.



TL/H/5690-16

$$V_{OUT} = V_{REF}\left(\frac{D - 2048}{2048}\right)$$

for $0 \leq D \leq 4095$

$$1\ LSB = \frac{|V_{REF}|}{2048}$$

Input Code MSB......LSB	Ideal V_{OUT}	
	$+V_{REF}$	$-V_{REF}$
1 1 1 1 1 1 1 1 1 1 1 1	V_{REF} −1 LSB	$-\lvert V_{REF}\rvert + 1$ LSB
1 1 0 0 0 0 0 0 0 0 0 0	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1 0 0 0 0 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1 1 1 1 1	−1 LSB	+1 LSB
0 0 1 1 1 1 1 1 1 1 1 1	$-\frac{V_{REF}}{2} - 1$ LSB	$\frac{\lvert V_{REF}\rvert}{2} + 1$ LSB
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}$	$+\lvert V_{REF}\rvert$

FIGURE 10. Bipolar Output Voltage Configuration

Application Hints (Continued)

2.2.1 Zero and Full-Scale Adjustments

To calibrate the bipolar output circuit, three adjustments are required. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) then null the V_{OS} of amplifier 1 by setting the voltage at its inverting input (pin 2) to zero volts. Next, with a code of all zeros still applied, adjust "−full-scale adjust", the reference voltage, for $V_{OUT} = \pm|V_{REF}\ \text{ideal}|$. The polarity of the output voltage at this time will be opposite that of the applied reference. Finally, set all of the digital inputs HIGH and adjust "+full-scale adjust" for

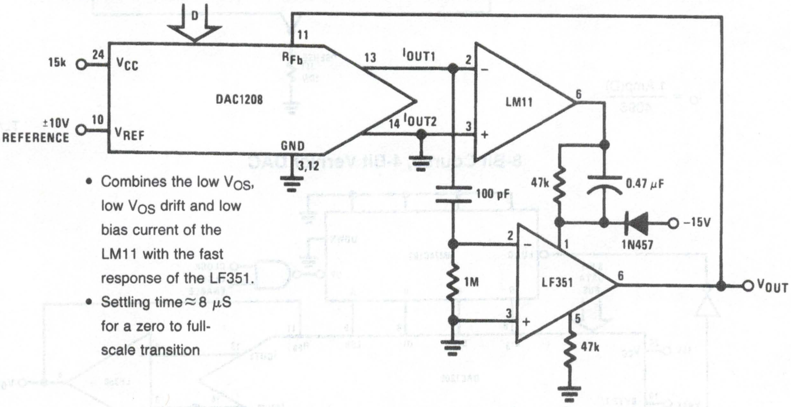
$$V_{OUT} = V_{REF}\,\frac{2047}{2048}.$$

The polarity of the output will be the same as that of the reference voltage.

3.0 APPLICATION IDEAS

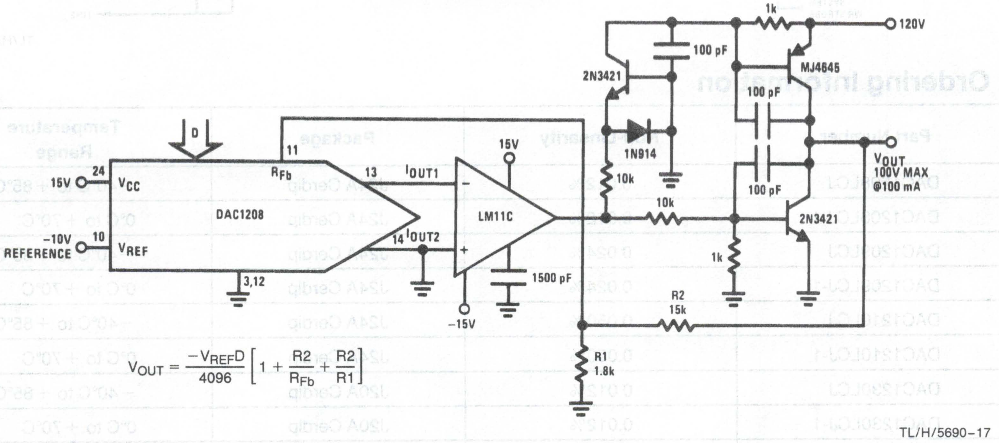
In this section the digital input word is represented by the letter D and is equal to the decimal equivalent of the 12-bit binary input. Hence D can be any integer value between 0 and 4095.

Composite Amplifier for Good DC Characteristics and Fast Output Response


D
15k
24
VCC
±10V
REFERENCE
10
VREF
DAC1208
11
RFb
13
IOUT1
14
IOUT2
GND
3,12
2
3
LM11
6
47k
0.47 µF
100 pF
1N457
−15V
2
1
1M
LF351
6
3
5
47k
VOUT

- Combines the low V_{OS}, low V_{OS} drift and low bias current of the LM11 with the fast response of the LF351.
- Settling time ≈ 8 µS for a zero to full-scale transition

High Voltage, Power DAC


D
15V
24
VCC
−10V
REFERENCE
10
VREF
DAC1208
11
RFb
13
IOUT1
14
IOUT2
3,12
15V
LM11C
−15V
1500 pF
2N3421
100 pF
1N914
10k
10k
1k
MJ4645
100 pF
100 pF
120V
VOUT
100V MAX
@100 mA
2N3421
1k
R2
15k
R1
1.8k

$$V_{OUT} = \frac{-V_{REF}D}{4096}\left[1 + \frac{R2}{R_{Fb}} + \frac{R2}{R1}\right]$$

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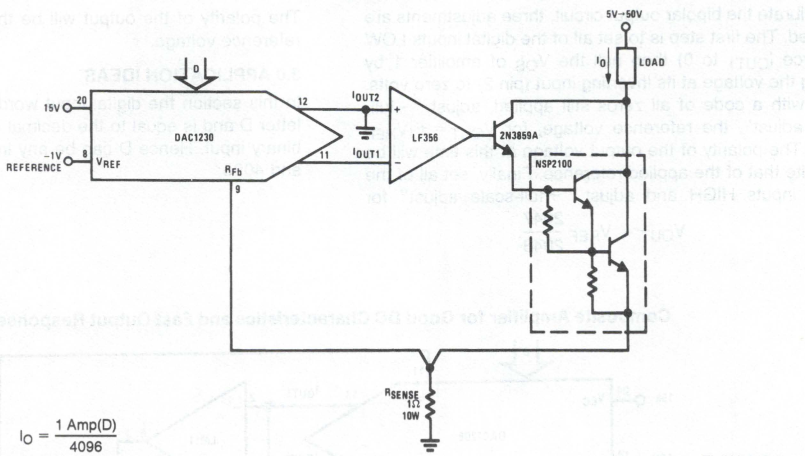
Application Hints (Continued)

High Current Controller


D
15V
20
12
DAC1230
IOUT2
LF356
2N3859A
NSP2100
-1V REFERENCE
8
VREF
11
IOUT1
RFb
9
5V–50V
IO
LOAD
RSENSE 1Ω 10W
IO = 1 Amp(D) / 4096

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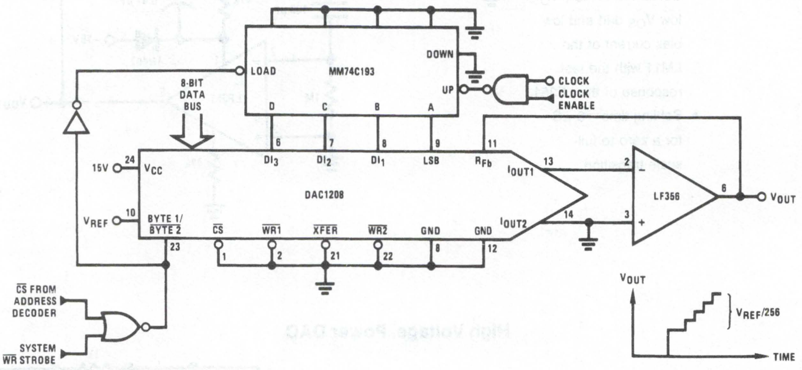
8-Bit Course, 4-Bit Vernier DAC


LOAD
MM74C193
DOWN
UP
CLOCK
CLOCK ENABLE
D
C
B
A
8-BIT DATA BUS
6
7
8
9
11
DI3
DI2
DI1
LSB
RFb
15V
24
VCC
DAC1208
IOUT1
13
2
LF356
6
VOUT
VREF
10
BYTE 1/BYTE 2
23
CS
WR1
XFER
WR2
GND
GND
IOUT2
14
3
1
2
21
22
8
12
CS FROM ADDRESS DECODER
SYSTEM WR STROBE
VOUT
VREF/256
TIME

TL/H/5690–20

Ordering Information

Part Number	Non-Linearity	Package	Temperature Range
DAC1208LCJ	0.012%	J24A Cerdip	−40°C to +85°C
DAC1208LCJ-1	0.012%	J24A Cerdip	0°C to +70°C
DAC1209LCJ	0.024%	J24A Cerdip	−40°C to +85°C
DAC1209LCJ-1	0.024%	J24A Cerdip	0°C to +70°C
DAC1210LCJ	0.050%	J24A Cerdip	−40°C to +85°C
DAC1210LCJ-1	0.050%	J24A Cerdip	0°C to +70°C
DAC1230LCJ	0.012%	J20A Cerdip	−40°C to +85°C
DAC1230LCJ-1	0.012%	J20A Cerdip	0°C to +70°C
DAC1231LCJ	0.024%	J20A Cerdip	−40°C to +85°C
DAC1231LCJ-1	0.024%	J20A Cerdip	0°C to +70°C
DAC1232LCJ	0.050%	J20A Cerdip	−40°C to +85°C
DAC1232LCJ-1	0.050%	J20A Cerdip	0°C to +70°C

National Semiconductor Corporation

DAC1218, DAC1219
12-Bit Binary Multiplying D/A Converter

General Description

The DAC1218 and the DAC1219 are 12-bit binary, 4-quadrant multiplying D to A converters. The linearity, differential non-linearity and monotonicity specifications for these converters are all guaranteed over temperature. In addition, these parameters are specified with standard zero and full-scale adjustment procedures as opposed to the impractical best fit straight line guarantee.

This level of precision is achieved though the use of an advanced silicon-chromium (SiCr) R-2R resistor ladder network. This type of thin-film resistor eliminates the parasitic diode problems associated with diffused resistors and allows the applied reference voltage to range from −25V to 25V, independent of the logic supply voltage.

CMOS current switches and drive circuitry are used to achieve low power consumption (20 mW typical) and minimize output leakage current errors (10 nA maximum). Unique digital input circuitry maintains TTL compatible input threshold voltages over the full operating supply voltage range.

The DAC1218 and DAC1219 are direct replacements for the AD7541 series, AD7521 series, and AD7531 series with a significant improvement in the linearity specification. In applications where direct interface of the D to A converter to a microprocessor bus is desirable, the DAC1208 and DAC1230 series eliminate the need for additional interface logic.

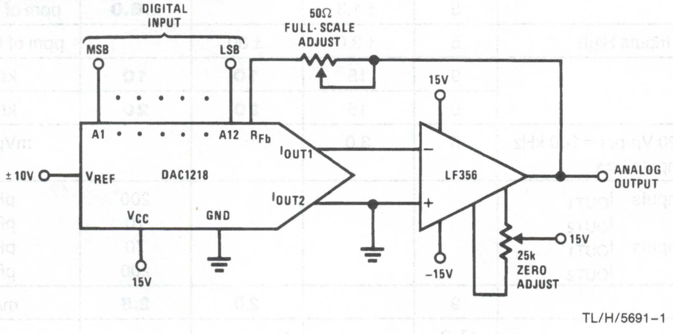
Features

- Linearity specified with zero and full-scale adjust only
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- All parts guaranteed 12-bit monotonic

Key Specifications

Current Settling Time	1 µs
Resolution	12 Bits
Linearity (Guaranteed over temperature)	12 Bits (DAC1218) 11 Bits (DAC1219)
Gain Tempco	1.5 ppm/°C
Low Power Dissipation	20 mW
Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



TL/H/5691-1

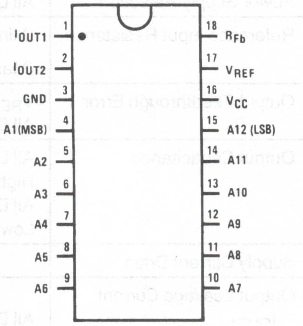
$$V_{OUT} = -V_{REF}\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\ldots\frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high

AN = 0 if digital input is low

Connection Diagram

Dual-In-Line Package



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Top View

Ordering Information

Temperature Range		0°C to +70°C	−40°C to +85°C	Package Outline
Non Linearity	0.012%	DAC1218LCJ-1	DAC1218LCJ	J18A Cerdip
	0.024%	DAC1219LCJ-1	DAC1219LCJ	J18A Cerdip

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$ (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead Temp. (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 11)	800V

Operating Conditions

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC1218LCJ, DAC1219LCJ	$-40°C \le T_A \le +85°C$
DAC1218LCJ-1, DAC1219LCJ-1	$0°C \le T_A \le 70°C$
Range of V_{CC}	5 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 9);** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	Notes	Typ (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Units
Resolution			12	**12**	**12**	Bits
Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted	4, 5, 9				
	DAC1218			**0.012**	**0.012**	% of FSR
	DAC1219			**0.024**	**0.024**	% of FSR
Differential Non-Linearity	Zero and Full-Scale Adjusted	4, 5, 9				
	DAC1218			**0.018**	**0.018**	% of FSR
	DAC1219			**0.024**	**0.024**	% of FSR
Monotonicity		4	12	12	**12**	Bits
Gain Error (Min)	Using Internal R_{Fb}, $V_{REF} = \pm 10V, \pm 1V$	5	−0.1	0.0		% of FSR
Gain Error (Max)		5	−0.1	+0.2		% of FSR
Gain Error Tempco		5	±1.3		**±6.0**	ppm of FS/°C
Power Supply Rejection	All Digital Inputs High	5	±3.0	±30		ppm of FSR/V
Reference Input Resistance	(Min)	9	15	**10**	**10**	kΩ
	(Max)	9	15	**20**	**20**	kΩ
Output Feedthrough Error	V_{REF} = 120 Vp-p, f = 100 kHz All Data Inputs Low	6	3.0			mVp-p
Output Capacitance	All Data Inputs High I_{OUT1}				200	pF
	I_{OUT2}				70	pF
	All Data Inputs Low I_{OUT1}				70	pF
	I_{OUT2}				200	pF
Supply Current Drain		9		2.0	**2.5**	mA
Output Leakage Current		7, 9				
I_{OUT1}	All Data Inputs Low			**10**	**10**	nA
I_{OUT2}	All Data Inputs High			**10**	**10**	nA
Digital Input Threshold	Low Threshold	9		**0.8**	**0.8**	V_{DC}
	High Threshold			**2.2**	**2.2**	V_{DC}
Digital Input Currents	Digital Inputs <0.8V	9		**−200**	**−200**	μA_{DC}
	Digital Inputs >2.2V			**10**	**10**	μA_{DC}
t_s Current Settling Time	$R_L = 100\Omega$, Output Settled to 0.01%, All Digital Inputs Switched Simultaneously		1			μs

Electrical Characteristics Notes

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1218 is 0.012% of FSR. This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within $0.012\% \times V_{REF}$ of a straight line which passes through zero and full-scale. The unit ppm of FSR (parts per million of full-scale range) and ppm of FS (parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. 1 ppm of $FSR = V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ±6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from −40°C to +85°C of $\pm(6)(V_{REF}/10^6)(125°C)$ or $\pm 0.75\ (10^{-3})\ V_{REF}$ which is ±0.075% of V_{REF}.

Note 6: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 7: A 10 nA leakage current with $R_{Fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

Note 8: Human body model, 100 pF discharged through 1.5 kΩ resistor.

Note 9: Tested limit for −1 suffix parts applies only at 25°C.

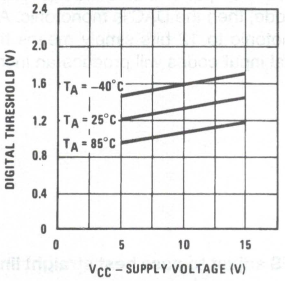
Note 10: Typicals are at 25°C and represent the most likely parametric norm.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

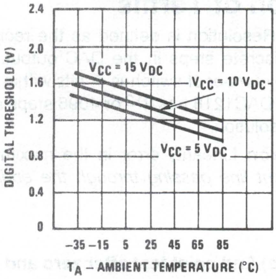
Note 12: Design limits are guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Performance Characteristics

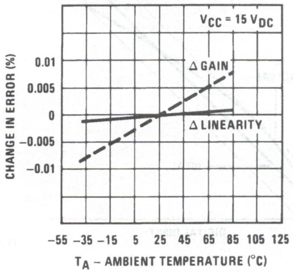
Digital Input Threshold vs V_{CC}



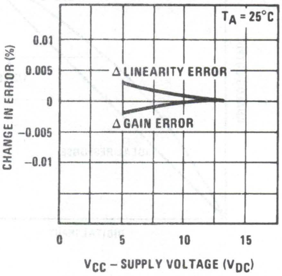
Digital Input Threshold vs Temperature



Gain and Linearity Error Variation vs Temperature



Gain and Linearity Error Variation vs Supply Voltage



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Definition of Package Pinouts

(A1–A12): Digital Inputs. A12 is the least significant digital input (LSB) and A1 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital input of all 1s, and is zero for a digital input of all 0s.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1}+I_{OUT2}=\text{constant}$ (for a fixed reference voltage).

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects to an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Ground. This is the ground for the circuit.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1218 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error in the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

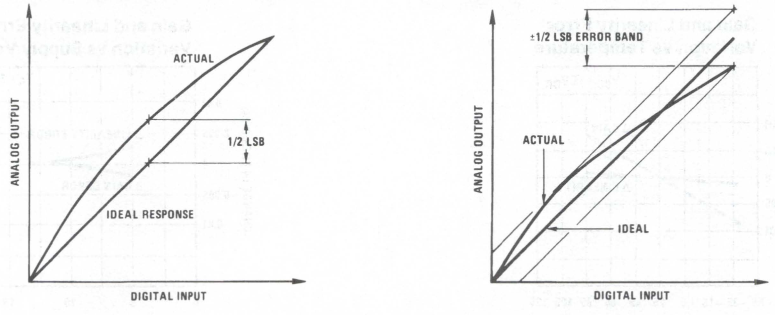
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ± 1/2 LSB of the final output value.

Full-scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1218 full-scale is $V_{REF}-1$ LSB. For $V_{REF}=10V$ and unipolar operation, $V_{FULL\text{-}SCALE}=10.0000V-2.44\ mV=9.9976V$. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End point test after zero and FS adjust

b) Shifting FS adjust to pass best straight line test

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Application Hints

The DAC1218 and DAC1219 are pin-for-pin compatible with the DAC1220 series but feature 12 and 11-bit linearity specifications. To preserve this degree of accuracy, care must be taken in the selection and adjustments of the output amplifier and reference voltage. Careful PC board layout is important, with emphasis made on compactness of components to prevent inadvertent noise pickup and utilization of single point grounding and supply distribution.

1.0 BASIC CIRCUIT DESCRIPTION

Figure 1 illustrates the R-2R current switching ladder network used in the DAC1218 and DAC1219. As a function of the logic state of each digital input, the binarily weighted current in each leg of the ladder is switched to either I_{OUT1} or I_{OUT2}. The voltage potential at I_{OUT1} and I_{OUT2} must be at zero volts to keep the current in each leg the same, independent of the switch state.

The switches operate with a small voltage drop across them and can therefore conduct currents of either polarity. This permits the reference to be positive or negative, thereby allowing 4-quadrant multiplication by the digital input word. The reference can be a stable DC source or a bipolar AC signal within the range of ±10V, for specified accuracy, with an absolute maximum range of ±25V. The reference can also exceed the applied V_{CC} of the DAC.

The maximum output current from either I_{OUT1} or I_{OUT2} is equal to

$$\frac{V_{REF(max)}}{R}\left(\frac{4095}{4096}\right),$$

where R is the reference input resistance (typically 15 kΩ). A high level on any digital input steers current to I_{OUT1} and a low level steers current to I_{OUT2}.

2.0 CREATING A UNIPOLAR OUTPUT VOLTAGE (A DIGITAL ATTENUATOR)

To generate an output voltage and keep the potential at the current output terminals at 0V, an op amp current to voltage converter is used. As shown in *Figure 2*, the current from I_{OUT1} flows through the feedback resistor, forcing a proportional voltage at the amplifier output. The voltage at I_{OUT1} is held at a virtual ground potential. The feedback resistor is provided on the chip and should always be used as it matches and tracks the R value of the R-2R ladder. The output voltage is the opposite polarity of the applied reference voltage.

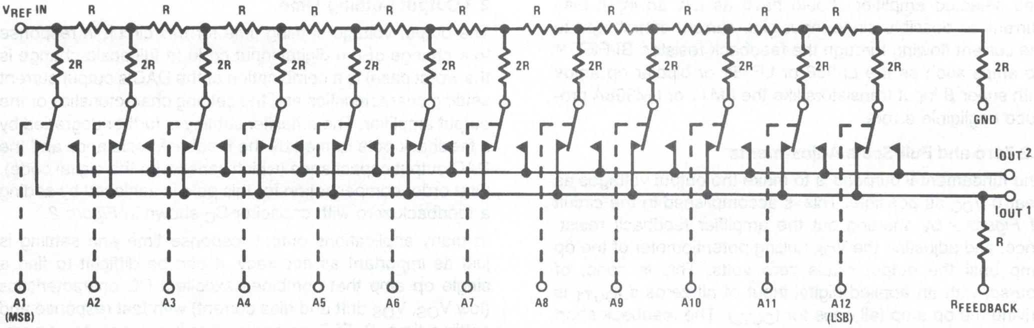
2.1 Amplifier Considerations

To maintain linearity of the output voltage with changing digital input codes the input offset voltage of the amplifier must be nulled. The resistance from I_{OUT1} to ground ($R_{I_{OUT1}}$) varies non-linearly with the applied digital code from a minimum of R with all ones applied to the input to near ∞ with an all zeros code. Any offset voltage between the amplifier inputs appears at the output with a gain of

$$1 + \frac{R_F}{R_{I_{OUT1}}}.$$

Since $R_{I_{OUT1}}$ varies with the input code, any offset will degrade output linearity. (See Note 4 of Electrical Characteristics.)

If the desired amplifier does not have offset balancing pins available (it could be part of a dual or quad package) the nulling circuit of *Figure 3* can be used. The voltage at the non-inverting input will be set to $-V_{OS}$ initially to force the inverting input to 0V. The common technique of summing current into the amplifier summing junction cannot be used as it directly introduces a zero code output current error.



Note: Switches shown in digital high state.

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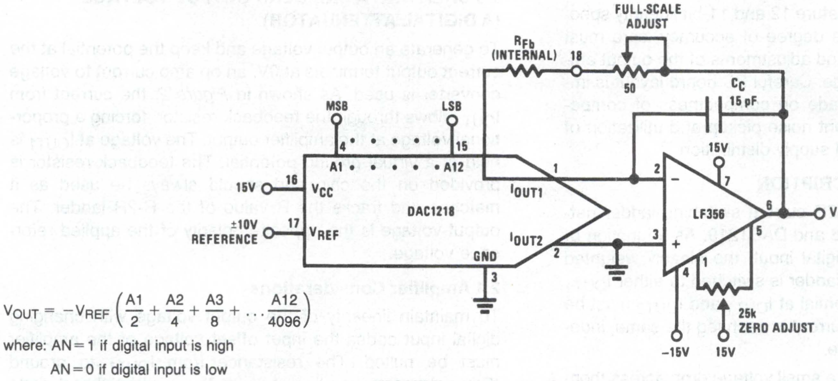
FIGURE 1. The R-2R Current Switching Ladder Network

Application Hints (Continued)



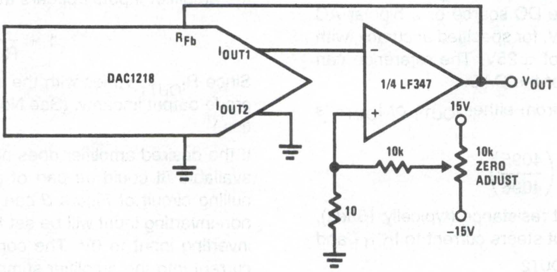
$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high

AN = 0 if digital input is low

TL/H/5691–5

FIGURE 2. Unipolar Output Voltage



TL/H/5691–6

FIGURE 3. Zeroing an Amplifier Which Does Not Have Balancing Provisions

The selected amplifier should have as low an input bias current as possible since input bias current contributes to the current flowing through the feedback resistor. BI-FET™ op amps such as the LF356 or LF351 or bipolar op amps with super β input transistors like the LM11 or LM308A produce negligible errors.

2.2 Zero and Full-Scale Adjustments

The fundamental purpose is to make the output voltages as near 0 V_{DC} as possible. This is accomplished in the circuit of *Figure 2* by shorting out the amplifier feedback resistance, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital input of all zeros if I_{OUT1} is driving the op amp (all ones for I_{OUT2}). The feedback short is then removed and the converter is zero adjusted.

A unique characteristic of these DACs is that any full-scale or gain error is always negative. This means that for a full-scale input code the output voltage, if not inherently correct, will always be less than what it should be. This ensures that adding an appropriate resistance in series with the internal feedback resistor, R_{Fb}, will always correct for any gain error. The 50Ω potentiometer in *Figure 2* is all that is needed to adjust the worst case DAC gain error.

Conversion accuracy is only as good as the applied reference voltage, so providing a source that is stable over time and temperature is important.

2.3 Output Settling Time

The output voltage settling time for this circuit in response to a change of the digital input code (a full-scale change is the worst case) is a combination of the DAC's output current settling characteristics and the settling characteristics of the output amplifier. The amplifier settling is further degraded by a feedback pole formed by the feedback resistance and the DAC output capacitance (which varies with the digital code). First order compensation for this pole is achieved by adding a feedback zero with capacitor C_C shown in *Figure 2*.

In many applications output response time and settling is just as important as accuracy. It can be difficult to find a single op amp that combines excellent DC characteristics (low V_{OS}, V_{OS} drift and bias current) with fast response and settling time. BI-FET op amps offer a reasonable compromise of high speed and good DC characteristics. The circuit of *Figure 4* illustrates a composite amplifier connection that combines the speed of a BI-FET LF351 with the excellent DC input characteristics of the LM11. If output settling time is not so critical, the LM11 can be used alone.

Figure 5 is a settling time test circuit for the complete voltage output DAC circuit. The circuit allows the settling time of the DAC amplifier to be measured to a resolution of 1 mV out of a zero to ±10V full-scale output change on an oscilloscope. *Figure 6* summarizes the measured settling times for several output amplifiers and feedback compensation capacitors.

Application Hint (Continued)

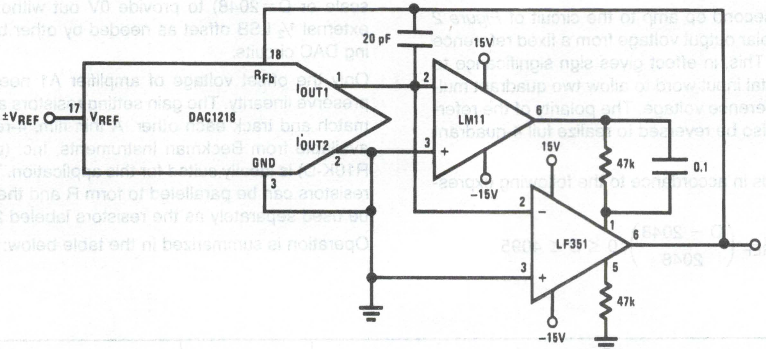

20 pF
18
RFb
1
IOUT1
2
–
15V
LM11
6
+
3
±VREF
17
VREF
DAC1218
IOUT2
2
GND
3
–15V
15V
47k
0.1
2
–
1
LF351
6
VOUT
3
+
5
47k
–15V

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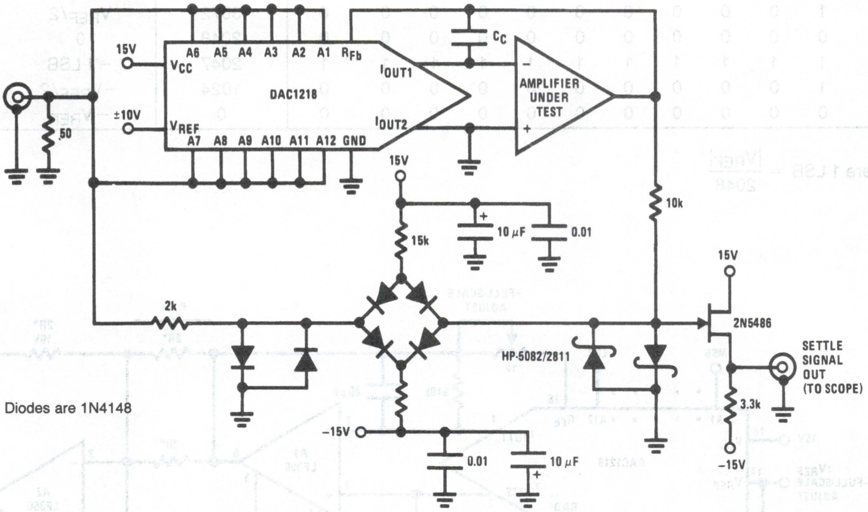
FIGURE 4. Composite Output Amplifier Connection


A6
A5
A4
A3
A2
A1
RFb
CC
15V
VCC
IOUT1
DAC1218
AMPLIFIER
UNDER
TEST
–
+
PULSE GENERATOR
INPUT
0V–5V
50
±10V
VREF
IOUT2
A7
A8
A9
A10
A11
A12
GND
15V
10k
10 μF
0.01
15k
15V
2k
2N5486
HP-5082/2811
SETTLE
SIGNAL
OUT
(TO SCOPE)
Diodes are 1N4148
3.3k
–15V
0.01
10 μF
–15V

TL/H/5691-8

FIGURE 5. DAC Settling Time Test Circuit

Amplifier	C_C	Settling Time to 0.01%
LM11	20 pF	30 μs
LF351	15 pF	8 μs
LF351	30 pF	5 μs
Composite LM11-LF351	20 pF	8 μs
LF356	15 pF	6 μs

FIGURE 6. Some Measured Settling Times

Application Hints (Continued)

3.0 OBTAINING A BIPOLAR OUTPUT VOLTAGE FROM A FIXED REFERENCE

The addition of a second op amp to the circuit of *Figure 2* can generate a bipolar output voltage from a fixed reference voltage (*Figure 7*). This, in effect gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference voltage can also be reversed to realize full 4-quadrant multiplication.

The output responds in accordance to the following expression:

$$V_O = V_{REF}\left(\frac{D - 2048}{2048}\right), 0 \le D \le 4095$$

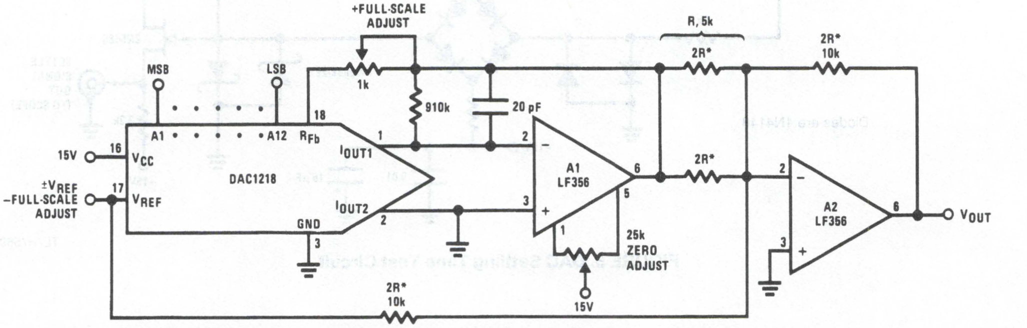
where D is the decimal equivalent of the true binary input word. This configuration inherently accepts a code (half-scale or D = 2048) to provide 0V out without requiring an external ½ LSB offset as needed by other bipolar multiplying DAC circuits.

Only the offset voltage of amplifier A1 need be nulled to preserve linearity. The gain setting resistors around A2 must match and track each other. A thin film, 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. Two of the four resistors can be paralleled to form R and the other two can be used separately as the resistors labeled 2R.

Operation is summarized in the table below:

Applied Digital Input												Decimal Equivalent	V_{OUT}	
MSB	.	.	.	.	.	.	.	.	.	.	LSB		$+V_{REF}$	$-V_{REF}$
1	1	1	1	1	1	1	1	1	1	1	1	4095	$V_{REF} - 1$ LSB	$-\lvert V_{REF}\rvert + 1$ LSB
1	1	0	0	0	0	0	0	0	0	0	0	3072	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1	0	0	0	0	0	0	0	0	0	0	0	2048	0	0
0	1	1	1	1	1	1	1	1	1	1	1	2047	−1 LSB	+1 LSB
0	1	0	0	0	0	0	0	0	0	0	0	1024	$-V_{REF}/2$	$+\lvert V_{REF}\rvert/2$
0	0	0	0	0	0	0	0	0	0	0	0	0	$-V_{REF}$	$+\lvert V_{REF}\rvert$

Where $1 \text{ LSB} = \frac{\lvert V_{REF}\rvert}{2048}$


+FULL-SCALE ADJUST
1k
MSB
LSB
A1
A12
18
R_{Fb}
910k
20 pF
R, 5k
2R*
2R* 10k
15V
16
V_{CC}
±V_{REF} −FULL-SCALE ADJUST
17
V_{REF}
DAC1218
I_{OUT1}
1
I_{OUT2}
2
GND
3
2
3
A1 LF356
6
5
1
25k ZERO ADJUST
15V
2R*
2
3
A2 LF356
6
V_{OUT}
2R* 10k

*0.1% matching

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FIGURE 7. Obtaining a Bipolar Output from a Fixed Reference

Application Hints (Continued)

3.1 Zero and Full-Scale Adjustments

The three adjustments needed for this circuit are shown in *Figure 7*. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) and then trim "zero adjust" for zero volts at the inverting input (pin 2) of OA1. Next, with a code of all zeros still applied, adjust "- full-scale adjust", the reference voltage, for $V_{OUT} = \pm|(\text{ideal } V_{REF})|$. The sign of the output voltage will be opposite that of the applied reference.

Finally, set all of the digital inputs HIGH and adjust "+ full-scale adjust" for $V_{OUT} = V_{REF}$ (511/512). The sign of the output at this time will be the same as that of the reference voltage. This + full-scale adjustment scheme takes into account the effects of the V_{OS} of amplifier A2 (as long as this offset is less than 0.1% of V_{REF}) and any gain errors due to external resistor mismatch.

4.0 MISCELLANEOUS APPLICATION HINTS

The devices are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to electrostatic discharge.

During power-up supply voltage sequencing, the negative supply of the output amplifier may appear first. This will typically cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is clamped to one diode drop below ground.

As a general rule, any unused digital inputs should be tied high or low as required by the application. As a trouble-shooting aid, if any digital input is left floating, the DAC will interpret that input as a logical 1 level.

Additional Application Ideas

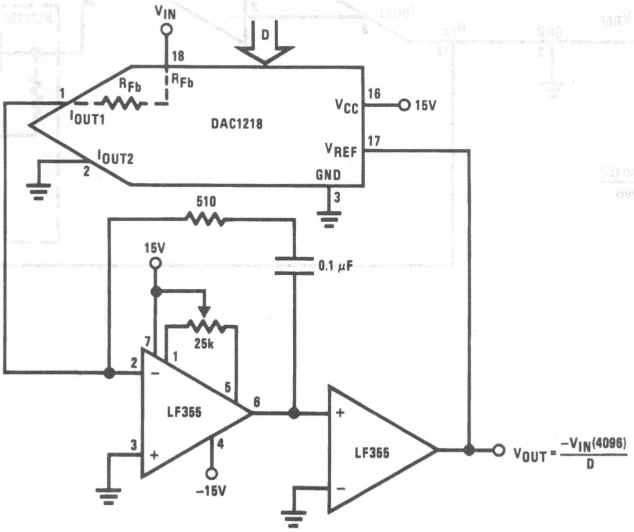
For the circuits shown, D represents the decimal equivalent of the binary digital input code. D ranges from 0 (for an all zeros input code) to 4095 (for an all ones input code) and for any code can be determined from:

$$D = 2048(A1) + 1024(A2) + 512(A2) + \ldots 2(A11) + 1(A12)$$

where AN = 1 if that input is high

AN = 0 if that input is low

DAC Controlled Amplifier



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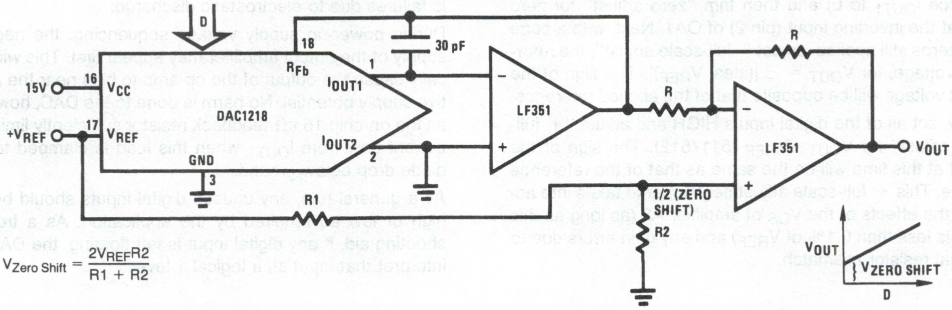
Additional Application Ideas (Continued)

Offsetting the Zero Code Output Voltage


D
18
30 pF
RFb
1
IOUT1
15V
16
VCC
DAC1218
+VREF
17
VREF
IOUT2
2
GND
3
R1
LF351
R
R
LF351
VOUT
1/2 (ZERO SHIFT)
R2
VOUT
VZERO SHIFT
D

$$V_{\text{Zero Shift}} = \frac{2V_{REF}R2}{R1 + R2}$$

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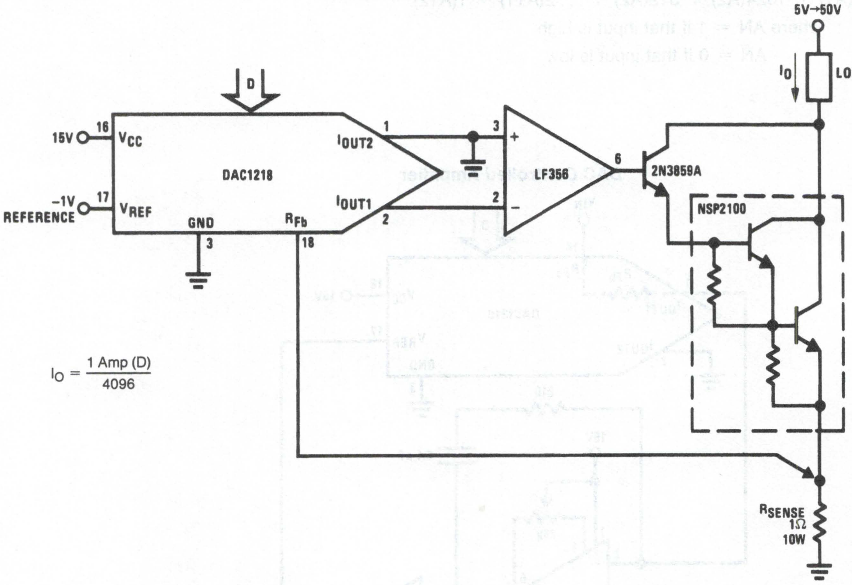
High Current Controller


5V→50V
IO
LOAD
D
15V
16
VCC
DAC1218
IOUT2
1
3
+
LF356
6
2N3859A
−1V REFERENCE
17
VREF
IOUT1
2
2
−
GND
3
RFb
18
NSP2100
RSENSE
1Ω
10W

$$I_O = \frac{1\ \text{Amp}\ (D)}{4096}$$

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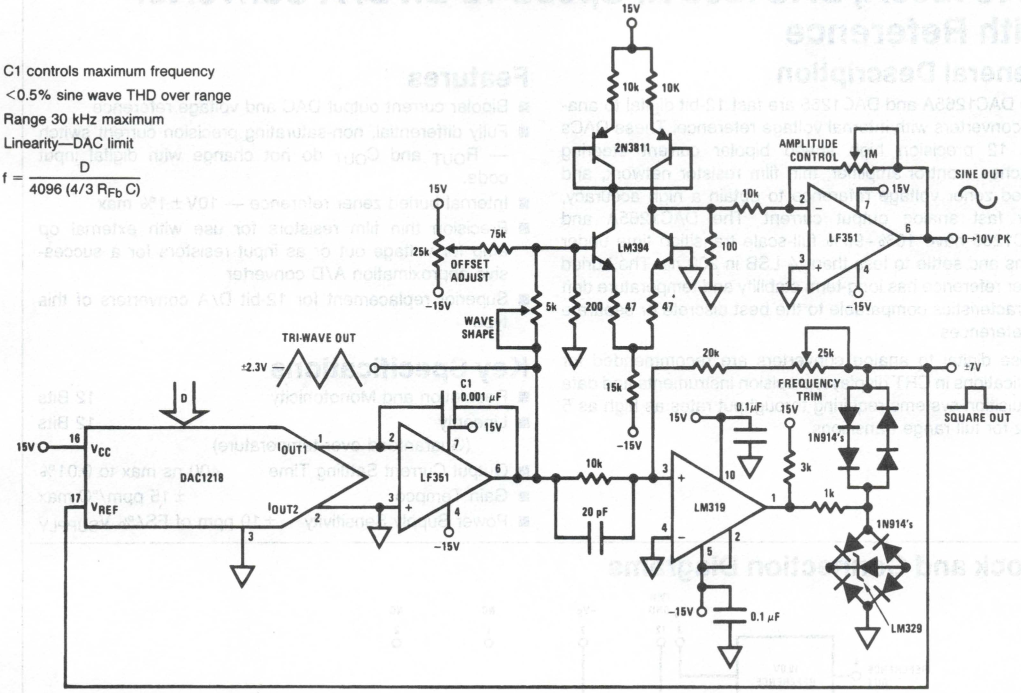
Additional Application Ideas (Continued)

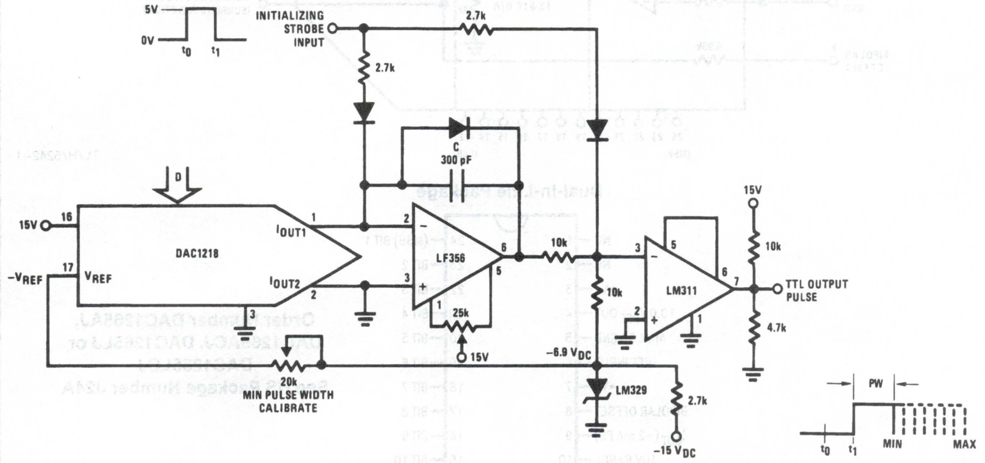
DAC Controlled Function Generator

- C1 controls maximum frequency
- <0.5% sine wave THD over range
- Range 30 kHz maximum
- Linearity—DAC limit
- $f = \dfrac{D}{4096\ (4/3\ R_{Fb}\ C)}$


15V
10k
10K
2N3811
AMPLITUDE CONTROL
1M
SINE OUT
15V
10k
15V
25k
75k
OFFSET ADJUST
−15V
LM394
100
LF351
0→10V PK
−15V
5k
WAVE SHAPE
200
47
47
TRI-WAVE OUT
±2.3V
D
C1 0.001 µF
15V
20k
25k
FREQUENCY TRIM
±7V
15k
−15V
15V
0.1 µF
15V
SQUARE OUT
1N914's
15V
16
VCC
DAC1218
IOUT1
1
2
7
LF351
6
10k
3
10
3k
17
VREF
IOUT2
2
3
4
−15V
20 pF
LM319
1
1k
1N914's
3
4
2
5
−15V
0.1 µF
LM329

TL/H/5691–13

Digitally Programmable Pulse-Width Generator


5V
0V
t0
t1
INITIALIZING STROBE INPUT
2.7k
2.7k
C
300 pF
D
15V
16
DAC1218
IOUT1
1
2
LF356
6
5
10k
3
5
15V
10k
6
7
TTL OUTPUT PULSE
LM311
−VREF
17
VREF
IOUT2
2
3
3
1
25k
15V
10k
2
1
4.7k
−6.9 VDC
20k
MIN PULSE WIDTH CALIBRATE
LM329
2.7k
−15 VDC
PW
t0
t1
MIN
MAX

$$PW \cong \frac{C(7.5V)\,(4096)\,(R_{Fb})}{D|V_{REF}}$$

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National Semiconductor Corporation

DAC1265A, DAC1265 Hi-Speed 12-Bit D/A Converter with Reference

General Description

The DAC1265A and DAC1265 are fast 12-bit digital to analog converters with internal voltage reference. These DACs use 12 precision high speed bipolar current steering switches, control amplifier, thin film resistor network, and buried zener voltage reference to obtain a high accuracy, very fast analog output current. The DAC1265A and DAC1265 have 10%–90% full-scale transition time under 35 ns and settle to less than ½ LSB in 200 ns. The buried zener reference has long-term stability and temperature drift characteristics comparable to the best discrete or separate IC references.

These digital to analog converters are recommended for applications in CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 5 MHz for full range transitions.

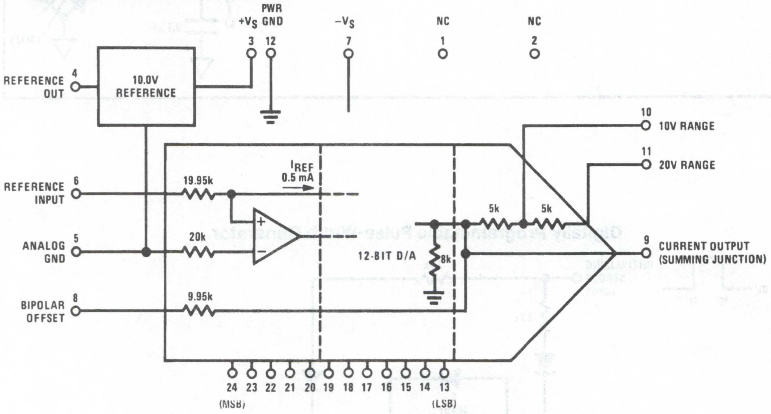
Features

- Bipolar current output DAC and voltage reference
- Fully differential, non-saturating precision current switch — R_{OUT} and C_{OUT} do not change with digital input code.
- Internal buried zener reference — 10V ± 1% max
- Precision thin film resistors for use with external op amp for voltage out or as input resistors for a successive approximation A/D converter
- Superior replacement for 12-bit D/A converters of this type

Key Specifications

■ Resolution and Monotonicity	12 Bits
■ Linearity (Guaranteed over temperature)	12 Bits
■ Output Current Settling Time	400 ns max to 0.01%
■ Gain Tempco	±15 ppm/°C max
■ Power Supply Sensitivity	±10 ppm of FS/% V_{SUPPLY}

Block and Connection Diagrams


+V_S
PWR GND
$-V_S$
NC
NC
3
12
7
1
2
REFERENCE OUT
4
10.0V REFERENCE
10
10V RANGE
11
20V RANGE
REFERENCE INPUT
6
19.95k
I_{REF} 0.5 mA
ANALOG GND
5
20k
5k
5k
12-BIT D/A
8k
9
CURRENT OUTPUT (SUMMING JUNCTION)
BIPOLAR OFFSET
8
9.95k
24
23
22
21
20
19
18
17
16
15
14
13
(MSB)
(LSB)

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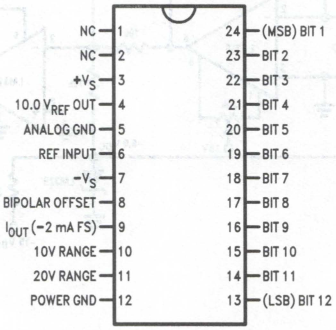
Dual-In-Line Package


NC 1
NC 2
+V_S 3
10.0 V_{REF} OUT 4
ANALOG GND 5
REF INPUT 6
$-V_S$ 7
BIPOLAR OFFSET 8
I_{OUT} (−2 mA FS) 9
10V RANGE 10
20V RANGE 11
POWER GND 12
24 (MSB) BIT 1
23 BIT 2
22 BIT 3
21 BIT 4
20 BIT 5
19 BIT 6
18 BIT 7
17 BIT 8
16 BIT 9
15 BIT 10
14 BIT 11
13 (LSB) BIT 12

Top View

TL/H/5242-2

Order Number DAC1265AJ, DAC1265ACJ, DAC1265LJ or DAC1265LCJ
See NS Package Number J24A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V^+ and V^-)	±18V
Current Output (Pin 9) Voltage	−3V, 12V
Logic Input Voltage	−1V, 7V
Reference Input Voltage (Pin 6)	±12V
Analog GND to Power GND	±1V
Bipolar Offset	±12V
10V Range	±12V

20V Range	V^- to +24V
Power Dissipation (Note 1)	1000 mW
Short-Circuit Duration (Pins 4 to 12)	Continuous
Operating Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
DAC1265AJ, DAC1265LJ	−55°C to +125°C
DAC1265ACJ, DAC1265LCJ	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 13)	TBD

Electrical Characteristics

$V_{SUPPLY} = \pm 15V \pm 5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	DAC1265A Typ (Note 11)	DAC1265A Tested Limit (Note 2)	DAC1265A Design Limit (Note 3)	DAC1265 Typ (Note 11)	DAC1265 Tested Limit (Note 2)	DAC1265 Design Limit (Note 3)	Units
CONVERTER CHARACTERISTICS									
Resolution				12			12		Bits
Linearity Error Max	Zero and Full-Scale Adjusted AJ and LJ Suffix Parts ACJ and LCJ Suffix Parts	4	±⅛	±¼ ±½	±½	±¼	±½ ±¾	±¾	LSB
Differential Non-Linearity Max	Zero and Full-Scale Adjusted		±¼	±½		±½	±¾		
Monotonicity	AJ and LJ Suffix Parts ACJ and LCJ Suffix Parts			**12** 12	**12**		**12** 12	**12**	Bits
Full-Scale (Gain) Error Max	R2 = 50Ω in *Figure 1*	5	±0.1	±0.20		±0.1	±0.20		% Full-Scale
Offset Error Max All Bits OFF, Logic "0"	Unipolar (*Figure 1* Pin 8 Open)	6	±0.01	±0.05		±0.01	±0.05		
	Bipolar (R1 and R2 = 50Ω in *Figure 2*)	7	±0.05	±0.1		±0.05	±0.15		
Zero Error Max MSB ON	Bipolar (R1 and R2 = 50Ω in *Figure 2*)	8	±0.05	±0.1		±0.05	±0.15		
Gain Adjustment Range Min	R2 = 50Ω ± 50Ω in *Figure 1*			±0.2			±0.2		
Bipolar Offset Adjustment Range Min	R1 = 50Ω ± 50Ω and R2 = 50Ω in *Figure 2*			±0.15			±0.15		
Full-Scale (Gain) Temperature Coefficients Max	Using the Internal Reference AJ and LJ Suffix	9	10	**15**		15	**30**		ppm/°C
	ACJ and LCJ Suffix		10		**20**	15		**50**	
Unipolar Offset Temperature Coefficients Max	AJ and LJ Suffix		1	**2**		1	**2**		
	ACJ and LCJ Suffix		1		**2**	1		**2**	
Bipolar Zero Temperature Coefficients Max	AJ and LJ Suffix		5	**10**		5	**10**		
	ACJ and LCJ Suffix		5		**10**	5		**10**	
Output Resistance	Exclusive of Offset and Range R_S		7.5	6 to 10		7.5	6 to 10		kΩ

Electrical Characteristics

(Continued) $V_{SUPPLY} = \pm 15V \pm 5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions	See Note	DAC1265A Typ (Note 11)	DAC1265A Tested Limit (Note 2)	DAC1265A Design Limit (Note 3)	DAC1265 Typ (Note 11)	DAC1265 Tested Limit (Note 2)	DAC1265 Design Limit (Note 3)	Units
Current Output		Unipolar		−2	−1.6 to −2.4		−2	−1.6 to −2.4		mA
		Bipolar		±1.0	±0.8 to ±1.2		±1.0	±0.8 to ±1.2		
Output Capacitance				25			25			pF
Output Noise (FS, 10V Range)		10 Hz to 100 kHz with Internal Reference		40			40			μVrms
Typ Output Voltage Ranges		Using Internal Offset and Range R_S		±2.5, ±5, ±10, 0 to 5, 0 to 10						V
Reference Input Resistance				20.8	15 to 25		20.8	15 to 25		kΩ
Output Compliance Voltage						**−1.5 to 10**			**−1.5 to 10**	V
REFERENCE OUTPUT CHARACTERISTICS										
Reference Voltage	Min	$I_{REF} = 1.5$ mA		10.00	9.90		10.00	9.90		V
	Max				10.10			10.10		
Temperature Coefficient				±8			±12			ppm/°C
Reference Output Current Min					3.0			3.0		mA
Output Resistance Max		$f_O = 1$ kHz, $0.5\text{ mA} \leq I_{REF} \leq 3$ mA		0.05	1.0		0.05	1.0		Ω
DIGITAL AND DC CHARACTERISTICS										
Logic Input Voltage		Logic High Bit ON — AJ and LJ Suffix			**2 to 5.5**			**2 to 5.5**		V
		Logic High Bit ON — ACJ and LCJ Suffix			1.9 to 5.5	**2 to 5.5**		1.9 to 5.5	**2 to 5.5**	
	Max	Logic Low Bit OFF — AJ and LJ Suffix			**0.8**			**0.8**		
		Logic Low Bit OFF — ACJ and LCJ Suffix			1.0	**0.8**		1.0	**0.8**	
Logic Input Current Max		Logic High — AJ and LJ Suffix		150	**300**		150	**300**		μA
		Logic High — ACJ and LCJ Suffix		150	280	**300**	150	280	**300**	
		Logic Low — AJ and LJ Suffix		45	**100**		45	**100**		
		Logic Low — ACJ and LCJ Suffix		45	90	**100**	45	90	**100**	
Power Supply Current Max	I+	V^+ Supply = 15V ± 10%		3	5		3	5		mA
	I−	V^- Supply = −15V ± 10%		−12	−18		−12	−18		
Power Dissipation Max		$V_{SUPPLY} = \pm 15V$		225	345		225	345		mW
Power Supply Sensitivity Max		V^+ Supply = 15V ± 10%	10	±3	±10		±3	±10		ppm of FS/% V_{SUPPLY}
		V^- Supply = −15V ± 10%	10	±15	±25		±15	±25		

Electrical Characteristics (Continued) $V_{SUPPLY} = \pm 15V \pm 5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	DAC1265A			DAC1265			Units
			Typ (Note 11)	Tested Limit (Note 2)	Design Limit (Note 3)	Typ (Note 11)	Tested Limit (Note 2)	Design Limit (Note 3)	
AC CHARACTERISTICS									
Settling Time Max	FSR Change		200		400	200		400	ns
Full-Scale Transition Max	10% to 90% Rise Time Plus Delay Time		15		30	15		30	ns
	90% to 10% Fall Time Plus Delay Time		30		50	30		50	

Note 1: The typical θ_{JA} of the 24-pin package is 80° C/W.

Note 2: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 3: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 4: Linearity error $= \dfrac{V_{OUT} - V_{OFFSET} - (D \times V_{LSB})}{V_{LSB}}$ where $V_{LSB} = \dfrac{V_{FS} - V_{OFFSET}}{4095}$ and D is the digital input (0 to 4095) which produced V_{OUT}.

Note 5: Percent gain error for 10V range $= \dfrac{(V_{FS} - V_{OFFSET}) - (4095/4096)10V}{10V} \times 100.$

Note 6: Unipolar offset error for 10V range $= (V_{OUT}/10V) \times 100$ in percent of full-scale.

Note 7: Bipolar offset error for 10V range $= \dfrac{V_{OUT} - (-5V)}{10V} \times 100$ in percent of full-scale.

Note 8: Bipolar zero error for 10V range $= (V_{OUT}/10V) \times 100$ in percent of full-scale.

Note 9: Gain error tempco $= \dfrac{(V_{FS} - V_{OFFSET}) \text{at} (T_{MAX} \text{ or } T_{MIN}) - (V_{FS} - V_{OFFSET}) \text{ at } 25°C}{10V \text{ range} \times (T_{MAX} \text{ or } T_{MIN} - 25°C)} \times 10^6$ in ppm/°C.

Note 10: Power supply sensitivity for 10V range $= 10^6 \times \dfrac{(V_{FS} - V_{OFFSET}) \text{ at } (16.5V \text{ or } -13.5V) - (V_{FS} - V_{OFFSET}) \text{ at } (13.5V \text{ or } -16.5V)}{10V \times 20\%}$ in ppm of FS/%V_S.

The opposite supply is held at −15V or +15V respectively.

Note 11: Typicals are at 25°C and represent most likely parametric norm.

Note 12: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 13: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description and Applications

1.0 BUFFERED VOLTAGE OUTPUT CONNECTION

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (LF401A) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV maximum offset voltage should be used to keep offset errors below ½ LSB). Unipolar zero will typically be within ±½ LSB (plus op amp offset), and if a 50Ω fixed resistor is substituted for the 100Ω trimmer (R2, *Figure 1*), full-scale accuracy will be within 0.1% (0.20% maximum). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer (R1, *Figure 2*) will give a bipolar zero error typically within ±2 LSB (0.05%).

1.1 Unipolar Configuration *(Figure 1)*

This configuration will provide a unipolar 0V to 9.9976V output range.

Step 1—Offset Adjust (Zero)

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000V (1 LSB = 2.44 mV). In most cases this trim is not needed.

Step 2—Gain Adjust

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976V (full-scale adjusted to 1 LSB less than nominal full-scale of 10.000V). If a 10.2375V full-scale is desired (exactly 2.5 mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

1.2 Bipolar Configuration *(Figure 2)*

This configuration will provide a bipolar output voltage from — 5.000V to 4.9976V, with positive full-scale occurring with all bits ON (all 1s).

Step 1—Offset Adjust

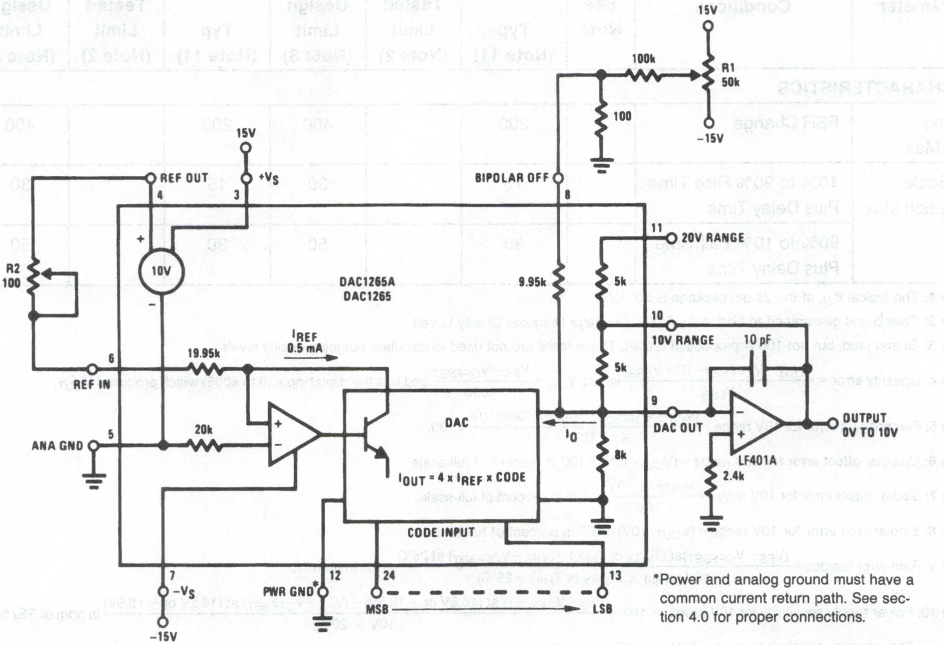
Turn OFF all bits. Adjust 100Ω offset trimmer, R1, to give −5.000V output.

Step 2—Gain Adjust

Turn ON all bits. Adjust 100Ω gain trimmer, R2, to give a reading of 4.9976V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive. Bipolar zero error (MSB bit ON) is not adjusted separately and is typically < ±0.05% of FS after offset and gain adjust.

Functional Description and Applications (Continued)


15V
100k
R1
50k
100
−15V
BIPOLAR OFF
8
15V
REF OUT
4
3
+VS
11
20V RANGE
R2
100
+
10V
−
DAC1265A
DAC1265
9.95k
5k
10
10V RANGE
10 pF
IREF
0.5 mA
19.95k
6
REF IN
5k
9
DAC OUT
OUTPUT
0V TO 10V
ANA GND
5
20k
DAC
IO
8k
LF401A
2.4k
IOUT = 4 x IREF x CODE
CODE INPUT
7
−VS
−15V
12
PWR GND*
24
MSB
13
LSB

*Power and analog ground must have a common current return path. See section 4.0 for proper connections.

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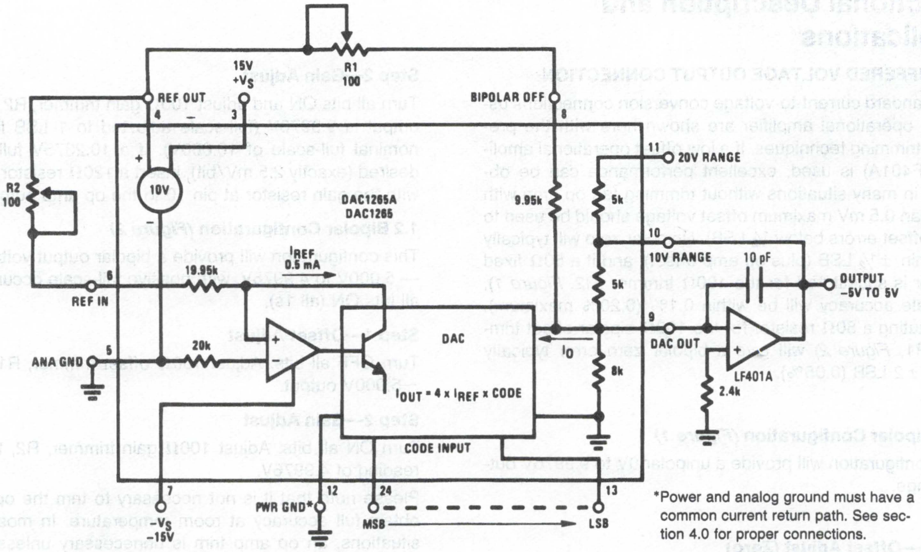
FIGURE 1. 0V to 10V Unipolar Voltage Output


R1
100
15V
+VS
REF OUT
4
3
BIPOLAR OFF
8
11
20V RANGE
+
10V
R2
100
DAC1265A
DAC1265
9.95k
5k
10
10V RANGE
10 pF
IREF
0.5 mA
19.95k
6
REF IN
5k
OUTPUT
−5V TO 5V
9
DAC OUT
ANA GND
5
20k
DAC
IO
8k
LF401A
2.4k
IOUT = 4 x IREF x CODE
CODE INPUT
7
−VS
−15V
12
PWR GND*
24
MSB
13
LSB

*Power and analog ground must have a common current return path. See section 4.0 for proper connections.

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FIGURE 2. ±5V Bipolar Voltage Output

Functional Description and Applications (Continued)

1.3 Other Voltage Ranges *(Figure 3)*

The DAC1265A and DAC1265 can also be easily configured for a unipolar 0V to 5V range or ±2.5V and ±10V bipolar ranges by using the additional 5k application resistor provided at the 20V range R terminal, pin 11. For a 5V range (0V to 5V or ±2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either left open for unipolar or connected through a 100Ω pot to the REF OUT for the bipolar range. For the ± 10V range use the 5k resistors in series by connecting only pin 11 to the op amp output and connecting the bipolar offset as shown. The ±10V option is shown in *Figure 3*.

2.0 INTERNAL/EXTERNAL REFERENCE USE

The performance of the DAC1265A and DAC1265 is specified with the internal reference driving the DAC since all trimming and testing (especially for full-scale error and bipolar operation) is done in this configuration.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5 mA to REF IN and 1.0 mA to BIPOLAR OFFSET, if used). A minimum of 1.5 mA is available for driving external circuits. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% maximum error. The temperature coefficient is comparable to that of the full-scale TC for a particular grade.

3.0 DIGITAL INPUT

The DAC1265A and DAC1265 use a standard positive true straight binary code for unipolar outputs (all 1s give full-scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0s on the inputs, the output will go to negative full-scale; with 100...00 (only the MSB on), the output will be 0.00V; with all 1s, the output will go to positive full-scale.

The threshold of the digital input circuitry is set at 1.4V and does not vary with supply voltage. The input lines can interface with any type of 5V logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in *Figure 4*. The input line can be modeled as a 30 kΩ resistance connected to a −0.7V rail.

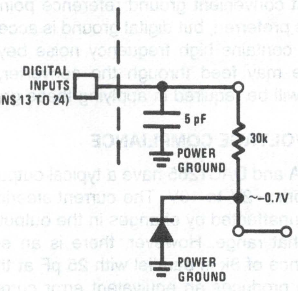
DIGITAL INPUTS (PINS 13 TO 24)
5 pF
30k
POWER GROUND
~−0.7V
TO LOGIC
POWER GROUND

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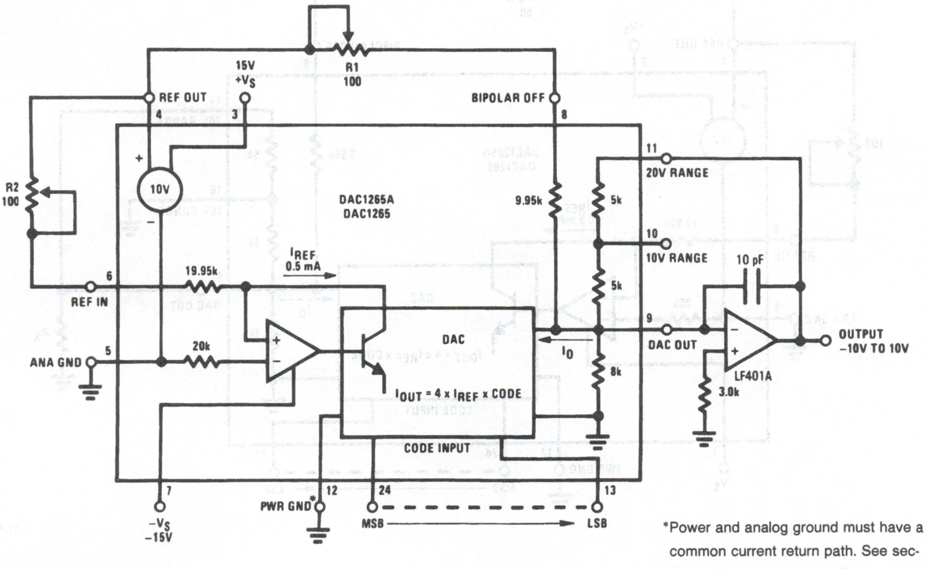
FIGURE 4. Equivalent Digital Input Circuit


R1
100
15V
+VS
REF OUT
4
3
BIPOLAR OFF
8
R2
100
10V
+
−
DAC1265A
DAC1265
9.95k
5k
11
20V RANGE
10
10V RANGE
5k
10 pF
6
19.95k
REF IN
IREF
0.5 mA
5
ANA GND
20k
DAC
IO
IOUT = 4 x IREF x CODE
9
DAC OUT
8k
LF401A
3.0k
OUTPUT
−10V TO 10V
CODE INPUT
7
−VS
−15V
12
PWR GND*
24
MSB
13
LSB

*Power and analog ground must have a common current return path. See section 4.0 for proper connections.

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FIGURE 3. ±10V Voltage Output

Functional Description and Applications (Continued)

4.0 APPLICATION OF ANALOG AND POWER GROUNDS

The DAC1265A and DAC1265 have separate analog and power ground pins to allow optimum connections for low noise and high speed performance. The two ground lines can be separated by up to 200 mV without any loss in performance. There may be some loss in linearity beyond that level. If these DACs are to be used in a system in which the two grounds will be ultimately connected at some distance from the device, it is recommended that parallel back-to-back diodes be connected between the ground lines near the device to prevent a fault condition.

The analog ground at pin 5 is the ground reference point for the internal reference and is thus the "high quality" ground; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground reference point; analog power return is preferred, but digital ground is acceptable. If power ground contains high frequency noise beyond 200 mV, this noise may feed through the converter, so that some caution will be required in applying these grounds.

5.0 OUTPUT VOLTAGE COMPLIANCE

The DAC1265A and DAC1265 have a typical output compliance range from −2V to 10V. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25 pF at the output terminal which produces an equivalent error current if the voltage deviates from power ground. This is a linear effect that does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in non-linear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply.

6.0 DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. *Figure 5* shows a connection using the gain and bipolar output resistors to give a ±1.60V bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 mA to −2 mA unipolar output current and using the 10.0V reference voltage for bipolar offset. For example, setting $R_X = 2.67\ k\Omega$ gives a ±1V range with a 1 kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. Using a 50Ω resistor for R_X would allow interface to a 50Ω cable with a ±50 mV full-scale swing.

7.0 HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the DAC1265A and DAC1265 make them ideal for high speed successive approximation A/D converters. The internal reference and trimmed internal resistors allow a 12-bit converter system to be constructed with a minimum parts count. Shown in *Figure 6* is a configuration using standard components; this system completes a full 12-bit conversion in 10 µs unipolar or bipolar. This converter will be accurate to ±½ LSB of 12 bits and have a typical gain TC of 10 ppm/°C.

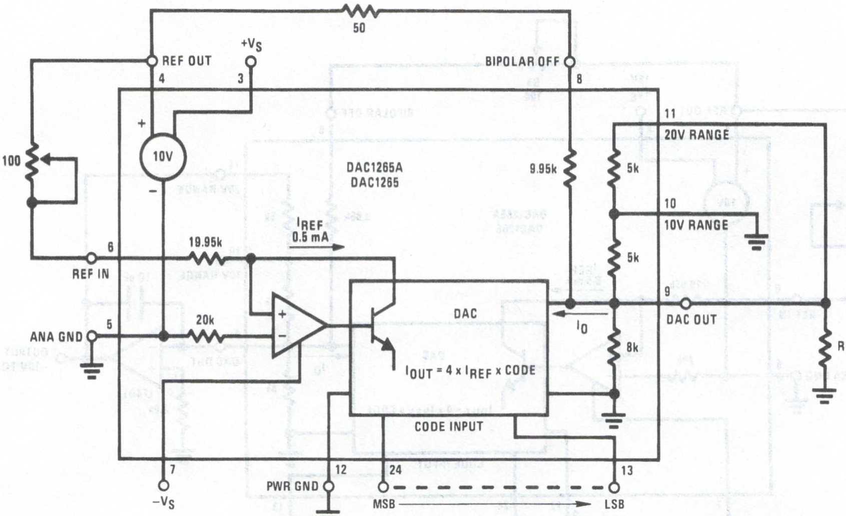

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FIGURE 5. Unbuffered Bipolar Voltage Output

Functional Description and Applications (Continued)

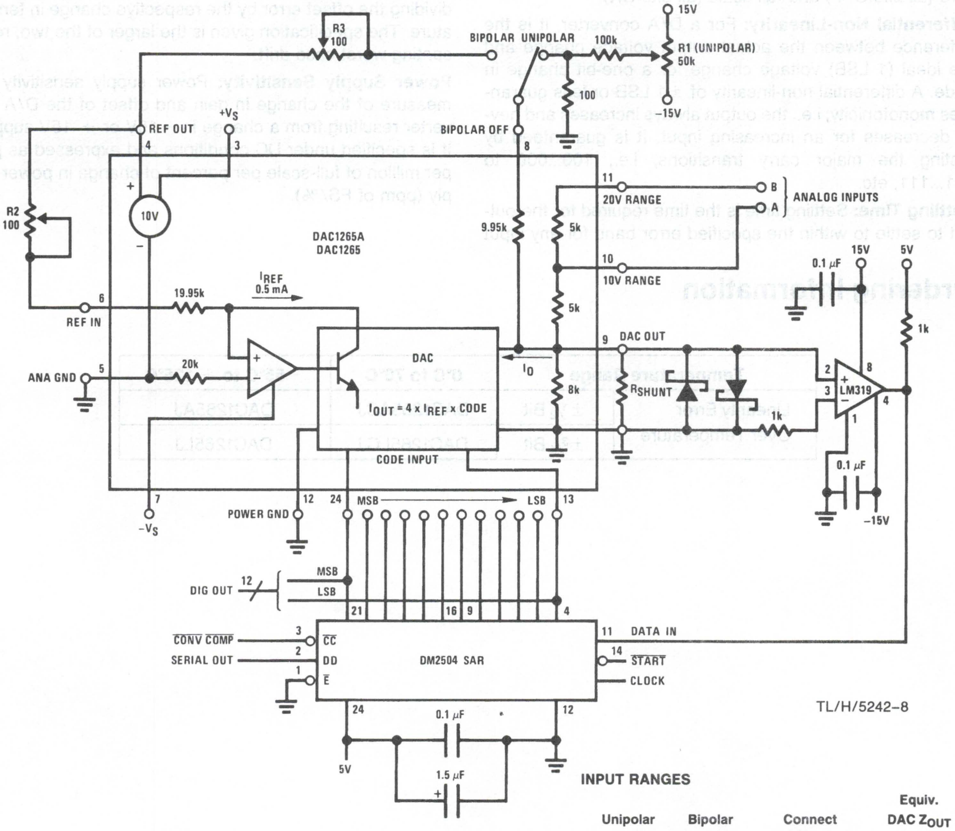
In the unipolar mode, the system range is 0V to 9.9976V, with each bit having a value of 2.44 mV. For true conversion accuracy, an A/D converter should be trimmed so that a given output code results from input levels from ½ LSB below to ½ LSB above the exact voltage represented by that code. Therefore, the converter zero point should be trimmed with an input voltage of 1.22 mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full-scale, use an input voltage of 9.9963V (10V-1 LSB-½ LSB); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is −5.0V to 4.9976V. Bipolar offset trimming is done by applying a −4.9988V input signal and trimming R3 for the LSB transition (all other bits "0").

Full-scale is set by applying 4.9963V and trimming R2 for the LSB transition (all other bits "1"). In many applications, the pretrimmed internal resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 12-bit ±½ LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of 1 kΩ, 1 LSB = 0.5 mV), to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will vary with the input configuration (*Figure 6,* Input Ranges Table).

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the LF411A op amp.


15V
BIPOLAR
UNIPOLAR
100k
R1 (UNIPOLAR)
50k
100
−15V
R3
100
+VS
REF OUT
4
3
BIPOLAR OFF
8
11
20V RANGE
B
A
ANALOG INPUTS
R2
100
10V
9.95k
5k
DAC1265A
DAC1265
10
10V RANGE
15V
5V
0.1 µF
6
19.95k
IREF
0.5 mA
REF IN
5k
1k
9
DAC OUT
ANA GND
5
20k
DAC
IO
8k
RSHUNT
2
8
LM319
3
4
1
IOUT = 4 × IREF × CODE
1k
CODE INPUT
0.1 µF
7
12
24
MSB
LSB
13
−VS
POWER GND
−15V
DIG OUT
12
MSB
LSB
21
16
9
4
CONV COMP
SERIAL OUT
3
2
1
CC
DD
E
DM2504 SAR
11
DATA IN
14
START
CLOCK
24
12
0.1 µF
5V
1.5 µF
TL/H/5242-8

INPUT RANGES

Unipolar	Bipolar	Connect	Equiv. DAC Z_{OUT}
0 to 5	±2.5	Input to A B to DAC OUT	1.60 kΩ
0 to 10	±5	Input to A	2.35 kΩ
0 to 20	±10	Input to B	3.08 kΩ

FIGURE 6. Fast Precision Analog to Digital Converter

Definition of Terms

Digital Inputs: The DAC1265A and DAC1265 accept digital input codes in binary format and may be user connected for any one of three binary codes: straight binary, two's complement, or offset binary.

Digital Input MSB LSB	Analog Output		
	Straight Binary	Offset Binary	Two's Complement*
000 . . 000	zero	−FS (Full-Scale)	zero
011 . . . 111	½ FS−1 LSB	zero−1 LSB	+FS−1 LSB
100 . . 000	½ FS	zero	−FS
111 . . . 111	+FS−1 LSB	+FS−1 LSB	zero−1 LSB

*Invert MSB with external inverter to obtain Two's Complement coding

Linearity Error: Linearity error of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full-scale (all bits ON).

Differential Non-Linearity: For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one-bit change in code. A differential non-linearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input. It is guaranteed by testing the major carry transitions, i.e., 100...000 to 011...111, etc.

Settling Time: Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full-scale or major carry transition.

Gain Tempco: The change in full-scale analog output over the specified temperature range expressed in parts per million of full-scale per °C (ppm of FS/°C). Gain error is measured with respect to 25°C at high (T_{MAX}) and low (T_{MIN}) temperatures. Gain tempco is calculated for both high ($T_{MAX}-25°C$) and low ($25°C-T_{MIN}$) ranges by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst-case drift.

Offset Tempco: The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full-scale per °C (ppm of FS/°C). Offset error is measured with respect to 25°C at high (T_{MAX}) and low (T_{MIN}) temperatures. Offset tempco is calculated for both high ($T_{MAX}-25°C$) and low ($25°C-T_{MIN}$) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity: Power supply sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V or + 15V supplies. It is specified under DC conditions and expressed as parts per million of full-scale per percent of change in power supply (ppm of FS/%).

Ordering Information

Temperature Range		0°C to 70°C	−55°C to + 125°C
Linearity Error Over Temperature	±½ Bit	DAC1265ACJ	DAC1265AJ
	±¾ Bit	DAC1265LCJ	DAC1265LJ

National Semiconductor Corporation

DAC1266A, DAC1266 Hi-Speed 12-Bit D/A Converter

General Description

The DAC1266A and DAC1266 are fast 12-bit digital to analog converters. These DACs use 12 precision high speed bipolar current steering switches, control amplifier, and a thin film resistor network to obtain a high accuracy, very fast analog output current. The DAC1266A and DAC1266 have 10%–90% full-scale transition time under 30 ns and settle to less than ½ LSB in 200 ns.

These digital to analog converters are recommended for applications in CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 5 MHz for full range transitions.

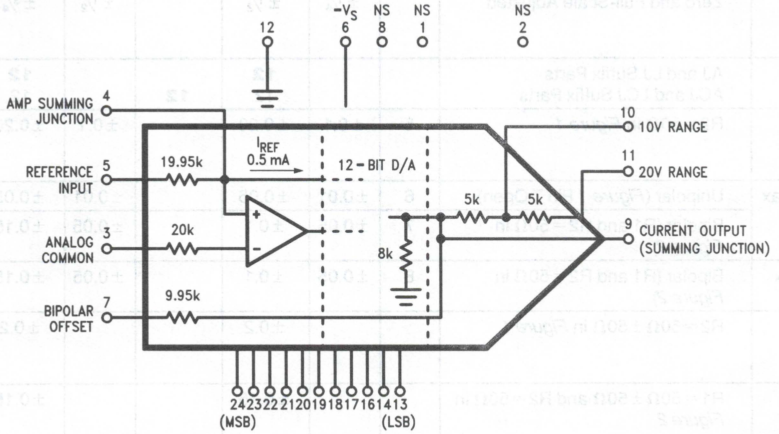
Features

- Bipolar current output DAC
- Fully differential, non-saturating precision current switch — R_{OUT} and C_{OUT} do not change with digital input code
- Precision thin film resistors for use with external op amp for voltage out or as input resistors for a successive approximate A/D converter
- Superior replacement for 12-bit D/A converters of this type

Key Specifications

Resolution and Monotonicity	12 Bits
Linearity (Guaranteed over temperature)	12 Bits
Output Current Settling Time	400 ns max to 0.01%
Full-Scale Transition Time (10%–90%)	30 ns
Power Supply Sensitivity	±15 ppm of FS/% V_{SUPPLY}

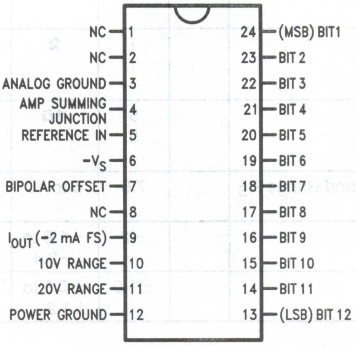
Block and Connection Diagrams



12
$-V_S$ 6
NS 8
NS 1
NS 2
AMP SUMMING JUNCTION 4
REFERENCE INPUT 5
ANALOG COMMON 3
BIPOLAR OFFSET 7
19.95k
20k
9.95k
I_{REF} 0.5 mA
12 - BIT D/A
5k
5k
8k
10 10V RANGE
11 20V RANGE
9 CURRENT OUTPUT (SUMMING JUNCTION)
24 23 22 21 20 19 18 17 16 14 13
(MSB)
(LSB)

TL/H/5068–7

Dual-In-Line Package



NC 1
NC 2
ANALOG GROUND 3
AMP SUMMING JUNCTION 4
REFERENCE IN 5
$-V_S$ 6
BIPOLAR OFFSET 7
NC 8
I_{OUT} (−2 mA FS) 9
10V RANGE 10
20V RANGE 11
POWER GROUND 12
24 (MSB) BIT1
23 BIT 2
22 BIT 3
21 BIT 4
20 BIT 5
19 BIT 6
18 BIT 7
17 BIT 8
16 BIT 9
15 BIT 10
14 BIT 11
13 (LSB) BIT 12

Top View

TL/H/5068–1

Order Number
DAC1266AJ, DAC1266ACJ,
DAC1266LJ or DAC1266LCJ
See NS Package Number J24A

Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V−)	0V to −18V
Current Output (Pin 9) Voltage	−3V, 12V
Logic Input Voltage	−1V, 7V
Reference Input Voltage (Pin 5)	±12V
Analog GND to Power GND	±1V
Bipolar Offset	±12V
10V Range	±12V
20V Range	V− to +24V
Power Dissipation (Note 1)	1000 mW
Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC1266AJ, DAC1266LJ	−55°C to +125°C
DAC1266ACJ, DAC1266LCJ	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD Susceptibility (Note 12)	TBD

Electrical Characteristics

$V_{SUPPLY} = -15V \pm 5\%$ and $V_{REF} = 10.000V$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	DAC1266A Typ	DAC1266A Tested Limit (Note 2)	DAC1266A Design Limit (Note 3)	DAC1266 Typ	DAC1266 Tested Limit (Note 2)	DAC1266 Design Limit (Note 3)	Units
CONVERTER CHARACTERISTICS									
Resolution				12			12		Bits
Linearity Error Max	Zero and Full-Scale Adjusted	4							LSB
	AJ and LJ Suffix Parts		±⅛	±¼ **±½**		±¼	±½ **±¾**		
	ACJ and LCJ Suffix Parts				**±½**			**±¾**	
Differential Non-Linearity Max	Zero and Full-Scale Adjusted		±¼	±½		±½	±¾		
Monotonicity	AJ and LJ Suffix Parts			**12**			**12**		Bits
	ACJ and LCJ Suffix Parts			12	**12**		12	**12**	
Full-Scale (Gain) Error Max	R2 = 50Ω in *Figure 1*	5	±0.1	±0.20		±0.1	±0.20		% Full-Scale
Offset Error Max All Bits OFF, Logic "0"	Unipolar (*Figure 1* Pin 7 Open)	6	±0.01	±0.05		±0.01	±0.05		
	Bipolar (R1 and R2 = 50Ω in *Figure 2*)	7	±0.05	±0.1		±0.05	±0.15		
Zero Error Max MSB ON	Bipolar (R1 and R2 = 50Ω in *Figure 2*)	8	±0.05	±0.1		±0.05	±0.15		
Gain Adjustment Range Min	R2 = 50Ω ± 50Ω in *Figure 1*			±0.2			±0.2		
Bipolar Offset Adjustment Range Min	R1 = 50Ω ± 50Ω and R2 = 50Ω in *Figure 2*			±0.15			±0.15		
Full-Scale (Gain) Temperature Coefficients Max	AJ and LJ Suffix	9	1	**3**		5	**10**		ppm/°C
	ACJ and LCJ Suffix		1		**3**	5		**10**	
Unipolar Offset Temperature Coefficients Max	AJ and LJ Suffix		1	**2**		1	**2**		
	ACJ and LCJ Suffix		1		**2**	1		**2**	
Bipolar Zero Temperature Coefficients Max	AJ and LJ Suffix		5	**10**		5	**10**		
	ACJ and LCJ Suffix		5		**10**	5		**10**	
Output Resistance	Exclusive of Offset and Range R_S		7.5	6 to 10		7.5	6 to 10		kΩ
Current Output	Unipolar		−2	−1.6 to −2.4		−2	−1.6 to −2.4		mA
	Bipolar		±1.0	±0.8 to ±1.2		±1.0	±0.8 to ±1.2		

Electrical Characteristics (Continued) $V_{SUPPLY} = -15V \pm 5\%$ and $V_{REF} = 10.000V$ unless otherwise noted.

Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$. For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	DAC1266A Typ	DAC1266A Tested Limit (Note 2)	DAC1266A Design Limit (Note 3)	DAC1266 Typ	DAC1266 Tested Limit (Note 2)	DAC1266 Design Limit (Note 3)	Units
Output Capacitance			25			25			pF
Typ Output Voltage Ranges	Using Internal Offset and Range R_S		±2.5, ±5, ±10, 0 to 5, 0 to 10						V
Reference Input Resistance			20.8	15 to 25		20.8	15 to 25		kΩ
Output Compliance Voltage					**−1.5 to 10**			**−1.5 to 10**	V
DIGITAL AND DC CHARACTERISTICS									
Logic Input Voltage	Logic High Bit ON, AJ and LJ Suffix			**2 to 5.5**			**2 to 5.5**		V
	Logic High Bit ON, ACJ and LCJ Suffix			1.9 to 5.5	**2 to 5.5**		1.9 to 5.5	**2 to 5.5**	
Max	Logic Low Bit OFF, AJ and LJ Suffix			**0.8**			**0.8**		
	Logic Low Bit OFF, ACJ and LCJ Suffix			1.0	**0.8**		1.0	**0.8**	
Logic Input Current Max	Logic High, AJ and LJ Suffix		150	**300**		150	**300**		µA
	Logic High, ACJ and LCJ Sufix		150	280	**300**	150	280	**300**	
	Logic Low, AJ and LJ Suffix		45	**100**		45	**100**		
	Logic Low, ACJ and LCJ Suffix		45	90	**100**	45	90	**100**	
Power Supply Current Max	V^- Supply $= -15V \pm 10\%$		−12	−18		−12	−18		mA
Power Dissipation Max	V^- Supply $= -15V$		180	270		180	270		mW
Power Supply Sensitivity Max	V^- Supply $= -12V \pm 5\%$	10	±15	±25		±15	±25		ppm of FS/% V_{SUPPLY}
	V^- Supply $= -15V \pm 10\%$	10	±15	±25		±15	±25		
AC CHARACTERISTICS									
Settling Time Max	FSR Change		200		400	200		400	ns
Full-scale Transition Max	Delay Plus 10% to 90% Rise Time		15		30	15		30	
	Delay Plus 90% to 10% Fall Time		30		50	30		50	ns

Note 1: The typical θ_{JA} of the 24-pin package is 80° C/W.

Note 2: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 3: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 4: Linearity error $= \dfrac{V_{OUT} - V_{OFFSET} - (D \times V_{LSB})}{V_{LSB}}$ where $V_{LSB} = \dfrac{V_{FS} - V_{OFFSET}}{4095}$ and D is the digital input (0 to 4095) which produced V_{OUT}.

Note 5: Percent gain error for 10V range $= \dfrac{(V_{FS} - V_{OFFSET}) - (4095/4096)V_{REF}}{V_{REF}} \times 100.$

Note 6: Unipolar offset error for 10V range $= (V_{OUT}/V_{REF}) \times 100$ in percent of full-scale.

Note 7: Bipolar offset error for 10V range $= \dfrac{V_{OUT} - (-V_{REF}/2)}{V_{REF}} \times 100$ in percent of full-scale.

Note 8: Bipolar zero error for 10V range $= (V_{OUT}/V_{REF}) \times 100$ in percent of full-scale.

Note 9: Gain error tempco $= \dfrac{(V_{FS} - V_{OFFSET}) \text{ at } (T_{MAX} \text{ or } T_{MIN}) - (V_{FS} - V_{OFFSET}) \text{ at } 25°C}{10V \text{ range} \times (T_{MAX} \text{ or } T_{MIN} - 25°C)} \times 10^6$ in ppm/°C.

Note 10: Power supply sensitivity for 10V range $= 10^6 \times \dfrac{(V_{FS} - V_{OFFSET}) \text{ at } (-13.5V) - (V_{FS} - V_{OFFSET}) \text{ at } (-16.5V)}{V_{REF} \times 20\%}$ in ppm of FS/% V_S.

Note 11: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 12: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description and Applications

1.0 BUFFERED VOLTAGE OUTPUT CONNECTION

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (LF401A) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV maximum offset voltage should be used to keep offset errors below ½ LSB). Unipolar zero will typically be within ±½ LSB (plus op amp offset), and if a 50Ω fixed resistor is substituted for the 100Ω trimmer (R2, *Figure 1*), full-scale accuracy will be within 0.1% (0.20% maximum). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer (R1, *Figure 2*) will give a bipolar zero error typically within ±2 LSB (0.05%).

1.1 Unipolar Configuration (*Figure 1*)

This configuration will provide a unipolar 0V to 9.9976V output range.

Step 1—Offset Adjust (Zero)

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000V (1 LSB = 2.44 mV). In most cases this trim is not needed.

Step 2—Gain Adjust

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976V (full-scale adjusted to 1 LSB less than nominal full-scale of 10.000V). If a 10.2375V full-scale is desired (exactly 2.5 mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output or use the LH0071 voltage reference.

1.2 Bipolar Configuration (*Figure 2*)

This configuration will provide a bipolar output voltage from −5.000V to 4.9976V, with positive full-scale occurring with all bits ON (all 1s).

Step 1—Offset Adjust

Turn OFF all bits. Adjust 100Ω offset trimmer, R1, to give −5.000V output.

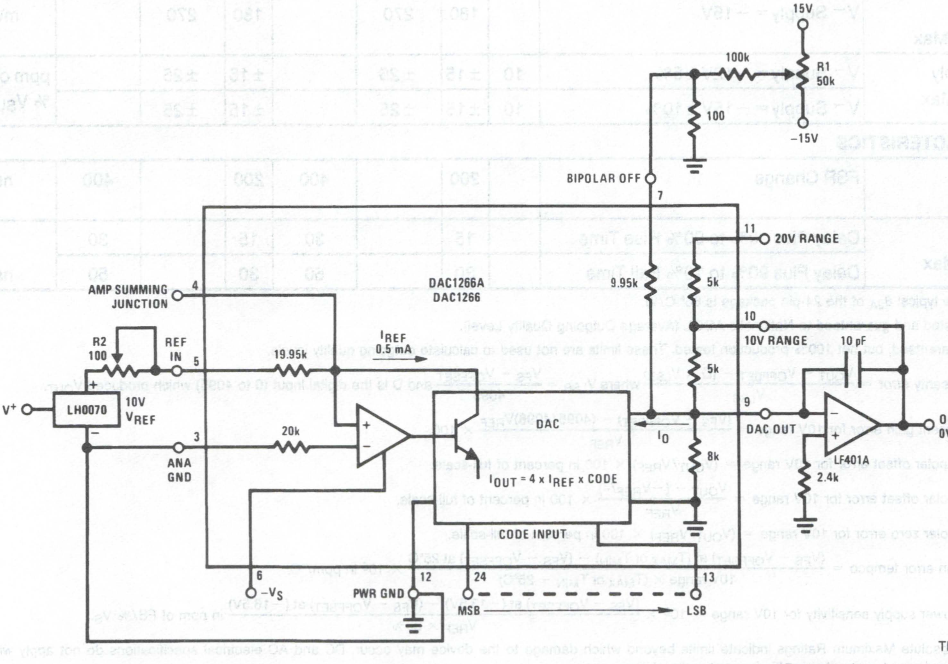
Step 2—Gain Adjust

Turn ON all bits. Adjust 100Ω gain trimmer, R2, to give a reading of 4.9976V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive. Bipolar zero error (MSB bit ON) is not adjusted separately and is typically <±0.05% of FS after offset and gain adjust.

1.3 Other Voltage Ranges (*Figure 3*)

The DAC1266A and DAC1266 can also be easily configured for a unipolar 0V to 5V range or ±2.5V and ±10V bipolar ranges by using the additional 5k application resistor provided at the 20V range R terminal, pin 11. For a 5V span (0V to 5V or ±2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either left open for unipolar or connected through a 100Ω pot to the external



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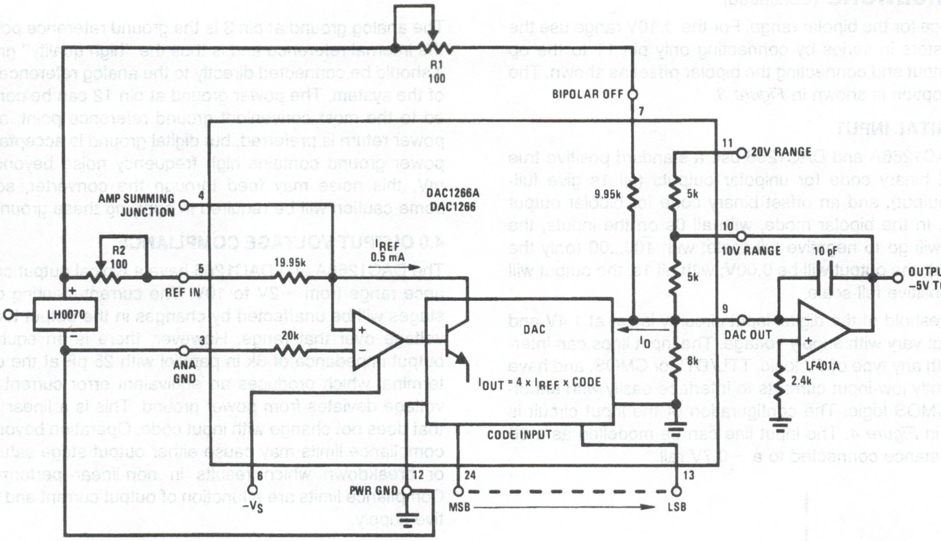
*Power and analog ground must have a common current return path. See section 3.0 for proper connections.

FIGURE 1. 0V to 10V Unipolar Voltage Output

Functional Description and Applications (Continued)


R1
100
BIPOLAR OFF
7
11
20V RANGE
9.95k
5k
DAC1266A
DAC1266
AMP SUMMING
JUNCTION
4
10
10V RANGE
10 pF
R2
100
5
REF IN
19.95k
I_{REF}
0.5 mA
OUTPUT
−5V TO 5V
V+
LH0070
+
9
20k
3
DAC
I_O
DAC OUT
+
LF401A
ANA
GND
8k
2.4k
$I_{OUT} = 4 \times I_{REF} \times CODE$
CODE INPUT
6
12
24
13
PWR GND
−V_S
MSB
LSB

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*Power and analog ground must have a common current return path. See section 3.0 for proper connections.

FIGURE 2. ±5V Bipolar Voltage Output

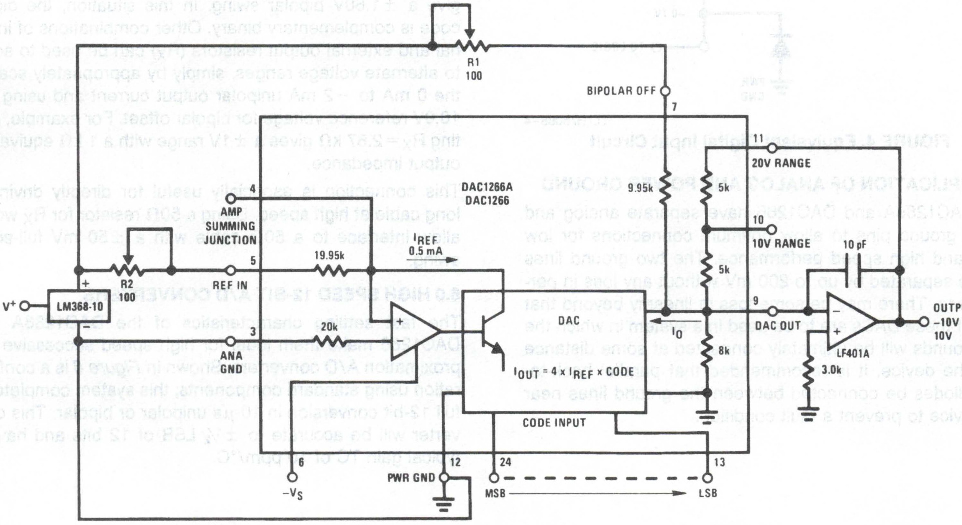
R1
100
BIPOLAR OFF
7
11
20V RANGE
DAC1266A
DAC1266
9.95k
5k
4
AMP
SUMMING
JUNCTION
10
10V RANGE
10 pF
REF
0.5 mA
5
19.95k
R2
100
REF IN
+
V+
LM368-10
9
OUTPUT
−10V TO
10V
DAC
20k
3
ANA
GND
I_O
DAC OUT
+
LF401A
8k
3.0k
$I_{OUT} = 4 \times I_{REF} \times CODE$
CODE INPUT
6
12
24
13
PWR GND
−V_S
MSB
LSB

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FIGURE 3. ±10V Voltage Output

*Power and analog ground must have a common current return path. See section 3.0 for proper connections.

Functional Description and Applications (Continued)

reference for the bipolar range. For the ±10V range use the 5k resistors in series by connecting only pin 11 to the op amp output and connecting the bipolar offset as shown. The ±10V option is shown in *Figure 3.*

2.0 DIGITAL INPUT

The DAC1266A and DAC1266 use a standard positive true straight binary code for unipolar outputs (all 1s give full-scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0s on the inputs, the output will go to negative full-scale; with 100...00 (only the MSB on), the output will be 0.00V; with all 1s, the output will go to positive full-scale.

The threshold of the digital input circuitry is set at 1.4V and does not vary with supply voltage. The input lines can interface with any type of 5V logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in *Figure 4.* The input line can be modelled as a 30 kΩ resistance connected to a −0.7V rail.

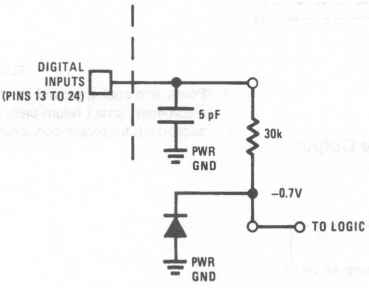

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FIGURE 4. Equivalent Digital Input Circuit

3.0 APPLICATION OF ANALOG AND POWER GROUND

The DAC1266A and DAC1266 have separate analog and power ground pins to allow optimum connections for low noise and high speed performance. The two ground lines can be separated by up to 200 mV without any loss in performance. There may be some loss in linearity beyond that level. If these DACs are to be used in a system in which the two grounds will be ultimately connected at some distance from the device, it is recommended that parallel back-to-back diodes be connected between the ground lines near the device to prevent a fault condition.

The analog ground at pin 3 is the ground reference point for the internal reference and is thus the "high quality" ground; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground reference point; analog power return is preferred, but digital ground is acceptable. If power ground contains high frequency noise beyond 200 mV, this noise may feed through the converter, so that some caution will be required in applying these grounds.

4.0 OUTPUT VOLTAGE COMPLIANCE

The DAC1266A and DAC1266 have a typical output compliance range from −2V to 10V. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25 pF at the output terminal which produces an equivalent error current if the voltage deviates from power ground. This is a linear effect that does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in non-linear performance. Compliance limits are a function of output current and negative supply.

5.0 DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. *Figure 5* shows a connection using the gain and bipolar output resistors to give a ±1.60V bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 mA to −2 mA unipolar output current and using the 10.0V reference voltage for bipolar offset. For example, setting $R_X = 2.67$ kΩ gives a ±1V range with a 1 kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. Using a 50Ω resistor for R_X would allow interface to a 50Ω cable with a ±50 mV full-scale swing.

6.0 HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the DAC1266A and DAC1266 make them ideal for high speed successive approximation A/D converters. Shown in *Figure 6* is a configuration using standard components; this system completes a full 12-bit conversion in 10 µs unipolar or bipolar. This converter will be accurate to ±½ LSB of 12 bits and have a typical gain TC of 10 ppm/°C.

Functional Description and Applications (Continued)

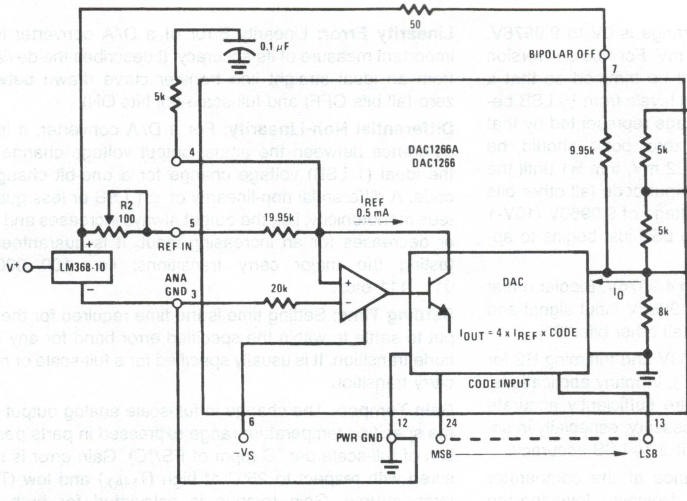
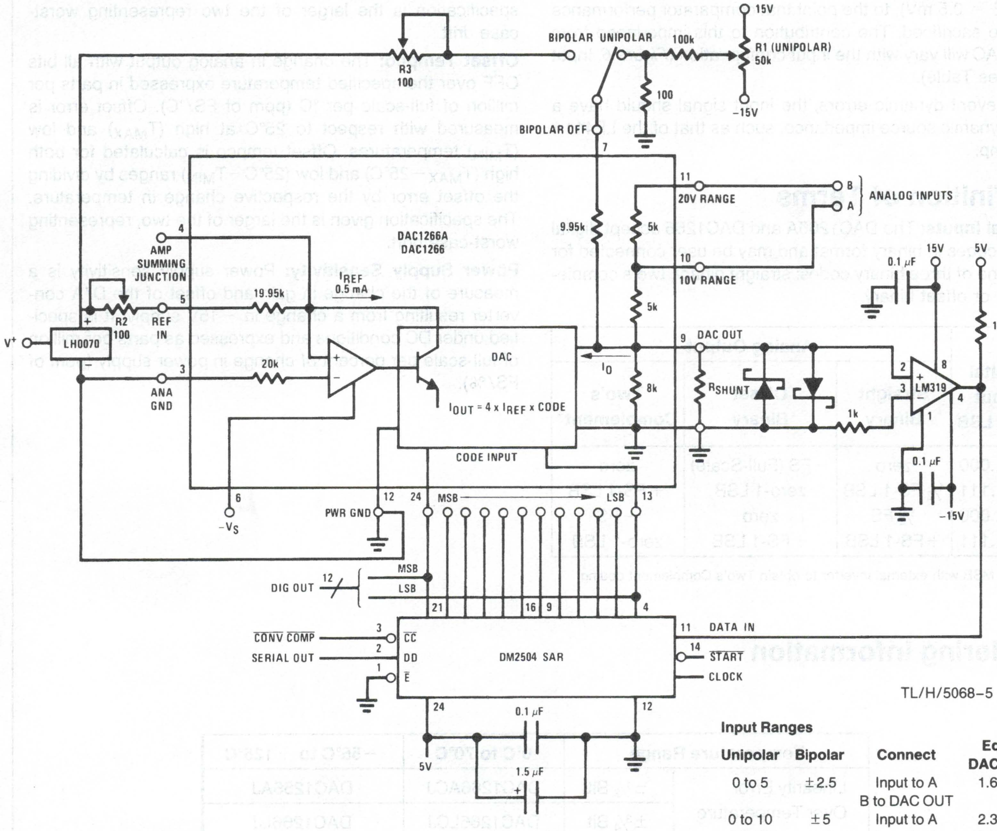

50
0.1 µF
BIPOLAR OFF
7
5k
11
20V RANGE
DAC1266A
DAC1266
4
9.95k
5k
10
10V RANGE
R2
100
I_REF
0.5 mA
5
19.95k
5k
REF IN
V+
LM368-10
ANA GND
3
20k
DAC
9
DAC OUT
I_O
8k
R_X
I_OUT = 4 x I_REF x CODE
CODE INPUT
6
12
24
13
PWR GND
-V_S
MSB
LSB

FIGURE 5. Unbuffered Bipolar Voltage Output


15V
BIPOLAR
UNIPOLAR
100k
R1 (UNIPOLAR)
50k
R3
100
100
-15V
BIPOLAR OFF
7
11
B
A
ANALOG INPUTS
20V RANGE
9.95k
5k
4
AMP SUMMING JUNCTION
DAC1266A
DAC1266
10
10V RANGE
15V
5V
0.1 µF
I_REF
0.5 mA
19.95k
5
5k
1k
R2
100
REF IN
V+
LH0070
20k
3
DAC
9
DAC OUT
ANA GND
I_O
8k
R_SHUNT
2
8
3
LM319
4
1
1k
I_OUT = 4 x I_REF x CODE
CODE INPUT
0.1 µF
6
12
24
MSB
LSB
13
-15V
PWR GND
-V_S
12
MSB
LSB
DIG OUT
21
16
9
4
3
CONV COMP
CC
11
DATA IN
2
SERIAL OUT
DD
DM2504 SAR
14
START
1
E
CLOCK
24
12
0.1 µF
1.5 µF
5V

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Input Ranges

Unipolar	Bipolar	Connect	Equiv. DAC Z_{OUT}
0 to 5	±2.5	Input to A B to DAC OUT	1.60 kΩ
0 to 10	±5	Input to A	2.35 kΩ
0 to 20	±10	Input to B	3.08 kΩ

FIGURE 6. Fast Precision Analog to Digital Converter

Functional Description and Applications (Continued)

In the unipolar mode, the system range is 0V to 9.9976V, with each bit having a value of 2.44 mV. For true conversion accuracy, an A/D converter should be trimmed so that a given output code results from input levels from ½ LSB below to ½ LSB above the exact voltage represented by that code. Therefore, the converter zero point should be trimmed with an input voltage of 1.22 mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full-scale, use an input voltage of 9.9963V (10V-1 LSB-½ LSB); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is −5.0V to 4.9976V. Bipolar offset trimming is done by applying a −4.9988V input signal and trimming R3 for the LSB transition (all other bits "0").

Full-scale is set by applying a 4.9963V and trimming R2 for the LSB transition (all other bits "1"). In many applications, the pretrimmed internal resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 12-bit ±½ LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of 1 kΩ, 1 LSB = 0.5 mV), to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will vary with the input configuration (*Figure 6*, Input Ranges Table).

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the LF411A op amp.

Definition of Terms

Digital Inputs: The DAC1266A and DAC1266 accept digital input codes in binary format and may be user connected for any one of three binary codes: straight binary, two's complement, or offset binary.

Digital Input MSB LSB	Analog Output		
	Straight Binary	**Offset Binary**	**Two's Complement***
000...000	zero	−FS (Full-Scale)	zero
011...111	½ FS-1 LSB	zero-1 LSB	+FS-1 LSB
100...000	½ FS	zero	−FS
111...111	+FS-1 LSB	+FS-1 LSB	zero-1 LSB

*Invert MSB with external inverter to obtain Two's Complement coding

Linearity Error: Linearity Error of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full-scale (all bits ON).

Differential Non-Linearity: For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one-bit change in code. A differential non-linearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input. It is guaranteed by testing the major carry transitions; i.e., 100...000 to 011...111 etc.

Settling Time: Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full-scale or major carry transition.

Gain Tempco: The change in full-scale analog output over the specified temperature range expressed in parts per million of full-scale per °C (ppm of FS/°C). Gain error is measured with respect to 25°C at high (T_{MAX}) and low (T_{MIN}) temperatures. Gain tempco is calculated for both high (T_{MAX}−25°C) and low (25°C−T_{MIN}) ranges by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst-case drift.

Offset Tempco: The change in analog output with all bits OFF over the specified temperature expressed in parts per million of full-scale per °C (ppm of FS/°C). Offset error is measured with respect to 25°C at high (T_{MAX}) and low (T_{MIN}) temperatures. Offset tempco is calculated for both high (T_{MAX}−25°C) and low (25°C−T_{MIN}) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity: Power supply sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V supply. It is specified under DC conditions and expressed as parts per million of full-scale per percent of change in power supply (ppm of FS/%).

Ordering Information

Temperature Range		0°C to 70°C	−55°C to +125°C
Linearity Error Over Temperature	±½ Bit	DAC1266ACJ	DAC1266AJ
	±¾ Bit	DAC1266LCJ	DAC1266LJ

National Semiconductor Corporation

ADVANCED INFORMATION

DAC1655 16-Bit D/A Converter

General Description

The DAC1655 is a 16-bit digital-to-analog converter. The DAC1655 consists of CMOS switches and thin film SiCr resistors connected to form a 4k potentiometer with an output impedance of 40 kΩ. This 16-bit D/A converter is monotonic to 16 bits over the specified temperature range. Force and sense functions minimize gain and offset errors.

The analog output voltage range is GND to the applied voltage reference.

The power dissipation is 28 mW at 10V supply. The power dissipation of each internal resistor does not change regardless of input data code which results in very low superposition error.

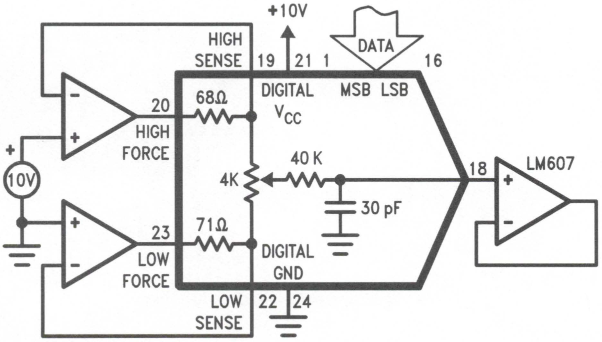
These digital-to-analog converters are recommended as 16-bit digitally controlled potentiometers. They look identical to mechanical potentiometers within the digital supply common mode voltage range.

The DAC1655 is also ideal for applications in precision instruments and data acquisition systems.

Features

- 16-bit monotonicity over temperature
- Full potentiometer capability
- Single 5V to 15V supply operation
- 0V to 10V output with constant 40 kΩ output impedance
- Offset error: ±0.002% of full scale
- Full scale error: ±0.003% of full scale
- Full scale tempco: ±0.3 ppm/°C
- Integral nonlinearity: ±0.012% or ±0.05%
- Settling time: 14 μs to 16 bits
- Output noise: 25 nV/$\sqrt{Hz}$
- Supply current: 300 μA
- STD 0.6″ 24-pin dual-in-line package

Typical Application


+10V
DATA
HIGH SENSE
19
21
1
16
DIGITAL VCC
MSB LSB
20
68Ω
HIGH FORCE
10V
4K
40 K
30 pF
18
LM607
23
71Ω
LOW FORCE
DIGITAL GND
LOW SENSE
22
24

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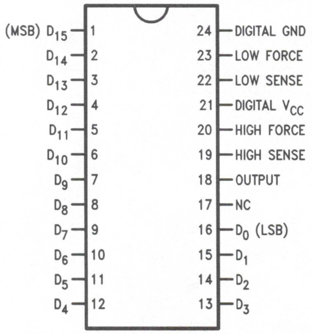
Connection Diagram

Dual-In-Line Package


(MSB) D15 1
D14 2
D13 3
D12 4
D11 5
D10 6
D9 7
D8 8
D7 9
D6 10
D5 11
D4 12
24 DIGITAL GND
23 LOW FORCE
22 LOW SENSE
21 DIGITAL VCC
20 HIGH FORCE
19 HIGH SENSE
18 OUTPUT
17 NC
16 D0 (LSB)
15 D1
14 D2
13 D3

TL/H/9286-2

Top View

Section 5

Sample and Hold

Section 5 Contents

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LH0023/LH0023C/LH0043/LH0043C Sample and Hold Circuits 5-22
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LH0094 Multifunction Converter 5-29

Sample and Hold Definition of Terms

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the "hold" logic command.

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is 5V.

National Semiconductor Corporation

Sample and Hold Selection Guide

	LF198A	LF398A	LF198	LF398	LF298	Units
Accuracy Gain/Offset Error	0.01	0.01	0.02	0.02	0.02	% Max
Offset Voltage	2	3	5	10	5	mV Max
Droop Rate (25°C)						
$C_S = 1000$ pF	30	30	30	30	30	mV/sec
$C_S = 10000$ pF	3	3	3	3	3	
Acquisition Time (25°C)						
$C_S = 1000$ pF	4	4	4	4	4	µs
$C_S = 10000$ pF	20	20	20	20	20	
Aperture Time (25°C)	25	25	25	25	25	ns
Temperature Range	−55 to +125	0 to +70	−55 to +125	0 to +70	−25 to +85	°C
Comment	Low Drift	Low Drift	General Purpose	General Purpose	Low Drift	

National Semiconductor Corporation

LF198/LF298/LF398, LF198A/LF398A Monolithic Sample and Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample and hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 µF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

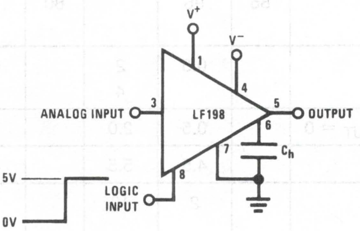
Features

- Operates from ±5V to ±18V supplies
- Less than 10 µs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01 µF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

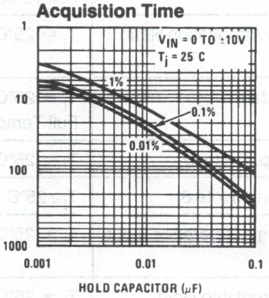
Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

An "A" version is available with tightened electrical specifications.

Typical Connection and Performance Curve



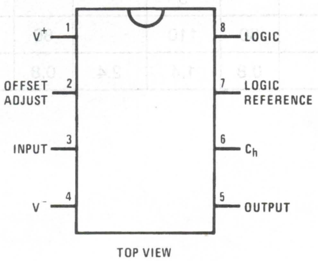
Acquisition Time



TL/H/5692-2

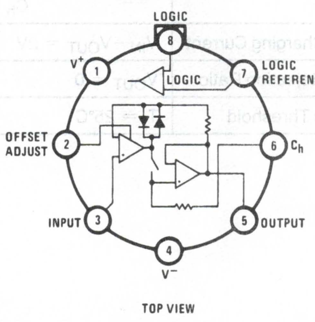
Connection Diagrams

Dual-In-Line Package



Order Number LF398N or LF398AN
See NS Package Number N08E

Metal Can Package



TL/H/5692-11

Order Number LF198H, LF298H,
LF398H, LF198AH or LF398AH
See NS Package Number H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 1)	500 mW
Operating Ambient Temperature Range	
LF198/LF198A	−55°C to +125°C
LF298	−25°C to +85°C
LF398/LF398A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 2)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering, 10 seconds)	260°C
Thermal Resistance (θ_{JA}) (typicals)	
H package	215°C/W (Board mount in still air) 85°C/W (Board mount in 400LF/min air flow)
N package	115°C/W
θ_{JC} (typical)	20°C/W

Electrical Characteristics (Note 3)

Parameter	Conditions	LF198/LF298			LF398			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\ \mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000\ pF$		4			4		μs
	$C_h = 0.01\ \mu F$		20			20		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Electrical Characteristics (Continued) (Note 3)

Parameter	Conditions	LF198A			LF398A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 6)	$T_j = 25°C$ Full Temperature Range		1	1 2		2	2 3	mV mV
Input Bias Current, (Note 6)	$T_j = 25°C$ Full Temperature Range		5	25 75		10	25 50	nA nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$ Full Temperature Range		0.002	0.005 0.01		0.004	0.005 0.01	% %
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\ \mu F$	86	96		86	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode Full Temperature Range		0.5	1 4		0.5	1 6	Ω Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	1		1.0	1	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF $C_h = 0.01\ \mu F$		4 20	6 25		4 20	6 25	μs μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	90	110		90	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum junction temperature of the LF198/LF198A is 150°C, for the LF298, 115°C, and for the LF398/LF398A, 100°C. When operating at elevated ambient temperature, the power dissipation must be derated based on a thermal resistance (Θ_{jA}) of 150°C/W.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 3: Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\ \mu F$, and $R_L = 10\ k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

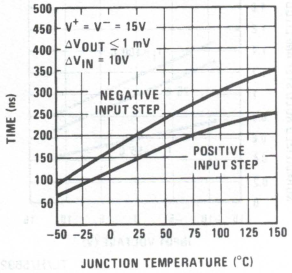
Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters guaranteed over a supply voltage range of ±5 to ±18V, and an input range of $-V_S + 3.5V \leq V_{IN} \leq +V_S - 3.5V$.

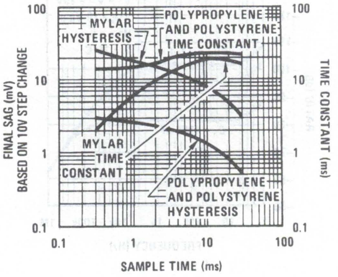
Typical Performance Characteristics

Aperture Time*

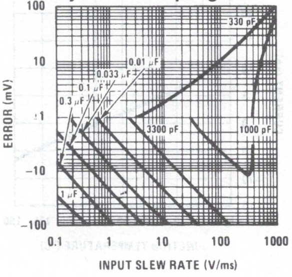


*See Definition of Terms

Dielectric Absorption Error in Hold Capacitor

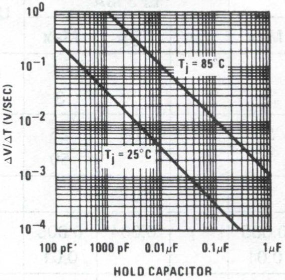


Dynamic Sampling Error

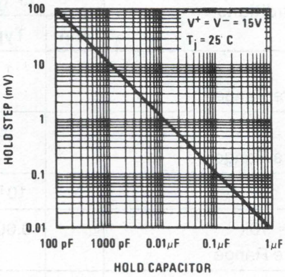


TL/H/5692-3

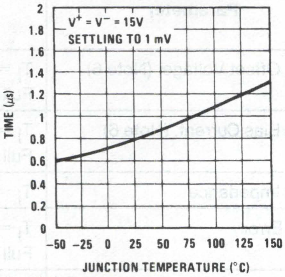
Typical Performance Characteristics (Continued)



Output Droop Rate

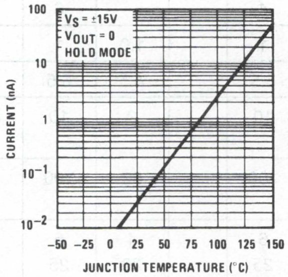


Hold Step

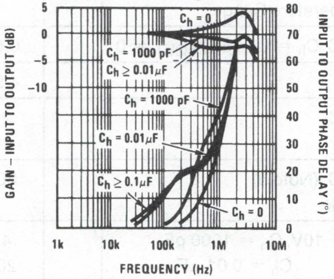


"Hold" Settling Time*

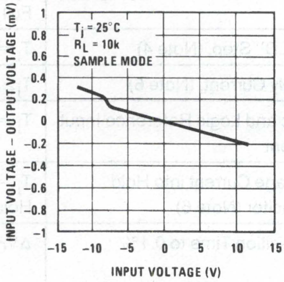
*See definition



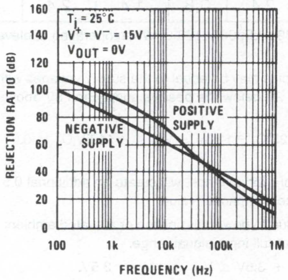
Leakage Current into Hold Capacitor



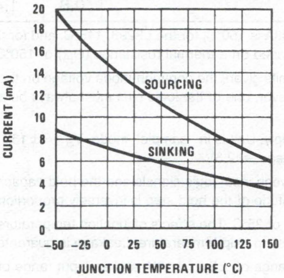
Phase and Gain (Input to Output, Small Signal)



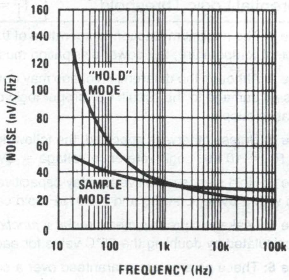
Gain Error



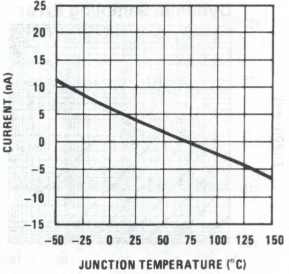
Power Supply Rejection



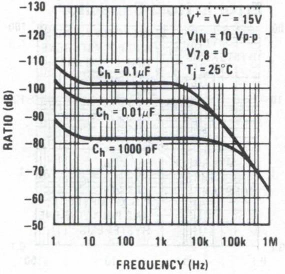
Output Short Circuit Current



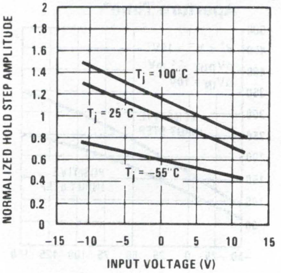
Output Noise



Input Bias Current



Feedthrough Rejection Ratio (Hold Mode)



Hold Step vs Input Voltage

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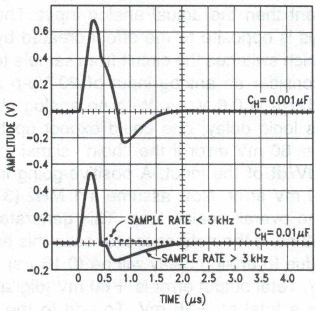
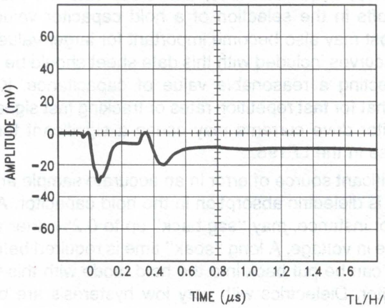
Typical Performance Characteristics (Continued)

Output Transient at Start of Sample Mode



TL/H/5692–12

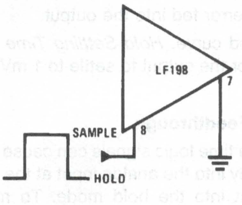
Output Transient at Start of Hold Mode



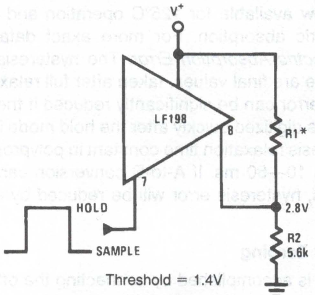
TL/H/5692–13

Logic Input Configurations

TTL & CMOS
3V ≤ V_L (Hi State) ≤ 7V


LF198
7
SAMPLE
8
HOLD

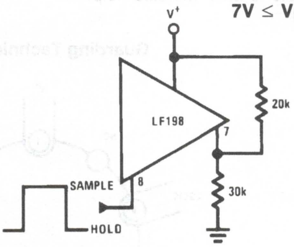
Threshold = 1.4V


V+
LF198
8
7
R1*
HOLD
2.8V
SAMPLE
R2
5.6k

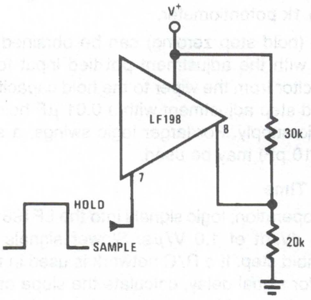
Threshold = 1.4V

*Select for 2.8V at pin 8

CMOS
7V ≤ V_L (Hi State) ≤ 15V

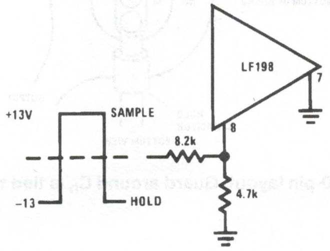

V+
LF198
20k
7
SAMPLE
8
30k
HOLD

Threshold = 0.6 (V+) + 1.4V

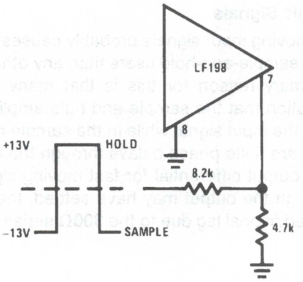

V+
LF198
8
30k
7
HOLD
SAMPLE
20k

Threshold = 0.6 (V+) − 1.4V

Op Amp Drive


LF198
7
+13V
SAMPLE
8
8.2k
−13
HOLD
4.7k

Threshold ≈ +4V


LF198
7
8
+13V
HOLD
8.2k
−13V
SAMPLE
4.7k

Threshold = −4V

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Application Hints

Hold Capacitor

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with > 1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. "NPO" or "COG" capacitors are now available for 125°C operation and also have low dielectric absorption. For more exact data, see the curve *Dielectric Absorption Error.* The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10—50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC and AC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01 μF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

Logic Rise Time

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 1.0 V/μs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/μs.

Sampling Dynamic Signals

Sample error to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1 μs) (0.6V/μs) = 60 mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 μs) (0.6 V/μs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportioned to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

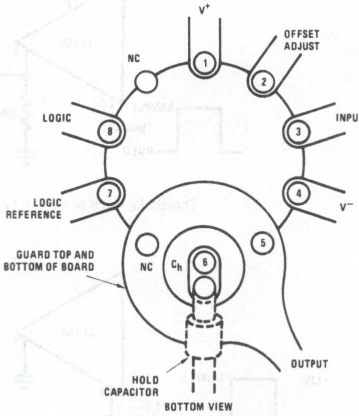
A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1 mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1 mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

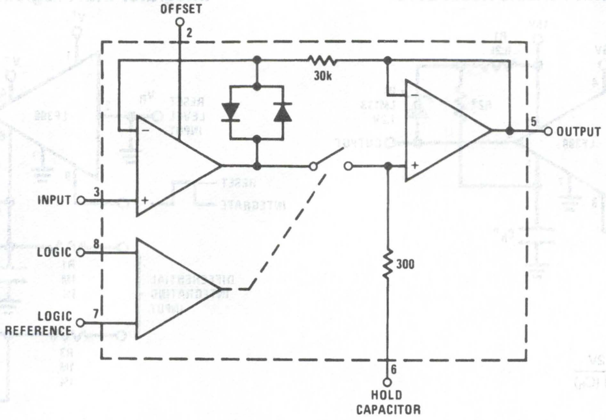
Guarding Technique



TL/H/5692-5

Use 10-pin layout. Guard around C_h is tied to output.

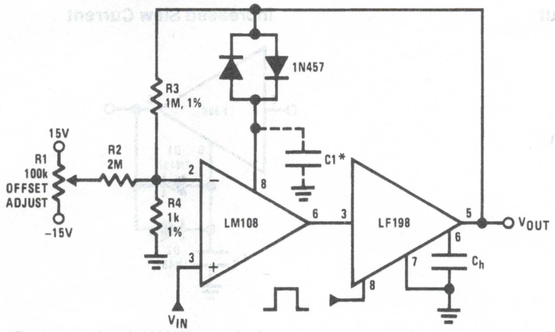
Functional Diagram


OFFSET
2
30k
5
OUTPUT
INPUT
3
LOGIC
8
LOGIC
REFERENCE
7
300
6
HOLD
CAPACITOR

TL/H/5692-1

Typical Applications (Continued)

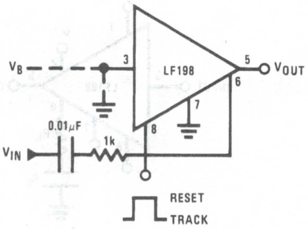
X1000 Sample & Hold


1N457
R3
1M, 1%
15V
R1
100k
OFFSET
ADJUST
-15V
R2
2M
R4
1k
1%
2
3
LM108
8
6
C1*
3
LF198
5
6
7
8
Ch
VOUT
VIN

*For lower gains, the LM108 must be frequency compensated

Use $\approx \frac{100}{A_V}$ pF from comp 2 to ground

Sample and Difference Circuit (Output Follows Input in *Hold* Mode)

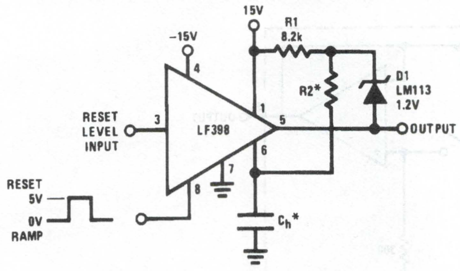

VB
3
LF198
5
VOUT
6
7
8
0.01µF
1k
VIN
RESET
TRACK

$V_{OUT} = V_B + \Delta V_{IN}$(HOLD MODE)

TL/H/5692-7

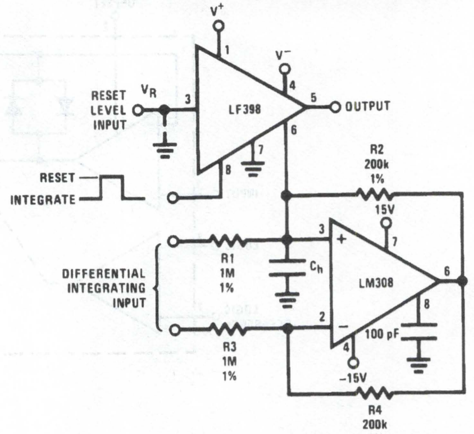
Typical Applications (Continued)

Ramp Generator with Variable Reset Level


15V
R1
8.2k
−15V
4
R2*
D1
LM113
1.2V
RESET
LEVEL
INPUT
3
LF398
1
5
OUTPUT
6
7
RESET
5V
0V
RAMP
8
C_h*

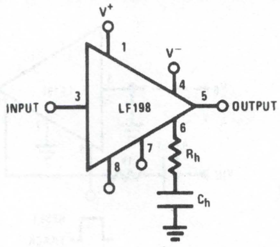
*Select for ramp rate $\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)(C_h)}$
R2 ≥ 10k

Integrator with Programmable Reset Level


V+
1
V−
RESET
LEVEL
INPUT
V_R
3
LF398
4
5
OUTPUT
6
7
8
RESET
INTEGRATE
R2
200k
1%
15V
7
3
+
C_h
DIFFERENTIAL
INTEGRATING
INPUT
R1
1M
1%
LM308
6
8
100 pF
2
−
4
−15V
R3
1M
1%
R4
200k
1%

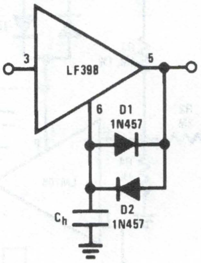
$$V_{OUT}\text{ (Hold Mode)} = \left[\frac{1}{(R1)(C_h)}\int_0^t V_{IN}\,dt\right] + \left[V_R\right]$$

Output Holds at Average of Sampled Input

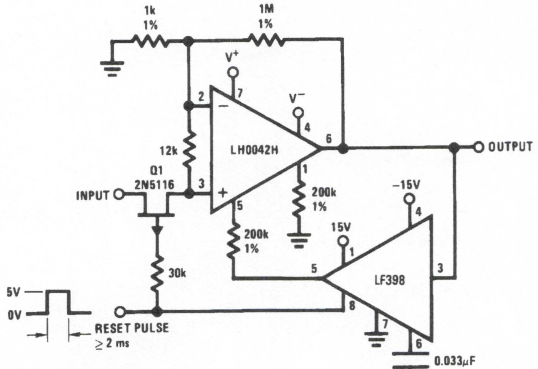

V+
1
V−
4
INPUT
3
LF198
5
OUTPUT
6
7
8
R_h
C_h

$$\text{Select } (R_h)(C_h) \gg \frac{1}{2\pi f_{IN}\text{ (Min)}}$$

Increased Slew Current


3
LF398
5
6
D1
1N457
C_h
D2
1N457

Reset Stabilized Amplifier (Gain of 1000)


1k
1%
1M
1%
V+
2
−
7
V−
4
6
OUTPUT
12k
LH0042H
Q1
2N5116
1
INPUT
3
+
5
200k
1%
200k
1%
−15V
4
15V
1
5
LF398
3
5V
0V
30k
8
7
RESET PULSE
≥ 2 ms
6
0.033μF
4.7k

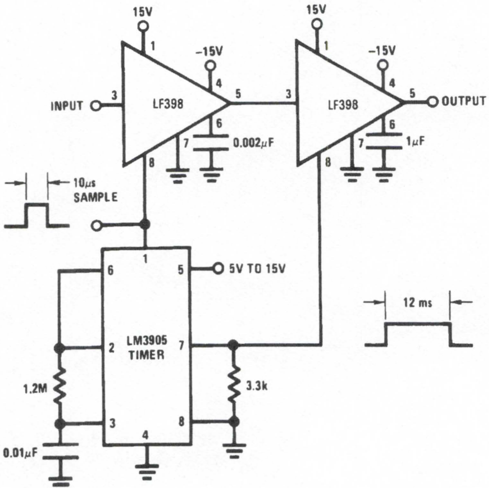
$V_{OS} \le 20\mu V$ (No trim)

$Z_{IN} \approx 1\ M\Omega$

$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/\text{sec}$

$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/°C$

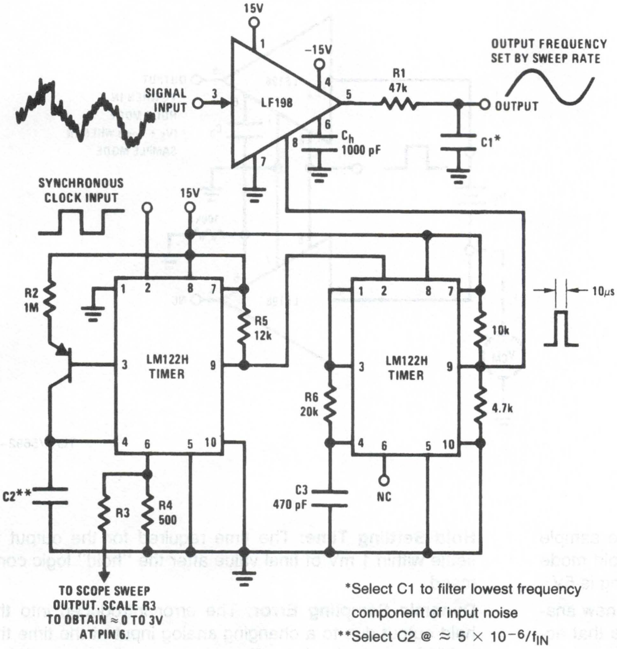
Fast Acquisition, Low Droop Sample & Hold


15V
1
−15V
4
INPUT
3
LF398
5
6
0.002μF
7
8
15V
1
−15V
4
3
LF398
5
OUTPUT
6
1μF
7
8
10μs
SAMPLE
1
6
5
5V TO 15V
LM3905
TIMER
2
7
1.2M
3.3k
3
4
8
0.01μF
12 ms

TL/H/5692-8

Typical Applications (Continued)

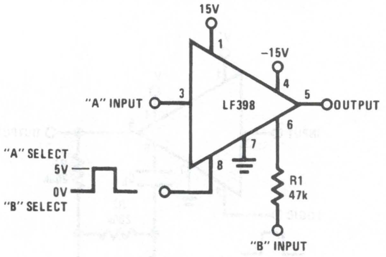
Synchronous Correlator for Recovering Signals Below Noise Level


15V
1
−15V
4
SIGNAL INPUT
3
LF198
5
R1
47k
OUTPUT
OUTPUT FREQUENCY SET BY SWEEP RATE
6
8
7
C_h
1000 pF
C1*
SYNCHRONOUS CLOCK INPUT
15V
R2
1M
1 2 8 7
LM122H TIMER
3
9
4 6 5 10
R5
12k
1 2 8 7
LM122H TIMER
3
9
4 6 5 10
10k
4.7k
R6
20k
C3
470 pF
NC
10μs
C2**
R3
R4
500
TO SCOPE SWEEP OUTPUT. SCALE R3 TO OBTAIN ≈ 0 TO 3V AT PIN 6.

*Select C1 to filter lowest frequency component of input noise

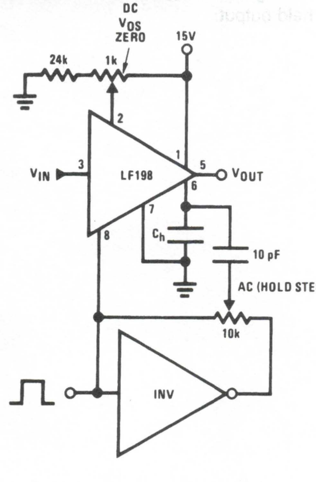
**Select C2 @ $\approx 5 \times 10^{-6}/f_{IN}$

2-Channel Switch

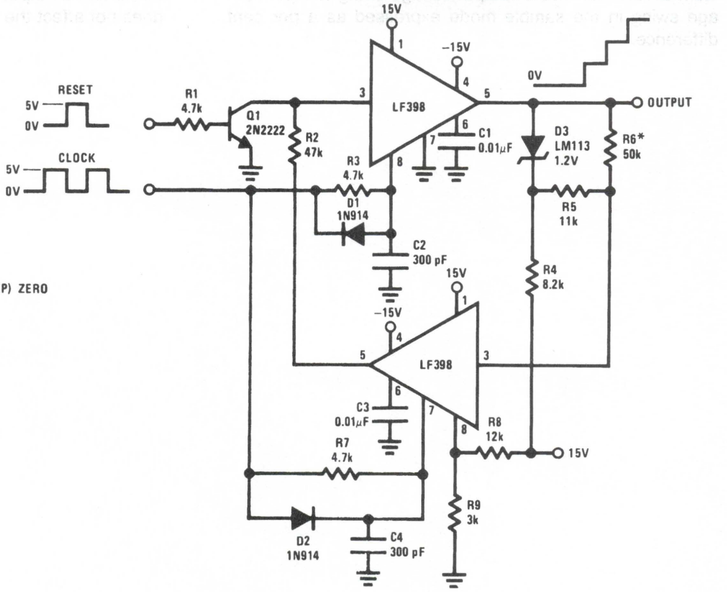

15V
1
−15V
4
"A" INPUT
3
LF398
5
OUTPUT
6
7
8
"A" SELECT
5V
0V
"B" SELECT
R1
47k
"B" INPUT

	A	B
Gain	1 ± 0.02%	1 ± 0.2%
Z_{IN}	$10^{10}\Omega$	47 kΩ
BW	≅ 1 MHz	≅ 400 kHz
Crosstalk @ 1 kHz	−90 dB	−90 dB
Offset	≤ 6 mV	≤ 75 mV

DC & AC Zeroing


DC V_OS ZERO
15V
24k
1k
2
V_IN
3
LF198
1
5
V_OUT
6
7
8
C_h
10 pF
AC (HOLD STEP) ZERO
10k
INV

Staircase Generator

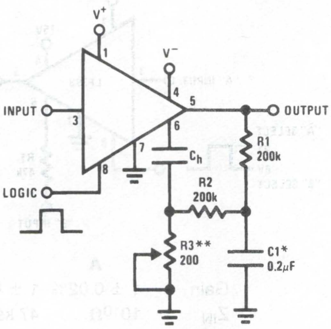

15V
1
−15V
4
0V
RESET
5V
0V
R1
4.7k
Q1
2N2222
R2
47k
3
LF398
5
OUTPUT
6
C1
0.01μF
7
8
D3
LM113
1.2V
R6*
50k
CLOCK
5V
0V
R3
4.7k
D1
1N914
R5
11k
C2
300 pF
R4
8.2k
15V
1
−15V
4
5
LF398
3
6
C3
0.01μF
7
8
R8
12k
15V
R7
4.7k
R9
3k
D2
1N914
C4
300 pF

TL/H/5692-9

*Select for step height
50k → ≅ 1V Step

Typical Applications (Continued)

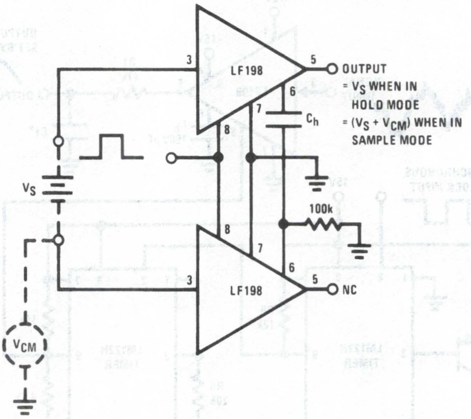
Capacitor Hysteresis Compensation


V+
1
V−
4
5
OUTPUT
INPUT
3
6
7
8
Ch
R1
200k
LOGIC
R2
200k
R3**
200
C1*
0.2μF

*Select for time constant $C1 = \frac{\tau}{100k}$

**Adjust for amplitude

Differential Hold


3
LF198
5
OUTPUT
= V_S WHEN IN
HOLD MODE
= (V_S + V_{CM}) WHEN IN
SAMPLE MODE
6
7
Ch
8
V_S
100k
8
7
6
3
LF198
5
NC
V_{CM}

TL/H/5692-10

Definition of Terms

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the "hold" logic command.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

National Semiconductor Corporation

PRELIMINARY

LF13006/LF13007 Digital Gain Set

General Description

The LF13006 and LF13007 are precision digital gain sets used for accurately setting non-inverting op amp gains. Gains are set with a 3-bit digital word which can be latched in with $\overline{WR}$ and $\overline{CS}$ pins. All digital inputs are TTL and CMOS compatible.

The LF13006 shown below will set binary scaled gains of 1, 2, 4, 8, 16, 32, 64, and 128. The LF13007 will set gains of 1, 2, 5, 10, 20, 50, and 100 (a common attenuator sequence). In addition, both versions have several taps and two uncommitted matching resistors that allow customization of the gain.

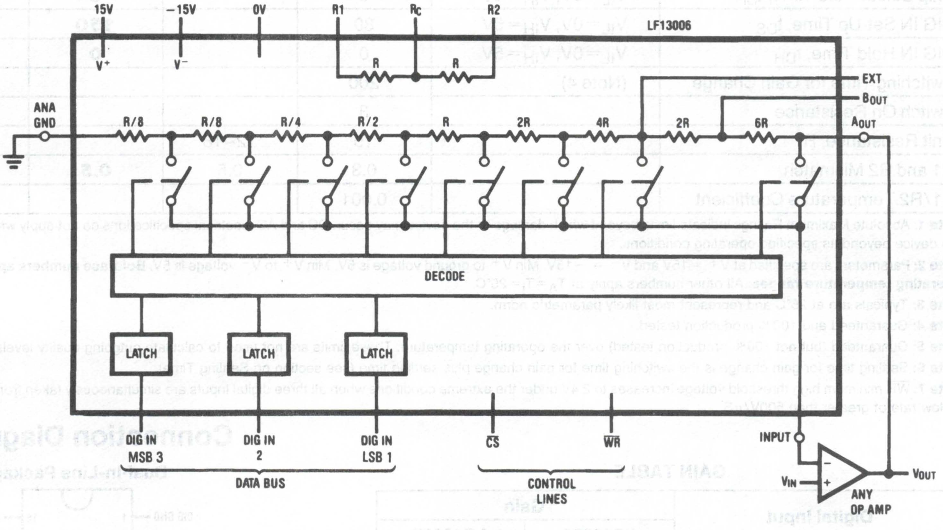
The gains are set with precision thin film resistors. The low temperature coefficient of the thin film resistors and their excellent tracking result in gain ratios which are virtually independent of temperature.

The LF13006, LF13007 used in conjunction with an amplifier not only satisfies the need for a digitally programmable amplifier in microprocessor based systems, but is also useful for discrete applications, eliminating the need to find 0.5% resistors in the ratio of 100 to 1 which track each other over temperature.

Features

- TTL and CMOS compatible logic levels
- Microprocessor compatible
- Gain error 0.5% max
- Binary or scope knob gains
- Wide supply range + 5V to ± 18V
- Packaged in 16-pin DIP

Block Diagram and Typical Application (LF13006)


15V
−15V
0V
R1
RC
R2
LF13006
V+
V−
R
R
EXT
BOUT
AOUT
ANA GND
R/8
R/8
R/4
R/2
R
2R
4R
2R
6R
DECODE
LATCH
LATCH
LATCH
DIG IN MSB 3
DIG IN 2
DIG IN LSB 1
DATA BUS
CS
WR
CONTROL LINES
INPUT
VIN
VOUT
ANY OP AMP

TL/H/5114-1

Note: R ≅ 15 kΩ

Order Number LF13006N or LF13007N
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V+ to V−	36V
Supply Voltage, V+ to GND	25V
Voltage at Any Digital Input	V+ to GND
Analog Voltage	V+ to (V− + 2V)

Operating Ratings (Note 1)

Operating Temperature Range	−40°C to +85°C
Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics (Note 2)

Parameter	Conditions	Typ (Note 3)	Tested Limit (Note 4)	Design Limit (Note 5)	Units
Gain Error	$A_{OUT} = \pm 10V$ ANA GND = 0V $I_{INPUT} < 10$ nA	0.3	0.5	**0.5**	%(max)
Gain Temperature Coefficient	$A_{OUT} = \pm 10V$ ANA GND = 0V	0.001			%/°C
Digital Input Voltage					
Low		1.4	0.8	**0.8**	V(max)
High		1.6	2.0	**2.0**	V(min)
Digital Input Current					
Low	$V_{IL} = 0V$	−38	−100	**−100**	µA(max)
High	$V_{IH} = 5V$	0.0001	1	**1**	µA(max)
Positive Power Supply Current	All Logic Inputs Low	2	5	**5**	mA(max)
Negative Power Supply Current	All Logic Inputs Low	−1.7	−5	**−5**	mA(max)
$\overline{\text{Write}}$ Pulse Width, t_W	$V_{IL} = 0V, V_{IH} = 5V$	40		**100**	ns(min)
$\overline{\text{Chip Select}}$ Set-Up Time, t_{CS}	$V_{IL} = 0V, V_{IH} = 5V$	60		**120**	ns(min)
$\overline{\text{Chip Select}}$ Hold Time, t_{CH}	$V_{IL} = 0V, V_{IH} = 5V$	0		**0**	ns(min)
DIG IN Set-Up Time, t_{DS}	$V_{IL} = 0V, V_{IH} = 5V$	80		**150**	ns(min)
DIG IN Hold Time, t_{DH}	$V_{IL} = 0V, V_{IH} = 5V$	0		**0**	ns(min)
Switching Time for Gain Change	(Note 4)	200			ns(max)
Switch On Resistance		3			kΩ
Unit Resistance, R		15	12–18		kΩ
R1 and R2 Mismatch		0.3	0.5	**0.5**	%(max)
R1/R2 Temperature Coefficient		0.001			%/°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Parameters are specified at V+ = 15V and V− = −15V. Min V+ to ground voltage is 5V. Min V+ to V− voltage is 5V. **Boldface numbers apply over full operating temperature ranges.** All other numbers apply at $T_A = T_j = 25°C$.

Note 3: Typicals are at 25°C and represent most likely parametric norm.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed (but not 100% production tested) over the operating temperature. These limits are not used to calculate outgoing quality levels.

Note 6: Settling time for gain change is the switching time for gain change plus settling time (see section on Settling Time).

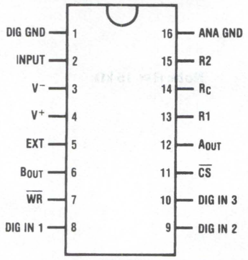
Note 7: $\overline{\text{WR}}$ minimum high threshold voltage increases to 2.4V under the extreme conditions when all three digital inputs are simultaneously taken from 0V to 5V at a slew rate of greater than 500V/µS.

GAIN TABLE

Digital Input			Gain			
			LF13006		LF13007	
DIG in 1	DIG in 2	DIG in 3	A_{OUT}	B_{OUT}	A_{OUT}	B_{OUT}
0	0	0	1	1	1	1
0	0	1	2	1.25	1.25	1
0	1	0	4	2.5	2	1.6
0	1	1	8	5	5	4
1	0	0	16	10	10	8
1	0	1	32	20	20	16
1	1	0	64	40	50	40
1	1	1	128	80	100	80

Connection Diagram

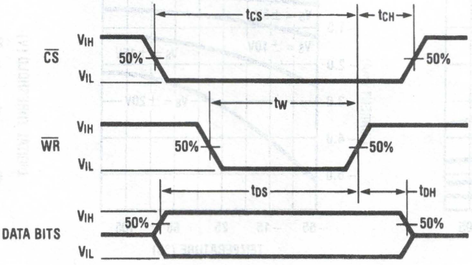
Dual-In-Line Package



TOP VIEW

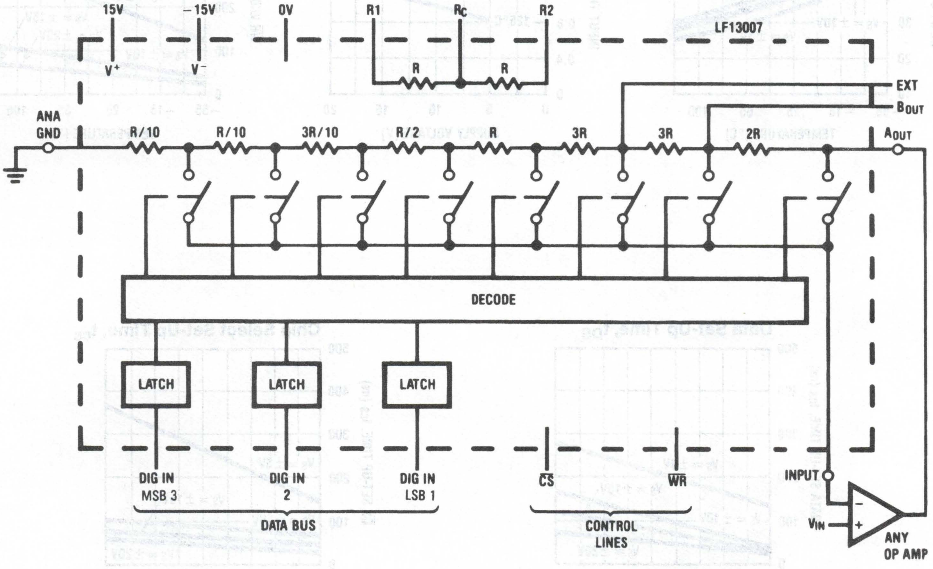
TL/H/5114–2

Switching Waveforms


tCS
tCH
VIH
CS
VIL
50%
50%
tW
VIH
WR
VIL
50%
50%
tDS
tDH
VIH
DATA BITS
VIL
50%
50%

TL/H/5114-3

Block Diagram and Typical Application (Continued) (LF13007)

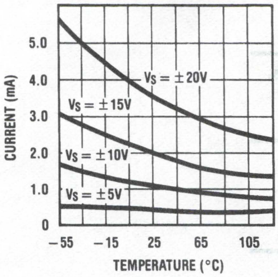

15V
−15V
0V
R1
RC
R2
V+
V−
R
R
LF13007
EXT
BOUT
ANA GND
R/10
R/10
3R/10
R/2
R
3R
3R
2R
AOUT
DECODE
LATCH
LATCH
LATCH
DIG IN MSB 3
DIG IN 2
DIG IN LSB 1
DATA BUS
CS
WR
CONTROL LINES
INPUT
VIN
ANY OP AMP

TL/H/5114-4

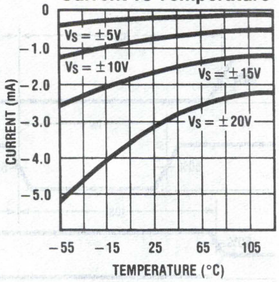
Note: R ≅ 15 kΩ

Typical Performance Characteristics

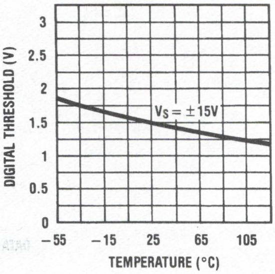
Positive Power Supply Current vs Temperature



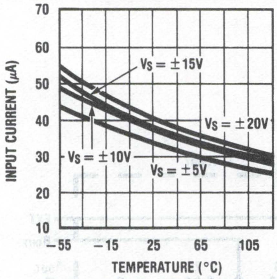
Negative Power Supply Current vs Temperature



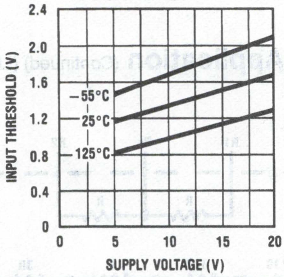
Digital Input Threshold vs Temperature



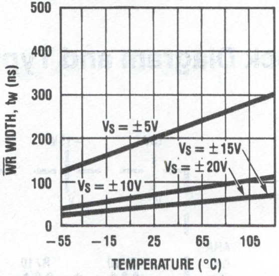
Logical 0 Input Bias Current vs Temperature



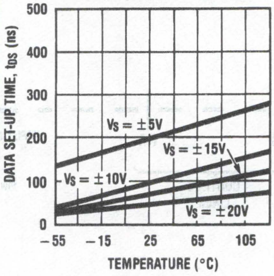
Digital Input Threshold vs Supply Voltage



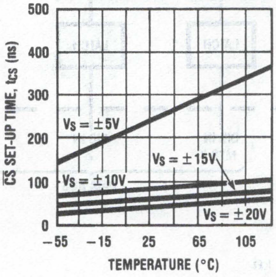
Write Width, t_W



Data Set-Up Time, t_{DS}



Chip Select Set-Up Time, t_{CS}



TL/H/5114-5

Application Information

FLOW-THROUGH OPERATION

THE LF13006, LF13007 can be operated with control lines $\overline{CS}$ and $\overline{WR}$ grounded. In this mode new data on the digital inputs will immediately set the new gain value. Input data cannot be latched in this mode.

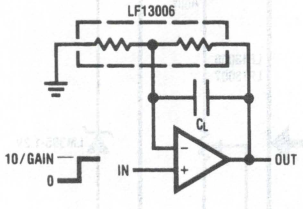
INPUT CURRENT

Current flowing through the input (pin 2) due to bias current of the op amp will result in a gain error due to switch impedance. Normally this error is very small. For example, 10 nA of bias current flowing through 3 kΩ of switch resistance will result in an error of 30 μV at the summing node. However, applications that have significant current flowing through the input must take this effect into account.

SETTLING TIME

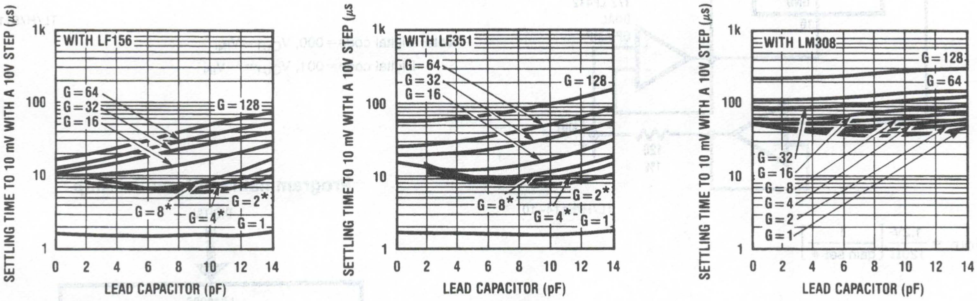
Settling time is a function of the particular op amp used with the LF13006/7 and the gain that is selected. It can be optimized and stability problems can be prevented through the use of a lead capacitor from the inverting input to the output of the amplifier. A lead capacitor is effective whenever the feedback around an amplifier is resistive, whether with discrete resistors or with the LF13006/7. It compensates for the feedback pole created by the parallel resistance and capacitance from the inverting input of the op amp to AC ground.

Settling Time Test Circuit


LF13006
C_L
10/GAIN
0
IN
OUT

TL/H/5114-6

Typical Settling Time Curves



TL/H/5114-7

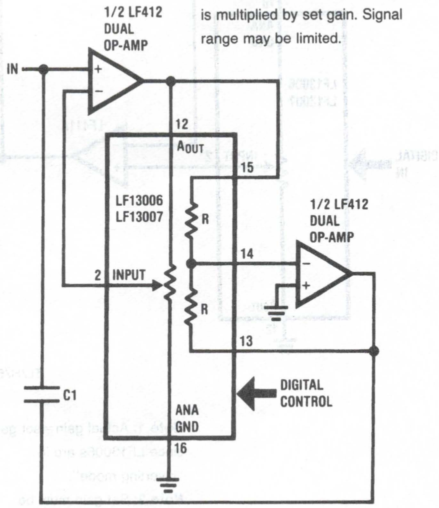
* Unstable at C_L less than 2 pF

Typical Applications

Variable Capacitance Multiplier

$C_{effective} = C1(\text{gain set } \#)$

Note: Output swing at input op amp is multiplied by set gain. Signal range may be limited.


1/2 LF412
DUAL
OP-AMP
IN
12
AOUT
15
LF13006
LF13007
R
1/2 LF412
DUAL
OP-AMP
14
2
INPUT
R
13
C1
DIGITAL
CONTROL
ANA
GND
16

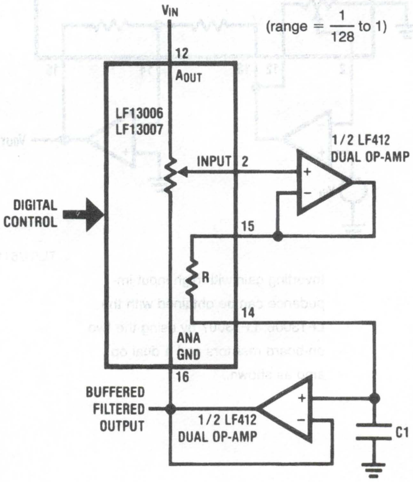
TL/H/5114-8

Variable Time Constant Filter

Time constant $= \frac{R}{N}C1$

N = setting of LF13006

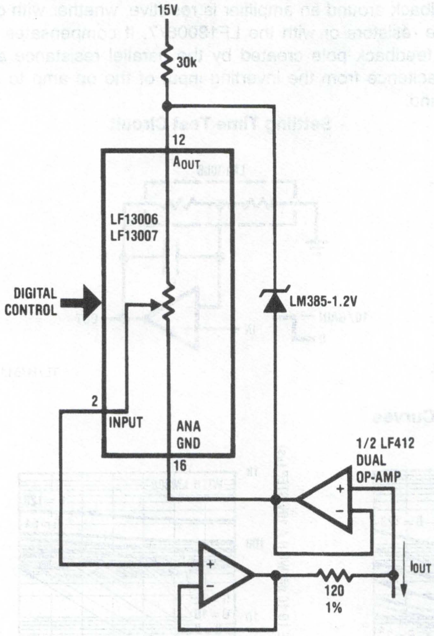
(range $= \frac{1}{128}$ to 1)


VIN
12
AOUT
LF13006
LF13007
INPUT
2
1/2 LF412
DUAL OP-AMP
DIGITAL
CONTROL
15
R
14
ANA
GND
16
BUFFERED
FILTERED
OUTPUT
1/2 LF412
DUAL OP-AMP
C1

TL/H/5114-9

Typical Applications (Continued)

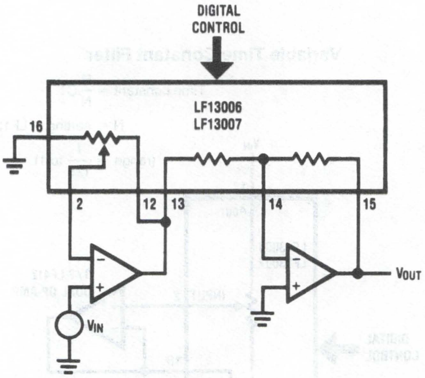
Programmable Current Source


15V
30k
12
AOUT
LF13006
LF13007
DIGITAL CONTROL
LM385-1.2V
2
INPUT
ANA GND
16
1/2 LF412 DUAL OP-AMP
IOUT
120 1%

TL/H/5114-10

$$I_{OUT} = \frac{1.2V}{120\Omega}\left[\frac{1}{\text{gain set \#}}\right]$$

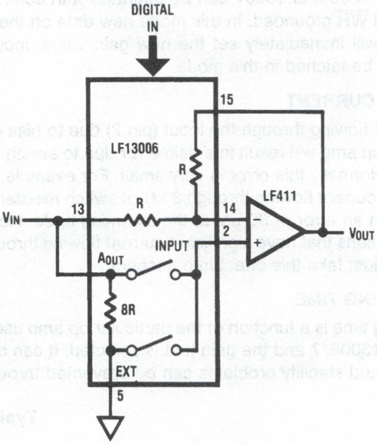
Inverting Gains


DIGITAL CONTROL
LF13006
LF13007
16
2
12
13
14
15
VIN
VOUT

TL/H/5114-12

Inverting gain with high input impedance can be obtained with the LF13006, LF13007 by using the two on-board resistors and a dual op amp as shown.

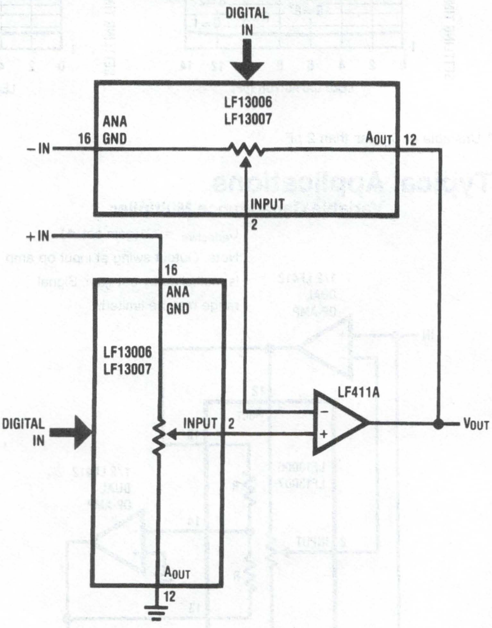
Switchable Gain of ±1


DIGITAL IN
15
LF13006
R
R
13
14
LF411
VIN
2
VOUT
INPUT
AOUT
8R
EXT
5

TL/H/5114-11

Note: Digital code = 000, $V_{OUT} = V_{IN}$;
Digital code = 001, $V_{OUT} = -V_{IN}$

Programmable Differential Amp


DIGITAL IN
LF13006
LF13007
ANA GND
16
−IN
AOUT
12
INPUT
2
+IN
16
ANA GND
LF13006
LF13007
LF411A
DIGITAL IN
INPUT
2
VOUT
AOUT
12

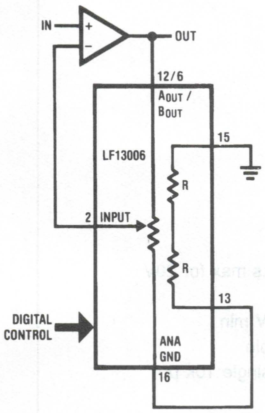
TL/H/5114-13

Note 1: Actual gain = set gain − 1 since LF13006s are in "inverting mode".

Note 2: Set gain must be same on both LF13006s.

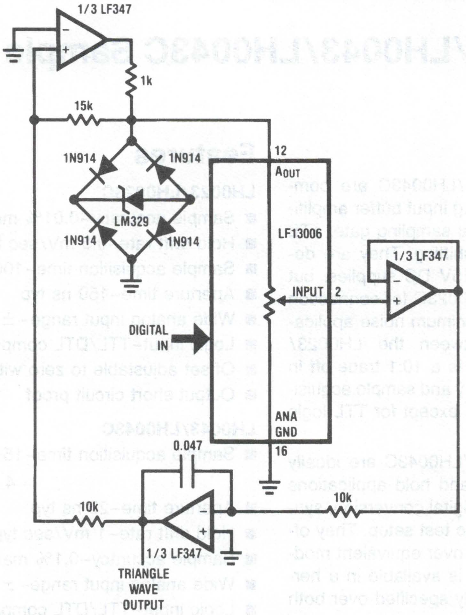
Typical Applications (Continued)

Altered Gain Range


IN
OUT
12/6
A_{OUT} / B_{OUT}
15
LF13006
R
2 INPUT
R
13
DIGITAL CONTROL
ANA GND
16

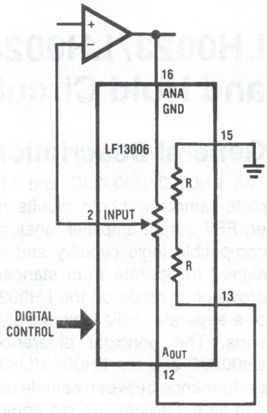
TL/H/5114-14

One Octave per Bit Function Generator


1/3 LF347
1k
15k
1N914
1N914
LM329
1N914
1N914
12
A_{OUT}
LF13006
1/3 LF347
INPUT 2
DIGITAL IN
ANA GND
16
0.047
10k
10k
1/3 LF347
TRIANGLE WAVE OUTPUT

TL/H/5114-15

Variable Gains of Almost 1


16
ANA GND
LF13006
15
R
2 INPUT
R
13
DIGITAL CONTROL
A_{OUT}
12

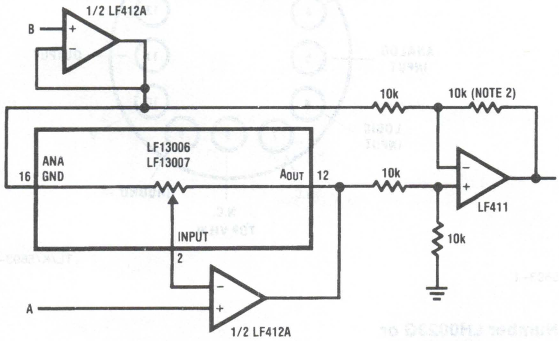
TL/H/5114-16

GAINS

A_{OUT}	B_{OUT}
1	1
1.8	1.2
3	2
4.5	3
6	4
7.2	4.8
8	5.33
8.47	5.65

GAINS
9
1.8
1.29
1.125
1.059
1.029
1.014
1.007

Programmable Instrumentation Amp

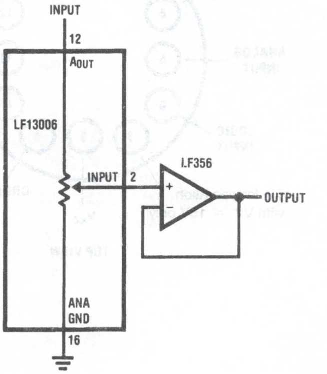

1/2 LF412A
B
10k
10k (NOTE 2)
LF13006
LF13007
ANA GND
16
A_{OUT}
12
10k
LF411
10k
INPUT
2
A
1/2 LF412A

TL/H/5114-17

Note 1: $V_{OUT} = N (A - B)$, N = set gain.

Note 2: All 10k resistors 0.1% matched.

Attenuator (0 dB to −42 dB in 6 dB steps)


INPUT
12
A_{OUT}
LF13006
INPUT
2
LF356
OUTPUT
ANA GND
16

TL/H/5114-18

National Semiconductor

LH0023/LH0023C/LH0043/LH0043C Sample and Hold Circuits

General Description

The LH0023/LH0023C and LH0043/LH0043C are complete sample and hold circuits including input buffer amplifier, FET output amplifier, analog signal sampling gate, TTL compatible logic circuitry and level shifting. They are designed to operate from standard ±15V DC supplies, but provision is made on the LH0023/LH0023C for connection of a separate +5V logic supply in minimum noise applications. The principal difference between the LH0023/LH0023C and the LH0043/LH0043C is a 10:1 trade-off in performance between sample accuracy and sample acquisition time. Devices are pin compatible except for TTL logic polarity.

The LH0023/LH0023C and LH0043/LH0043C are ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup. They offer significant cost and size reduction over equivalent module or discrete designs. Each device is available in a hermetic TO-8 package and is completely specified over both full military and industrial temperature ranges.

The LH0023 and LH0043 are specified for operation over the −55°C to +125°C military temperature range. The LH0023C and LH0043C are specified for operation over the −25°C to +85°C temperature range.

Features

LH0023/LH0023C

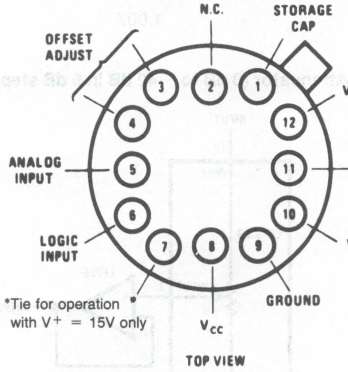
- Sample accuracy–0.01% max
- Hold drift rate–0.5 mV/sec typ
- Sample acquisition time–100 µs max for 20V
- Aperture time–150 ns typ
- Wide analog input range–±10V min
- Logic input–TTL/DTL compatible
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

LH0043/LH0043C

- Sample acquisition time–15 µs max for 20V
  4 µs typ for 5V
- Aperture time–20 ns typ
- Hold drift rate–1 mV/sec typ
- Sample accuracy–0.1% max
- Wide analog input range–±10V min
- Logic input–TTL/DTL compatible
- Offset adjustable to zero with single 10k pot
- Output short circuit protection

Connection Diagrams

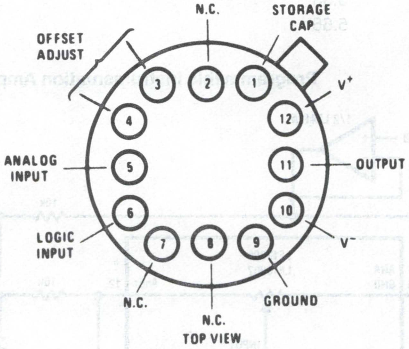
LH0023/LH0023C



*Tie for operation with V+ = 15V only

TL/K/5693-1

LH0043/LH0043C



TL/K/5693-8

Order Number LH0023G or LH0023CG or LH0043G or LH0043CG
See Package Number G12B

National Semiconductor Corporation

LH0053/LH0053C High Speed Sample and Hold Amplifier

General Description

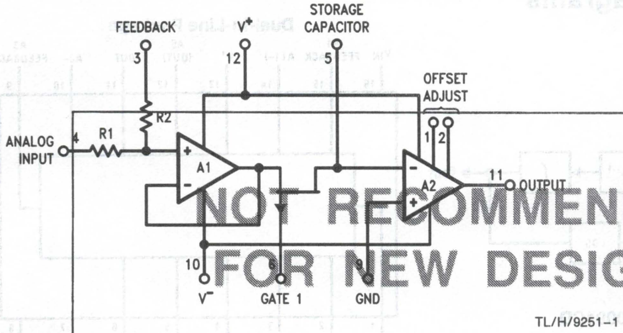
The LH0053/LH0053C is a high speed sample and hold circuit capable of acquiring a 20V step signal in under 5.0 μs.

The device is ideally suited for a variety of high speed data acquisition applications including analog buffer memories for A to D conversion and synchronous demodulation.

Features

- Sample acquisition time 10 μs max. for 20V signal
- FET switch for preset or reset function
- Sample accuracy null
- Offset adjust to 0V
- DTL/TTL compatible FET gate
- Single storage capacitor

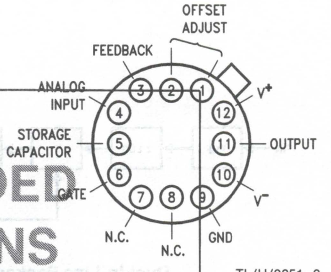
Schematic and Connection Diagrams


FEEDBACK
3
V+
12
STORAGE CAPACITOR
5
OFFSET ADJUST
1
2
R2
ANALOG INPUT
4
R1
A1
A2
11
OUTPUT
10
V−
6
GATE 1
9
GND

TL/H/9251–1

NOT RECOMMENDED FOR NEW DESIGNS

Metal Can Package


OFFSET ADJUST
FEEDBACK
ANALOG INPUT
STORAGE CAPACITOR
GATE
N.C.
N.C.
GND
V−
OUTPUT
V+
1
2
3
4
5
6
7
8
9
10
11
12

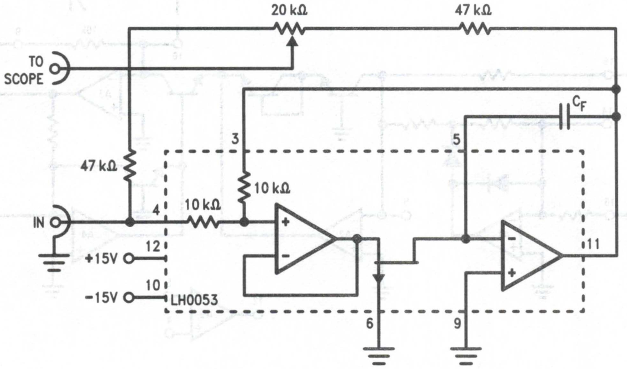
TL/H/9251–2

Top View

Order Number LH0053G or LH0053CG
See NS Package Number G12B

AC Test Circuit

Acquisition Time Test Circuit


20 kΩ
47 kΩ
TO SCOPE
CF
3
5
47 kΩ
10 kΩ
10 kΩ
IN
4
12
+15V
10
−15V
LH0053
11
6
9

TL/H/9251–3

National Semiconductor Corporation

PRELIMINARY

LH0091 True RMS to DC Converter

General Description

The LH0091, rms to dc converter generates a dc output equal to the rms value of any input per the transfer function:

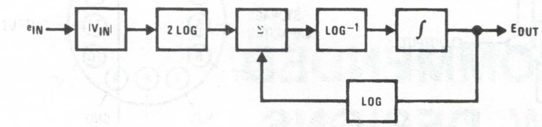
$$E_{OUT(DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)\,dt}$$

The device provides rms conversion to an accuracy of 0.1% of reading using the external trim procedure. It is possible to trim for maximum accuracy (0.5 mV ± 0.05% typ) for decade ranges i.e., 10 mV → 100 mV, 0.7V → 7V, etc.

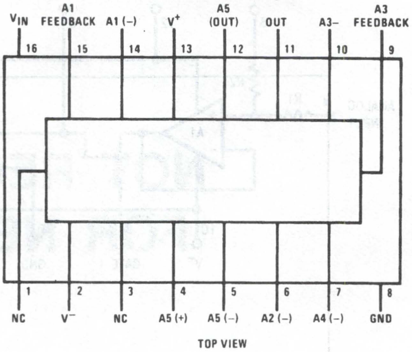
Features

- Low cost
- True rms conversion
- 0.5% of reading accuracy untrimmed
- 0.05% of reading accuracy with external trim
- Minimum component count
- Input voltage to ±15V peak for $V_S = \pm 15V$
- Uncommitted amplifier for filtering, gain, or high crest factor configuration
- Military or commercial temperature range.

Block and Connection Diagrams


eIN
|VIN|
2 LOG
Σ
LOG⁻¹
∫
EOUT
LOG

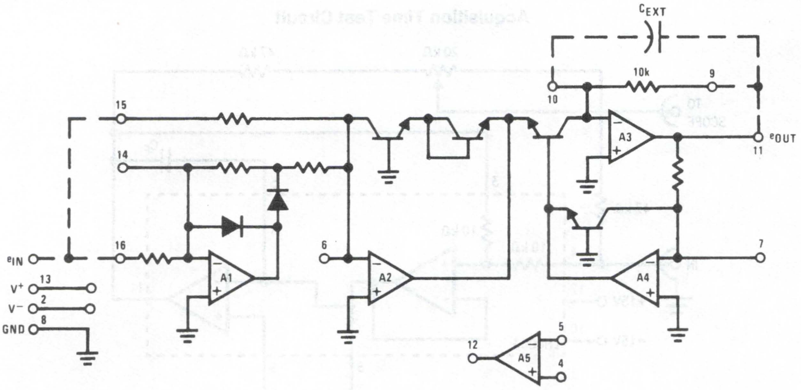
Dual-In-Line Package


VIN
A1 FEEDBACK
A1 (−)
V⁺
A5 (OUT)
OUT
A3−
A3 FEEDBACK
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
NC
V⁻
NC
A5 (+)
A5 (−)
A2 (−)
A4 (−)
GND
TOP VIEW

Dual-In-Line Package
Order Number LH0091D or LH0091CD
See Package D16D

TL/H/5694-1

Simplified Schematic


CEXT
10k
9
10
15
14
16
6
11
eOUT
7
A1
A2
A3
A4
A5
eIN
V⁺
V⁻
GND
13
2
8
12
5
4

TL/H/5694-2

Note: Dotted lines denote external connections.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±22V
Input Voltage	±15V peak
Output Short Circuit Duration	Continuous

	T_{MIN}	T_{MAX}
Operating Temperature Range		
LH0091	−55°C	125°C
LH0091C	−25°C	85°C
Storage Temperature Range		
LH0091	−65°C to +150°C	
LH0091C	−25°C to +85°C	
Lead Temp. (Soldering, 10 seconds)	260°C	

Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

Transfer Function $= E_{O(DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)\,dt}$

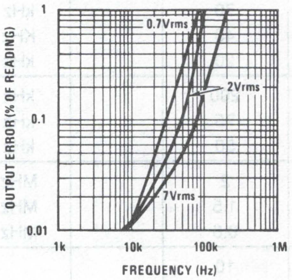
Parameter	Conditions	Min	Typ	Max	Units
ACCURACY (See Definition of Terms)					
Total Unadjusted Error	50 mVrms $\leq V_{IN} \leq$ 7Vrms (*Figure 1*)		20, ±0.5	40, ±1.0	mV, %
Total Adjusted Error	50 mVrms $\leq V_{IN} \leq$ 7Vrms (*Figure 3*)		0.5, ±0.05	1, ±0.2	mV, %
Total Unadjusted Error vs Temperature	$-25°C \leq T_A \leq +70°C$		0.25, ±0.2%		mV, %/°C
Total Unadjusted Error vs Supply Voltage			1		mV/V
AC PERFORMANCE					
Frequency for Specified Adjusted Error	Input = 7Vrms, Sinewave (*Figure 3*)	30	70		kHz
	Input = 0.7Vrms, Sinewave (*Figure 3*)		40		KHz
	Input = 0.1Vrms, Sinewave (*Figure 3*)		20		kHz
Frequency for 1% Additional Error	Input = 7Vrms, Sinewave (*Figure 3*)	100	200		kHz
	Input = 0.7Vrms, Sinewave (*Figure 3*)		75		kHz
	Input = 0.1Vrms, Sinewave (*Figure 3*)		50		kHz
Bandwidth (3 dB)	Input = 7Vrms, Sinewave (*Figure 3*)		2		MHz
	Input = 0.7Vrms, Sinewave (*Figure 3*)		1.5		MHz
	Input = 0.1Vrms, Sinewave (*Figure 3*)		0.8		MHz
Crest Factor	Rated Adjusted Accuracy Using the High Crest Factor Circuit (*Figure 5*)	5	10		
INPUT CHARACTERISTICS					
Input Voltage Range	For Rated Performance	±0.05		±11	Vpeak
Input Impedance		4.5	5		kΩ
OUTPUT CHARACTERISTICS					
Rated Output Voltage	$R_L \geq 2.5\ k\Omega$	10			V
Output Short Circuit Current			22		mA
Output Impedance			1		Ω
POWER SUPPLY REQUIREMENTS					
Operating Range		±5		±20	V
Quiescent Current	$V_S = \pm 15V$		14	18	mA

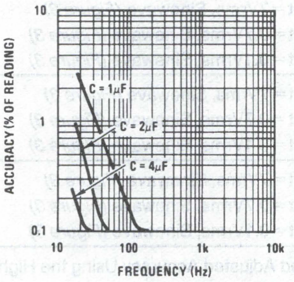
Op Amp Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

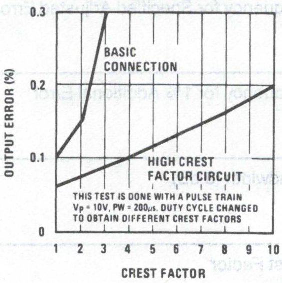
	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	10	mV
I_{OS}	Input Offset Current			4.0	200	nA
I_B	Input Bias Current			30	500	nA
R_{IN}	Input Resistance			2.5		MΩ
A_{OL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	15	160		V/mv
V_O	Output Voltage Swing	$R = 10\ k\Omega$	±10	±13		V
V_I	Input Voltage Range		±10			V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$		90		dB
PSRR	Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		96		dB
I_{SC}	Output Short-Circuit Current			25		mA
S_r	Slew Rate (Unity Gain)			0.5		V/µs
BW	Small Signal Bandwidth			1.0		MHz

Refer to RETS0091D drawing for Military specifications.

Typical Performance Characteristics

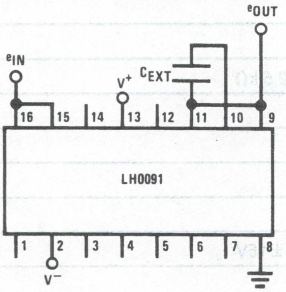

Error vs Frequency


Error vs Frequency


Error vs Crest Factor

TL/H/5694-3

Typical Applications (All applications require power supply by-pass capacitors.)

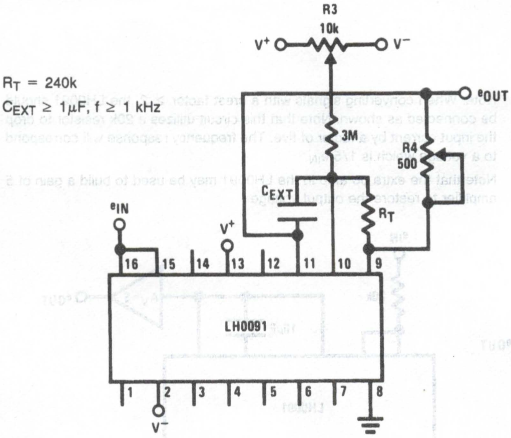


TL/H/5694-4

$C_{EXT} \geq 1\ \mu F$; frequency ≥ 1 kHz

FIGURE 1. LH0091 Basic Connection (No Trim)

Typical Applications (Continued)


R3
10k
V+
V−
eOUT
3M
R4
500
CEXT
RT
eIN
V+
16
15
14
13
12
11
10
9
LH0091
1
2
3
4
5
6
7
8
V−

R_T = 240k

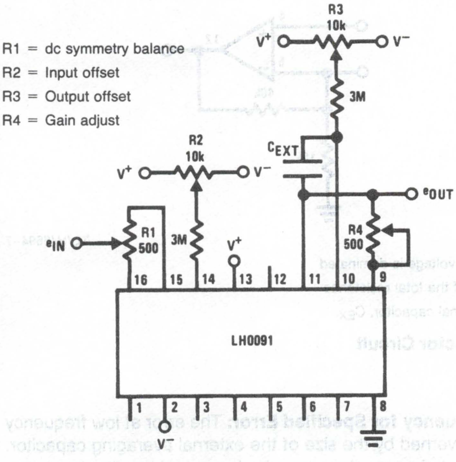
$C_{EXT} \geq 1\mu F$, f ≥ 1 kHz

Note. The easy trim procedure is used for ac coupled input signals. It involves two trims and can achieve accuracies of 2 mV offset ±0.1% reading.

Procedure:

1. Apply 100 mV rms (sine wave) to input, adjust R3 until the output reads 100 mV_{DC}.
2. Apply 5 V_{rms} (sine wave) to input, adjust R4 until the output reads 5 V_{DC}.
3. Repeat steps 1 and 2 until the desired initial accuracy is achieved.

FIGURE 2. LH0091 "Easy Trim" (For ac Inputs Only)


R3
10k
V+
V−
3M
R2
10k
V+
V−
CEXT
eOUT
R1
500
3M
V+
R4
500
eIN
16
15
14
13
12
11
10
9
LH0091
1
2
3
4
5
6
7
8
V−

R1 = dc symmetry balance

R2 = Input offset

R3 = Output offset

R4 = Gain adjust

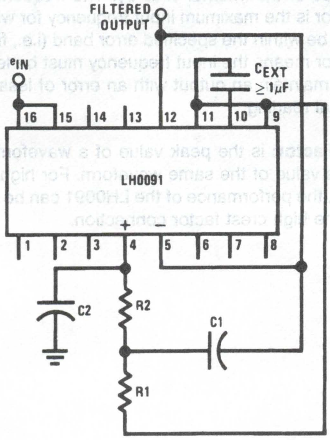
Note. This procedure will give accuracies of 0.5 mV offset ±0.05% reading for inputs from 0.05V peak to 10V peak.

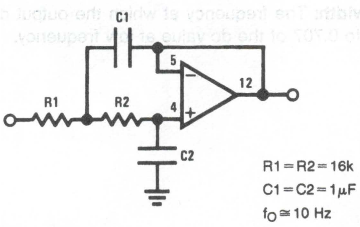
Procedure:

1. Apply 50 mV_{DC} to the input. Read and record the output.
2. Apply −50 mV_{DC} to the input. Use R2 to adjust for an output of the same magnitude as in step 1.
3. Apply 50 mV to the input. Use R3 to adjust the output for 50 mV.
4. Apply −50 mV to input. Use R2 to adjust the output for 50 mV.
5. Apply ±10V alternately to the input. Adjust R1 until the output readings for both polarities are equal (not necessary that they be exactly 10V).
6. Apply 10V to the input. Use R4 to adjust for 10V at the output.
7. Repeat this procedure to obtain the desired accuracy.

FIGURE 3. LH0091 Standard dc Trim Procedure

Note. The additional op amp in the LH0091 may be used as a low pass filter as shown in *Figure 4.*


FILTERED
OUTPUT
eIN
CEXT
≥ 1μF
16
15
14
13
12
11
10
9
LH0091
+
−
1
2
3
4
5
6
7
8
C2
R2
C1
R1


C1
5
−
12
R1
R2
4
+
C2

R1 = R2 = 16k

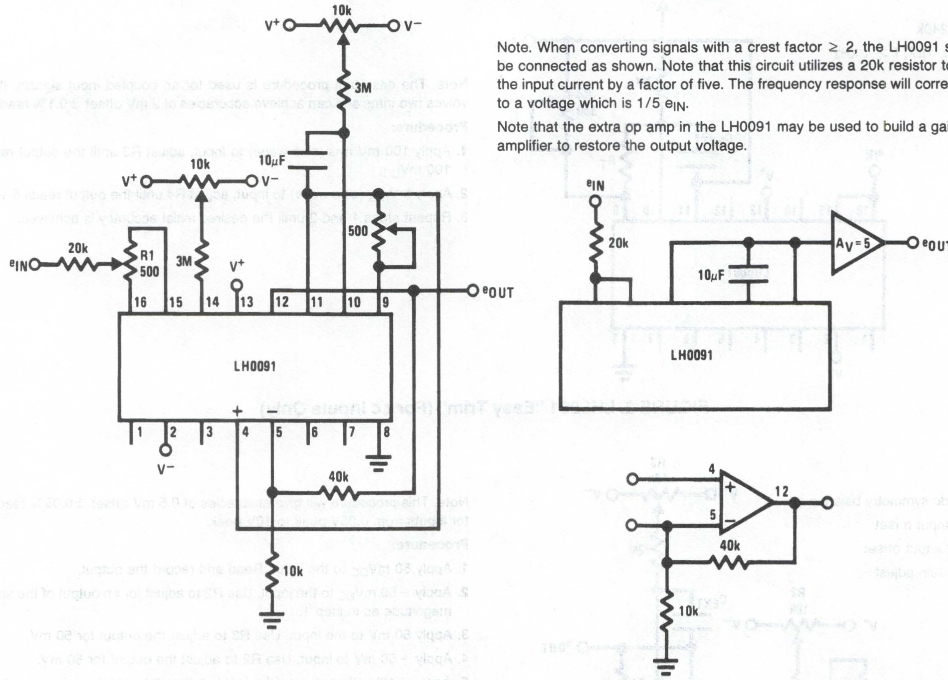
C1 = C2 = 1μF

$f_O \cong$ 10 Hz

TL/H/5694-6

FIGURE 4. Output Filter Connection Using the Internal Op Amp

Typical Applications (Continued)



Note. When converting signals with a crest factor ≥ 2, the LH0091 should be connected as shown. Note that this circuit utilizes a 20k resistor to drop the input current by a factor of five. The frequency response will correspond to a voltage which is 1/5 e_{IN}.

Note that the extra op amp in the LH0091 may be used to build a gain of 5 amplifier to restore the output voltage.

TL/H/5694-7

Note. Respond time of the dc output voltage is dominated by the RC time constant consisting of the total resistance between pins 9 and 10 and the external capacitor, C_{EX}.

FIGURE 5. High Crest Factor Circuit

Definition of Terms

True rms to dc Converter: A device which converts any signal (ac, dc, ac + dc) to the dc equivalent of the rms value.

Error: is the amount by which the actual output differs from the theoretical value. Error is defined as a sum of a fixed term and a percent of reading term. The fixed term remains constant, regardless of input while the percent of reading term varies with the input.

Total Unadjusted Error: The total error of the device without any external adjustments.

Bandwidth: The frequency at which the output dc voltage drops to 0.707 of the dc value at low frequency.

Frequency for Specified Error: The error at low frequency is governed by the size of the external averaging capacitor. At high frequencies, error is dependent on the frequency response of the internal circuitry. The frequency for specified error is the maximum input frequency for which the output will be within the specified error band (i.e., frequency for 1% error means the input frequency must be less than 200 kHz to maintain an output with an error of less than 1% of the initial reading.

Crest Factor: is the peak value of a waveform divided by the rms value of the same waveform. For high crest factor signals, the performance of the LH0091 can be improved by using the high crest factor connection.

National Semiconductor Corporation

LH0094 Multifunction Converter

General Description

The LH0094 multifunction converter generates an output voltage per the transfer function:

$$E_O = V_y\left(\frac{V_Z}{V_X}\right)^m, 0.1 \le m \le 10, \text{ m continuously adjustable}$$

m is set by 2 resistors.

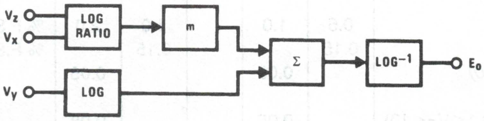
Features

- Low cost
- Versatile
- High accuracy − 0.05%
- Wide supply range − ±5V to ±22V
- Minimum component count
- Internal matched resistor pair for setting m = 2 and m = 0.5

Applications

- Precision divider, multiplier
- Square root
- Square
- Trigonometric function generator
- Companding
- Linearization
- Control systems
- Log amp

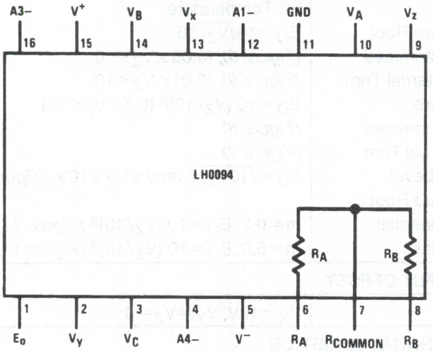
Block and Connection Diagrams



Vz
Vx
LOG RATIO
m
Σ
LOG⁻¹
Eo
Vy
LOG

Order Number LH0094D or LH0094CD
See NS Package Number D16D

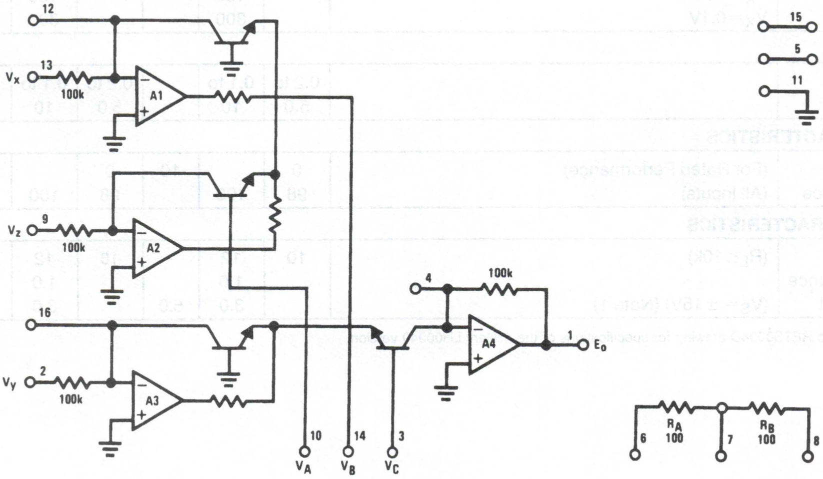
Dual-In-Line Package



A3−
V⁺
VB
Vx
A1−
GND
VA
Vz
16
15
14
13
12
11
10
9
LH0094
RA
RB
1
2
3
4
5
6
7
8
Eo
Vy
VC
A4−
V⁻
RA
RCOMMON
RB

TOP VIEW

Simplified Schematic



12
13
Vx
100k
A1
9
Vz
100k
A2
16
2
Vy
100k
A3
4
100k
A4
1
Eo
10
VA
14
VB
3
VC
15
V⁺
5
V⁻
11
6
RA 100
7
RB 100
8

TL/H/5695-1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±22V
Input Voltage	±22V
Output Short-Circuit Duration	Continuous

Operating Temperature Range	
LH0094CD	−25°C to +85°C
LH0094D	−55°C to +125°C
Storage Temperature Range	
LH0094D	−65°C to +150°C
LH0094CD	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics

$V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified. Transfer function: $E_O = V_Y \frac{V_Z{}^m}{V_X}$; $0.1 \leq m \leq 10$; $OV \leq V_X, V_Y, V_Z \leq 10V$

Parameter	Conditions	LH0094			LH0094C			Units
		Min	Typ	Max	Min	Typ	Max	
ACCURACY								
Multiply	$E_O = V_Z V_Y$ $(0.03 \leq V_Y \leq 10V;\ 0.01 \leq V_Z \leq 10V)$							% F.S.
Untrimmed	*(Figure 2)*		0.25	0.45		0.45	0.9	(10V)
External Trim	*(Figure 3)*		0.10			0.1		% F.S.
	vs. Temperature		0.2			0.2		mV/°C
Divide	$E_O = 10V_Z/V_X$							
Untrimmed	*(Figure 4)*, $0.5 \leq V_X \leq 10;\ 0.01 \leq V_Z \leq 10)$		0.25	0.45		0.45	0.9	% F.S.
External Trim	*(Figure 5)*, $(0.1 \leq V_X \leq 10;\ 0.01 \leq V_Z \leq 10)$		0.10			0.1		% F.S.
	vs. Temperature		0.2			0.2		mV/°C
Square Root	$E_O = 10\sqrt{V_Z/10}$							
Untrimmed	*(Figure 8)*, $(0.03 \leq V_Z \leq 10$		0.25	0.45		0.45	0.9	% F.S.
External Trim	*(Figure 9)*, $(0.01 \leq V_Z \leq 10$		0.15			0.15		% F.S.
Square	$E_O = 10\ (V_Z/10)^2\ (0.1 \leq V_Z \leq 10)$							
Untrimmed	*(Figure 6)*	0.5	1.0		1.0	2.0	% F.S.	
External Trim	*(Figure 7)*	0.15			0.15		% F.S.	
Low Level Square Root	$E_O = \sqrt{10V_Z}$; $5.0mV \leq V_Z \leq 10V$, *(Figure 10)*		0.05			0.05		% F.S.
Exponential	$m = 0.2$, $E_O = 10\ (V_Z/10)^2$ *(Figure 11)*, $(0.1 \leq V_Z \leq 10)$		0.05			0.08		% F.S.
Circuits	$m = 5.0$, $E_O = 10\ (V_Z/10)^5$ *(Figure 11)*, $(1.0 \leq V_Z \leq 10)$		0.05			0.08		% F.S.
OUTPUT OFFSET								
	$V_X = 10V$, $V_Y = V_Z = 0$		2.0	5.0		5.0	10	mV
AC CHARACTERISTICS								
3 dB Bandwidth	$m = 1.0$, $V_X = 10V$, $V_Y = 0.1\ V_{rms}$		10			10		kHz
Noise	10 Hz to 1.0 kHz, $m = 1.0$, $V_Y = V_Z = OV$							
	$V_X = 10V$		100			100		μV/rms
	$V_X = 0.1V$		300			300		μV/rms
EXPONENT								
m		0.2 to 5.0	0.1 to 10		0.2 to 5.0	0.1 to 10		
INPUT CHARACTERISTICS								
Input Voltage	(For Rated Performance)	0		10	0		10	V
Input Impedance	(All Inputs)	98	100		98	100		kΩ
OUTPUT CHARACTERISTICS								
Output Swing	$(R_L \leq 10k)$	10	12		10	12		V
Output Impedance			1.0			1.0		Ω
Supply Current	$(V_S = \pm 15V)$ (Note 1)		3.0	5.0		3.0	5.0	mA

Note 1: Refer to RETS0094D drawing for specifications of the military LH00940 version.

Applications Information

GENERAL INFORMATION

Power supply bypass capacitors (0.1 μF) are recommended for all applications.

The LH0094 series is designed for positive input signals only. However, negative input up to the supply voltage will not damage the device.

A clamp diode (*Figure 1*) is recommended for those applications in which the inputs may be subjected to open circuit or negative input signals.

For basic applications (multiply, divide, square, square root) it is possible to use the device without any external adjustments or components. Two matched resistors are provided internally to set m for square or square root.

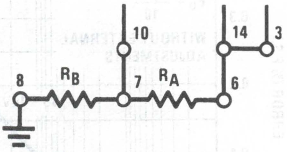
When using external resistors to set m, such resistors should be as close to the device as possible.

SELECTION OF RESISTORS TO SET m

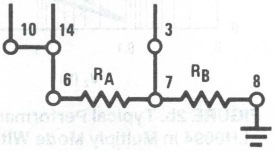
Internal Matched Resistors

R_A and R_B are matched internal resistors. They are 100Ω ± 10%, but matched to 0.1%.

(a) m = 2*



(b) m = 0.5*



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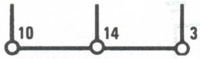
*No external resistors required, strap as indicated

External Resistors

The exponent is set by 2 external resistors or it may be continuously varied by a single trim pot. (R1 + R2 ≤ 500Ω.

(a) m = 1



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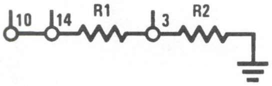
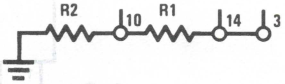
(b) m < 1



$$m = \frac{R2}{R1 + R2} \quad R1 + R2 \approx 200\Omega$$

(c) m > 1



$$m = \frac{R1 + R2}{R2}$$

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ACCURACY (ERROR)

The accuracy of the LH0094 is specified for both externally adjusted and unadjusted cases.

Although it is customary to specify the errors in percent of full-scale (10V), it is seen from the typical performance curves that the actual errors are in percent of reading. Thus, the specified errors are overly conservative for small input voltages. An example of this is the LH0094 used in the multiplication mode. The specified typical error is 0.25% of full-scale (25 mV). As seen from the curve, the unadjusted error is ≈25 mV at 10V input, but the error is less than 10 mV for inputs up to 1V. Note also that if either the multiplicand or the multiplier is at less than 10V, (5V for example) the unadjusted error is less. Thus, the errors specified are at full-scale—the worst case.

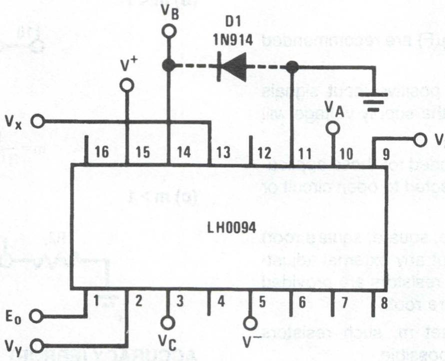
The LH0094 is designed such that the user is able to externally adjust the gain and offset of the device—thus trim out all of the errors of conversion. In most applications, the gain adjustment is the only external trim needed for super accuracy—except in division mode, where a denominator offset adjust is needed for small denominator voltages.

EXPONENTS

The LH0094 is capable of performing roots to 0.1 and powers up to 10. However, care should be taken when applying these exponent—otherwise, results may be misinterpreted. For example, consider the $\frac{1}{10}$th power of a number: i.e., 0.001 raised to 0.1 power is 0.5011; 0.1 raised to the 0.1 power is 0.7943; and 10 raised to the 0.1 power is 1.2589. Thus, it is seen that while the input has changed 4 decades, the output has only changed a little more than a factor of 2. It is also seen that with as little as 1 mV of offset, the output will also be greater than zero with zero input.

Applications Information (Continued)

1. CLAMP DIODE CONNECTION


V_B
D1
1N914
V+
V_x
V_A
V_z
16
15
14
13
12
11
10
9
LH0094
1
2
3
4
5
6
7
8
E_0
V_y
V_C
V−

$$E_O = V_y \left(\frac{V_Z}{V_X}\right)^m$$

$0.1 \leq m \leq 10$

Note. This clamp diode connection is recommended for those applications in which the inputs may be subject to open circuit or negative signals.

FIGURE 1. Clamp Diode Connection

2. MULTIPLY

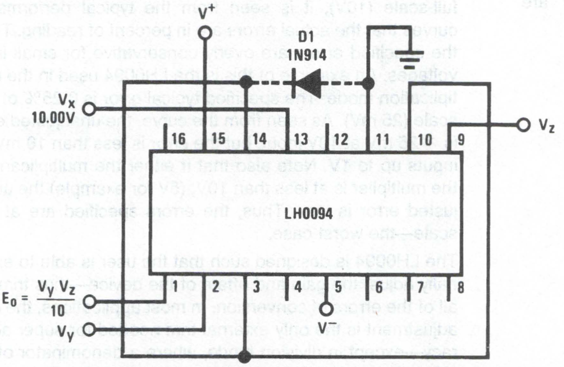

V+
D1
1N914
V_x
10.00V
V_z
16
15
14
13
12
11
10
9
LH0094
1
2
3
4
5
6
7
8
E_0 = V_y V_z / 10
V_y
V−

FIGURE 2a. LH0094 Used to Multiply (No External Adjustment)

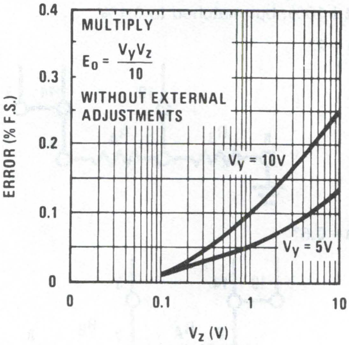
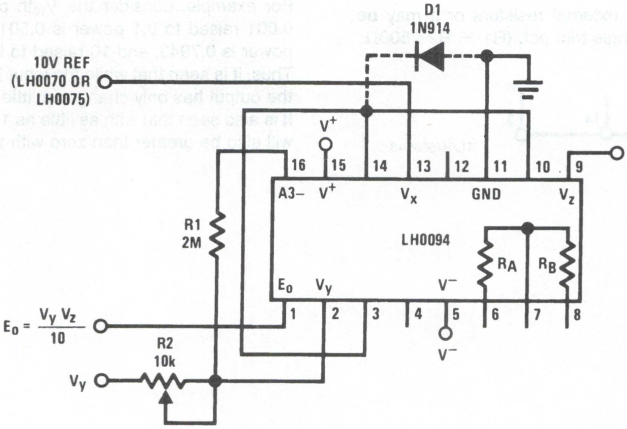


FIGURE 2b. Typical Performance of LH0094 in Multiply Mode Without External Adjustment


D1
1N914
10V REF
(LH0070 OR LH0075)
V+
V_z
16
15
14
13
12
11
10
9
A3−
V+
V_x
GND
V_z
R1
2M
LH0094
R_A
R_B
E_0
V_y
V−
1
2
3
4
5
6
7
8
E_0 = V_y V_z / 10
R2
10k
V_y
V−

$\frac{V_y V_z}{10}$ $m=1$

Trim Procedure

Set $V_Z = V_Y = 10V$

Adjust R2 until output = 10.000V

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FIGURE 3. Precision Multiplier (0.02% Typ) with 1 External Adjustment

Applications Information (Continued)

3. DIVIDE

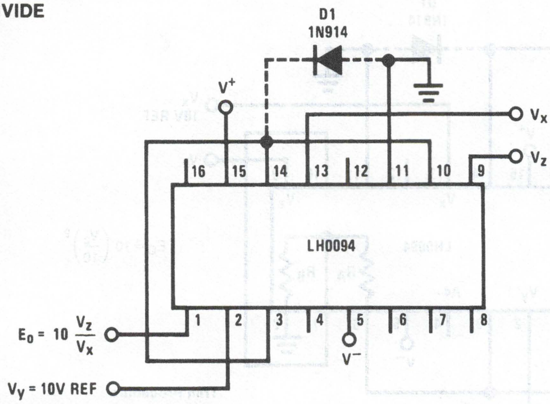
D1
1N914
V+
16
15
14
13
12
11
10
9
Vx
Vz
LH0094
1
2
3
4
5
6
7
8
V−
E0 = 10 Vz/Vx
Vy = 10V REF

FIGURE 4a. LH0094 Used to Divide (No External Adjustment)

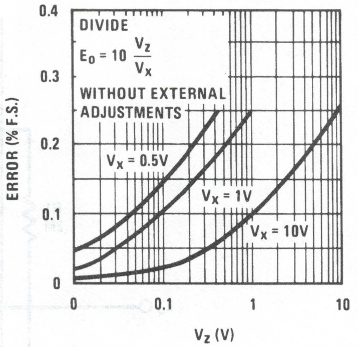

FIGURE 4b. Typical Performance, Divide Mode, Without External Adjustments

Trim Procedures

Apply 10V to V_Y, 0.1V to V_X and V_Z.
Adjust R3 until E_O = 10.000V.

Apply 10.000V to all inputs.
Adjust R2 until E_O = 10.000V

Repeat procedure.

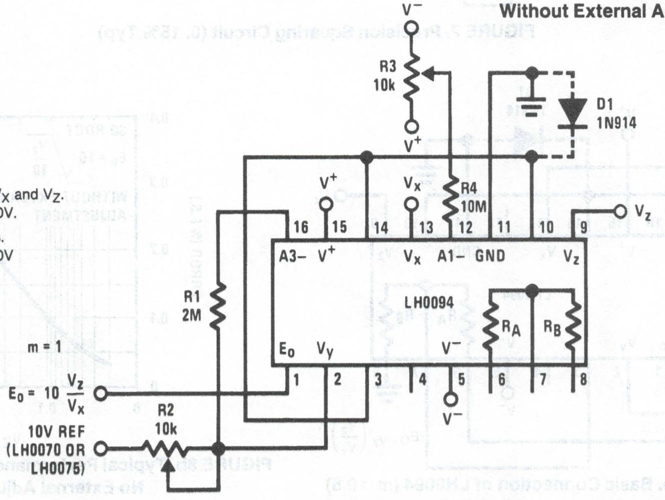
V−
R3
10k
V+
D1
1N914
V+
Vx
R4
10M
Vz
16
15
14
13
12
11
10
9
A3−
V+
Vx
A1−
GND
Vz
R1
2M
LH0094
RA
RB
E0
Vy
V−
1
2
3
4
5
6
7
8
V−
m = 1
E0 = 10 Vz/Vx
R2
10k
10V REF
(LH0070 OR
LH0075)

FIGURE 5. Precision Divider (0.05% Typ)

4. SQUARE

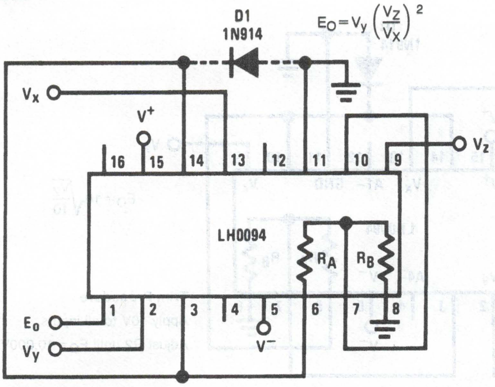
D1
1N914
E0 = Vy (Vz/Vx)²
Vx
V+
16
15
14
13
12
11
10
9
Vz
LH0094
RA
RB
E0
Vy
1
2
3
4
5
6
7
8
V−

FIGURE 6a. Basic Connection of LH0094 (m = 2) without External Adjustment Using Internal Resistors to Set m

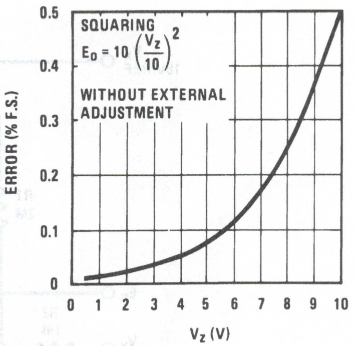

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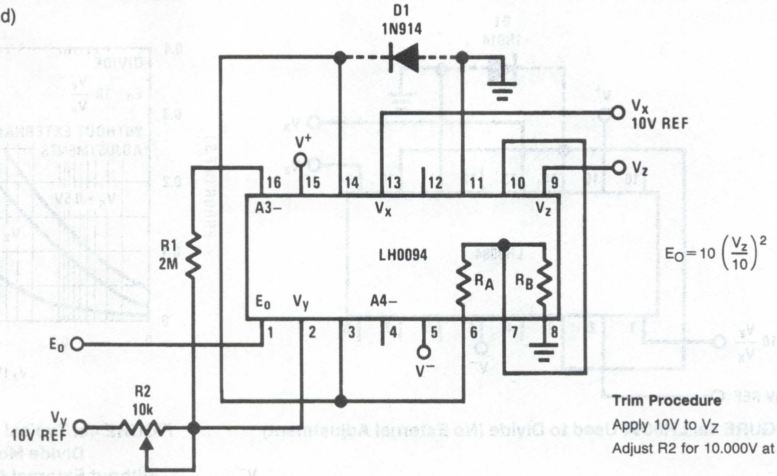
FIGURE 6b. Squaring Mode without External Adjustment

5

Applications Information (Continued)

4. SQUARE (Continued)


D1
1N914
V_X
10V REF
V^+
V_Z
16
15
14
13
12
11
10
9
A3−
V_X
V_Z
R1
2M
LH0094
R_A
R_B
E_O
V_Y
A4−
E_O
1
2
3
4
5
6
7
8
V^-
R2
10k
V_Y
10V REF
$E_O = 10\left(\frac{V_Z}{10}\right)^2$

Trim Procedure

Apply 10V to V_Z

Adjust R2 for 10.000V at output

FIGURE 7. Precision Squaring Circuit (0. 15% Typ)

5. SQUARE ROOT

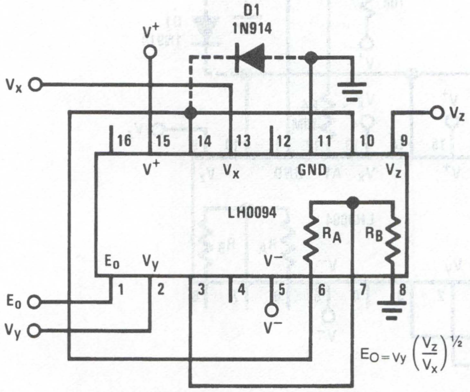

D1
1N914
V^+
V_X
V_Z
16
15
14
13
12
11
10
9
V^+
V_X
GND
V_Z
LH0094
R_A
R_B
E_O
V_Y
V^-
1
2
3
4
5
6
7
8
E_O
V_Y
V^-
$E_O = V_Y\left(\frac{V_Z}{V_X}\right)^{1/2}$

FIGURE 8a. Basic Connection of LH0094 (m = 0.5) without External Adjustment Using Internal Resistors to Set m

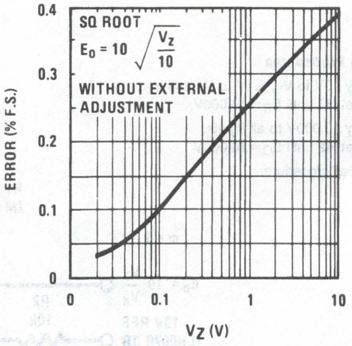
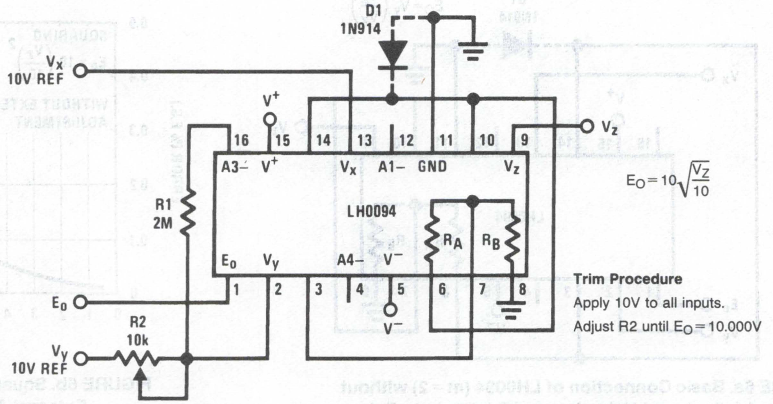


FIGURE 8b. Typical Performance Curve Square Root, No External Adjustment


D1
1N914
V_X
10V REF
V^+
V_Z
16
15
14
13
12
11
10
9
A3−
V^+
V_X
A1−
GND
V_Z
R1
2M
LH0094
R_A
R_B
E_O
V_Y
A4−
V^-
1
2
3
4
5
6
7
8
E_O
V^-
R2
10k
V_Y
10V REF
$E_O = 10\sqrt{\frac{V_Z}{10}}$

Trim Procedure

Apply 10V to all inputs.

Adjust R2 until $E_O = 10.000V$

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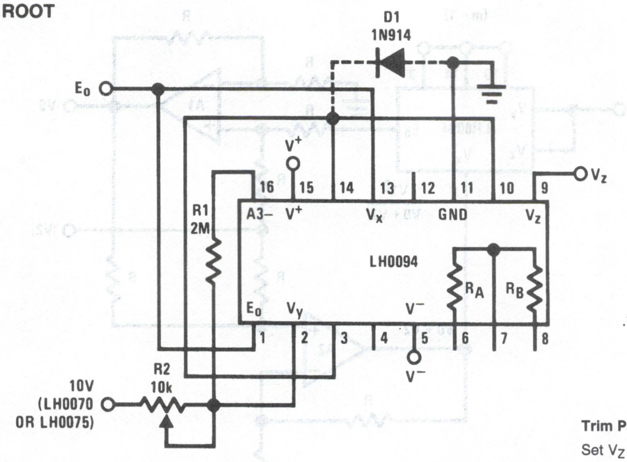
FIGURE 9. Precision Square Rooter (0.15% Typ)

Applications Information (Continued)

6. LOW LEVEL SQUARE ROOT


D1
1N914
E_0
V^+
16
15
14
13
12
11
10
9
V_z
R1
2M
A3−
V^+
V_x
GND
V_z
LH0094
R_A
R_B
E_0
V_y
V^-
1
2
3
4
5
6
7
8
V^-
R2
10k
10V
(LH0070
OR LH0075)

m = 1

$$E_O = 10\,\frac{V_Z}{E_O}$$

$$E_O{}^2 = 10\,V_Z$$

$$\therefore\ E_O = \sqrt{10\,V_Z}$$

$$5\text{ mV} \le V_Z \le 10\text{V}$$

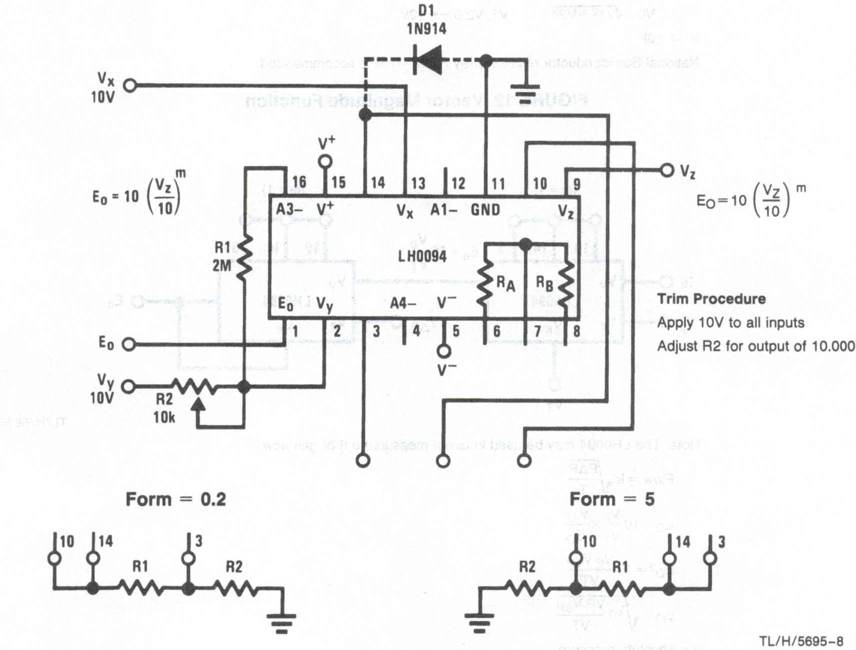
Trim Procedure

Set $V_Z = 10\text{V}$

Adjust R2 until output = 10.000V

FIGURE 10. 3-Decade Precision Square Root Circuit Using the LH0094 with m = 1

Typical Applications


D1
1N914
V_x
10V
V^+
$E_0 = 10\left(\frac{V_z}{10}\right)^m$
16
15
14
13
12
11
10
9
V_z
$E_O = 10\left(\frac{V_Z}{10}\right)^m$
R1
2M
A3−
V^+
V_x
A1−
GND
V_z
LH0094
R_A
R_B
E_0
V_y
A4−
V^-
1
2
3
4
5
6
7
8
V^-
E_0
V_y
10V
R2
10k
Form = 0.2
10
14
3
R1
R2
Form = 5
10
14
3
R2
R1
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Trim Procedure

Apply 10V to all inputs

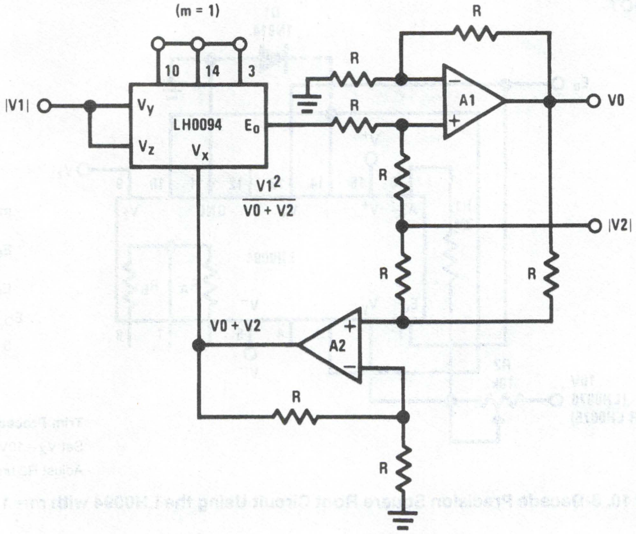
Adjust R2 for output of 10.000V

$m = \frac{R2}{R1 + R2}$; Choose R1 = 200Ω
∴ R2 = 50Ω

$m = \frac{R1 + R2}{R2}$; Choose R2 = 50Ω
∴ R1 = 200Ω

FIGURE 11. Precision Exponentiator (m = 0.2 to 5)

Typical Applications (Continued)


(m = 1)
10
14
3
|V1|
Vy
LH0094
Eo
Vz
Vx
V1²/(V0 + V2)
R
R
R
A1
V0
R
|V2|
R
R
V0 + V2
A2
R
R

Note. The LH0094 may be used to generate a voltage equivalent to:

$V0=\sqrt{V1^2+V2^2}$

$V0=V2+\dfrac{V1^2}{V0+V2}$

$V0^2+V0\ V2=V2\ V0+V2^2+V1^2$

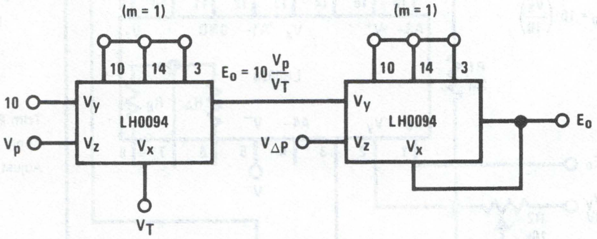
$V0^2=V1^2+V2^2$

$\therefore\ V0=\sqrt{V1^2+V2^2}$ V1, V2 0 → 10V

$R \approx 10k$

National Semiconductor resistor array RA08—10k is recommended

FIGURE 12. Vector Magnitude Function


(m = 1)
10
14
3
10
Vy
LH0094
Vp
Vz
Vx
VT
Eo = 10 Vp/VT
(m = 1)
10
14
3
Vy
LH0094
VΔP
Vz
Vx
Eo

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Note. The LH0094 may be used in direct measurement of gas flow.

$\text{Flow} = k\sqrt{\dfrac{P\Delta P}{T}}$

$E_O=10\,\dfrac{V_P}{V_T}\times\dfrac{V_{\Delta P}}{E_O}$

$E_O{}^2=10\,\dfrac{V_P\,V_{\Delta P}}{VT}$

$E_O=\sqrt{10\,\dfrac{VP\,V_{\Delta P}}{VT}}$

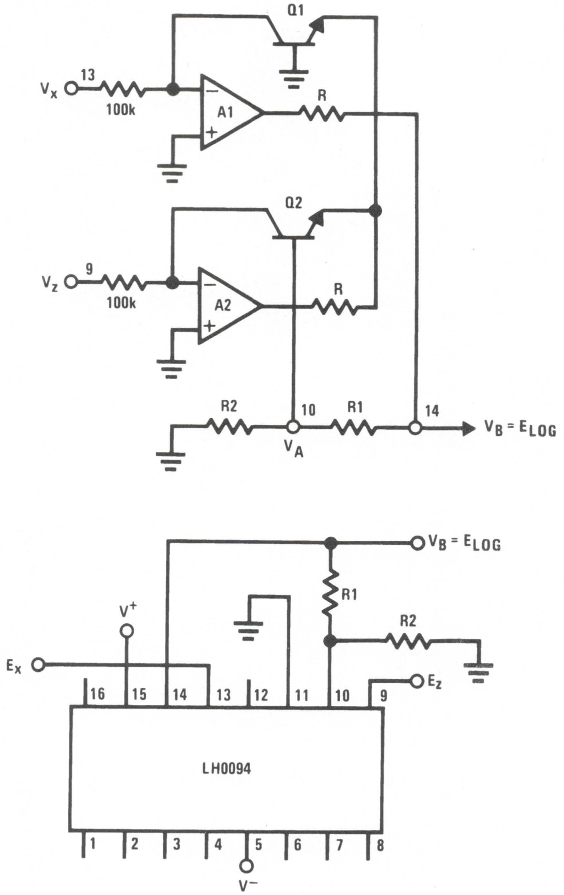
P = Absolute pressure

T = Absolute temperature

ΔP = Pressure drop

FIGURE 13. Mass Gas Flow Circuit

Typical Applications (Continued)


Q1
13
V_X
100k
A1
R
Q2
9
V_Z
100k
A2
R
R2
10
R1
14
$V_B = E_{LOG}$
V_A
$V_B = E_{LOG}$
R1
R2
V^+
E_X
E_Z
16
15
14
13
12
11
10
9
LH0094
1
2
3
4
5
6
7
8
V^-

TL/H/5695–10

Note. The LH0094 may also be used to generate the Log of a ratio of 2 voltages. The output is taken from pin 14 of the LH0094 for the Log application.

$$E_{LOG} = K1 \frac{KT}{q} \ell n \frac{V_Z}{V_X}$$

$$\text{where } K1 = \frac{R1 + R2}{R2}$$

$$\text{If } K1 = \frac{1}{KT/q \, \ell n 10}$$

$$\text{then } E_{LOG} = \text{Log}_{10} \frac{V_Z}{V_X}$$

$R1 = 15.9\ R2$

$R2 \approx 400\Omega$

R2 must be a thermistor with a tempco of ≈ 0.33%/°C to be compensated over temperature.

FIGURE 14. Log Amp Application

Section 6

Temperature Sensors

6

Section 6 Contents

Temperature Sensor Selection Guide 6-3
LM34/LM34A/LM34C/LM34CA/LM34D Precision Fahrenheit Temperature Sensors 6-4
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LM3911 Temperature Controller 6-30

National Semiconductor Corporation

Temperature Sensor Selection Guide

Part	Temp. Range	*Accuracy	Output Scale
LM34A	−50°F to +300°F	±2.0°F	10 mV/°F
LM34	−50°F to +300°F	±3.0°F	10 mV/°F
LM34CA	−40°F to +230°F	±2.0°F	10 mV/°F
LM34C	−40°F to +230°F	±3.0°F	10 mV/°F
LM34D	+32°F to +212°F	±4.0°F	10 mV/°F
LM35A	−55°C to +150°C	±1.0°C	10 mV/°C
LM35	−55°C to +150°C	±1.5°C	10 mV/°C
LM35CA	−40°C to +110°C	±1.0°C	10 mV/°C
LM35C	−40°C to +110°C	±1.5°C	10 mV/°C
LM35D	0°C to +100°C	±2.0°C	10 mV/°C
LM134-3	−55°C to +125°C	±3.0°C	$I_{SET} \propto$ °k
LM134-6	−55°C to +125°C	±6.0°C	$I_{SET} \propto$ °k
LM234-3	−25°C to +100°C	±3.0°C	$I_{SET} \propto$ °k
LM234-6	−25°C to +100°C	±6.0°C	$I_{SET} \propto$ °k
LM135A	−55°C to +150°C	±1.3°C	10 mV/°k
LM135	−55°C to +150°C	±2.0°C	10 mV/°k
LM235A	−40°C to +125°C	±1.3°C	10 mV/°k
LM235	−40°C to +125°C	±2.0°C	10 mV/°k
LM335A	−40°C to +100°C	±2.0°C	10 mV/°k
LM335	−40°C to +100°C	±4.0°C	10 mV/°k
LM3911	−25°C to +85°C	±10.0°C	10 mV/°k (or °F)

***Note:** Accuracy is measured over T(Min) to T(Max) uncalibrated

Note: The LM134/234/334 3-Terminal Adjustable current sources Datasheet can be found in Linear 1, Section 1.

National
Semiconductor
Corporation

LM34/LM34A/LM34C/LM34CA/LM34D Precision Fahrenheit Temperature Sensors

General Description

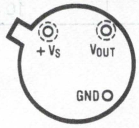
The LM34 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Fahrenheit temperature. The LM34 thus has an advantage over linear temperature sensors calibrated in degrees Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Fahrenheit scaling. The LM34 does not require any external calibration or trimming to provide typical accuracies of ±½°F at room temperature and ±1½°F over a full −50 to +300°F temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM34's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies or with plus and minus supplies. As it draws only 70 μA from its supply, it has very low self-heating, less than 0.2°F in still air. The LM34 is rated to operate over a −50° to +300°F temperature range, while the LM34C is rated for a −40° to +230°F range (0°F with improved accuracy). The LM34 series is available packaged in hermetic TO-46 transistor packages, while the LM34C is also available in the plastic TO-92 transistor package. The LM34 is a complement to the LM35 (Centigrade) temperature sensor.

Features

- Calibrated directly in degrees Fahrenheit
- Linear +10.0 mV/°F scale factor
- 1.0°F accuracy guaranteed (at +77°F)
- Rated for full −50° to +300°F range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 5 to 30 volts
- Less than 70 μA current drain
- Low self-heating, 0.18°F in still air
- Nonlinearity only ±0.5°F typical
- Low-impedance output, 0.4Ω for 1 mA load

Connection Diagrams

TO-46 Metal Can Package*

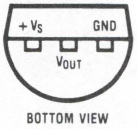


TL/H/6685-1

*Case is connected to negative pin.

Order Numbers LM34H, LM34AH, LM34CH, LM34CAH or LM34DH
See NS Package Number H03H

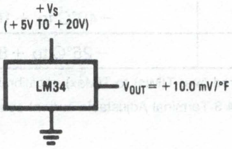
TO-92 Plastic Package



TL/H/6685-2

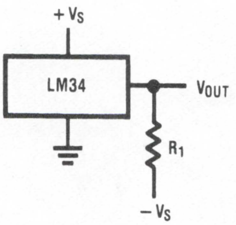
Order Number LM34CZ or LM34DZ
See NS Package Number Z03A

Typical Applications



TL/H/6685-3

FIGURE 1. Basic Fahrenheit Temperature Sensor (+5° to +300°F)



CHOOSE $R_1 = (-V_S)/50\ \mu A$
$V_{OUT} = +3{,}000$ mV AT +300°F
$= +750$ mV AT +75°F
$= -500$ mV AT −50°F

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FIGURE 2. Full-Range Fahrenheit Temperature Sensor

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temperature,	
TO-46 Package	−76°F to +356°F
TO-92 Package	−76°F to +300°F

Lead Temp. (Soldering, 10 seconds)	
TO-46 Package	+300°C
TO-92 Package	+260°C
Specified Operating Temp. Range (Note 2)	
	T_{MIN} to T_{MAX}
LM34, LM34A	−50°F to +300°F
LM34C, LM34CA	−40°F to +230°F
LM34D	+32°F to +212°F

DC Electrical Characteristics (Note 1, Note 6)

Parameter	Conditions	LM34A			LM34CA			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	$T_A = +77°F$	±0.4	±1.0		±0.4	±1.0		°F
	$T_A = 0°F$	±0.6			±0.6		±2.0	°F
	$T_A = T_{MAX}$	±0.8	±2.0		±0.8	±2.0		°F
	$T_A = T_{MIN}$	±0.8	±2.0		±0.8		±3.0	°F
Nonlinearity (Note 8)	$T_{MIN} \leq T_A \leq T_{MAX}$	**±0.35**		**±0.7**	**±0.30**		**±0.6**	°F
Sensor Gain (Average Slope)	$T_{MIN} \leq T_A \leq T_{MAX}$	**+10.0**	**+9.9,**		**+10.0**		**+9.9,**	mV/°F, min
			+10.1				**+10.1**	mV/°F, max
Load Regulation (Note 3)	$T_A = +77°F$	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \leq T_A \leq T_{MAX}$ $0 \leq I_L \leq 1$ mA	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
Line Regulation (Note 3)	$T_A = +77°F$	±0.01	±0.05		±0.01	±0.05		mV/V
	$5V \leq V_S \leq 30V$	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	$V_S = +5V, +77°F$	75	90		75	90		μA
	$V_S = +5V$	**131**		**160**	**116**		**139**	μA
	$V_S = +30V, +77°F$	76	92		76	92		μA
	$V_S = +30V$	**132**		**163**	**117**		**142**	μA
Change of Quiescent Current (Note 3)	$4V \leq V_S \leq 30V, +77°F$	+0.5	2.0		0.5	2.0		μA
	$5V \leq V_S \leq 30V$	**+1.0**		**3.0**	**1.0**		**3.0**	μA
Temperature Coefficient of Quiescent Current		**+0.30**		**+0.5**	**+0.30**		**+0.5**	μA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1,* $I_L = 0$	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	$T_j = T_{MAX}$ for 1000 hours	±0.16			±0.16			°F

Note 1: Unless otherwise noted, these specifications apply: $-50°F \leq T_j \leq +300°F$ for the LM34 and LM34A; $-40°F \leq T_j \leq +230°F$ for the LM34C and LM34CA; and $+32°F \leq T_j \leq +212°F$ for the LM34D. $V_S = +5$ Vdc and $I_{LOAD} = 50$ μA in the circuit of *Figure 2;* +6 Vdc for LM34 and LM34A for $230°F \leq T_j \leq 300°F$. These specifications also apply from +5°F to T_{MAX} in the circuit of *Figure 1.*

Note 2: Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1.*

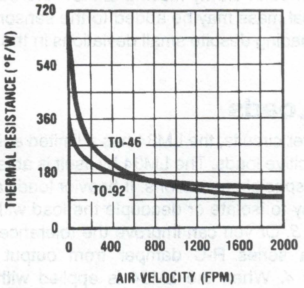
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

DC Electrical Characteristics (Note 1, **Note 6**) (Continued)

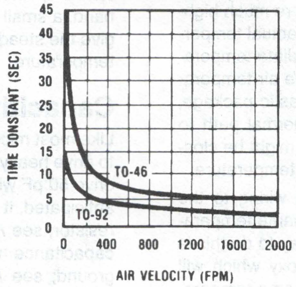
Parameter	Conditions	LM34			LM34C, LM34D			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM34, LM34C (Note 7)	T_A = +77°F	±0.8	±2.0		±0.8	±2.0		°F
	T_A = 0°F	±1.0			±1.0		±3.0	°F
	$T_A = T_{MAX}$	±1.6	±3.0		±1.6		±3.0	°F
	$T_A = T_{MIN}$	±1.6		±3.0	±1.6		±4.0	°F
Accuracy, LM34D (Note 7)	T_A = +77°F				±1.2	±3.0		°F
	$T_A = T_{MAX}$				±1.8		±4.0	°F
	$T_A = T_{MIN}$				±1.8		±4.0	°F
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.6**		**±1.0**	**±0.4**		**±1.0**	°F
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.8,**		**+10.0**		**+9.8,**	mV/°F, min
			+10.2				**+10.2**	mV/°F, max
Load Regulation (Note 3)	T_A = +77°F	±0.4	±2.5		±0.4	±2.5		mV/mA
	$T_{MIN} \le T_A \le$ +150°F	**±0.5**		**±6.0**	**±0.5**		**±6.0**	mV/mA
	$0 \le I_L \le 1$ mA							
Line Regulation (Note 3)	T_A = +77°F	±0.01	±0.1		±0.01	±0.1		mV/V
	$5V \le V_S \le 30V$	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +77°F	75	100		75	100		μA
	V_S = +5V	**131**		**176**	**116**		**154**	μA
	V_S = +30V, +77°F	76	103		76	103		μA
	V_S = +30V	**132**		**181**	**117**		**159**	μA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +77°F	+0.5	3.0		0.5	3.0		μA
	$5V \le V_S \le 30V$	**+1.0**		**5.0**	**1.0**		**5.0**	μA
Temperature Coefficient of Quiescent Current		**+0.30**		**+0.7**	**+0.30**		**+0.7**	μA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	$T_j = T_{MAX}$ for 1000 hours	±0.16			±0.16			°F

Typical Performance Characteristics

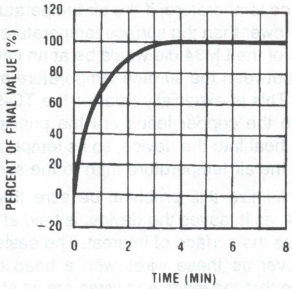
Thermal Resistance Junction to Air



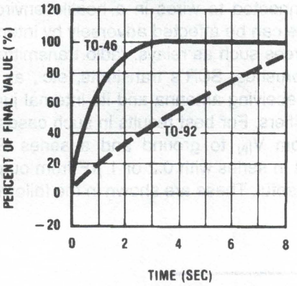
Thermal Time Constant



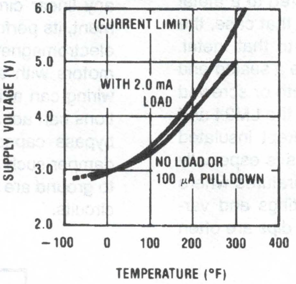
Thermal Response in Still Air



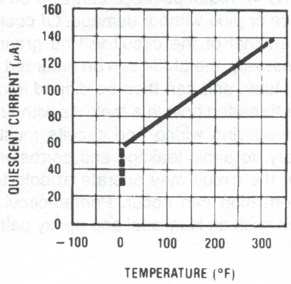
Thermal Response in Stirred Oil Bath



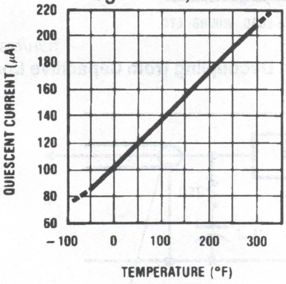
Minimum Supply Voltage vs. Temperature



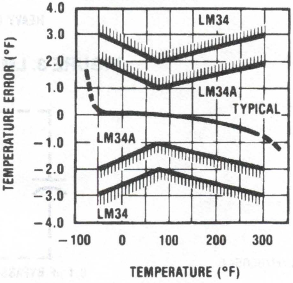
Quiescent Current vs. Temperature (In Circuit of *Figure 1*)



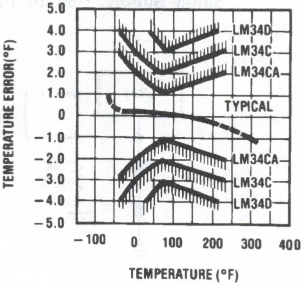
Quiescent Current vs. Temperature (In Circuit of *Figure 2*; $-V_S = -5V$, R1 = 100k)



Accuracy vs. Temperature (Guaranteed)



Accuracy vs. Temperature (Guaranteed)



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Typical Applications

The LM34 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.02°F of the surface temperature. This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM34 die would be at an intermediate temperature between the surface temperature and the air temperature. This is expecially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM34, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM34 die's temperature will not be affected by the air temperature.

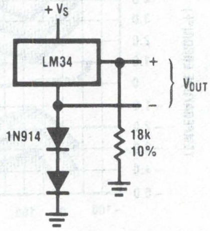
The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course in that case, the V_- terminal of the circuit will be grounded to that metal. Alternatively, the LM34 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM34 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM34 or its connections.

These devices are sometimes soldered to a small, lightweight heat fin to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor to give the steadiest reading despite small deviations in the air temperature.

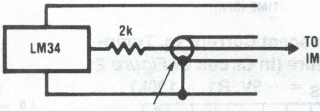
Capacitive Loads

Like most micropower circuits, the LM34 has a limited ability to drive heavy capacitive loads. The LM34 by itself is able to drive 50 pF without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3.* Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4.* When the LM34 is applied with a 499Ω load resistor (as shown), it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR's transients, etc., as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 μF from output to ground are often useful. These are shown in the following circuits.

Temperature Sensor, Single Supply, −50° to +300°F

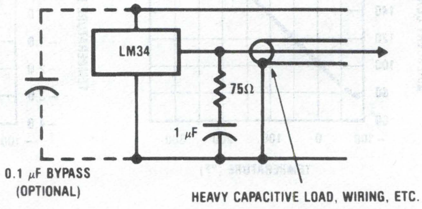


TL/H/6685-6



TL/H/6685-7

FIGURE 3. LM34 with Decoupling from Capacitive Load



TL/H/6685-8

FIGURE 4. LM34 with R-C Damper

Temperature Rise of LM34 Due to Self-Heating (Thermal Resistance)

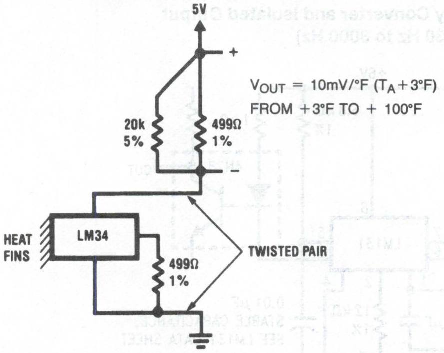
Conditions	TO-46, No Heat Sink	TO-46, Small Heat Fin*	TO-92, No Heat Sink	TO-92, Small Heat Fin**
Still air	720°F/W	180°F/W	324°F/W	252°F/W
Moving air	180°F/W	72°F/W	162°F/W	126°F/W
Still oil	180°F/W	72°F/W	162°F/W	126°F/W
Stirred oil	90°F/W	54°F/W	81°F/W	72°F/W
(Clamped to metal, infinite heat sink)	(43°F/W)			

*Wakefield type 201 or 1″ disc of 0.020″ sheet brass, soldered to case, or similar.

**TO-92 package glued and leads soldered to 1″ square of ¹⁄₁₆″ printed circuit board with 2 oz copper foil, or similar.

Typical Applications (Continued)

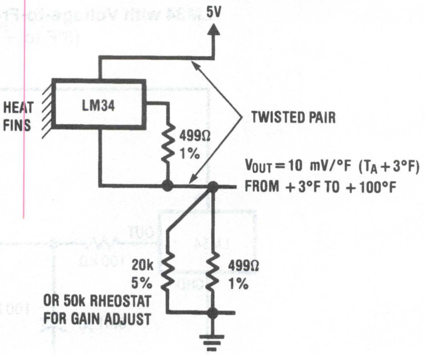
Two-Wire Remote Temperature Sensor (Grounded Sensor)


5V
+
−
20k
5%
499Ω
1%
HEAT
FINS
LM34
499Ω
1%
TWISTED PAIR

V_{OUT} = 10mV/°F (T_A+3°F)
FROM +3°F TO + 100°F

TL/H/6685-9

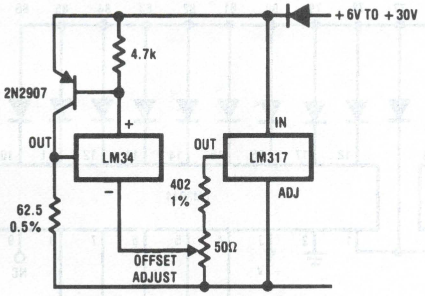
Two-Wire Remote Temperature Sensor (Output Referred to Ground)


5V
HEAT
FINS
LM34
499Ω
1%
TWISTED PAIR
20k
5%
499Ω
1%
OR 50k RHEOSTAT
FOR GAIN ADJUST

V_{OUT} = 10 mV/°F (T_A+3°F)
FROM +3°F TO +100°F

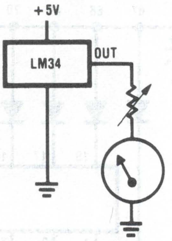
TL/H/6685-10

4-to-20 mA Current Source (0 to +100°F)


+6V TO +30V
4.7k
2N2907
+
IN
OUT
LM34
OUT
LM317
−
402
1%
ADJ
62.5
0.5%
50Ω
OFFSET
ADJUST

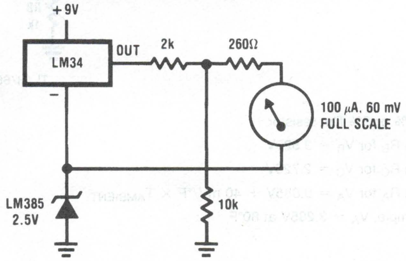
TL/H/6685-11

Fahrenheit Thermometer (Analog Meter)



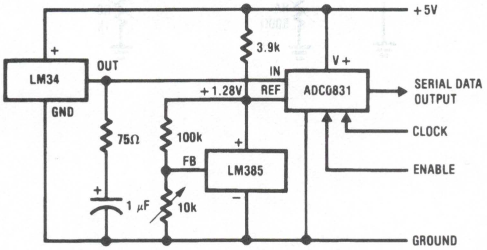
TL/H/6685-12

Expanded Scale Thermometer (50° to 80° Fahrenheit, for Example Shown)


+9V
LM34
OUT
2k
260Ω
−
100 µA, 60 mV
FULL SCALE
LM385
2.5V
10k

TL/H/6685-13

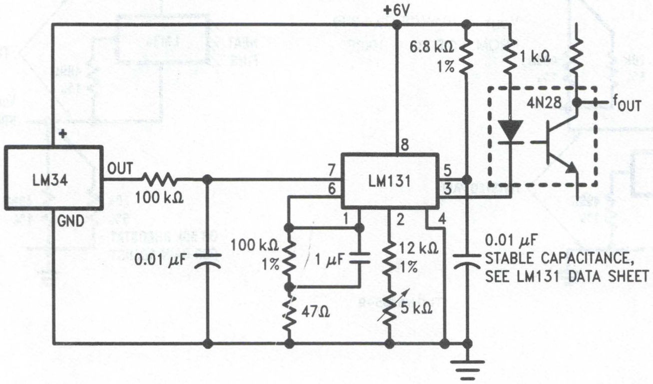
Temperature-to-Digital Converter (Serial Output, +128°F Full Scale)


+5V
+
3.9k
V+
LM34
OUT
IN
+1.28V
REF
ADC0831
SERIAL DATA
OUTPUT
GND
75Ω
100k
+
CLOCK
FB
LM385
ENABLE
+
1 µF
10k
−
GROUND

TL/H/6685-14

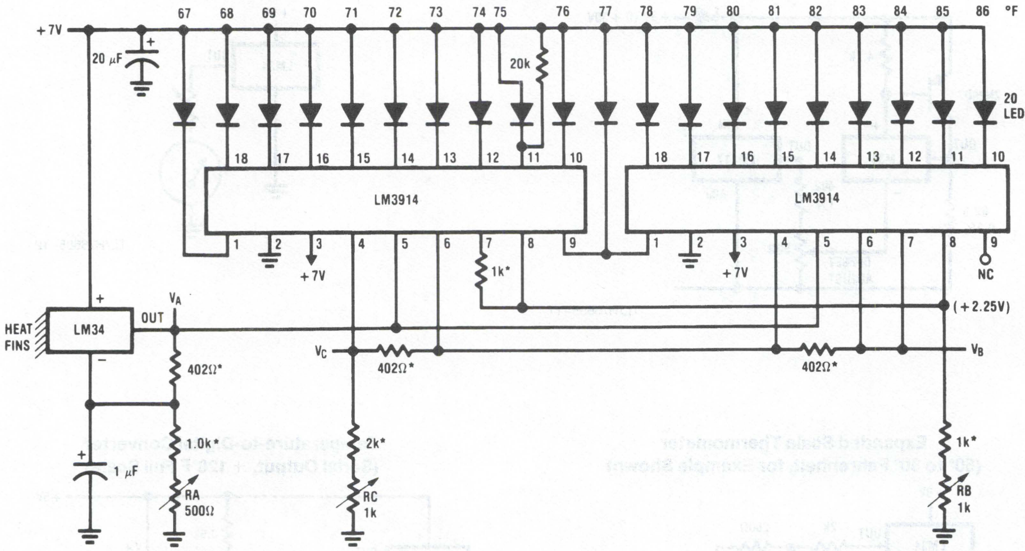
Typical Applications (Continued)

LM34 with Voltage-to-Frequency Converter and Isolated Output (3°F to + 300°F; 30 Hz to 3000 Hz)


+6V
6.8 kΩ
1%
1 kΩ
4N28
f_{OUT}
+
LM34
OUT
GND
100 kΩ
LM131
8
7
6
5
3
1
2
4
100 kΩ
1%
1 µF
12 kΩ
1%
5 kΩ
47Ω
0.01 µF
0.01 µF
STABLE CAPACITANCE,
SEE LM131 DATA SHEET

TL/H/6685–15

Bar-Graph Temperature Display (Dot Mode)


67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
°F
+7V
20 µF
20k
20 LEDs
LM3914
LM3914
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9
+7V
1k*
NC
(+2.25V)
HEAT FINS
LM34
OUT
V_A
V_C
V_B
402Ω*
402Ω*
402Ω*
1.0k*
RA 500Ω
2k*
RC 1k
1k*
RB 1k
1 µF

TL/H/6685–16

* = 1% or 2% film resistor

—Trim R_B for V_B = 3.525V

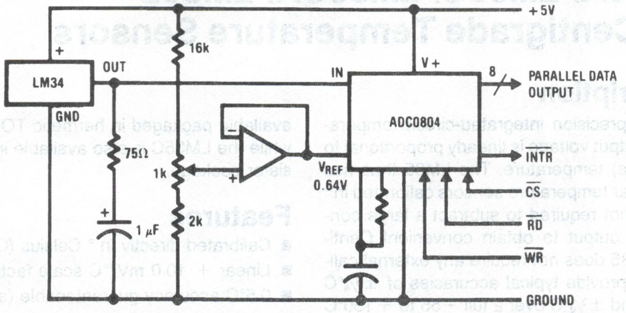
—Trim R_C for V_C = 2.725V

—Trim R_A for V_A = 0.085V + 40 mV/°F × $T_{AMBIENT}$

—Example, V_A = 3.285V at 80°F

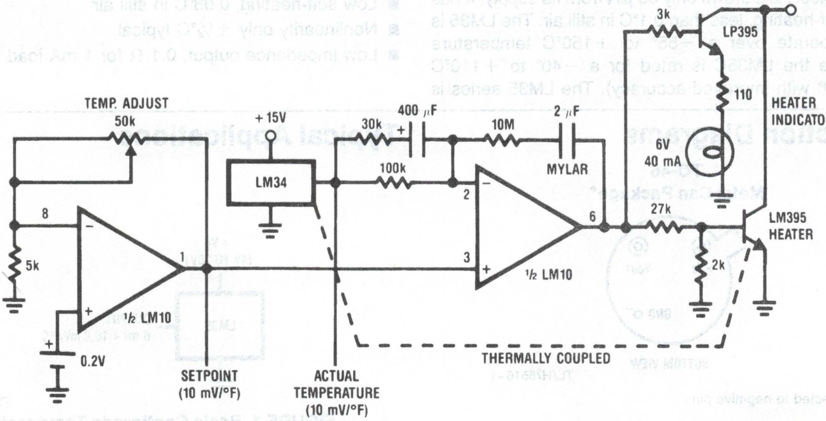
Typical Applications (Continued)

Temperature-to-Digital Converter
(Parallel TRI-STATE® Outputs for Standard Data Bus to μP Interface, 128 °F Full Scale)


+5V
16k
+
LM34
OUT
GND
75Ω
+
1 μF
1k
2k
IN
V+
8
PARALLEL DATA
OUTPUT
ADC0804
INTR
V_{REF}
0.64V
CS
RD
WR
GROUND

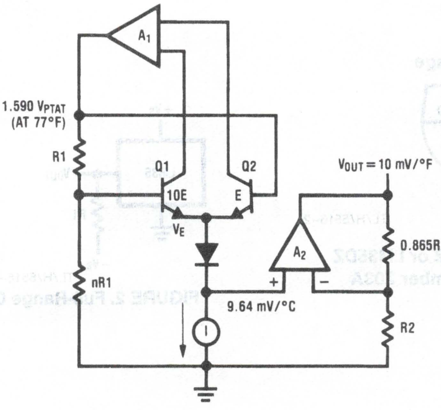
TL/H/6685-17

Temperature Controller


TEMP. ADJUST
50k
+15V
30k
400 μF
+
10M
2 μF
+15V
3k
LP395
110
HEATER
INDICATOR
6V
40 mA
LM34
100k
MYLAR
8
−
2
−
6
27k
LM395
HEATER
5k
1
3
+
2k
+
½ LM10
½ LM10
+
0.2V
THERMALLY COUPLED
SETPOINT
(10 mV/°F)
ACTUAL
TEMPERATURE
(10 mV/°F)

TL/H/6685-18

Block Diagram


A_1
1.590 V_{PTAT}
(AT 77°F)
R1
Q1
10E
Q2
E
V_E
V_{OUT} = 10 mV/°F
A_2
0.865R2
nR1
+
−
9.64 mV/°C
I
R2

TL/H/6685-19

National Semiconductor Corporation

LM35/LM35A/LM35C/LM35CA/LM35D Precision Centigrade Temperature Sensors

General Description

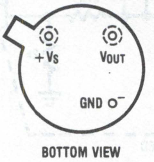
The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 μA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C is also available in the plastic TO-92 transistor package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 μA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Connection Diagrams

TO-46
Metal Can Package*

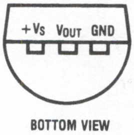


TL/H/5516-1

*Case is connected to negative pin

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

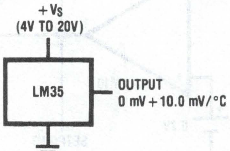
TO-92
Plastic Package



TL/H/5516-2

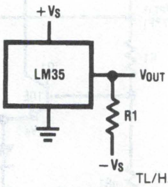
Order Number LM35CZ or LM35DZ
See NS Package Number Z03A

Typical Applications



TL/H/5516-3

FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)



TL/H/5516-4

Choose $R_1 = -V_S/50\ \mu A$

$V_{OUT} = +1{,}500$ mV at +150°C
$= +250$ mV at +25°C
$= -550$ mV at −55°C

FIGURE 2. Full-Range Centigrade Temperature Sensor

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temp., TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
Lead Temp. (Soldering, 10 seconds):	
TO-46 Package,	300°C
TO-92 Package,	260°C

Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)

LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

Electrical Characteristics (Note 1) **(Note 6)**

Parameter	Conditions	LM35A			LM35CA			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	$T_A = +25°C$	±0.2	±0.5		±0.2	±0.5		°C
	$T_A = -10°C$	±0.3			±0.3		±1.0	°C
	$T_A = T_{MAX}$	±0.4	±1.0		±0.4	±1.0		°C
	$T_A = T_{MIN}$	±0.4	±1.0		±0.4		±1.5	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.18**		**±0.35**	**±0.15**		**±0.3**	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9,** **+10.1**		**+10.0**		**+9.9,** **+10.1**	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	$T_A = +25°C$	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
Line Regulation (Note 3)	$T_A = +25°C$	±0.01	±0.05		±0.01	±0.05		mV/V
	$4V \le V_S \le 30V$	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	$V_S = +5V$, +25°C	56	67		56	67		µA
	$V_S = +5V$	**105**		**131**	**91**		**114**	µA
	$V_S = +30V$, +25°C	56.2	68		56.2	68		µA
	$V_S = +30V$	**105.5**		**133**	**91.5**		**116**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +25°C	0.2	1.0		0.2	1.0		µA
	$4V \le V_S \le 30V$	**0.5**		**2.0**	**0.5**		**2.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.5**	**+0.39**		**+0.5**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, $I_L = 0$	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	$T_J = T_{MAX}$, for 1000 hours	±0.08			±0.08			°C

Note 1: Unless otherwise noted, these specifications apply: $-55°C \le T_J \le +150°C$ for the LM35 and LM35A; $-40° \le T_J \le +110°C$ for the LM35C and LM35CA; and $0° \le T_J \le +100°C$ for the LM35D. $V_S = +5$Vdc and $I_{LOAD} = 50$ µA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 440°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient.

Electrical Characteristics (Note 1) **(Note 6)** (Continued)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM35, LM35C (Note 7)	$T_A = +25°C$	±0.4	±1.0		±0.4	±1.0		°C
	$T_A = -10°C$	±0.5			±0.5		±1.5	°C
	$T_A = T_{MAX}$	±0.8	±1.5		±0.8		±1.5	°C
	$T_A = T_{MIN}$	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	$T_A = +25°C$				±0.6	±1.5		°C
	$T_A = T_{MAX}$				±0.9		±2.0	°C
	$T_A = T_{MIN}$				±0.9		±2.0	°C
Nonlinearity (Note 8)	$T_{MIN} \leq T_A \leq T_{MAX}$	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	$T_{MIN} \leq T_A \leq T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) $0 \leq I_L \leq 1$ mA	$T_A = +25°C$	±0.4	±2.0		±0.4	±2.0		mV/mA
	$T_{MIN} \leq T_A \leq T_{MAX}$	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation (Note 3)	$T_A = +25°C$	±0.01	±0.1		±0.01	±0.1		mV/V
	$4V \leq V_S \leq 30V$	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	$V_S = +5V, +25°C$	56	80		56	80		μA
	$V_S = +5V$	**105**		**158**	**91**		**138**	μA
	$V_S = +30V, +25°C$	56.2	82		56.2	82		μA
	$V_S = +30V$	**105.5**		**161**	**91.5**		**141**	μA
Change of Quiescent Current (Note 3)	$4V \leq V_S \leq 30V, +25°C$	0.2	2.0		0.2	2.0		μA
	$4V \leq V_S \leq 30V$	**0.5**		**3.0**	**0.5**		**3.0**	μA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39**		**+0.7**	μA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, $I_L = 0$	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	$T_J = T_{MAX}$, for 1000 hours	±0.08			±0.08			°C

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

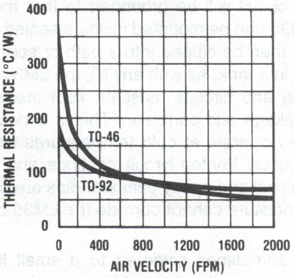
Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

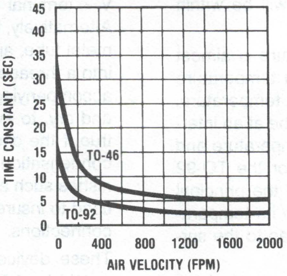
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Typical Performance Characteristics

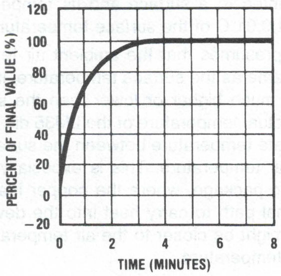
Thermal Resistance Junction to Air



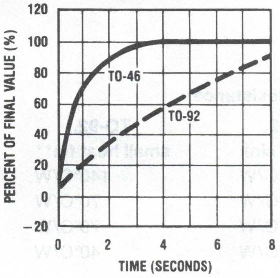
Thermal Time Constant



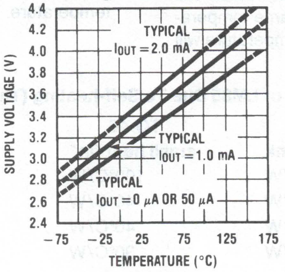
Thermal Response in Still Air



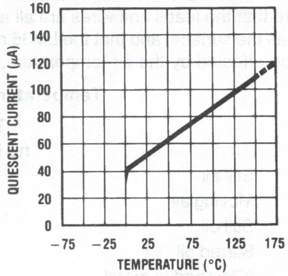
Thermal Response in Stirred Oil Bath



Minimum Supply Voltage vs. Temperature

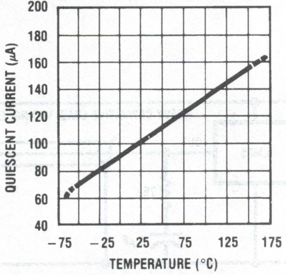


Quiescent Current vs. Temperature (In Circuit of *Figure 1.*)

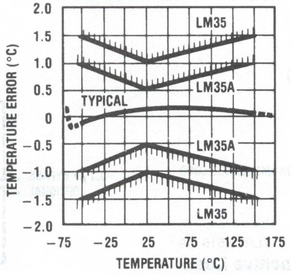


TL/H/5516–17

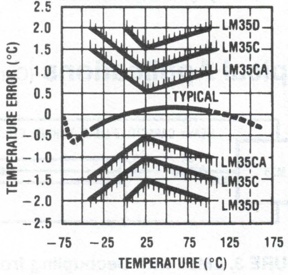
Quiescent Current vs. Temperature (In Circuit of *Figure 2.*)



Accuracy vs. Temperature (Guaranteed)



Accuracy vs. Temperature (Guaranteed)



TL/H/5516–18

Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is expecially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

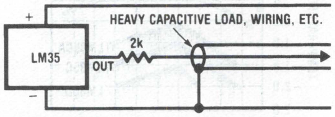
Temperature Rise of LM35 Due To Self-heating (Thermal Resistance)

	TO-46, no heat sink	**TO-46, small heat fin***	**TO-92, no heat sink**	**TO-92, small heat fin****
Still air	400°C/W	100°C/W	180°C/W	140°C/W
Moving air	100°C/W	40°C/W	90°C/W	70°C/W
Still oil	100°C/W	40°C/W	90°C/W	70°C/W
Stirred oil	50°C/W	30°C/W	45°C/W	40°C/W
(Clamped to metal, Infinite heat sink)	(24°C/W)			

* Wakefield type 201, or 1″ disc of 0.020″ sheet brass, soldered to case, or similar.

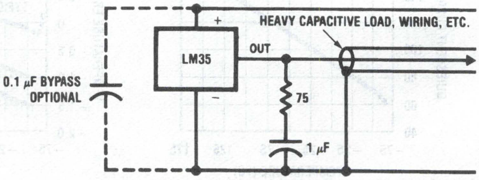
** TO-92 package glued and leads soldered to 1″ square of 1/16″ printed circuit board with 2 oz. foil or similar.

Typical Applications (Continued)



TL/H/5516–19

FIGURE 3. LM35 with Decoupling from Capacitive Load



TL/H/5516–20

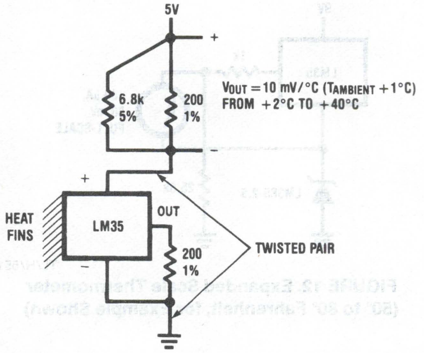
FIGURE 4. LM35 with R-C Damper

CAPACITIVE LOADS

Like most micropower circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pf without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4*.

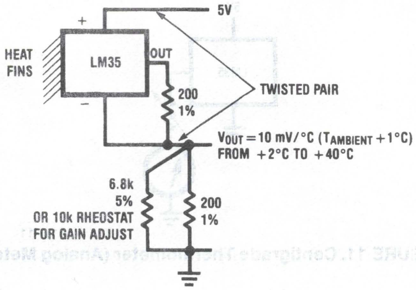
When the LM35 is applied with a 200Ω load resistor as shown in *Figure 5, 6,* or *8,* it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 μF from output to ground are often useful. These are shown in *Figures 13, 14,* and *16.*

Typical Applications (Continued)


5V
+
6.8k
5%
200
1%
V_{OUT} = 10 mV/°C ($T_{AMBIENT}$ +1°C)
FROM +2°C TO +40°C
−
+
HEAT FINS
LM35
OUT
200
1%
TWISTED PAIR
−

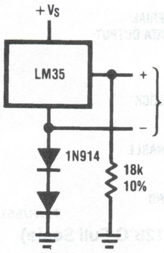
TL/H/5516–5

FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)


+
5V
HEAT FINS
LM35
OUT
−
200
1%
TWISTED PAIR
V_{OUT} = 10 mV/°C ($T_{AMBIENT}$ +1°C)
FROM +2°C TO +40°C
6.8k
5%
OR 10k RHEOSTAT
FOR GAIN ADJUST
200
1%

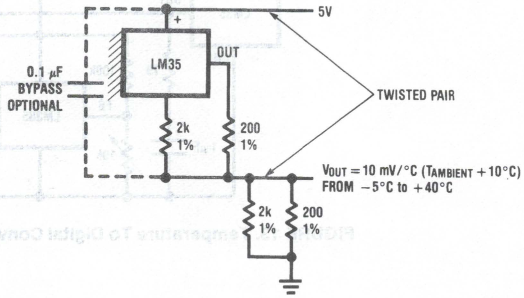
TL/H/5516–6

FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)


+V_S
LM35
+
V_{OUT}
−
1N914
18k
10%

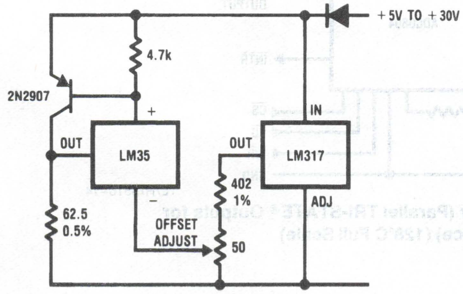
TL/H/5516–7

FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C


5V
+
LM35
OUT
0.1 μF
BYPASS
OPTIONAL
2k
1%
200
1%
TWISTED PAIR
V_{OUT} = 10 mV/°C ($T_{AMBIENT}$ +10°C)
FROM −5°C to +40°C
2k
1%
200
1%

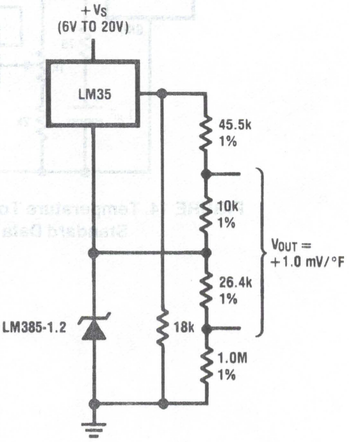
TL/H/5516–8

FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)


+5V TO +30V
4.7k
2N2907
+
IN
OUT
LM35
OUT
LM317
−
402
1%
ADJ
62.5
0.5%
OFFSET
ADJUST
50

TL/H/5516–9

FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)


+V_S
(6V TO 20V)
LM35
45.5k
1%
10k
1%
V_{OUT} =
+1.0 mV/°F
26.4k
1%
LM385-1.2
18k
1.0M
1%

TL/H/5516–10

FIGURE 10. Fahrenheit Thermometer

Typical Applications (Continued)

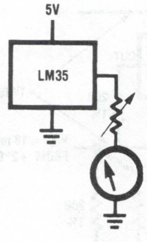

5V
LM35
TL/H/5516-11

FIGURE 11. Centigrade Thermometer (Analog Meter)

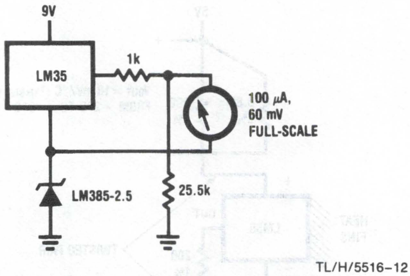

9V
LM35
1k
100 μA,
60 mV
FULL-SCALE
LM385-2.5
25.5k
TL/H/5516-12

FIGURE 12. Expanded Scale Thermometer (50° to 80° Fahrenheit, for Example Shown)

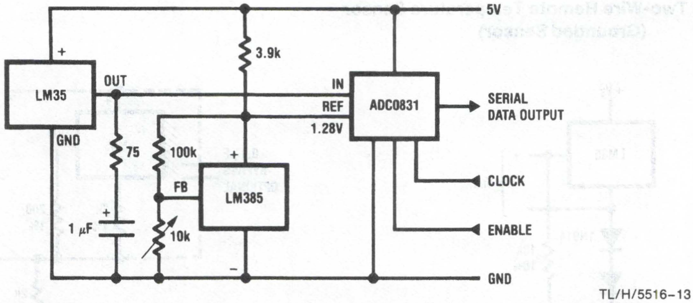

5V
+
LM35
OUT
GND
3.9k
75
100k
1 μF
+
FB
LM385
+
−
10k
IN
REF
1.28V
ADC0831
SERIAL
DATA OUTPUT
CLOCK
ENABLE
GND
TL/H/5516-13

FIGURE 13. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

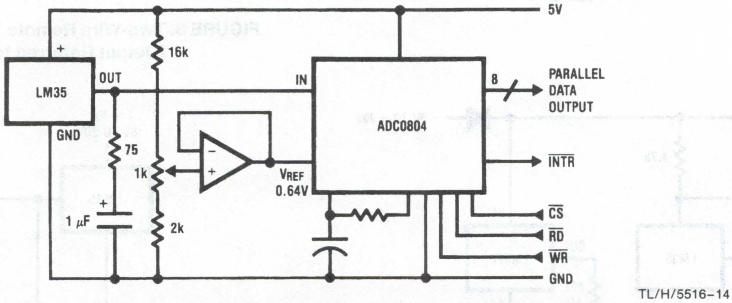
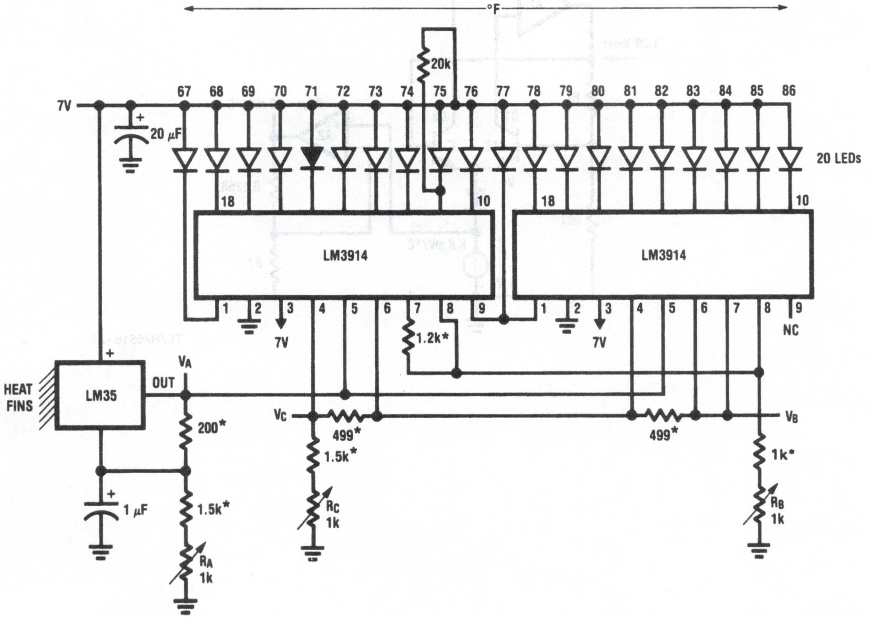

5V
+
LM35
OUT
GND
16k
75
1k
1 μF
+
2k
−
+
IN
V_{REF}
0.64V
ADC0804
8
PARALLEL
DATA
OUTPUT
INTR
CS
RD
WR
GND
TL/H/5516-14

FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE® Outputs for Standard Data Bus to μP Interface) (128°C Full Scale)

Typical Applications (Continued)


°F
20k
67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86
7V
+
20 µF
20 LEDs
18
10
LM3914
18
10
LM3914
1 2 3 4 5 6 7 8 9
7V
1.2k*
1 2 3 4 5 6 7 8 9
7V
NC
+
V_A
HEAT FINS
LM35
OUT
200*
+
1 µF
1.5k*
R_A 1k
V_C
499*
1.5k*
R_C 1k
499*
V_B
1k*
R_B 1k

TL/H/5516-16

* = 1% or 2% film resistor

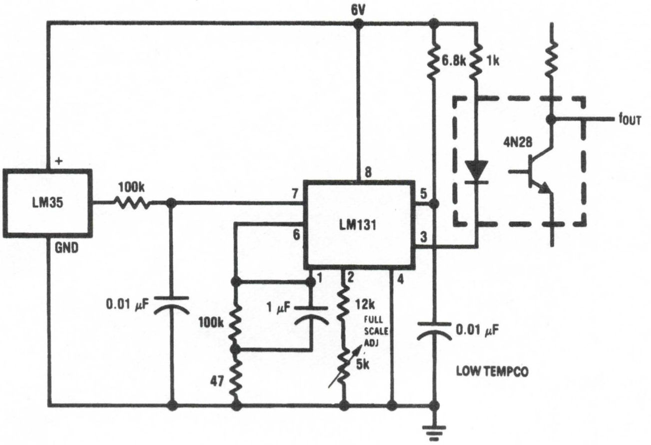
-Trim R_B for $V_B = 3.075V$

-Trim R_C for $V_C = 1.955V$

-Trim R_A for $V_A = 0.075V + 100mV/°C \times T_{ambient}$

-Example, $V_A = 2.275V$ at 22°C

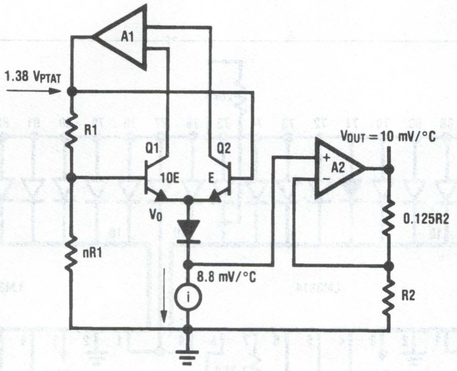
FIGURE 15. Bar-Graph Temperature Display (Dot Mode)


6V
6.8k
1k
f_{OUT}
4N28
+
LM35
GND
100k
7
8
LM131
5
6
3
1
2
4
0.01 µF
100k
1 µF
12k
FULL SCALE ADJ
5k
47
0.01 µF
LOW TEMPCO

TL/H/5516-15

FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to + 150°C; 20 Hz to 1500 Hz)

Block Diagram


A1
1.38 V_{PTAT}
R1
Q1
Q2
10E
E
V_O
nR1
8.8 mV/°C
i
V_{OUT} = 10 mV/°C
+
A2
−
0.125R2
R2

TL/H/5516–21

National Semiconductor Corporation

LM135/LM235/LM335, LM135A/LM235A/LM335A Precision Temperature Sensors

General Description

The LM135 series are precision, easily-calibrated, integrated circuit temperature sensors. Operating as a 2-terminal zener, the LM135 has a breakdown voltage directly proportional to absolute temperature at +10 mV/°K. With less than 1Ω dynamic impedance the device operates over a current range of 400 μA to 5 mA with virtually no change in performance. When calibrated at 25°C the LM135 has typically less than 1°C error over a 100°C temperature range. Unlike other sensors the LM135 has a linear output.

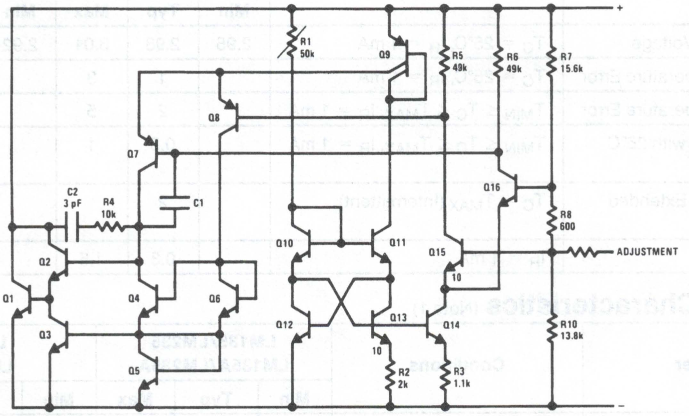
Applications for the LM135 include almost any type of temperature sensing over a −55°C to +150°C temperature range. The low impedance and linear output make interfacing to readout or control circuitry especially easy.

The LM135 operates over a −55°C to +150°C temperature range while the LM235 operates over a −40°C to +125°C temperature range. The LM335 operates from −40°C to +100°C. The LM135/LM235/LM335 are available packaged in hermetic TO-46 transistor packages while the LM335 is also available in plastic TO-92 packages.

Features

- Directly calibrated in °Kelvin
- 1°C initial accuracy available
- Operates from 400 μA to 5 mA
- Less than 1Ω dynamic impedance
- Easily calibrated
- Wide operating temperature range
- 200°C overrange
- Low cost

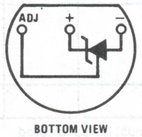
Schematic Diagram



TL/H/5698–1

Connection Diagrams

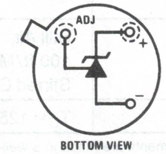
TO-92
Plastic Package



BOTTOM VIEW

Order Number LM335Z or LM335AZ
See NS Package Number Z03A

TO-46
Metal Can Package*



BOTTOM VIEW

TL/H/5698–8

*Case is connected to negative pin

Order Number LM135H, LM235H,
LM335H, LM135AH, LM235AH or LM335AH
See NS Package Number H03H

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Reverse Current	15 mA
Forward Current	10 mA
Storage Temperature	
TO-46 Package	−60°C to +180°C
TO-92 Package	−60°C to +150°C

Specified Operating Temp. Range

	Continuous	Intermittent (Note 2)
LM135, LM135A	−55°C to +150°C	150°C to 200°C
LM235, LM235A	−40°C to +125°C	125°C to 150°C
LM335, LM335A	−40°C to +100°C	100°C to 125°C

Lead Temp. (Soldering, 10 seconds)

TO-92 Package:	260°C
TO-46 Package:	300°C

Temperature Accuracy LM135/LM235, LM135A/LM235A (Note 1)

Parameter	Conditions	LM135A/LM235A			LM135/LM235			Units
		Min	Typ	Max	Min	Typ	Max	
Operating Output Voltage	$T_C = 25°C, I_R = 1$ mA	2.97	2.98	2.99	2.95	2.98	3.01	V
Uncalibrated Temperature Error	$T_C = 25°C, I_R = 1$ mA		0.5	1		1	3	°C
Uncalibrated Temperature Error	$T_{MIN} \le T_C \le T_{MAX}, I_R = 1$ mA		1.3	2.7		2	5	°C
Temperature Error with 25°C Calibration	$T_{MIN} \le T_C \le T_{MAX}, I_R = 1$ mA		0.3	1		0.5	1.5	°C
Calibrated Error at Extended Temperatures	$T_C = T_{MAX}$ (Intermittent)		2			2		°C
Non-Linearity	$I_R = 1$ mA		0.3	0.5		0.3	1	°C

Temperature Accuracy LM335, LM335A (Note 1)

Parameter	Conditions	LM335A			LM335			Units
		Min	Typ	Max	Min	Typ	Max	
Operating Output Voltage	$T_C = 25°C, I_R = 1$ mA	2.95	2.98	3.01	2.92	2.98	3.04	V
Uncalibrated Temperature Error	$T_C = 25°C, I_R = 1$ mA		1	3		2	6	°C
Uncalibrated Temperature Error	$T_{MIN} \le T_C \le T_{MAX}, I_R = 1$ mA		2	5		4	9	°C
Temperature Error with 25°C Calibration	$T_{MIN} \le T_C \le T_{MAX}, I_R = 1$ mA		0.5	1		1	2	°C
Calibrated Error at Extended Temperatures	$T_C = T_{MAX}$ (Intermittent)		2			2		°C
Non-Linearity	$I_R = 1$ mA		0.3	1.5		0.3	1.5	°C

Electrical Characteristics (Note 1)

Parameter	Conditions	LM135/LM235 LM135A/LM235A			LM335 LM335A			Units
		Min	Typ	Max	Min	Typ	Max	
Operating Output Voltage Change with Current	$400\ \mu A \le I_R \le 5$ mA At Constant Temperature		2.5	10		3	14	mV
Dynamic Impedance	$I_R = 1$ mA		0.5			0.6		Ω
Output Voltage Temperature Coefficient			+10			+10		mV/°C
Time Constant	Still Air 100 ft/Min Air Stirred Oil		80 10 1			80 10 1		sec sec sec
Time Stability	$T_C = 125°C$		0.2			0.2		°C/khr

Note 1: Accuracy measurements are made in a well-stirred oil bath. For other conditions, self heating must be considered.

Note 2: Continuous operation at these temperatures for 10,000 hours for H package and 5,000 hours for Z package may decrease life expectancy of the device.

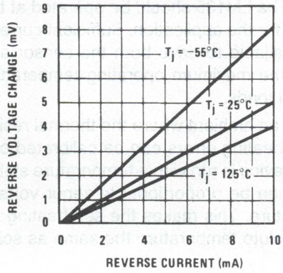
Note 3: Thermal Resistance

	TO-92	TO-46
θ_{JA} (junction to ambient)	202°C/W	400°C/W
θ_{JC} (junction to case)	170°C/W	N/A

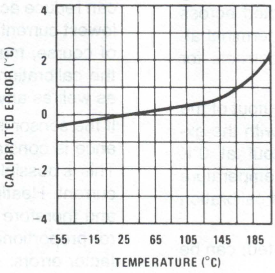
Note 4: Refer to RETS135H for military specifications.

Typical Performance Characteristics

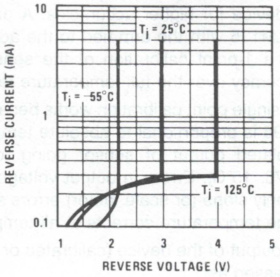
Reverse Voltage Change



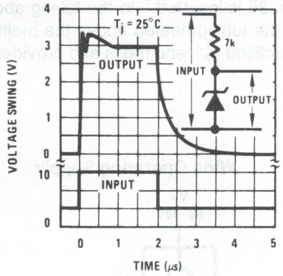
Calibrated Error



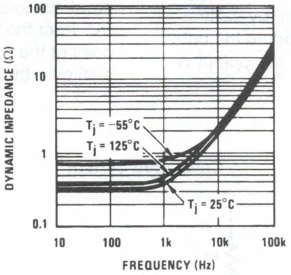
Reverse Characteristics



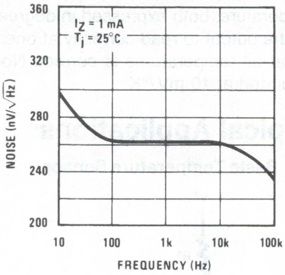
Response Time



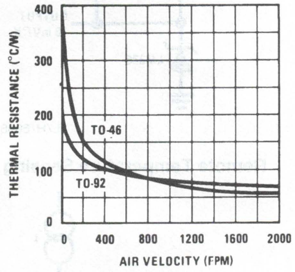
Dynamic Impedance



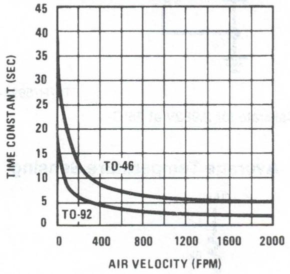
Noise Voltage



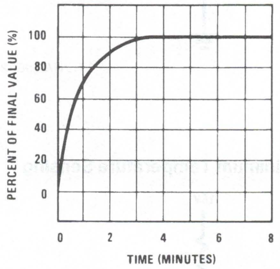
Thermal Resistance Junction to Air



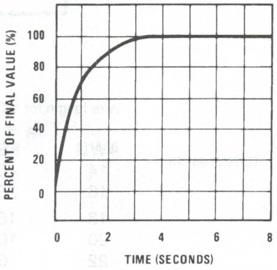
Thermal Time Constant



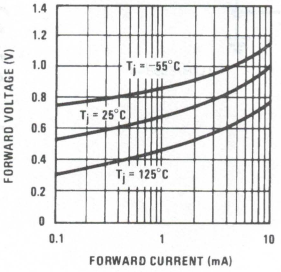
Thermal Response in Still Air



Thermal Response in Stirred Oil Bath



Forward Characteristics



TL/H/5698–3

Application Hints

CALIBRATING THE LM135

Included on the LM135 chip is an easy method of calibrating the device for higher accuracies. A pot connected across the LM135 with the arm tied to the adjustment terminal allows a 1-point calibration of the sensor that corrects for inaccuracy over the full temperature range.

This single point calibration works because the output of the LM135 is proportional to absolute temperature with the extrapolated output of sensor going to 0V output at 0°K (−273. 15°C). Errors in output voltage versus temperature are only slope (or scale factor) errors so a slope calibration at one temperature corrects at all temperatures.

The output of the device (calibrated or uncalibrated) can be expressed as:

$$V_{OUT_T} = V_{OUT_{T_o}} \times \frac{T}{T_o}$$

where T is the unknown temperature and T_o is a reference temperature, both expressed in degrees Kelvin. By calibrating the output to read correctly at one temperature the output at all temperatures is correct. Nominally the output is calibrated at 10 mV/°K.

To insure good sensing accuracy several precautions must be taken. Like any temperature sensing device, self heating can reduce accuracy. The LM135 should be operated at the lowest current suitable for the application. Sufficient current, of course, must be available to drive both the sensor and the calibration pot at the maximum operating temperature as well as any external loads.

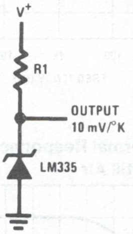
If the sensor is used in an ambient where the thermal resistance is constant, self heating errors can be calibrated out. This is possible if the device is run with a temperature stable current. Heating will then be proportional to zener voltage and therefore temperature. This makes the self heating error proportional to absolute temperature the same as scale factor errors.

WATERPROOFING SENSORS

Meltable inner core heat shrinkable tubing such as manufactured by Raychem can be used to make low-cost waterproof sensors. The LM335 is inserted into the tubing about ½″ from the end and the tubing heated above the melting point of the core. The unfilled ½″ end melts and provides a seal over the device.

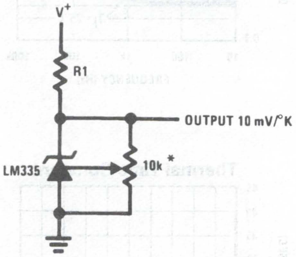
Typical Applications

Basic Temperature Sensor



TL/H/5698-2

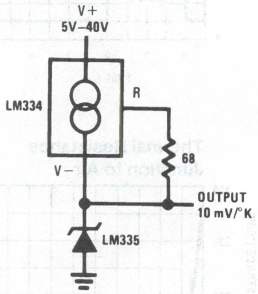
Calibrated Sensor



TL/H/5698-9

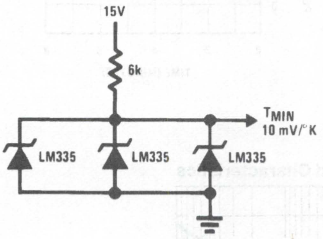
*Calibrate for 2.982V at 25°C

Wide Operating Supply



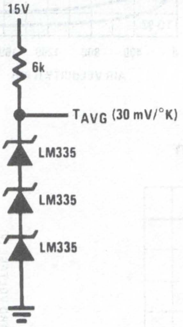
TL/H/5698-10

Minimum Temperature Sensing



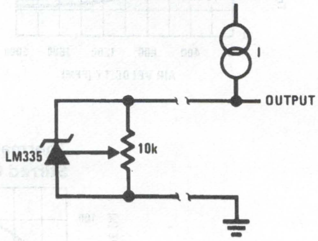
TL/H/5698-4

Average Temperature Sensing



TL/H/5698-18

Remote Temperature Sensing



TL/H/5698-19

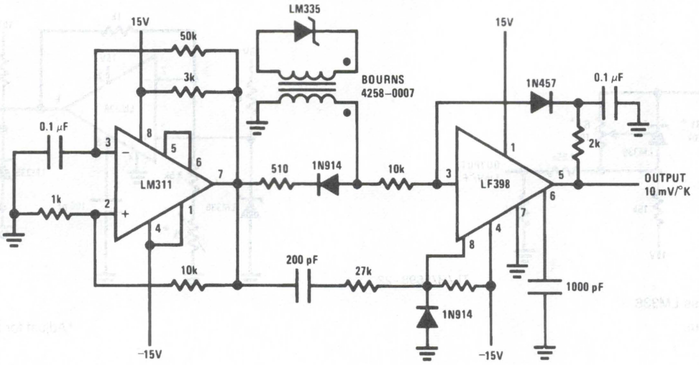
Wire length for 1°C error due to wire drop

AWG	I_R = 1 mA FEET	I_R = 0.5 mA* FEET
14	4000	8000
16	2500	5000
18	1600	3200
20	1000	2000
22	625	1250
24	400	800

*For I_R = 0.5 mA, the trim pot must be deleted.

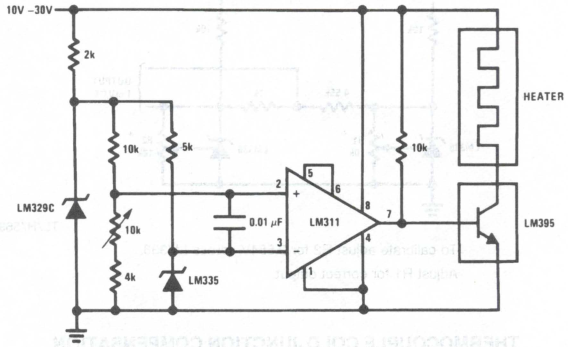
Typical Applications (Continued)

Isolated Temperature Sensor


LM335
15V
50k
3k
BOURNS
4258-0007
0.1 µF
1k
LM311
510
1N914
10k
200 pF
27k
1N914
−15V
15V
1N457
0.1 µF
2k
LF398
OUTPUT
10 mV/°K
1000 pF
−15V

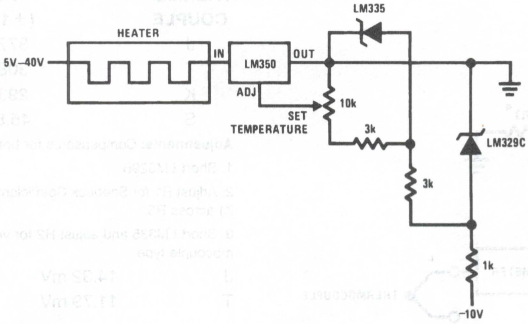
TL/H/5698-20

Simple Temperature Controller


10V −30V
2k
10k
5k
LM329C
10k
4k
LM335
0.01 µF
LM311
10k
HEATER
LM395

TL/H/5698-5

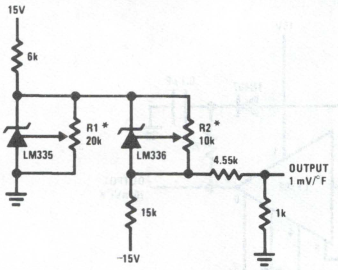
Simple Temperature Control


HEATER
5V–40V
IN
LM350
OUT
ADJ
LM335
10k
SET
TEMPERATURE
3k
LM329C
3k
1k
−10V

TL/H/5698-21

Typical Applications (Continued)

Ground Referred Fahrenheit Thermometer

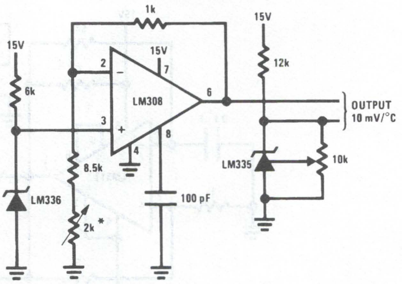

15V
6k
R1 *
20k
LM335
R2 *
10k
LM336
4.55k
OUTPUT
1 mV/°F
1k
15k
−15V

TL/H/5698–22

*Adjust R2 for 2.554V across LM336.

Adjust R1 for correct output.

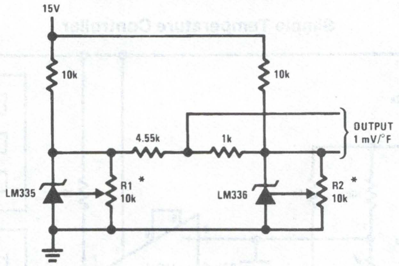
Centigrade Thermometer


1k
15V
15V
2
−
7
LM308
6
3
+
8
4
6k
8.5k
LM336
2k *
100 pF
12k
OUTPUT
10 mV/°C
LM335
10k

TL/H/5698–23

*Adjust for 2.7315V at output of LM308

Fahrenheit Thermometer


15V
10k
10k
OUTPUT
1 mV/°F
4.55k
1k
LM335
R1 *
10k
LM336
R2 *
10k

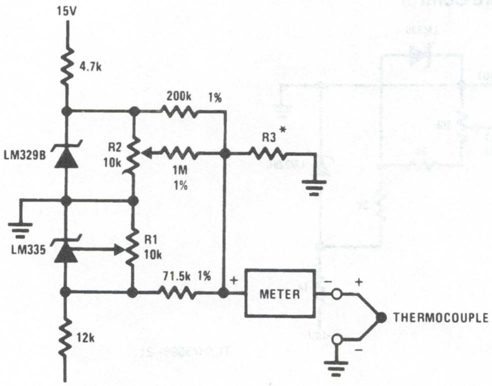
TL/H/5698–24

*To calibrate adjust R2 for 2.554V across LM336.

Adjust R1 for correct output.

THERMOCOUPLE COLD JUNCTION COMPENSATION

Compensation for Grounded Thermocouple


15V
4.7k
200k 1%
LM329B
R2
10k
1M
1%
R3 *
LM335
R1
10k
71.5k 1%
+
METER
−
+
THERMOCOUPLE
−
12k
−15V

TL/H/5698–6

*Select R3 for proper thermocouple type

THERMO-COUPLE	R3 (±1%)	SEEBECK COEFFICIENT
J	377Ω	52.3 μV/°C
T	308Ω	42.8 μV/°C
K	293Ω	40.8 μV/°C
S	45.8Ω	6.4 μV/°C

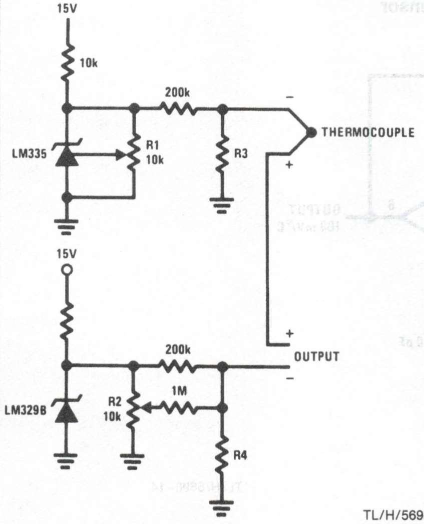
Adjustments: Compensates for both sensor and resistor tolerances

1. Short LM329B
2. Adjust R1 for Seebeck Coefficient times ambient temperature (in degrees K) across R3.
3. Short LM335 and adjust R2 for voltage across R3 corresponding to thermocouple type

J	14.32 mV	K	11.17 mV
T	11.79 mV	S	1.768 mV

Typical Applications (Continued)

Single Power Supply Cold Junction Compensation


15V
10k
200k
LM335
R1
10k
R3
THERMOCOUPLE
−
+
15V
200k
1M
LM329B
R2
10k
R4
+
OUTPUT
−

*Select R3 and R4 for thermocouple type

THERMO-COUPLE	R3	R4	SEEBECK COEFFICIENT
J	1.05K	385Ω	52.3 μV/°C
T	856Ω	315Ω	42.8 μV/°C
K	816Ω	300Ω	40.8 μV/°C
S	128Ω	46.3Ω	6.4 μV/°C

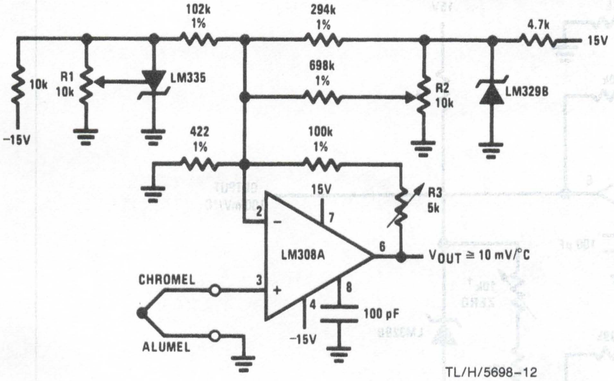
Adjustments:

1. Adjust R1 for the voltage across R3 equal to the Seebeck Coefficient times ambient temperature in degrees Kelvin.
2. Adjust R2 for voltage across R4 corresponding to thermocouple

J	14.32 mV
T	11.79 mV
K	11.17 mV
S	1.768 mV

TL/H/5698–11

Centigrade Calibrated Thermocouple Thermometer


102k
1%
294k
1%
4.7k
15V
10k
R1
10k
LM335
698k
1%
R2
10k
LM329B
−15V
422
1%
100k
1%
15V
R3
5k
2
7
6
LM308A
V_OUT ≅ 10 mV/°C
CHROMEL
3
8
4
100 pF
ALUMEL
−15V

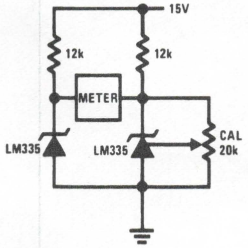
Terminate thermocouple reference junction in close proximity to LM335.

Adjustments:

1. Apply signal in place of thermocouple and adjust R3 for a gain of 245.7.
2. Short non-inverting input of LM308A and output of LM329B to ground.
3. Adjust R1 so that V_{OUT} = 2.982V @ 25°C.
4. Remove short across LM329B and adjust R2 so that V_{OUT} = 246 mV @ 25°C.
5. Remove short across thermocouple.

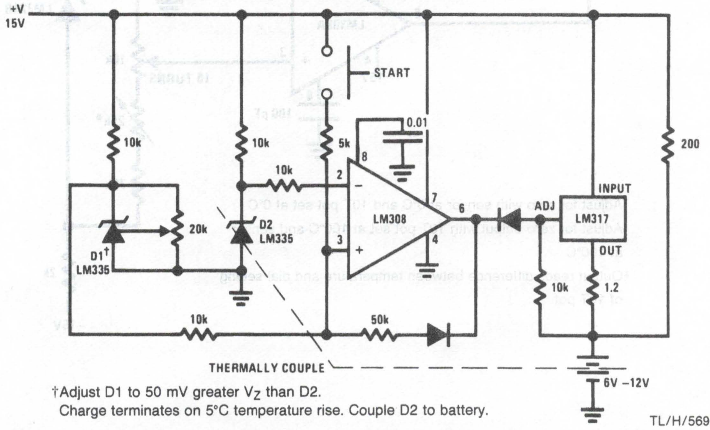
TL/H/5698–12

Differential Temperature Sensor


15V
12k
12k
METER
LM335
LM335
CAL
20k

TL/H/5698–7

Fast Charger for Nickel-Cadmium Batteries

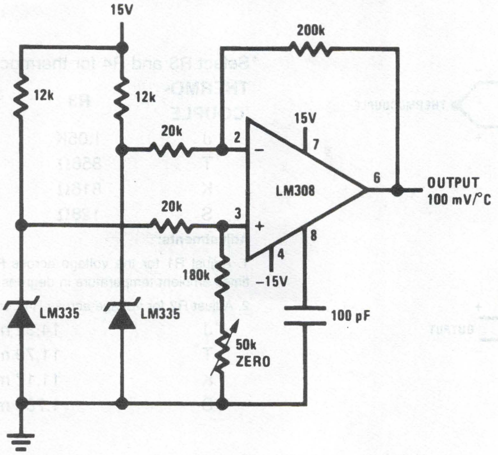

+V
15V
START
0.01
10k
10k
5k
8
10k
2
20k
D1†
LM335
D2
LM335
LM308
7
6
3
4
ADJ
INPUT
LM317
OUT
200
10k
1.2
10k
50k
THERMALLY COUPLE
6V −12V

†Adjust D1 to 50 mV greater V_Z than D2.
Charge terminates on 5°C temperature rise. Couple D2 to battery.

TL/H/5698–13

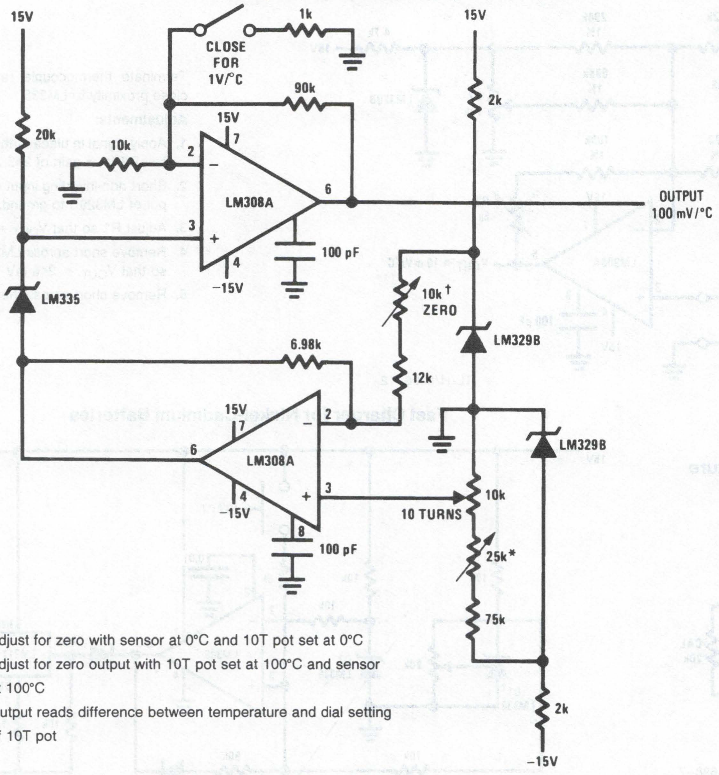
Typical Applications (Continued)

Differential Temperature Sensor


15V
200k
12k
12k
15V
20k
2
7
−
6
OUTPUT
100 mV/°C
LM308
20k
3
+
8
4
180k
−15V
100 pF
LM335
LM335
50k
ZERO

TL/H/5698-14

Variable Offset Thermometer‡


15V
CLOSE
FOR
1V/°C
1k
15V
90k
2k
15V
7
20k
10k
2
−
LM308A
6
OUTPUT
100 mV/°C
3
+
100 pF
4
−15V
10k†
ZERO
LM335
LM329B
6.98k
12k
15V
7
2
−
6
LM308A
LM329B
4
+
3
10k
−15V
10 TURNS
8
100 pF
25k*
75k
2k
−15V

†Adjust for zero with sensor at 0°C and 10T pot set at 0°C

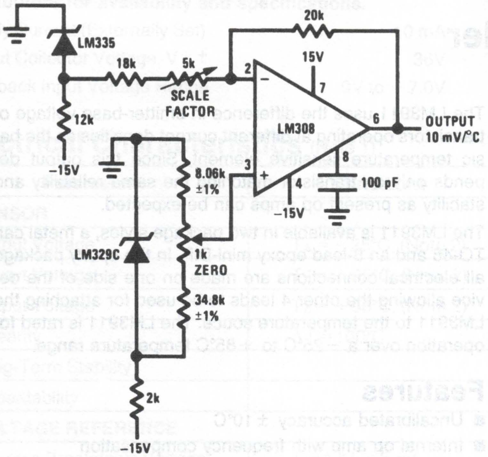
*Adjust for zero output with 10T pot set at 100°C and sensor at 100°C

‡Output reads difference between temperature and dial setting of 10T pot

TL/H/5698-15

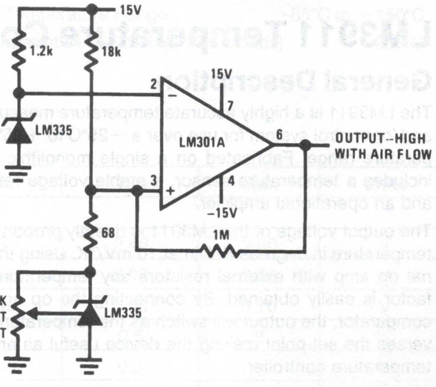
Typical Applications (Continued)

Ground Referred Centigrade Thermometer


LM335
18k
5k
SCALE
FACTOR
20k
15V
2
7
6
3
8
4
LM308
OUTPUT
10 mV/°C
12k
−15V
8.06k
±1%
100 pF
−15V
LM329C
1k
ZERO
34.8k
±1%
2k
−15V

TL/H/5698–16

Air Flow Detector*


15V
1.2k
18k
15V
2
7
6
3
4
LM335
LM301A
OUTPUT–HIGH
WITH AIR FLOW
−15V
68
1M
50K
TRIP POINT
ADJUST
LM335

TL/H/5698–17

*Self heating is used to detect air flow

Definition of Terms

Operating Output Voltage: The voltage appearing across the positive and negative terminals of the device at specified conditions of operating temperature and current.

Uncalibrated Temperature Error: The error between the operating output voltage at 10 mV/°K and case temperature at specified conditions of current and case temperature.

Calibrated Temperature Error: The error between operating output voltage and case temperature at 10 mV/°K over a temperature range at a specified operating current with the 25°C error adjusted to zero.

Typical Performance Characteristics

Temperature Conversion

$T_{CENTIGRADE} = T_C$

$T_{FAHRENHEIT} = T_F$

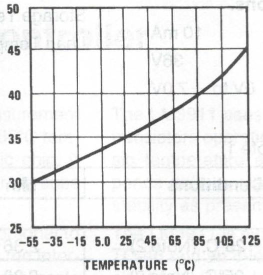
$T_{KELVIN} = T_K$

$T_K = T_C + 273.16$

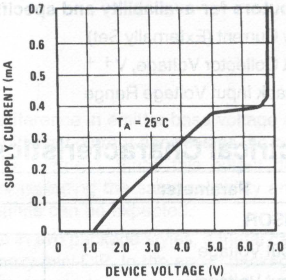
$$T_C = (40 + T_F)\ \frac{5}{9} - 40$$

$$T_F = (40 + T_C)\ \frac{9}{5} - 40$$

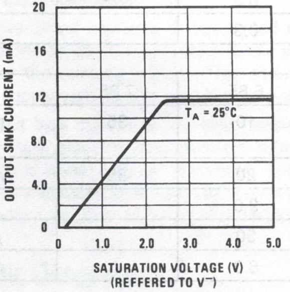
Op Amp Input Current



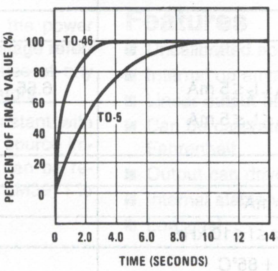
Power Supply Current



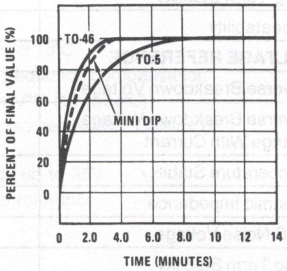
Output Saturation Voltage



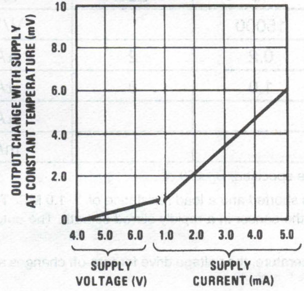
Thermal Time Constant in Stirred Oil Bath



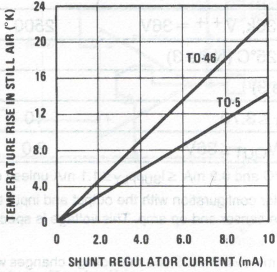
Thermal Time Constant in Still Air



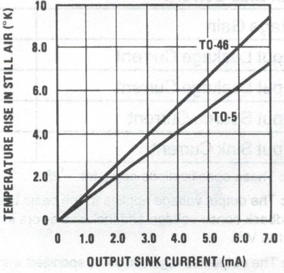
Supply Sensitivity



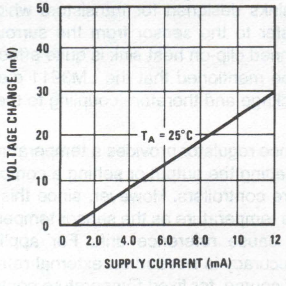
Device Temperature Rise



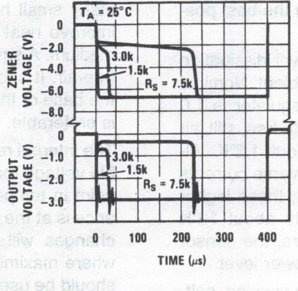
Device Temperature Rise



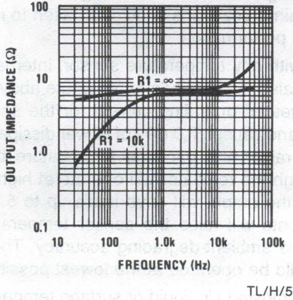
Reference Regulation



Turn "ON" Response

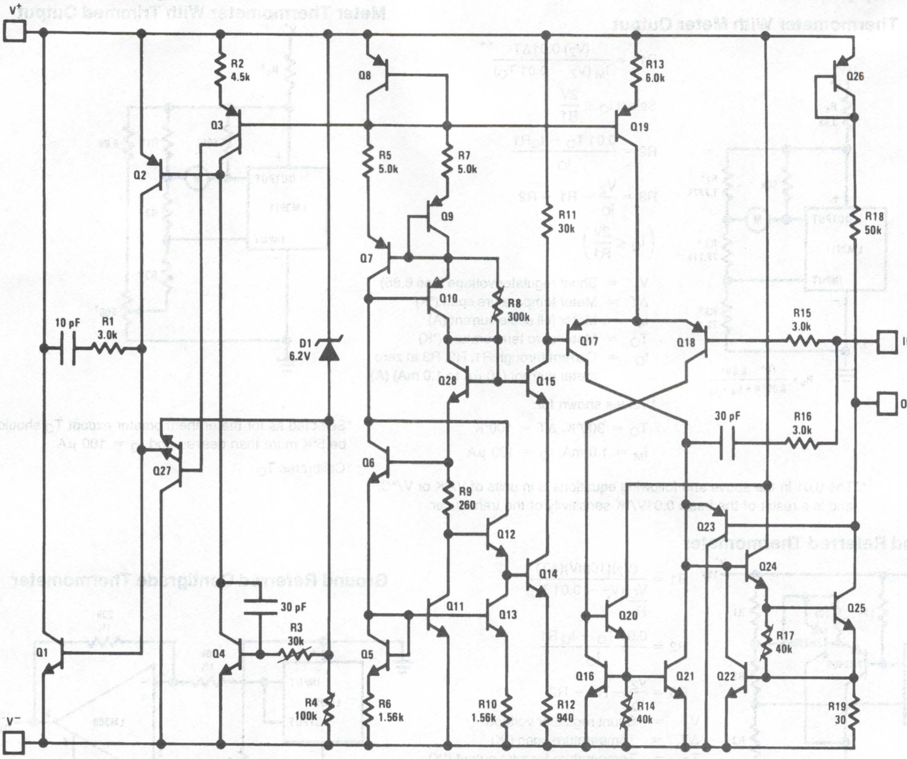


Amplifier Output Impedance



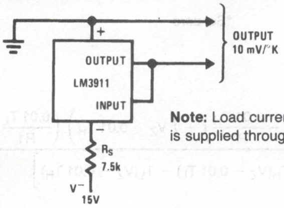
TL/H/5701–2

Schematic Diagram


V+
R2
4.5k
Q8
R13
6.0k
Q26
Q3
Q19
Q2
R5
5.0k
R7
5.0k
Q9
R11
30k
R18
50k
Q7
Q10
R8
300k
10 pF
R1
3.0k
D1
6.2V
Q17
Q18
R15
3.0k
INPUT
Q28
Q15
OUTPUT
30 pF
R16
3.0k
Q27
Q6
R9
260
Q23
Q12
Q24
Q14
30 pF
R3
30k
Q11
Q13
Q20
Q25
R17
40k
Q1
Q4
Q5
Q16
Q21
Q22
R4
100k
R6
1.56k
R10
1.56k
R12
940
R14
40k
R19
30
V−

Typical Applications (Continued)

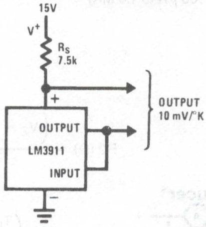
Basic Thermometer for Negative Supply


+
OUTPUT
10 mV/°K
OUTPUT
LM3911
INPUT
−
R_S
7.5k
V−
15V

Note: Load current to GND is supplied through R_S

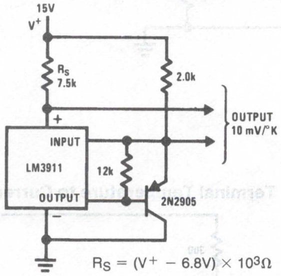
$R_S = (V^- - 6.8V) \times 10^3\Omega$

Basic Thermometer for Positive Supply


15V
V+
R_S
7.5k
+
OUTPUT
10 mV/°K
OUTPUT
LM3911
INPUT
−

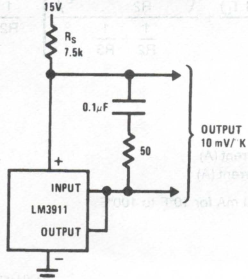
$R_S = (V^- - 6.8V) \times 10^3\Omega$

Increasing Gain and Output Drive

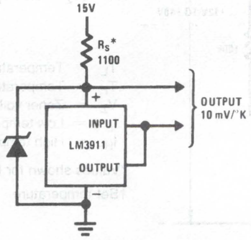

15V
V+
R_S
7.5k
2.0k
+
OUTPUT
10 mV/°K
INPUT
LM3911
12k
OUTPUT
2N2905
−

$R_S = (V^+ - 6.8V) \times 10^3\Omega$

External Frequency Compensation for Greater Stability when Driving Capacitive Loads

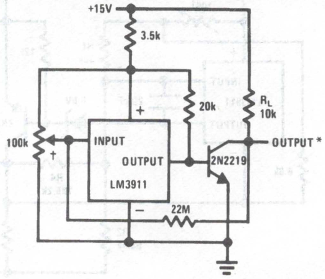

15V
R_S
7.5k
0.1μF
50
OUTPUT
10 mV/°K
+
INPUT
LM3911
OUTPUT
−

Operating With External Zener for Lower Power Dissipation


15V
R_S*
1100
+
OUTPUT
10 mV/°K
INPUT
1N827
LM3911
OUTPUT
−

*Depends on Zener current.

Temperature Controller With Hysteresis


+15V
3.5k
20k
R_L
10k
+
INPUT
100k
†
OUTPUT
LM3911
OUTPUT*
2N2219
−
22M

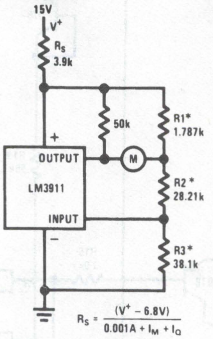
*Output goes positive on temperature increase

†Set temperature

TL/H/5701-3

Typical Applications (Continued)

Thermometer With Meter Output


15V
V+
Rs
3.9k
50k
R1*
1.787k
+
OUTPUT
M
LM3911
R2*
28.21k
INPUT
−
R3*
38.1k

$$R_S = \frac{(V^+ - 6.8V)}{0.001A + I_M + I_Q}$$

$$R1^* = \frac{(V_Z)\,0.01\Delta T}{I_M\,(V_Z - 0.01\,T_O)}\ ^{**}$$

$$\text{Select } I_Q \le \frac{2V}{R1}$$

$$R2 = \frac{0.01\,T_O - I_Q R1}{I_Q}$$

$$R3 = \frac{V_Z}{I_Q} - R1 - R2$$

$$\left(I_Q \le \frac{2V}{R1}\right)$$

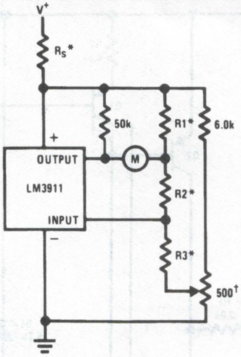
V_Z = Shunt regulator voltage (use 6.85)
ΔT = Meter temperature span (°K)
I_M = Meter full scale current (A)
T_O = Meter zero temperature (°K)
I_Q = Current through R1, R2, R3 at zero meter current (10 μA to 1.0 mA) (A)

*Values shown for:

T_O = 300°K, ΔT = 100°K,
I_M = 1.0 mA, I_Q = 100 μA

**The 0.01 in the above and following equations is in units of V/°K or V/°C, and is a result of the basic 0.01V/°K sensitivity of the transducer

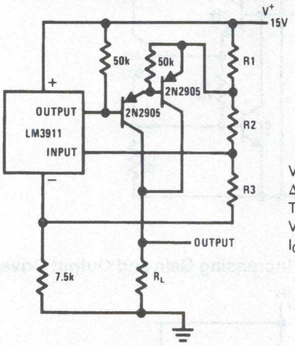
Meter Thermometer With Trimmed Output


V+
Rs*
50k
R1*
6.0k
+
OUTPUT
M
LM3911
R2*
INPUT
−
R3*
500†

*Selected as for meter thermometer except T_O should be 5°K more than desired and I_Q = 100 μA

†Calibrates T_O

Ground Referred Thermometer


V+
15V
50k
50k
2N2905
2N2905
R1
R2
R3
+
OUTPUT
LM3911
INPUT
−
OUTPUT
7.5k
RL

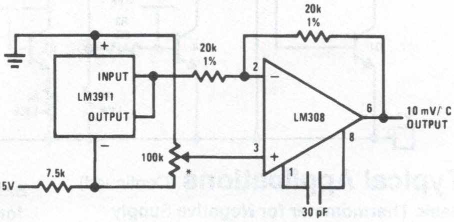
$$R1 = \frac{(V_Z)(10mV)(\Delta T)}{\frac{V_O}{R_L}(V_Z - 0.01\,T_O)}$$

$$R2 = \frac{0.01\,T_O - I_Q\,R1}{I_Q}$$

$$R3 = \frac{V_Z}{I_Q} - R1 - R2$$

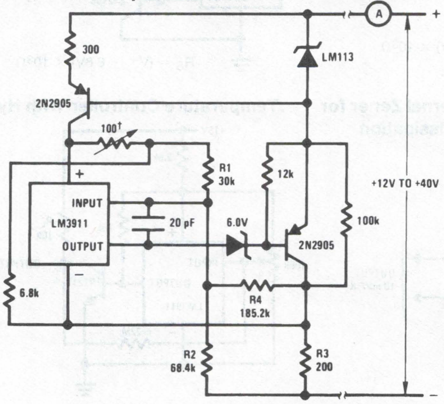
V_Z = Shunt regulator voltage
ΔT = Temperature span (°K)
T_O = Temperature for zero output (°K)
V_O = Full scale output voltage ≤ 10V
I_Q = Current through R1, R2, R3 at zero output voltage (typically 100 μA to 1.0 mA)

Ground Referred Centigrade Thermometer


20k
1%
20k
1%
+
INPUT
LM3911
OUTPUT
−
2
3
6
8
1
LM308
10 mV/°C
OUTPUT
100k
*
−15V
7.5k
30 pF

*Set zero

Two Terminal Temperature to Current Transducer*


A
+
−
300
LM113
2N2905
100†
R1
30k
12k
+12V TO +40V
+
INPUT
LM3911
OUTPUT
20 pF
6.0V
2N2905
100k
R4
185.2k
6.8k
R2
68.4k
R3
200

$$R2\,(\Omega) = \frac{\left(V_Z - 0.01\,T_L\right)\left(I_H - \frac{0.01\,T_H}{R1}\right) + \left(V_Z - 0.01\,T_H\right)\left(\frac{0.01\,T_L}{R1} - I_L\right)^{**}}{\frac{0.01}{R1\,R3}\left[T_H(V_Z - 0.01\,T_L) - T_L(V_Z - 0.01\,T_H)\right]}$$

$$R3(\Omega) \ge \frac{V_Z\left(\frac{T_H}{T_L} - 1\right)}{I_H - \frac{I_L\,T_H}{T_L}}$$

$$\frac{1}{R4} = \frac{1}{(V_Z - 0.01\,T_L)(R2)}\left[\frac{(R2)(0.01\,T_L)}{R1} + \frac{\left(\frac{V_Z - 0.01\,T_L}{R2} - I_L\right)}{\frac{1}{R2} + \frac{1}{R3}}\right] - \frac{1}{R2}$$

T_L = Temperature for I_L (°K)
T_H = Temperature for I_H (°K)
V_Z = Zener voltage (V)
I_L = Low temperature output current (A)
I_H = High temperature output current (A)

*Values shown for I_{OUT} = 1 mA to 10 mA for 10°F to 100°F

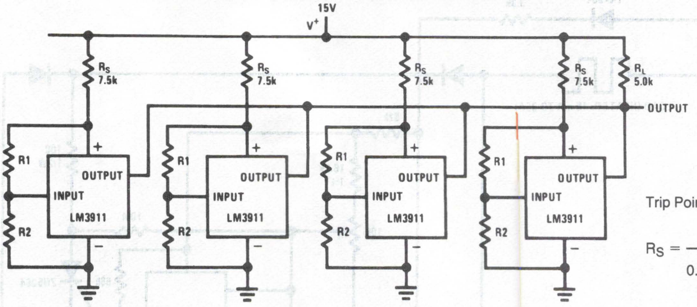
†Set temperature

TL/H/5701–4

**The 0.01 in the above and following equations is in units of V/°K or V/°C, and is a result of the basic 0.01V/°K sensitivity of the transducer

Typical Applications (Continued)

Over Temperature Detectors With Common Output

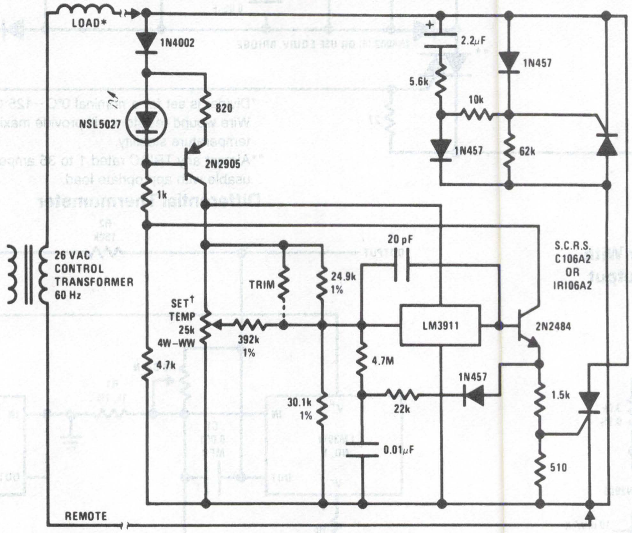

15V
V+
RS
7.5k
RL
5.0k
OUTPUT
R1
R2
+
−
OUTPUT
INPUT
LM3911

$$\text{Trip Point} = V_Z \frac{R1}{R1 + R2}$$

$$R_S = \frac{(V^+ - 6.8V)}{0.001\ A + \dfrac{6.8V}{R1 + R2}}$$

TL/H/5701-5

Two-Wire Remote A.C. Electronic Thermostat (Gas or Oil Furnace Control)


LOAD*
1N4002
820
NSL5027
2N2905
1k
26 VAC
CONTROL
TRANSFORMER
60 Hz
SET†
TEMP
25k
4W-WW
4.7k
TRIM
392k
1%
24.9k
1%
30.1k
1%
20 pF
LM3911
4.7M
22k
0.01µF
1N457
2N2484
1.5k
510
2.2µF
+
5.6k
10k
1N457
1N457
62k
S.C.R.S.
C106A2
OR
IR106A2
REMOTE

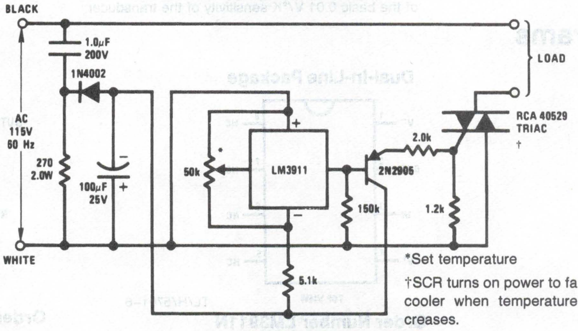
TL/H/5701-8

*Solenoid or 6–15W heater

†Pot will provide about a 50°F to 90°F setting range. The trim resistor (100k) is selected to bring 70°F near the middle of the pot rotation.

SCR heating, by proper positioning, can preheat the sensor giving control anticipation as is presently used in many home thermostats.

Electronic Thermostat


BLACK
1.0µF
200V
1N4002
AC
115V
60 Hz
270
2.0W
100µF
25V
+
−
50k
*
LM3911
+
−
2N2905
150k
2.0k
1.2k
5.1k
RCA 40529
TRIAC
†
LOAD
WHITE

SENSITIVE GATE TRIAC
$I_{GT} = \leq 5$ mA
RCA T2300, 40529
OR SIMILAR

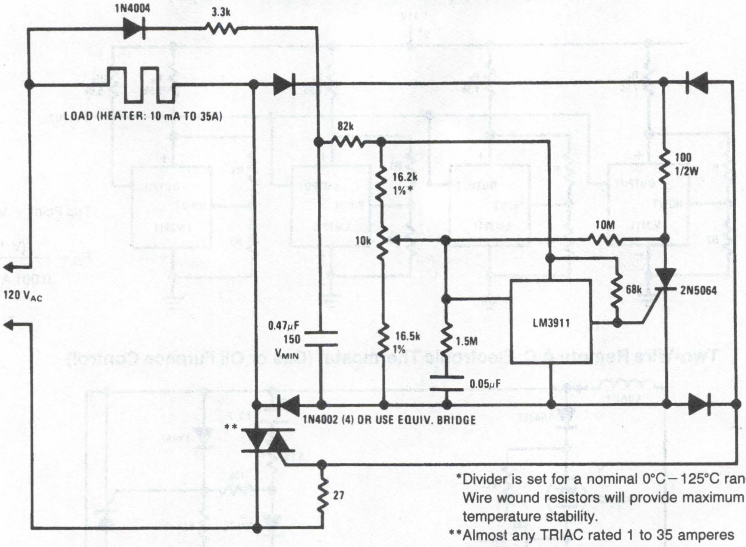
*Set temperature

†SCR turns on power to fan or cooler when temperature increases.

TL/H/5701-9

Typical Applications (Continued)

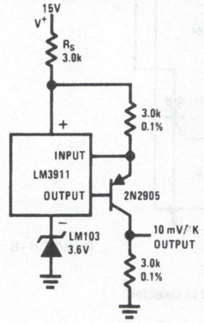
Three-Wire Electronic Thermostat


1N4004
3.3k
LOAD (HEATER: 10 mA TO 35A)
82k
16.2k 1%*
10k
100 1/2W
10M
68k
2N5064
LM3911
0.47μF 150 VMIN
16.5k 1%
1.5M
0.05μF
1N4002 (4) OR USE EQUIV. BRIDGE
**
27
TO 120 VAC

*Divider is set for a nominal 0°C–125°C range. Wire wound resistors will provide maximum temperature stability.

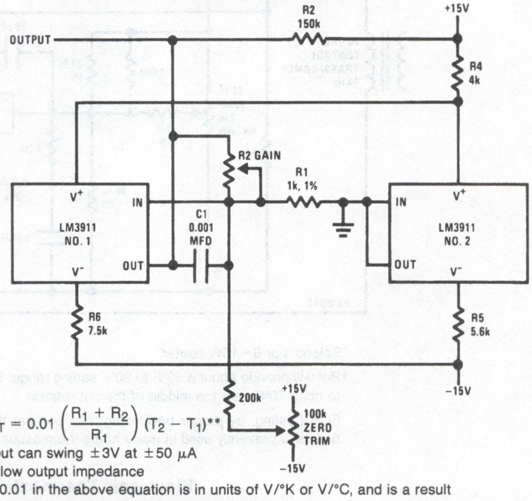
**Almost any TRIAC rated 1 to 35 amperes usable with appropriate load.

Kelvin Thermometer With Ground Referred Output


15V
V+
RS 3.0k
3.0k 0.1%
+
INPUT
LM3911
OUTPUT
2N2905
−
LM103 3.6V
10 mV/°K OUTPUT
3.0k 0.1%

$$R_S = \frac{V_S^+ - 6.8V \times 10^3\Omega}{2}$$

Differential Thermometer


OUTPUT
R2 150k
+15V
R4 4k
R2 GAIN
R1 1k, 1%
V+
IN
LM3911 NO. 1
C1 0.001 MFD
OUT
V−
IN
V+
LM3911 NO. 2
OUT
V−
R6 7.5k
R5 5.6k
−15V
200k
+15V
100k ZERO TRIM
−15V

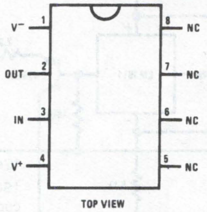
$$V_{OUT} = 0.01\left(\frac{R_1 + R_2}{R_1}\right)(T_2 - T_1)^{**}$$

Output can swing ±3V at ±50 μA with low output impedance

**The 0.01 in the above equation is in units of V/°K or V/°C, and is a result of the basic 0.01 V/°K sensitivity of the transducer

Connection Diagrams

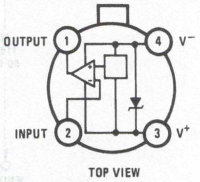
Dual-In-Line Package


V− 1
OUT 2
IN 3
V+ 4
8 NC
7 NC
6 NC
5 NC
TOP VIEW

TL/H/5701-6

Order Number LM3911N
See NS Package N08E

TO-46 Package


OUTPUT 1
INPUT 2
3 V+
4 V−
TOP VIEW

Note: Pin 4 connected to case.

TL/H/5701-7

Order Number LM3911H-46
See NS Package H04A

Section 7

Voltage References

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***Devices Not Covered In Last Publication**

National Semiconductor Corporation

Voltage Reference Selection Guide

Shunt Type

Reverse Breakdown Voltage (V_R)	Device	Operating Temp. Range*	Voltage Tolerance Max, T_A = 25°C	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance (Typ)
				ppm/°C (Max)	Over Range		
1.22	LM113-2	M	±1%	50 (Typ)	−55°C to +125°C	500 μA to 20 mA	0.8
1.22	LM113-1	M	±2%	50 (Typ)	−55°C to +125°C	500 μA to 20 mA	0.8
1.22	LM113	M	±5%	100 (Typ)	−55°C to +125°C	500 μA to 20 mA	0.8
1.22	LM313	C	±5%	100 (Typ)	0°C to +70°C	500 μA to 20 mA	0.8
1.235	LM185BX-1.2	M	±1%	30	−55°C to +125°C	10 μA to 20 mA	1
1.235	LM185BY-1.2	M	±1%	50	−55°C to +125°C	10 μA to 20 mA	1
1.235	LM185-1.2	M	±1%	150	−55°C to +125°C	10 μA to 20 mA	1
1.235	LM285BX-1.2	I	±1%	30	−40°C to +85°C	10 μA to 20 mA	1
1.235	LM285BY-1.2	I	±1%	50	−40°C to +85°C	10 μA to 20 mA	1
1.235	LM285-1.2	I	±1%	150	−40°C to +85°C	10 μA to 20 mA	1
1.235	LM385BX-1.2	C	±1%	30	0°C to +70°C	15 μA to 20 mA	1
1.235	LM385BY-1.2	C	±1%	50	0°C to +70°C	15 μA to 20 mA	1
1.235	LM385B-1.2	C	±1%	150	0°C to +70°C	15 μA to 20 mA	1
1.235	LM385-1.2	C	+2%, −2.4%	150	0°C to +70°C	15 μA to 20 mA	1
1.24 to 5.3 (Adj.)	LM185B	M	±1%	150	−55°C to +125°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM185BX	M	±1%	50	−55°C to +125°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM185BY	M	±1%	50	−55°C to +125°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM285BX	I	±1%	30	−40°C to +85°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM285BY	I	±1%	50	−40°C to +85°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM285	I	±2%	150	−40°C to +85°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM385BX	C	±1%	30	0°C to +70°C	13 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM385BY	C	±1%	50	0°C to +70°C	13 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM385	C	±2%	150	0°C to +70°C	13 μA to 20 mA	0.3
2.49	LM136A	M	±1%	72	−55°C to +125°C	400 μA to 10 mA	0.4
2.49	LM136	M	±2%	72	−55°C to +125°C	400 μA to 10 mA	0.4
2.49	LM236A	I	±1%	72	−25°C to +85°C	400 μA to 10 mA	0.4
2.49	LM236	I	±2%	72	−25°C to +85°C	400 μA to 10 mA	0.4
2.49	LM336	I	±4%	54	0°C to +70°C	400 μA to 10 mA	0.4
2.49	LM336B	C	±2%	54	0°C to +70°C	400 μA to 10 mA	0.4
2.5	LM185BX-2.5	M	±1.5%	30	−55°C to +125°C	20 μA to 20 mA	1
2.5	LM185BY-2.5	M	±1.5%	50	−55°C to +125°C	20 μA to 20 mA	1
2.5	LM185B-2.5	M	±1.5%	150	−55°C to +125°C	20 μA to 20 mA	1
2.5	LM285BX-2.5	I	±1.5%	30	−40°C to +85°C	20 μA to 20 mA	1
2.5	LM285BY-2.5	I	±1.5%	50	−40°C to +85°C	20 μA to 20 mA	1
2.5	LM285-2.5	I	±1.5%	150	−40°C to +85°C	20 μA to 20 mA	1
2.5	LM385BX-2.5	C	±1.5%	30	0°C to +70°C	20 μA to 20 mA	1
2.5	LM385BY-2.5	C	±1.5%	50	0°C to +70°C	20 μA to 20 mA	1
2.5	LM385B-2.5	C	±1.5%	150	0°C to +70°C	20 μA to 20 mA	1
2.5	LM385-2.5	C	±3%	150	0°C to +70°C	20 μA to 20 mA	1

Shunt Type (Continued)

Reverse Breakdown Voltage (V_R)	Device	Operating Temp. Range*	Voltage Tolerance Max, $T_A = 25°C$	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance (Typ)
				ppm/°C (Max)	Over Range		
5.0	LM136A	M	±1%	72	−55°C to +125°C	400 µA to 10 mA	0.8
5.0	LM136	M	±2%	72	−55°C to +125°C	400 µA to 10 mA	0.8
5.0	LM236A	I	±1%	72	−25°C to +85°C	400 µA to 10 mA	0.8
5.0	LM236	I	±2%	72	−25°C to +85°C	400 µA to 10 mA	0.8
5.0	LM336B	C	±2%	54	0°C to +70°C	400 µA to 10 mA	0.8
5.0	LM336	C	±4%	54	0°C to +70°C	400 µA to 10 mA	0.8
6.9	LM129A	M	+3%, −2%	10	−55°C to +125°C	600 µA to 15 mA	0.6
6.9	LM129B	M	+3%, −2%	20	−55°C to +125°C	600 µA to 15 mA	0.6
6.9	LM129C	M	+3%, −2%	50	−55°C to +125°C	600 µA to 15 mA	0.6
6.9	LM329B	C	±5%	50	0°C to +70°C	600 µA to 15 mA	0.8
6.9	LM329C	C	±5%	20	0°C to +70°C	600 µA to 15 mA	0.8
6.9	LM329D	C	±5%	100	0°C to +70°C	600 µA to 15 mA	0.8
6.95	LM199A	M	±2%	0.5	−55°C to +125°C	500 µA to 10 mA	0.5
6.95	LM199A-20	M	Same as LM199A with 20 ppm guaranteed long term drift.				
6.95	LM199	M	±2%	1.0	−55°C to +125°C	500 µA to 10 mA	0.5
6.95	LM299A	I	±2%	0.5	−25°C to +85°C	500 µA to 10 mA	0.5
6.95	LM299A-20	I	Same as LM299A with 20 ppm guaranteed long term drift.				
6.95	LM299	I	±2%	1	−25°C to +85°C	500 µA to 10 mA	0.5
6.95	LM399A	C	±5%	1	0°C to +70°C	500 µA to 10 mA	0.5
6.95	LM399A-50	C	Same as LM399A with 50 ppm guaranteed long term drift.				
6.95	LM399	C	±5%	2	0°C to +70°C	500 µA to 10 mA	0.5
6.95	LM3999	C	±5%	5	0°C to +70°C	600 µA to 10 mA	0.6

*C (Commercial) = 0°C to 70°C, I (Industrial) = −25°C to +85°C for the LM236 and LM299, I = −40°C to +85°C for all others.
M (Military) = −55°C to +125°C

Current References

Output Current Range	Device	Operating Temperature Range	Set Current Error			Operating Voltage Range	Set Current Temperature Dependence*
			2 µA to 10 µA	10 µA to 1 mA	1 mA to 5 mA		
2 µA to 10 mA	LM134	−55°C to +125°C	±8%	±3%	±5%	1V to 40V	0.96T to 0.104T
2 µA to 10 mA	LM134-3	−55°C to +125°C	N/A	±1%	N/A	1V to 40V	0.98T to 0.102T
2 µA to 10 mA	LM134-6	−55°C to +125°C	N/A	±2%	N/A	1V to 40V	0.97T to 0.103T
2 µA to 10 mA	LM234	−25°C to +100°C	±8%	±3%	±5	1V to 40V	0.96T to 0.104T
2 µA to 10 mA	LM234-3	−25°C to +100°C	N/A	±1%	N/A	1V to 40V	0.98T to 0.102T
2 µA to 10 mA	LM234-6	−25°C to +100°C	N/A	±2%	N/A	1V to 40V	0.97T to 0.103T
2 µA to 10 mA	LM334	0°C to +70°C	±12%	±6%	±8%	1V to 40V	0.96T to 0.104T

*Set current changes linearly with temperature at a rate of 0.33%/°C.

Series Type (Buffered Output)

Output Voltage	Device	Oper. Temp. Range*	Voltage Tolerance Max, $T_A = 25°C$	Temperature Drift		Load Reg. ppm/mA	Over Current Range	Quiescent Current (mA)
				ppm/°C (Max)	Over Range			
2.5	LM368Y-2.5	C	±0.2%	20	0°C to +70°C	25	0 mA to +10 mA	0.55
2.5	LM368-2.5	C	±0.2%	30	0°C to +70°C	25	0 mA to +10 mA	0.55
5.0	LM168BY-5.0	M	±0.05%	10	−55°C to +125°C	10	−10 mA to +10 mA	0.35
5.0	LM268BY-5.0	I	±0.05%	15	−40°C to +85°C	10	−10 mA to +10 mA	0.35
5.0	LM368BY-5.0	C	±0.1%	20	0°C to +70°C	10	−10 mA to +10 mA	0.35
5.0	LM368-5.0	C	±0.1%	30	0°C to +70°C	10	−10 mA to +10 mA	0.35
10	LM169B	M	±0.05%	3	−55°C to +125°C	8	−10 mA to +10 mA	1.8
10	LM168BY-10	M	±0.05%	10	−55°C to +125°C	10	−10 mA to +10 mA	0.35
10	LH0070-2	M	±0.05%	8	−40°C to +85°C	60	0 to 5 mA	5
10	LM169	M	±0.05%	5	−55°C to +125°C	8	−10 mA to +10 mA	1.8
10	LM581U	M	±0.05%	10	−55°C to +125°C	50	0 mA to 5 mA	1.8
10	LH0070-0	M	±0.1%	40	−40°C to +85°C	60	0 mA to 5 mA	5
10	LM581T	M	±0.1%	10	−55°C to +125°C	50	0 mA to 5 mA	1.8
10	LH0070-1	M	±0.1%	20	−40°C to +85°C	60	0 mA to 5 mA	5
10	LM581S	M	±0.3%	30	−55°C to +125°C	50	0 mA to 5 mA	1.8
10	LM268BY-10	I	±0.05%	15	−40°C to +85°C	10	−10 mA to +10 mA	0.35
10	LM581L	C	±0.05%	5	0°C to +70°C	50	0 mA to 5 mA	1.8
10	LM369C	C	±0.05%	10	0°C to +70°C	8	−10 mA to +10 mA	1.8
10	LM369	C	±0.05%	5	0°C to +70°C	8	−10 mA to +10 mA	1.8
10	LM369B	C	±0.05%	3	0°C to +70°C	8	−10 mA to +10 mA	1.8
10	LM581K	C	±0.1%	10	0°C to +70°C	50	0 mA to 5 mA	1.8
10	LM368Y-10	C	±0.1%	20	0°C to +70°C	10	−10 mA to +10 mA	0.35
10	LM368-10	C	±0.1%	30	0°C to +70°C	10	−10 mA to +10 mA	0.35
10	LM369D	C	±0.1%	30	0°C to +70°C	8	−10 mA to +10 mA	2
10	LM581J	C	±0.3%	30	0°C to +70°C	50	0 mA to 5 mA	1.8
10.24	LH0071-2	M	±0.05%	8	−40°C to +85°C	60	0 mA to 5 mA	5
10.24	LH0071-1	M	±0.1%	20	−40°C to +85°C	60	0 mA to 5 mA	5
10.24	LH0071-0	M	±0.1%	30	−40°C to +85°C	60	0 mA to 5 mA	5

*C (Commercial) = 0°C to 70°C, I (Industrial) = −40°C to +85°C, M (Military) = −55°C to +125°C

Low Current Reference Diodes

Output Voltage	Device	Operating Temp. Range*	Voltage Tolerance Max, $T_A = 25°C$	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance (Typ)
				ppm/°C (Max)	Over Range		
3.0	LM103-3.0	M	±10%	−1700	−55°C to +125°C	10 µA to 10 mA	25
3.3	LM103-3.3	M	±10%	−1500	−55°C to +125°C	10 µA to 10 mA	25
3.6	LM103-3.6	M	±10%	−1400	−55°C to +125°C	10 µA to 10 mA	25
3.9	LM103-3.9	M	±10%	−1300	−55°C to +125°C	10 µA to 10 mA	25

*M (Military) = −55°C to +125°C

"Reference Grade" Voltage Regulators*

Output Voltage	Device	Operating Temperature Range	Voltage Tolerance Max, $T_A = 25°C$	Output Variation Over Operating Range	Load Reg. ppm/mA	Line Reg. ppm/V	Output Current (Max)	Quiescent Current
Adjustable: 1.235V to 30V	LP2951	−55°C to +150°C	±0.5%	±0.5%	100	42	100 mA	120 μA
	LP2951AC	−40°C to +125°C	±0.5%	±0.5%	100	42	100 mA	120 μA
	LP2951C	−40°C to +125°C	±1%	±1%	200	83	100 mA	120 μA
Programmable: 5V, 6V, 10V, 12V, 15V	LH0075	−55°C to +125°C	±0.5%	±0.14% (Typ)	15	200	200 mA	8 mA
	LH0075C	0°C to +70°C	±1%	±0.3% (Typ)	25	400	200 mA	10 mA
Programmable −5V, −6V, −10V	LH0076	−55°C to +125°C	±0.5%	±0.14% (Typ)	15	200	200 mA	15 mA
−10V, −15V	LH0076C	0°C to +70°C	±1%	±0.3% (Typ)	25	400	200 mA	15 mA
5V	LP2950AC	−40°C to +125°C	±0.5%	±0.5%	100	42	100 mA	120 μA
5V	LP2950C	−40°C to +125°C	±1%	±1%	200	83	100 mA	120 μA

*For more information on these circuits, refer to the Voltage Regulator section of the Databook.

National Semiconductor Corporation

LH0070 Series Precision BCD Buffered Reference
LH0071 Series Precision Binary Buffered Reference

General Description

The LH0070 and LH0071 are precision, three terminal, voltage references consisting of a temperature compensated zener diode driven by a current regulator and a buffer amplifier. The devices provide an accurate reference that is virtually independent of input voltage, load current, temperature and time. The LH0070 has a 10.000V nominal output to provide equal step sizes in BCD applications. The LH0071 has a 10.240V nominal output to provide equal step sizes in binary applications.

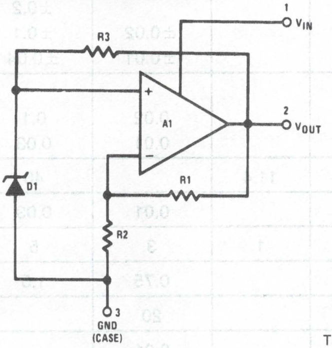
The output voltage is established by trimming ultra-stable, low temperature drift, thin film resistors under actual operating circuit conditions. The devices are shortcircuit proof in both the current sourcing and sinking directions.

The LH0070 and LH0071 series combine excellent long term stability, ease of application, and low cost, making them ideal choices as reference voltages in precision D to A and A to D systems.

Features

- Accuracy output voltage
  - LH0070 10V ± 0.02%
  - LH0071 10.24V ± 0.02%
- Single supply operation 11.4V to 40V
- Low output impedance 0.2Ω
- Excellent line regulation 0.1 mV/V
- Low zener noise 20 μVp-p
- 3-lead TO-5 (pin compatible with the LM109)
- Short circuit proof
- Low standby current 3 mA

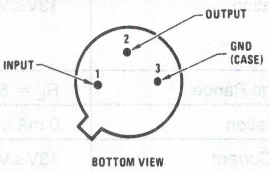
Equivalent Schematic



TL/H/5550-1

Connection Diagram

TO-5 Metal Can Package

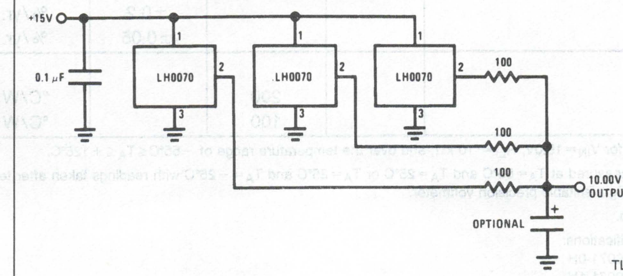


TL/H/5550-7

Order Number LH0070-0H, LH0071-0H, LH0070-1H, LH0071-1H, LH0070-2H or LH0071-2H
See NS Package Number H03B

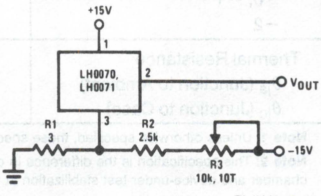
Typical Applications

Statistical Voltage Standard



TL/H/5550-8

***Output Voltage Fine Adjustment**



TL/H/5550-9

***Note:** The output of the LH0070 and LH0071 may be adjusted to a precise voltage by using the above circuit since the supply current of the devices is relatively small and constant with temperature and input voltage. For the circuit shown, supply sensitivities are degraded slightly to 0.01%/V change in V_{OUT} for changes in V_{IN} and V^-.

An additional temperature drift of 0.0001%/°C is added due to the variation of supply current with temperature of the LH0070 and LH0071. Sensitivity to the value of R1, R2 and R3 is less than 0.001%/%.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 4)

Supply Voltage	40V
Power Dissipation (See Curve)	600 mW
Short Circuit Duration	Continuous
Output Current	± 20 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to ±150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage LH0070 LH0071	$T_A = 25°C$		 10.000 10.24		 V V
Output Accuracy −0, −1 −2	$T_A = 25°C$		 ±0.03 ±0.02	 ±0.1 ±0.05	 % %
Output Accuracy −0, −1 −2	$T_A = -55°C, 125°C$			 ±0.3 ±0.2	 % %
Output Voltage Change With Temperature −0 −1 −2	(Note 2)		 ±0.02 ±0.01	 ±0.2 ±0.1 ±0.04	 % % %
Line Regulation −0, −1 −2	$13V \leq V_{IN} \leq 33V, T_C = 25°C$		 0.02 0.01	 0.1 0.03	 % %
Input Voltage Range	$R_L = 50\ k\Omega$	11.4		40	V
Load Regulation	$0\ mA \leq I_{OUT} \leq 5\ mA$		0.01	0.03	%
Quiescent Current	$13V \leq V_{IN} \leq 33V, I_{OUT} = 0\ mA$	1	3	5	mA
Change In Quiescent Current	$\Delta V_{IN} = 20V$ From 23V To 33V		0.75	1.5	mA
Output Noise Voltage	BW = 0.1 Hz To 10 Hz, $T_A = 25°C$		20		µVp-p
Ripple Rejection	f = 120 Hz		0.01		%/Vp-p
Output Resistance			0.2	0.6	Ω
Long Term Stability −0, −1 −2	$T_A = 25°C$ (Note 3)			 ±0.2 ±0.05	 %/yr. %/yr.
Thermal Resistance θ_{ja} (Junction to Ambient) θ_{jc} (Junction to Case)	$T_j = 150°C$		 200 100		 °C/W °C/W

Note 1: Unless otherwise specified, these specifications apply for $V_{IN} = 15.0V$, $R_L = 10\ k\Omega$, and over the temperature range of $-55°C \leq T_A \leq +125°C$.

Note 2: This specification is the difference in output voltage measured at $T_A = 85°C$ and $T_A = 25°C$ or $T_A = 25°C$ and $T_A = -25°C$ with readings taken after test chamber and device-under-test stabilization at temperature using a suitable precision voltmeter.

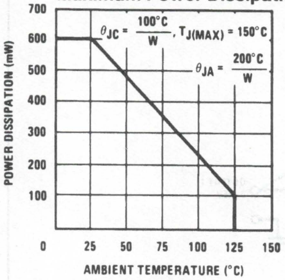
Note 3: This parameter is guaranteed by design and not tested.

Note 4: Refer to the following RETS drawings for military specifications:

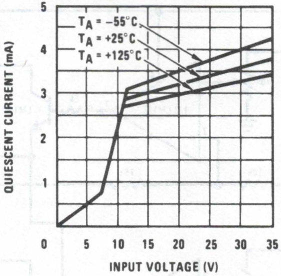
RETS0070-0H for LH0070-0H	RETS0071-0H for LH0071-0H
RETS0070-1H for LH0070-1H	RETS0071-1H for LH0071-1H
RETS0070-2H for LH0070-2H	RETS0071-2H for LH0071-2H

Typical Performance Characteristics

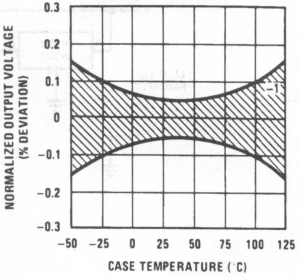
Maximum Power Dissipation



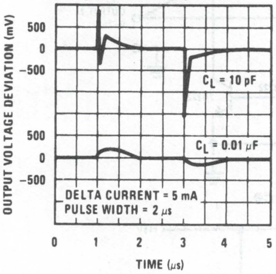
Quiescent Current vs Input Voltage



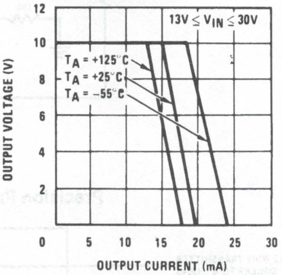
Normalized Output Voltage vs Temperature



Step Load Response

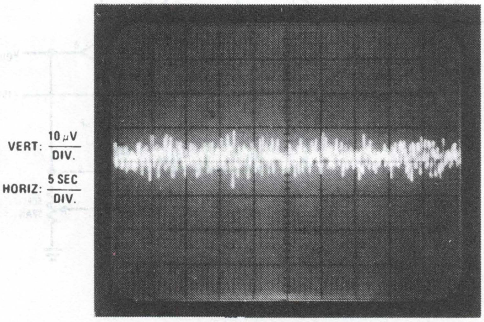


Output Short Circuit Characteristics



TL/H/5550-2

Noise Voltage

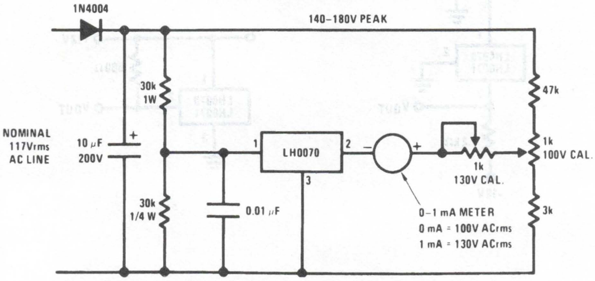


BW = 0.1 Hz TO 10 Hz

TL/H/5550-6

Typical Applications (Continued)

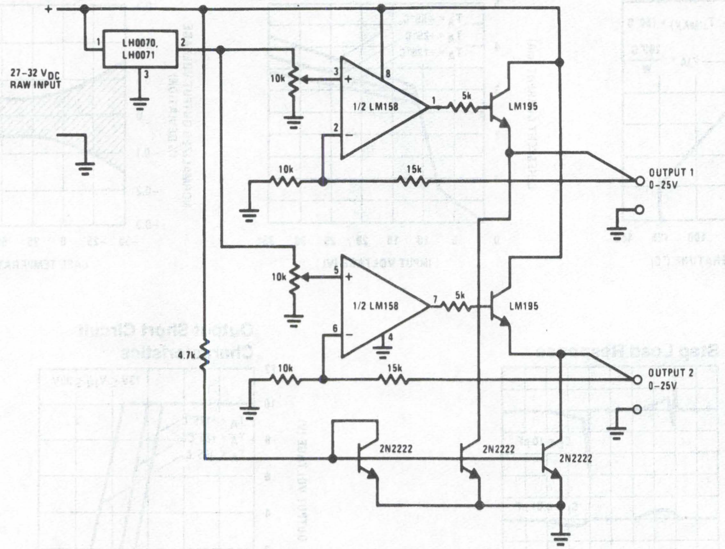
Expanded Scale AC Voltmeter


1N4004
140–180V PEAK
30k
1W
NOMINAL
117Vrms
AC LINE
10 μF
200V
30k
1/4 W
0.01 μF
1
LH0070
2
3
47k
1k
100V CAL.
1k
130V CAL.
3k
0–1 mA METER
0 mA = 100V ACrms
1 mA = 130V ACrms

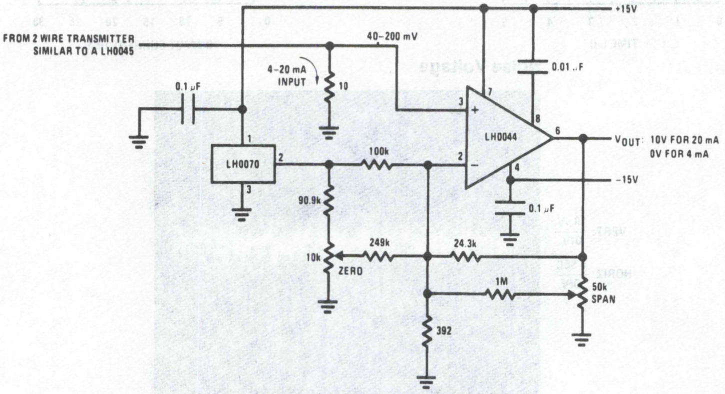
TL/H/5550-4

Typical Applications (Continued)

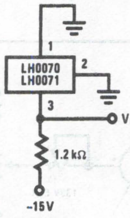
Dual Output Bench Power Supply


+
27–32 V$_{DC}$ RAW INPUT
LH0070, LH0071
1
2
3
10k
3
2
8
1/2 LM158
1
5k
LM195
10k
15k
OUTPUT 1 0–25V
10k
5
6
1/2 LM158
4
7
5k
LM195
4.7k
10k
15k
OUTPUT 2 0–25V
2N2222
2N2222
2N2222

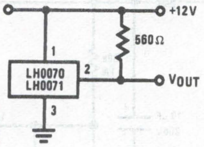
Precision Process Control Interface


FROM 2 WIRE TRANSMITTER SIMILAR TO A LH0045
40–200 mV
4–20 mA INPUT
10
0.1 μF
1
LH0070
2
3
100k
90.9k
10k
ZERO
249k
24.3k
1M
392
+15V
0.01 μF
7
3
+
LH0044
8
6
2
−
4
0.1 μF
V$_{OUT}$: 10V FOR 20 mA 0V FOR 4 mA
−15V
50k SPAN

Negative 10V Reference


1
LH0070 LH0071
2
3
V$_{OUT}$
1.2 kΩ
−15V

Boosted Reference For Low Input Voltages


+12V
560Ω
1
LH0070 LH0071
2
V$_{OUT}$
3

TL/H/5550–5

National Semiconductor

LM103 Reference Diode**

General Description

The LM103 is a two-terminal monolithic reference diode electrically equivalent to a breakdown diode. The device makes use of the reverse punch-through of double-diffused transistors, combined with active circuitry, to produce a breakdown characteristic which is ten times sharper than single-junction zener diodes at low voltages. Breakdown voltages from 3.0V to 3.9V are available; and, although the design is optimized for operation between 100 μA and 1 mA, it is completely specified from 10 μA to 10 mA.

Features

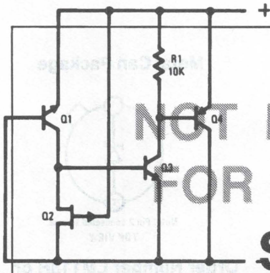
- Exceptionally sharp breakdown
- Low dynamic impedance from 10 μA to 10 mA
- Performance guaranteed over full military temperature range
- Planar, passivated junctions for stable operation
- Low capacitance.

The LM103, packaged in a hermetically sealed, modified TO-46 header is useful in a wide range of circuit applications from level shifting to simple voltage regulation. It can also be employed with operational amplifiers in producing breakpoints to generate nonlinear transfer functions. Finally, its unique characteristics recommend it as a reference element in low voltage power supplies with input voltages down to 4V.

Schematic and Connection Diagrams

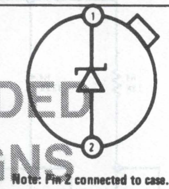
NOT RECOMMENDED FOR NEW DESIGNS

SEE LM185


+
R1
10K
Q1
Q4
Q3
Q2

TL/H/6170–1

Metal Can Package



Note: Pin 2 connected to case.

TOP VIEW

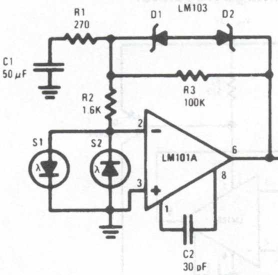
TL/H/6170–2

Order Number LM103H-3.0, LM103H-3.3, LM103H-3.6 or LM103H-3.9

See NS Package H02A

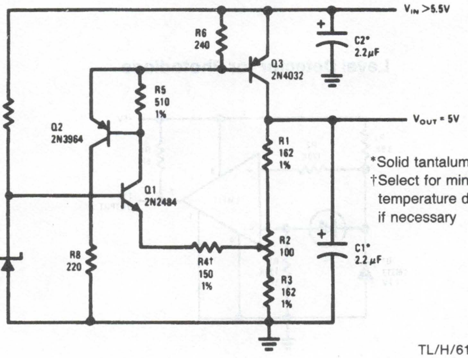
Typical Applications

Saturating Servo Preamplifier with Rate Feedback


R1
270
D1
LM103
D2
C1
50 μF
R2
1.6K
R3
100K
S1
S2
2
3
6
8
1
LM101A
OUTPUT
C2
30 pF

TL/H/6170–3

200 mA Positive Regulator


V_IN >5.5V
R6
240
Q3
2N4032
C2*
2.2 μF
R5
510
1%
R7
10K
Q2
2N3964
V_OUT = 5V
R1
162
1%
Q1
2N2484
D1
LM103
3.3V
R8
220
R4†
150
1%
R2
100
R3
162
1%
C1*
2.2 μF

*Solid tantalum

†Select for minimum temperature drift, if necessary

TL/H/6170–4

**Covered by U.S. Patent Number 3,571,630

National Semiconductor Corporation

LM113/LM313 Reference Diode

General Description

The LM113/LM313 are temperature compensated, low voltage reference diodes. They feature extremely-tight regulation over a wide range of operating currents in addition to an unusually-low breakdown voltage and good temperature stability.

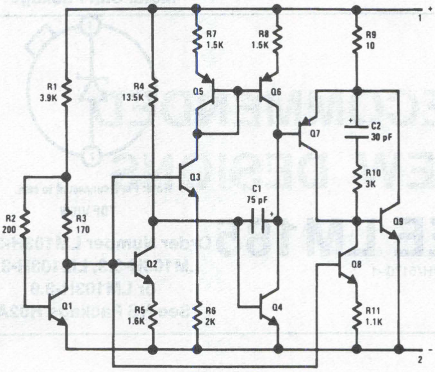
The diodes are synthesized using transistors and resistors in a monolithic integrated circuit. As such, they have the same low noise and long term stability as modern IC op amps. Further, output voltage of the reference depends only on highly-predictable properties of components in the IC; so they can be manufactured and supplied to tight tolerances.

Features

- Low breakdown voltage: 1.220V
- Dynamic impedance of 0.3Ω from 500 µA to 20 mA
- Temperature stability typically 1% over −55°C to 125°C range (LM113), 0°C to 70°C (LM313)
- Tight tolerance: ±5%, ±2% or ±1%

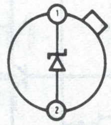
The characteristics of this reference recommend it for use in bias-regulation circuitry, in low-voltage power supplies or in battery powered equipment. The fact that the breakdown voltage is equal to a physical property of silicon—the energy-band gap voltage—makes it useful for many temperature-compensation and temperature-measurement functions.

Schematic and Connection Diagrams



R1 3.9K
R4 13.5K
R7 1.5K
R8 1.5K
R9 10
Q5
Q6
Q7
C2 30 pF
R10 3K
Q3
C1 75 pF
Q9
R2 200
R3 170
Q2
Q8
R5 1.6K
R6 2K
Q4
R11 1.1K
Q1
1 +
2 −

Metal Can Package



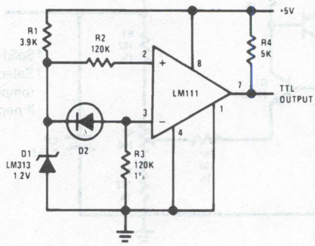
Note: Pin 2 connected to case.
TOP VIEW

Order Number LM113H or LM113-1H or LM113-2H or LM313H
See NS Package Number H02A

TL/H/5713–1

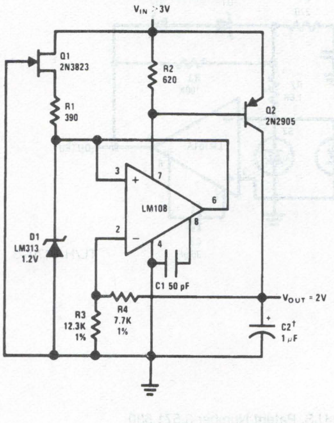
Typical Applications

Level Detector for Photodiode



R1 3.9K
R2 120K
+5V
R4 5K
LM111
TTL OUTPUT
D1 LM313 1.2V
D2
R3 120K 1%
2
3
8
7
1
4

Low Voltage Regulator



V_IN ≥ 3V
Q1 2N3823
R2 620
R1 390
Q2 2N2905
LM108
D1 LM313 1.2V
C1 50 pF
R3 12.3K 1%
R4 7.7K 1%
V_OUT = 2V
C2† 1 µF
3
7
6
8
2
4

TL/H/5713–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 3)

Power Dissipation (Note 1)	100 mW
Reverse Current	50 mA
Forward Current	50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature Range	
LM113	−55°C to + 125°C
LM313	0°C to +70°C

Electrical Characteristics (Note 2)

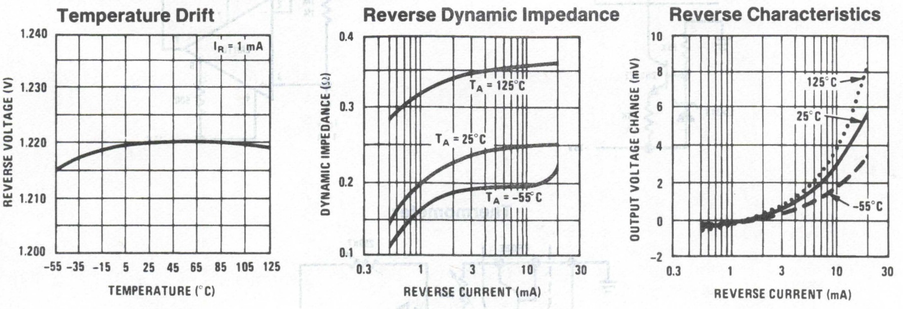
Parameter	Conditions	Min	Typ	Max	Units
Reverse Breakdown Voltage					
LM113/LM313	$I_R = 1$ mA	1.160	1.220	1.280	V
LM113-1		1.210	1.22	1.232	V
LM113-2		1.195	1.22	1.245	V
Reverse Breakdown Voltage Change	0.5 mA $\leq I_R \leq$ 20 mA		6.0	15	mV
Reverse Dynamic Impedance	$I_R = 1$ mA $I_R = 10$ mA		0.2 0.25	1.0 0.8	Ω Ω
Forward Voltage Drop	$I_F = 1.0$ mA		0.67	1.0	V
RMS Noise Voltage	10 Hz $\leq f \leq$ 10 kHz $I_R = 1$ mA		5		μV
Reverse Breakdown Voltage Change with Current	0.5 mA $\leq I_R \leq$ 10 mA $T_{MIN} \leq T_A \leq T_{MAX}$			15	mV
Breakdown Voltage Temperature Coefficient	1.0 mA $\leq I_R \leq$ 10 mA $T_{MIN} \leq T_A \leq T_{MAX}$		0.01		%/°C

Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction and a thermal resistance of 80°C/W junction to case or 440°C/W junction to ambient.

Note 2: These specifications apply for $T_A = 25°C$, unless stated otherwise. At high currents, breakdown voltage should be measured with lead lengths less than ¼ inch. Kelvin contact sockets are also recommended. The diode should not be operated with shunt capacitances between 200 pF and 0.1 μF, unless isolated by at least a 100Ω resistor, as it may oscillate at some currents.

Note 3: Refer to the following RETS drawings for military specifications: RETS113-1X for LM113-1, RETS113-2X for LM113-2 or RETS113X for LM113.

Typical Performance Characteristics



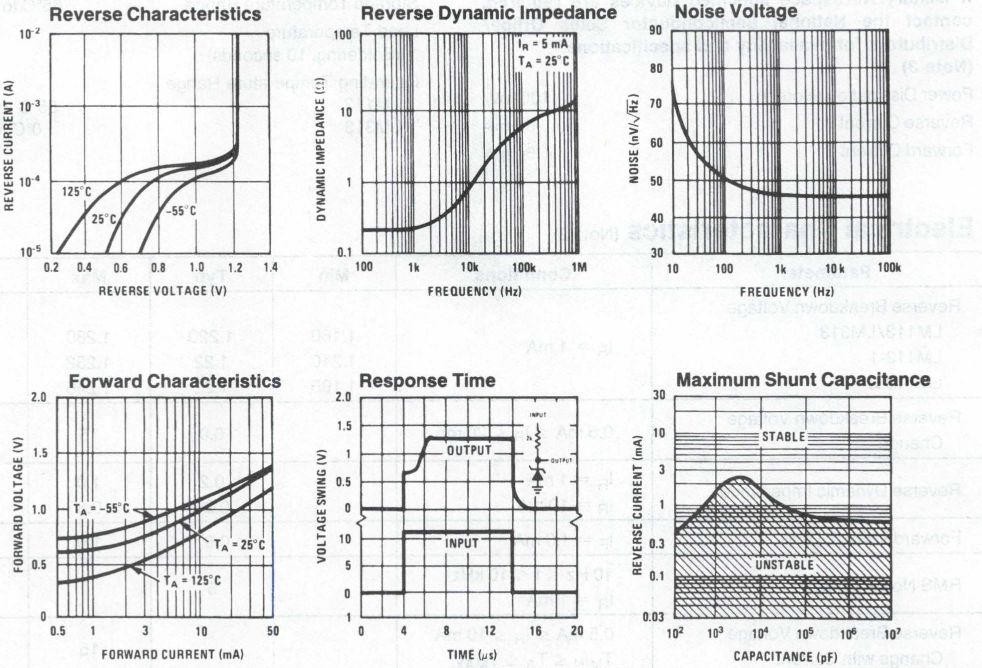
Temperature Drift

Reverse Dynamic Impedance

Reverse Characteristics

TL/H/5713-3

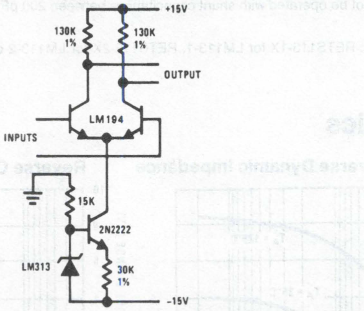
Typical Performance Characteristics (Continued)



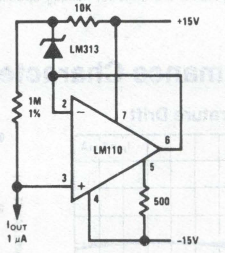
TL/H/5713-4

Typical Applications (Continued)

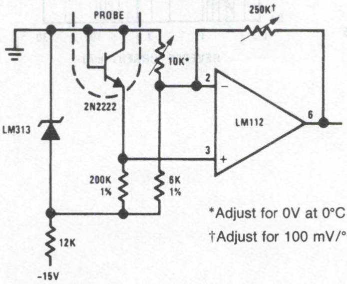
Amplifier Biasing for Constant Gain with Temperature


+15V
130K 1%
130K 1%
OUTPUT
LM194
INPUTS
15K
2N2222
LM313
30K 1%
−15V

Constant Current Source


10K
+15V
LM313
1M 1%
2
7
LM110
6
3
5
4
500
I_{OUT} 1 μA
−15V

Thermometer


PROBE
250K†
10K*
2N2222
LM313
2
LM112
6
3
200K 1%
6K 1%
12K
−15V

*Adjust for 0V at 0°C

†Adjust for 100 mV/°C

TL/H/5713-5

National
Semiconductor
Corporation

LM129/LM329 Precision Reference

General Description

The LM129 and LM329 family are precision multi-current temperature-compensated 6.9V zener references with dynamic impedances a factor of 10 to 100 less than discrete diodes. Constructed in a single silicon chip, the LM129 uses active circuitry to buffer the internal zener allowing the device to operate over a 0.5 mA to 15 mA range with virtually no change in performance. The LM129 and LM329 are available with selected temperature coefficients of 0.001, 0.002, 0.005 and 0.01%/°C. These new references also have excellent long term stability and low noise.

A new subsurface breakdown zener used in the LM129 gives lower noise and better long-term stability than conventional IC zeners. Further the zener and temperature compensating transistor are made by a planar process so they are immune to problems that plague ordinary zeners. For example, there is virtually no voltage shift in zener voltage due to temperature cycling and the device is insensitive to stress on the leads.

The LM129 can be used in place of conventional zeners with improved performance. The low dynamic impedance simplifies biasing and the wide operating current allows the replacement of many zener types.

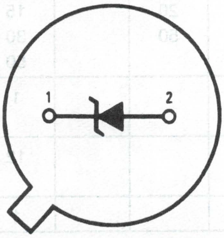
The LM129 is packaged in a 2-lead TO-46 package and is rated for operation over a −55°C to +125°C temperature range. The LM329 for operation over 0°C to 70°C is available in both a hermetic TO-46 package and a TO-92 epoxy package.

Features

- 0.6 mA to 15 mA operating current
- 0.6Ω dynamic impedance at any current
- Available with temperature coefficients of 0.001%/°C
- 7μV wideband noise
- 5% initial tolerance
- 0.002% long term stability
- Low cost
- Subsurface zener

Connection Diagrams

Metal Can Package



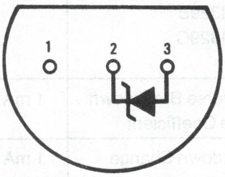
TL/H/5714-6

Bottom View

Pin 2 is electrically connected to case

Order Number LM129AH, LM129BH, LM129CH, LM329AH, LM329BH, LM329CH or LM329DH
See NS Package H02A

Plastic Package



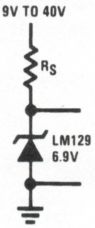
TL/H/5714-4

Bottom View

Order Number LM329BZ, LM329CZ or LM329DZ
See NS Package Z03A

Typical Applications

Simple Reference



TL/H/5714-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 2)

Reverse Breakdown Current	30 mA
Forward Current	2 mA
Operating Temperature Range	
LM129	−55°C to +125°C
LM329	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
TO-92 package: 10 sec.	260°C
TO-46 package: 10 sec.	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	LM129A, B, C			LM329A, B, C, D			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$T_A = 25°C$, $0.6\ mA \le I_R \le 15\ mA$	6.7	6.9	7.2	6.6	6.9	7.25	V
Reverse Breakdown Change with Current (Note 3)	$T_A = 25°C$, $0.6\ mA \le I_R \le 15\ mA$		9	14		9	20	mV
Reverse Dynamic Impedance (Note 3)	$T_A = 25°C, I_R = 1\ mA$		0.6	1		0.8	2	Ω
RMS Noise	$T_A = 25°C$, $10\ Hz \le F \le 10\ kHz$		7	20		7	100	μV
Long Term Stability (1000 hours)	$T_A = 45°C \pm 0.1°C$, $I_R = 1\ mA \pm 0.3\%$		20			20		ppm
Temperature Coefficient	$I_R = 1\ mA$							
LM129A, LM329A			6	10		6	10	ppm/°C
LM129B, LM329B			15	20		15	20	ppm/°C
LM129C, LM329C			30	50		30	50	ppm/°C
LM329D						50	100	ppm/°C
Change In Reverse Breakdown Temperature Coefficient	$1\ mA \le I_R \le 15\ mA$		1			1		ppm/°C
Reverse Breakdown Change with Current	$1\ mA \le I_R \le 15\ mA$		12			12		mV
Reverse Dynamic Impedance	$1\ mA \le I_R \le 15\ mA$		0.8			1		Ω

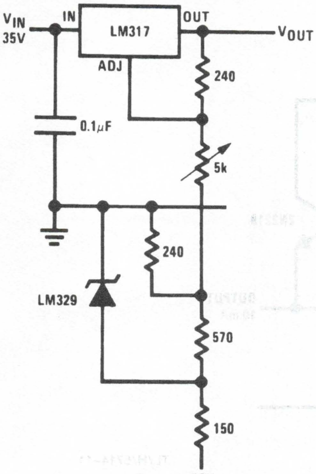
Note 1: These specifications apply for $-55°C \le T_A \le +125°C$ for the LM129 and $0°C \le T_A \le +70°C$ for the LM329 unless otherwise specified. The maximum junction temperature for an LM129 is 150°C and LM329 is 100°C. For operating at elevated temperature, devices in TO-46 package must be derated based on a thermal resistance of 440°C/W junction to ambient or 80°C/W junction to case. For the TO-92 package, the derating is based on 180°C/W junction to ambient with 0.4″ leads from a PC board and 160°C/W junction to ambient with 0.125″ lead length to a PC board.

Note 2: Refer to RETS129H for LM129 family military specifications.

Note 3: These changes are tested on a pulsed basis with a low duty-cycle. For changes versus temperature, compute in terms of tempco.

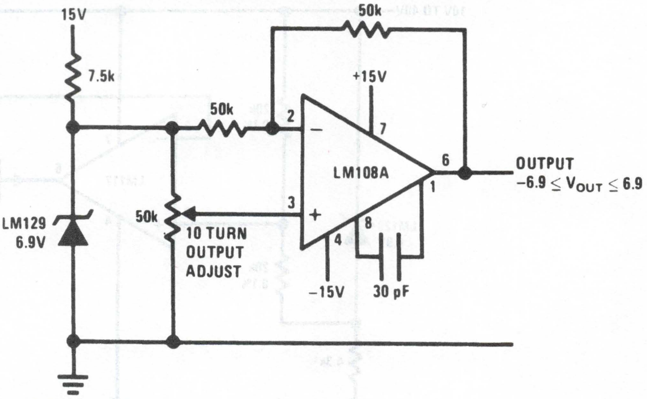
Typical Applications (Continued)

Low Cost 0–25V Regulator


V_IN
35V
IN
LM317
OUT
V_OUT
ADJ
0.1μF
240
5k
240
LM329
570
150
-10V

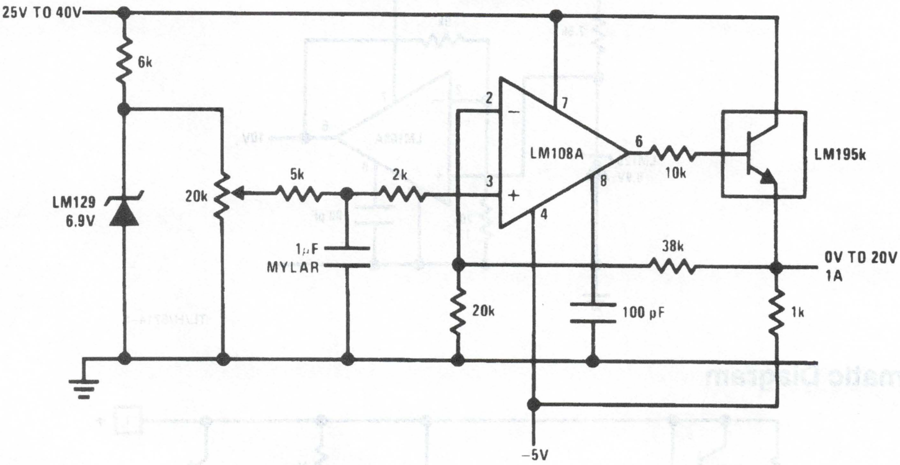
TL/H/5714–7

Adjustable Bipolar Output Reference


15V
7.5k
50k
+15V
50k
2
7
LM108A
6
1
OUTPUT
-6.9 ≤ V_OUT ≤ 6.9
LM129
6.9V
50k
10 TURN
OUTPUT
ADJUST
3
8
4
-15V
30 pF

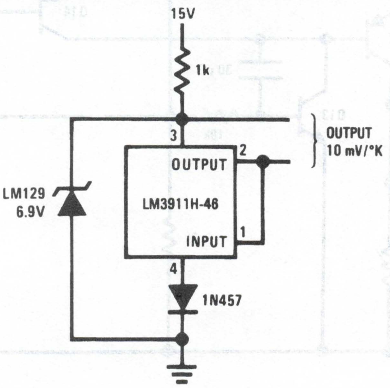
TL/H/5714–8

0V to 20V Power Reference


25V TO 40V
6k
LM129
6.9V
20k
5k
2k
1μF
MYLAR
2
7
LM108A
6
10k
LM195k
3
8
4
38k
0V TO 20V
1A
20k
100 pF
1k
-5V

TL/H/5714–9

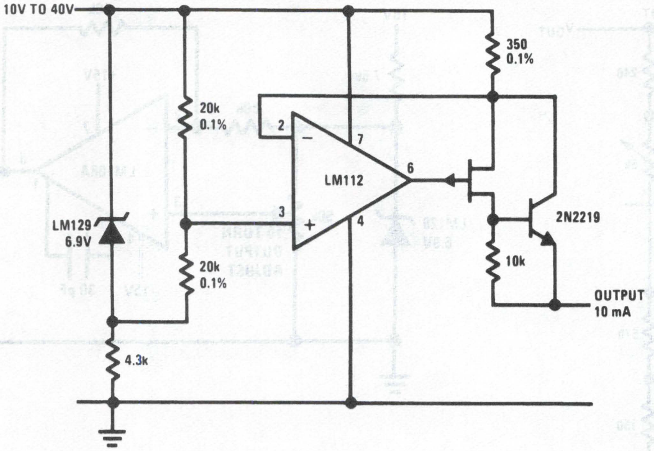
External Reference for Temperature Transducer


15V
1k
3
OUTPUT
2
OUTPUT
10 mV/°K
LM129
6.9V
LM3911H-46
INPUT
1
4
1N457

TL/H/5714–2

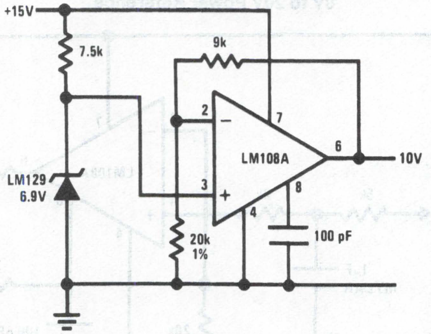
Typical Applications (Continued)

Positive Current Source


10V TO 40V
20k
0.1%
20k
0.1%
LM129
6.9V
4.3k
2
3
7
6
4
LM112
350
0.1%
2N2219
10k
OUTPUT
10 mA

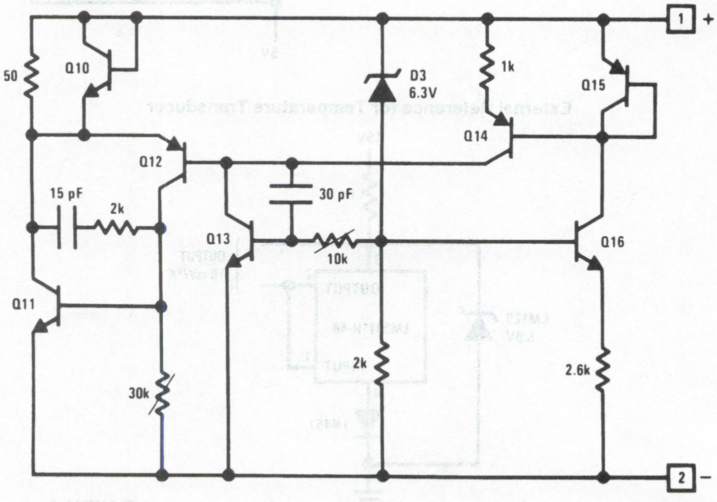
TL/H/5714-11

Buffered Reference with Single Supply


+15V
7.5k
9k
LM129
6.9V
2
3
7
6
8
4
LM108A
10V
20k
1%
100 pF

TL/H/5714-3

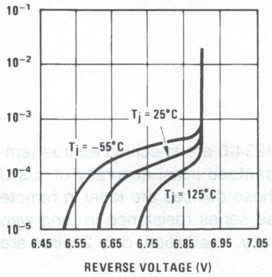
Schematic Diagram


50
Q10
Q12
15 pF
2k
Q11
30k
Q13
30 pF
10k
D3
6.3V
2k
1k
Q14
Q15
Q16
2.6k
1
+
2
−

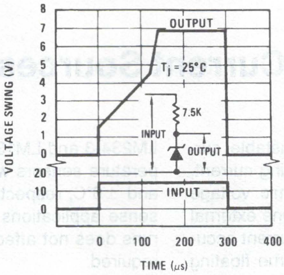
TL/H/5714-10

Typical Performance Characteristics

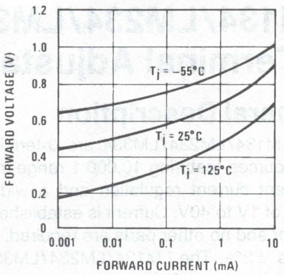
Reverse Characteristics



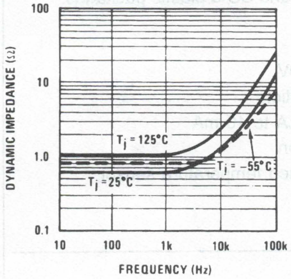
Response Time



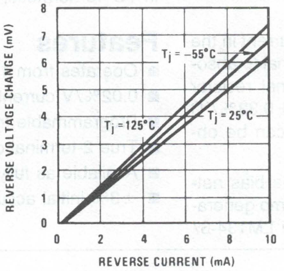
Forward Characteristics



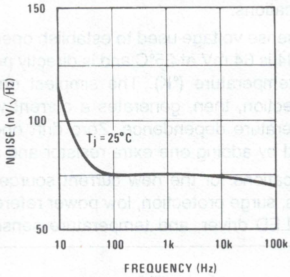
Dynamic Impedance



Reverse Voltage Change

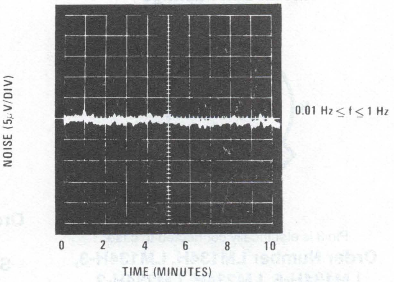


Zener Noise Voltage



TL/H/5714–12

Low Frequency Noise Voltage



TL/H/5714–5

National Semiconductor Corporation

LM134/LM234/LM334
3-Terminal Adjustable Current Sources

General Description

The LM134/LM234/LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V. Current is established with one external resistor and no other parts are required. Initial current accuracy is ±3%. The LM134/LM234/LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few dozen microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The sense voltage used to establish operating current in the LM134 is 64 mV at 25°C and is directly proportional to absolute temperature (°K). The simplest one external resistor connection, then, generates a current with ≈ +0.33%/°C temperature dependence. Zero drift operation can be obtained by adding one extra resistor and a diode.

Applications for the new current sources include bias networks, surge protection, low power reference, ramp generation, LED driver, and temperature sensing. The LM134-3/LM234-3 and LM134-6/LM234-6 are specified as true temperature sensors with guaranteed initial accuracy of ±3°C and ±6°C, respectively. These devices are ideal in remote sense applications because series resistance in long wire runs does not affect accuracy. In addition, only 2 wires are required.

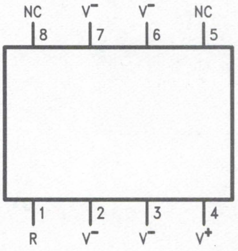
The LM134 is guaranteed over a temperature range of −55°C to +125°C, the LM234 from −25°C to +100°C and the LM334 from 0°C to +70°C. These devices are available in TO-46 hermetic, TO-92 and SO-8 plastic packages.

Features

- Operates from 1V to 40V
- 0.02%/V current regulation
- Programmable from 1 μA to 10 mA
- True 2-terminal operation
- Available as fully specified temperature sensor
- ±3% initial accuracy

Connection Diagrams

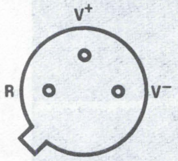
SO-8
Surface Mount Package



TL/H/5697-24

Order Number LM334M
See NS Package Number M08A

TO-46
Metal Can Package



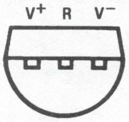
TL/H/5697-12

Bottom View

Pin 3 is electrically connected to case.

Order Number LM134H, LM134H-3, LM134H-6, LM234H, LM234H-3, LM234H-6, or LM334H
See NS Package Number H03H

TO-92
Plastic Package



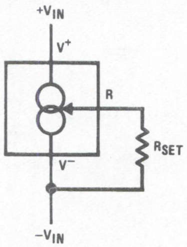
TL/H/5697-10

Bottom View

Order Number LM334Z, LM234Z-3 or LM234Z-6
See NS Package Number Z03A

Typical Application

Basic 2-Terminal Current Source



TL/H/5697-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V^+ to V^- Forward Voltage	
LM134/LM234	40V
LM334/LM134-3/LM134-6/LM234-3/LM234-6	30V
V^+ to V^- Reverse Voltage	20V
R Pin to V^- Voltage	5V
Set Current	10 mA
Power Dissipation	400 mW

Operating Temperature Range (Note 4)	
LM134/LM134-3/LM134-6	−55°C to +125°C
LM234/LM234-3/LM234-6	−25°C to +100°C
LM334	0°C to +70°C
Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM134/LM234			LM334			Units
		Min	Typ	Max	Min	Typ	Max	
Set Current Error, $V^+ = 2.5V$, (Note 2)	$10\ \mu A \le I_{SET} \le 1\ mA$			3			6	%
	$1\ mA < I_{SET} \le 5\ mA$			5			8	%
	$2\ \mu A \le I_{SET} < 10\ \mu A$			8			12	%
Ratio of Set Current to V^- Current	$100\ \mu A \le I_{SET} \le 1\ mA$	14	18	23	14	18	26	
	$1\ mA \le I_{SET} \le 5\ mA$		14			14		
	$2\ \mu A \le I_{SET} \le 100\ \mu A$		18	23		18	26	
Minimum Operating Voltage	$2\ \mu A \le I_{SET} \le 100\ \mu A$		0.8			0.8		V
	$100\ \mu A < I_{SET} \le 1\ mA$		0.9			0.9		V
	$1\ mA < I_{SET} \le 5\ mA$		1.0			1.0		V
Average Change in Set Current with Input Voltage	$2\ \mu A \le I_{SET} \le 1\ mA$							
	$1.5 \le V^+ \le 5V$		0.02	0.05		0.02	0.1	%/V
	$5V \le V^+ \le 40V$		0.01	0.03		0.01	0.05	%/V
	$1\ mA < I_{SET} \le 5\ mA$							
	$1.5V \le V \le 5V$		0.03			0.03		%/V
	$5V \le V \le 40V$		0.02			0.02		%/V
Temperature Dependence of Set Current (Note 3)	$25\ \mu A \le I_{SET} \le 1\ mA$	0.96T	T	1.04T	0.96T	T	1.04T	
Effective Shunt Capacitance			15			15		pF

Note 1: Unless otherwise specified, tests are performed at $T_j = 25°C$ with pulse testing so that junction temperature does not change during test.

Note 2: Set current is the current flowing into the V^+ pin. It is determined by the following formula: $I_{SET} = 67.7\ mV/R_{SET}$ (@ 25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C @ $T_j = 25°C$.

Note 3: I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: $I_{SET} = I_o\ (T/T_o)$ where I_o is I_{SET} measured at T_o (°K).

Note 4: For elevated temperature operation, T_j max is:

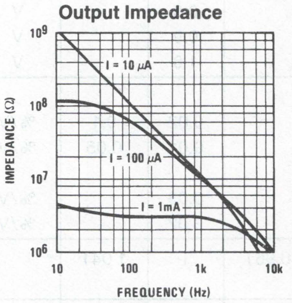
LM134	150°C
LM234	125°C
LM334	100°C

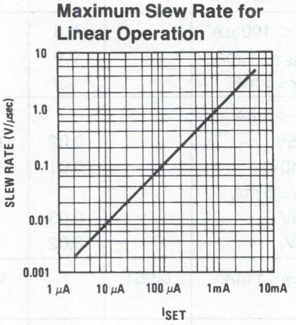
Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4″ leads) 160°C/W (0.125″ leads)	440°C/W	165°C/W
θ_{jc} (Junction to Case)	N/A	32°C/W	N/A

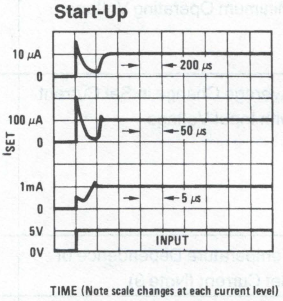
Electrical Characteristics (Note 1) (Continued)

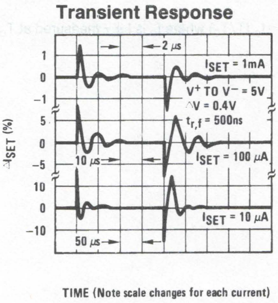
Parameter	Conditions	LM134-3, LM234-3			LM134-6, LM234-6			Units
		Min	Typ	Max	Min	Typ	Max	
Set Current Error, $V^+ = 2.5V$, (Note 2)	$100\ \mu A \leq I_{SET} \leq 1\ mA$ $T_j = 25°$			±1			±2	%
Equivalent Temperature Error				±3			±6	°C
Ratio of Set Current to V^- Current	$100\ \mu A \leq I_{SET} \leq 1\ mA$	14	18	26	14	18	26	
Minimum Operating Voltage	$100\ \mu A\ I_{SET} \leq 1\ mA$		0.9			0.9		V
Average Change in Set Current with Input Voltage	$100\ \mu A \leq I_{SET} \leq 1\ mA$							
	$1.5 \leq V^+ \leq 5V$		0.02	0.05		0.02	0.01	%/V
	$5V \leq V^+ \leq 30V$		0.01	0.03		0.01	0.05	%/V
Temperature Dependence of Set Current (Note 3) and	$100\ \mu A \leq I_{SET} \leq 1\ mA$	0.98T	T	1.02T	0.97T	T	1.03T	
Equivalent Slope Error				±2			±3	%
Effective Shunt Capacitance			15			15		pF

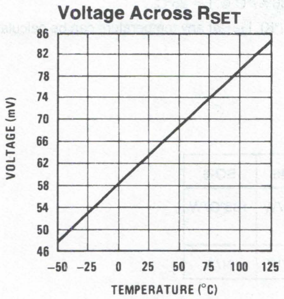
Typical Performance Characteristics

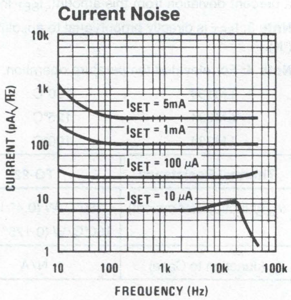

Output Impedance


Maximum Slew Rate for Linear Operation


Start-Up

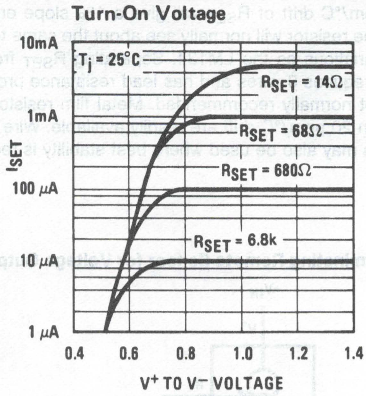

Transient Response

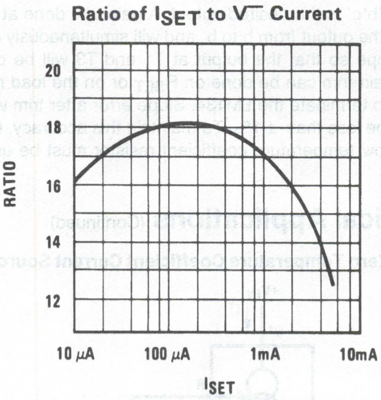

Voltage Across R_{SET}


Current Noise

TL/H/5697–2

Typical Performance Characteristics (Continued)





TL/H/5697-3

Application Hints

The LM134 has been designed for ease of application, but a general discussion of design features is presented here to familiarize the designer with device characteristics which may not be immediately obvious. These include the effects of slewing, power dissipation, capacitance, noise, and contact resistance.

SLEW RATE

At slew rates above a given threshold (see curve), the LM134 may exhibit non-linear current shifts. The slewing rate at which this occurs is directly proportional to I_{SET}. At $I_{SET} = 10\ \mu A$, maximum dV/dt is 0.01V/μs; at $I_{SET} = 1$ mA, the limit is 1V/μs. Slew rates above the limit do not harm the LM134, or cause large currents to flow.

THERMAL EFFECTS

Internal heating can have a significant effect on current regulation for I_{SET} greater than 100 μA. For example, each 1V increase across the LM134 at $I_{SET} = 1$ mA will increase junction temperature by ≈ 0.4°C in still air. Output current (I_{SET}) has a temperature coefficient of ≈0.33%/°C, so the change in current due to temperature rise will be (0.4) (0.33) = 0.132%. This is a 10:1 degradation in regulation compared to true electrical effects. Thermal effects, therefore, must be taken into account when DC regulation is critical and I_{SET} exceeds 100 μA. Heat sinking of the TO-46 package or the TO-92 leads can reduce this effect by more than 3:1.

SHUNT CAPACITANCE

In certain applications, the 15 pF shunt capacitance of the LM134 may have to be reduced, either because of loading problems or because it limits the AC output impedance of the current source. This can be easily accomplished by buffering the LM134 with an FET as shown in the applications. This can reduce capacitance to less than 3 pF and improve regulation by at least an order of magnitude. DC characteristics (with the exception of minimum input voltage), are not affected.

NOISE

Current noise generated by the LM134 is approximately 4 times the shot noise of a transistor. If the LM134 is used as an active load for a transistor amplifier, input referred noise will be increased by about 12 dB. In many cases, this is acceptable and a single stage amplifier can be built with a voltage gain exceeding 2000.

LEAD RESISTANCE

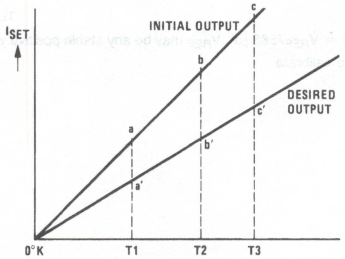
The sense voltage which determines operating current of the LM134 is less than 100 mV. At this level, thermocouple or lead resistance effects should be minimized by locating the current setting resistor physically close to the device. Sockets should be avoided if possible. It takes only 0.7Ω contact resistance to reduce output current by 1% at the 1 mA level.

SENSING TEMPERATURE

The LM134 makes an ideal remote temperature sensor because its current mode operation does not lose accuracy over long wire runs. Output current is directly proportional to absolute temperature in degrees Kelvin, according to the following formula:

$$I_{SET} = \frac{(227\ \mu V/°K)(T)}{R_{SET}}$$

Calibration of the LM134 is greatly simplified because of the fact that most of the initial inaccuracy is due to a gain term (slope error) and not an offset. This means that a calibration consisting of a gain adjustment only will trim both slope and zero at the same time. In addition, gain adjustment is a one point trim because the output of the LM134 extrapolates to zero at 0°K, independent of R_{SET} or any initial inaccuracy.



TL/H/5697-4

This property of the LM134 is illustrated in the accompanying graph. Line abc is the sensor current before trimming.

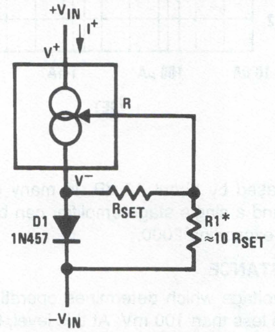
Application Hints (Continued)

Line a′b′c′ is the desired output. A gain trim done at T2 will move the output from b to b′ and will simultaneously correct the slope so that the output at T1 and T3 will be correct. This gain trim can be done on R_{SET} or on the load resistor used to terminate the LM134. Slope error after trim will normally be less than ±1%. To maintain this accuracy, however, a low temperature coefficient resistor must be used for R_{SET}.

A 33 ppm/°C drift of R_{SET} will give a 1% slope error because the resistor will normally see about the same temperature variations as the LM134. Separating R_{SET} from the LM134 requires 3 wires and has lead resistance problems, so is not normally recommended. Metal film resistors with less than 20 ppm/°C drift are readily available. Wire wound resistors may also be used where best stability is required.

Typical Applications (Continued)

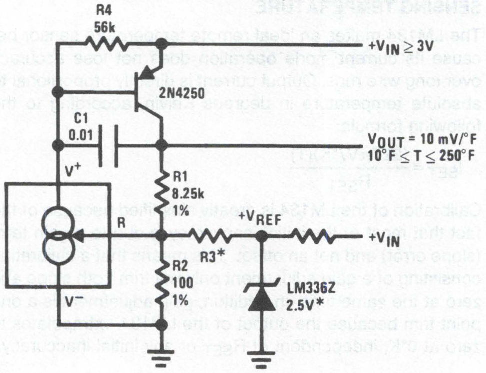
Zero Temperature Coefficient Current Source


+V_{IN}
I+
V+
R
V−
R_{SET}
D1
1N457
R1*
≈10 R_{SET}
−V_{IN}

TL/H/5697–13

*Select ratio of R1 to R_{SET} to obtain zero drift. $I^+ \approx 2\ I_{SET}$

Ground Referred Fahrenheit Thermometer

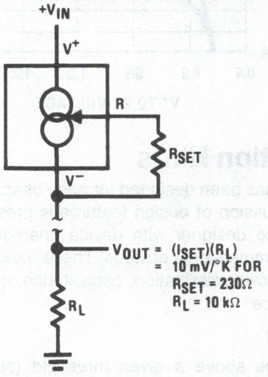

R4
56k
+V_{IN} ≥ 3V
2N4250
C1
0.01
V_{OUT} = 10 mV/°F
10°F ≤ T ≤ 250°F
V+
R1
8.25k
1%
R
+V_{REF}
+V_{IN}
R3*
R2
100
1%
LM336Z
2.5V*
V−

TL/H/5697–15

*Select R3 = $V_{REF}/583\ \mu A$. V_{REF} may be any stable positive voltage ≥2V

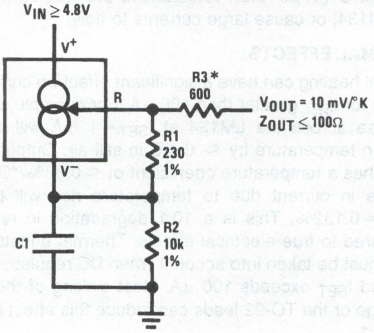
Trim R3 to calibrate

Terminating Remote Sensor for Voltage Output


+V_{IN}
V+
R
R_{SET}
V−
V_{OUT} = (I_{SET})(R_L)
= 10 mV/°K FOR
R_{SET} = 230Ω
R_L = 10 kΩ
R_L

TL/H/5697–14

Low Output Impedance Thermometer

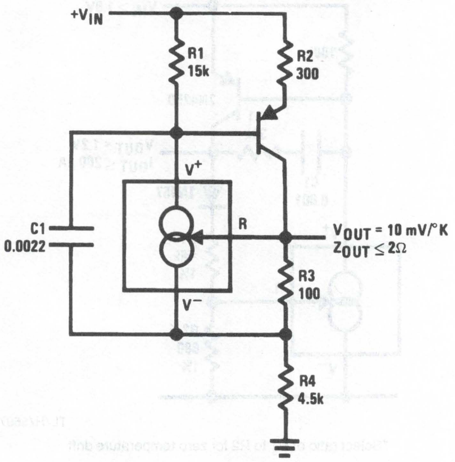

V_{IN} ≥ 4.8V
V+
R3*
600
R
V_{OUT} = 10 mV/°K
Z_{OUT} ≤ 100Ω
R1
230
1%
V−
C1
R2
10k
1%

TL/H/5697–6

*Output impedance of the LM134 at the "R" pin is approximately $\frac{-R_o\Omega}{16}$ where R_o is the equivalent external resistance connected to the V^- pin. This negative resistance can be reduced by a factor of 5 or more by inserting an equivalent resistor in series with the output.

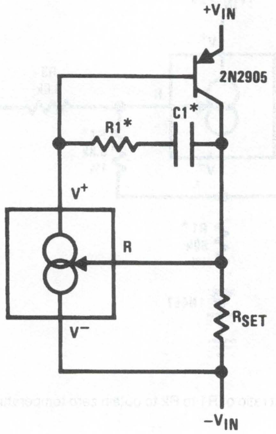
Typical Applications (Continued)

Low Output Impedance Thermometer


+V_{IN}
R1
15k
R2
300
V^+
C1
0.0022
R
V_{OUT} = 10 mV/°K
Z_{OUT} ≤ 2Ω
R3
100
V^-
R4
4.5k

TL/H/5697-16

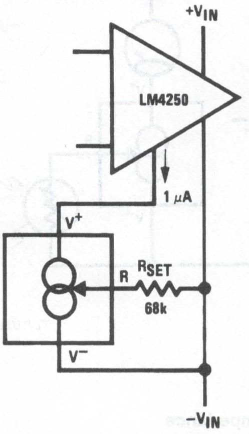
Higher Output Current


+V_{IN}
2N2905
$C1^*$
$R1^*$
V^+
R
R_{SET}
V^-
−V_{IN}

TL/H/5697-5

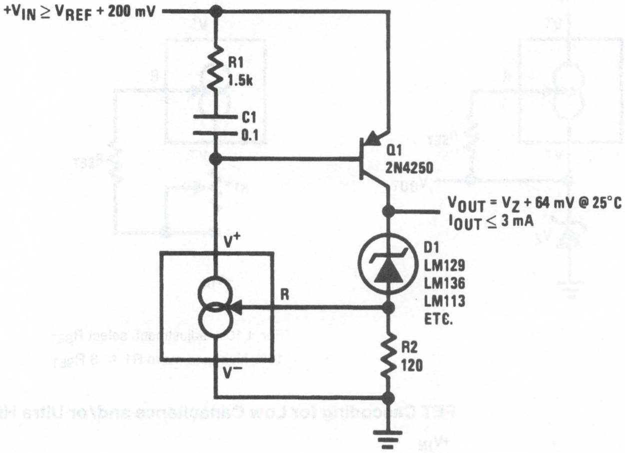
*Select R1 and C1 for optimum stability

Micropower Bias


+V_{IN}
LM4250
1 µA
V^+
R
R_{SET}
68k
V^-
−V_{IN}

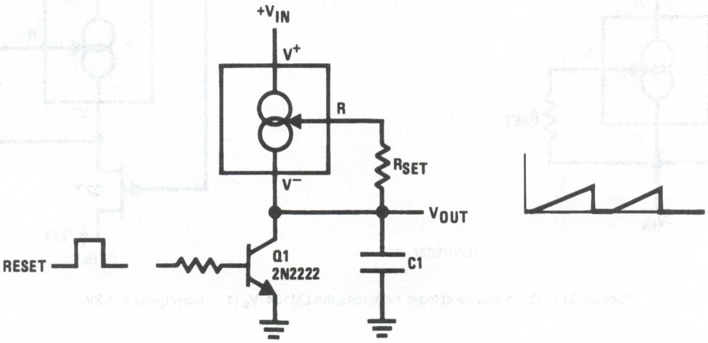
TL/H/5697-17

Low Input Voltage Reference Driver


+V_{IN} ≥ V_{REF} + 200 mV
R1
1.5k
C1
0.1
Q1
2N4250
V_{OUT} = V_Z + 64 mV @ 25°C
I_{OUT} ≤ 3 mA
V^+
D1
LM129
LM136
LM113
ETC.
R
R2
120
V^-

TL/H/5697-18

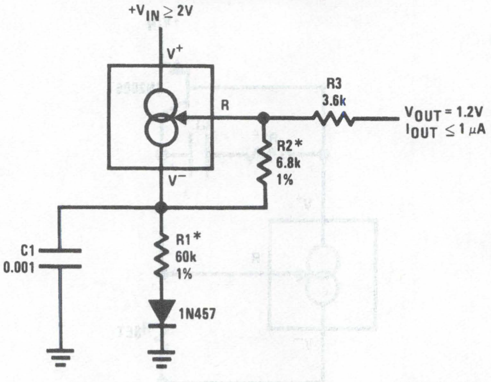
Ramp Generator


+V_{IN}
V^+
R
R_{SET}
V^-
V_{OUT}
RESET
Q1
2N2222
C1

TL/H/5697-19

Typical Applications (Continued)

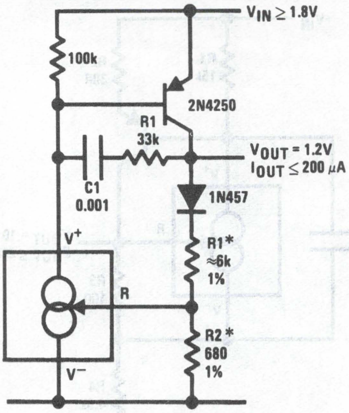
1.2V Reference Operates on 10 μA and 2V


$+V_{IN} \geq 2V$
V^+
R
R3
3.6k
$V_{OUT} = 1.2V$
$I_{OUT} \leq 1\ \mu A$
R2*
6.8k
1%
V^-
C1
0.001
R1*
60k
1%
1N457

TL/H/5697-20

*Select ratio of R1 to R2 to obtain zero temperature drift

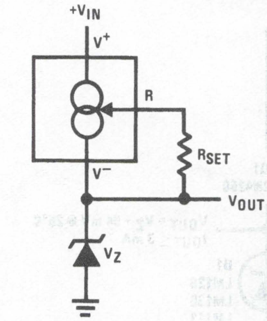
1.2V Regulator with 1.8V Minimum Input


$V_{IN} \geq 1.8V$
100k
2N4250
R1
33k
$V_{OUT} = 1.2V$
$I_{OUT} \leq 200\ \mu A$
C1
0.001
1N457
V^+
R1*
≈6k
1%
R
R2*
680
1%
V^-

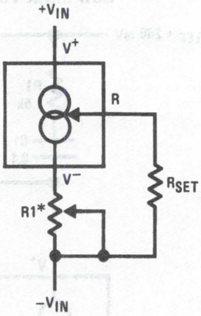
TL/H/5697-7

*Select ratio of R1 to R2 for zero temperature drift

Zener Biasing

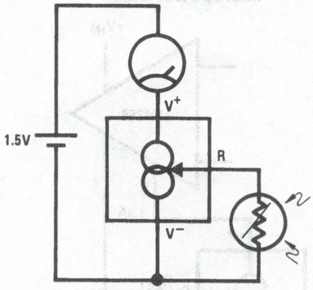

$+V_{IN}$
V^+
R
R_{SET}
V^-
V_{OUT}
V_Z

Alternate Trimming Technique


$+V_{IN}$
V^+
R
V^-
R_{SET}
R1*
$-V_{IN}$

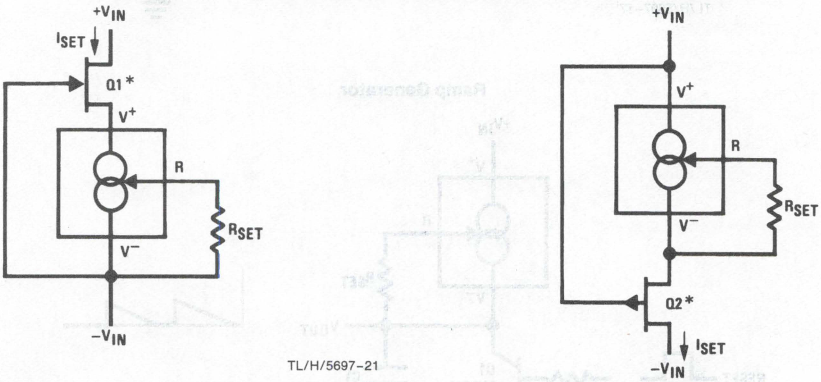
*For ±10% adjustment, select R_{SET} 10% high, and make R1 ≈ 3 R_{SET}

Buffer for Photoconductive Cell



TL/H/5697-8

FET Cascoding for Low Capacitance and/or Ultra High Output Impedance


$+V_{IN}$
I_{SET}
Q1*
V^+
R
R_{SET}
V^-
$-V_{IN}$
$+V_{IN}$
V^+
R
R_{SET}
V^-
Q2*
I_{SET}
$-V_{IN}$

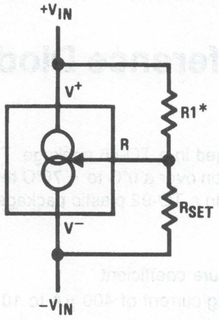
TL/H/5697-21

TL/H/5697-22

*Select Q1 or Q2 to ensure at least 1V across the LM134. $V_P\ (1 - I_{SET}/I_{DSS}) \geq 1.2V$.

Typical Applications (Continued)

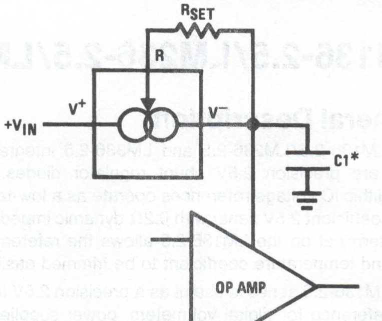
Generating Negative Output Impedance


+V_IN
V+
R1*
R
R_SET
V−
−V_IN

TL/H/5697-23

$^{*}Z_{OUT} \approx -16 \bullet R1$ ($R1/V_{IN}$ must not exceed I_{SET})

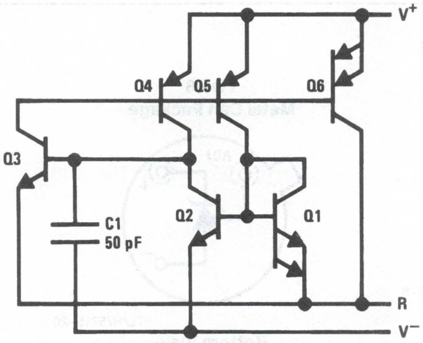
In-Line Current Limiter


R_SET
R
V+
V−
+V_IN
C1*
OP AMP

TL/H/5697-9

*Use minimum value required to ensure stability of protected device. This minimizes inrush current to a direct short.

Schematic Diagram


V+
Q4
Q5
Q6
Q3
C1
50 pF
Q2
Q1
R
V−

TL/H/5697-11

National Semiconductor Corporation

LM136-2.5/LM236-2.5/LM336-2.5V Reference Diode

General Description

The LM136-2.5/LM236-2.5 and LM336-2.5 integrated circuits are precision 2.5V shunt regulator diodes. These monolithic IC voltage references operate as a low-temperature-coefficient 2.5V zener with 0.2Ω dynamic impedance. A third terminal on the LM136-2.5 allows the reference voltage and temperature coefficient to be trimmed easily.

The LM136-2.5 series is useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from 5V logic supplies. Further, since the LM136-2.5 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

The LM136-2.5 is rated for operation over −55°C to +125°C while the LM236-2.5 is rated over a −25°C to +85°C temperature range.

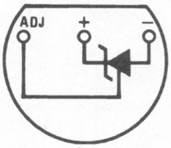
Both are packaged in a TO-46 package. The LM336-2.5 is rated for operation over a 0°C to +70°C temperature range and is available in a TO-92 plastic package.

Features

- Low temperature coefficient
- Wide operating current of 400 μA to 10 mA
- 0.2Ω dynamic impedance
- ±1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

Connection Diagrams

TO-92
Plastic Package

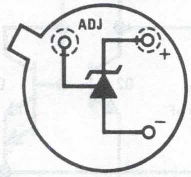


TL/H/5715–8

Bottom View

Order Number LM336Z-2.5
or LM336BZ-2.5
See NS Package Number Z03A

TO-46
Metal Can Package

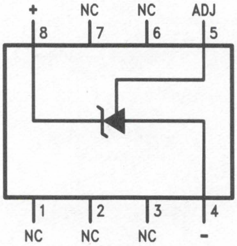


TL/H/5715–20

Bottom View

Order Number LM136H-2.5,
LM236H-2.5, LM336H-2.5,
LM136AH-2.5 or LM236AH-2.5
See NS Package Number H03H

SO Package



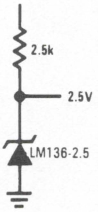
TL/H/5715–12

Top View

Order Number LM336M-2.5
or LM336BM-2.5
See NS Package Number M08A

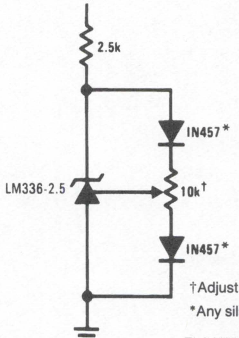
Typical Applications

2.5V Reference



TL/H/5715–9

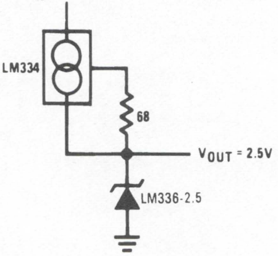
2.5V Reference with Minimum Temperature Coefficient



†Adjust to 2.490V
*Any silicon signal diode

TL/H/5715–10

Wide Input Range Reference



TL/H/5715–11

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Reverse Current	15 mA
Forward Current	10 mA
Storage Temperature	−60°C to +150°C
Operating Temperature Range	
LM136	−55°C to +150°C
LM236	−25°C to +85°C
LM336	0°C to +70°C

Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM136A-2.5/LM236A-2.5 LM136-2.5/LM236-2.5			LM336B-2.5 LM336-2.5			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1$ mA							
	LM136/LM236/LM336	2.440	2.490	2.540	2.390	2.490	2.590	V
	LM136A/LM236A, LM336B	2.465	2.490	2.515	2.440	2.490	2.540	V
Reverse Breakdown Change With Current	$T_A = 25°C$, $400\ \mu A \leq I_R \leq 10$ mA		2.6	6		2.6	10	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1$ mA		0.2	0.6		0.2	1	Ω
Temperature Stability (Note 2)	V_R Adjusted to 2.490V $I_R = 1$ mA, *(Figure 2)*							
	$0°C \leq T_A \leq 70°C$ (LM336)					1.8	6	mV
	$-25°C \leq T_A \leq +85°C$ (LM236)		3.5	9				mV
	$-55°C \leq T_A \leq +125°C$ (LM136)		12	18				mV
Reverse Breakdown Change With Current	$400\ \mu A \leq I_R \leq 10$ mA		3	10		3	12	mV
Reverse Dynamic Impedance	$I_R = 1$ mA		0.4	1		0.4	1.4	Ω
Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1$ mA		20			20		ppm

Note 1: Unless otherwise specified, the LM136-2.5 is specified from $-55°C \leq T_A \leq +125°C$, the LM236-2.5 from $-25°C \leq T_A \leq +85°C$ and the LM336-2.5 from $0°C \leq T_A \leq +70°C$.

Note 2: Temperature stability for the LM336 and LM236 family is guaranteed by design. Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels. Stability is defined as the maximum change in V_{ref} from 25°C to T_A (min) or T_A (max).

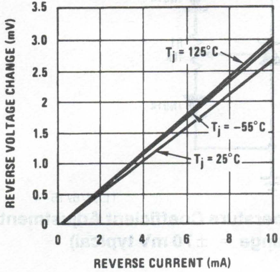
Note 3: For elevated temperature operation, T_j max is:

LM136	150°C
LM236	125°C
LM336	100°C

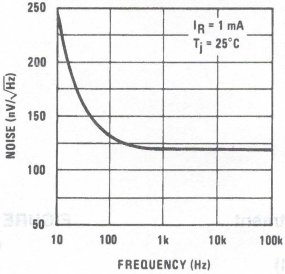
Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4″ leads) 170°C/W (0.125″ lead)	440°C/W	165°C/W
θ_{ja} (Junction to Case)	n/a	80°C/W	n/a

Typical Performance Characteristics

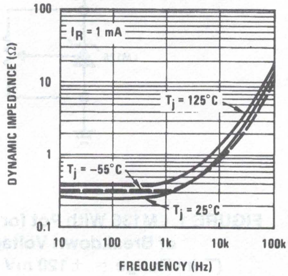
Reverse Voltage Change



Zener Noise Voltage

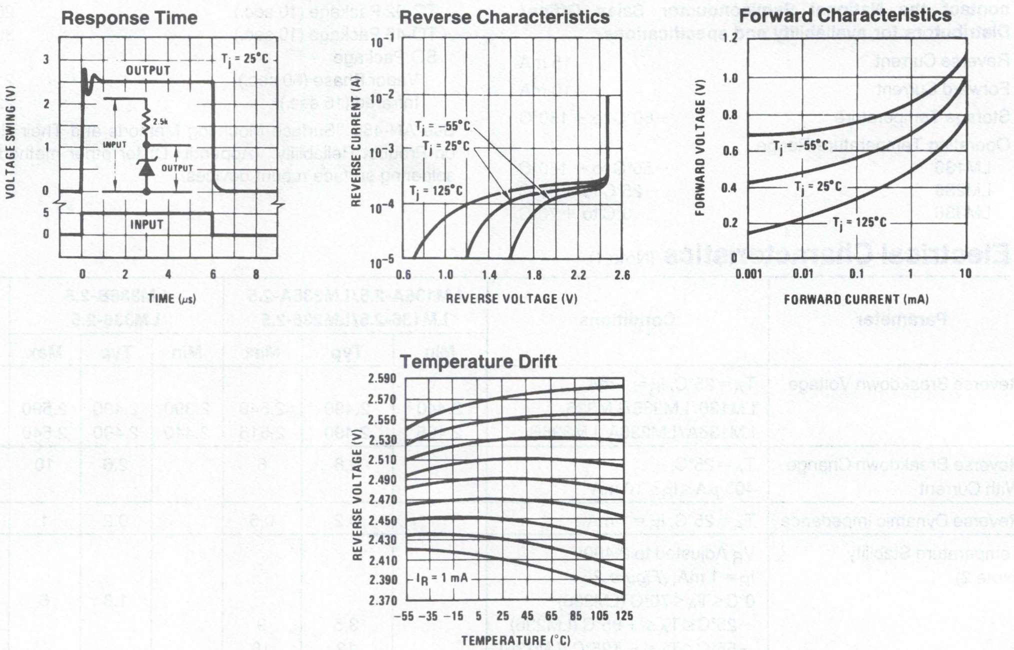


Dynamic Impedance



TL/H/5715–2

Typical Performance Characteristics (Continued)



TL/H/5715–3

Application Hints

The LM136 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

Figure 1 shows an LM136 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device tolerance and inaccuracies in buffer circuitry.

If minimum temperature coefficient is desired, two diodes can be added in series with the adjustment potentiometer as shown in *Figure 2.* When the device is adjusted to 2.490V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136. It is usually sufficient to mount the diodes near the LM136 on the printed circuit board. The absolute resistance of R1 is not critical and any value from 2k to 20k will work.

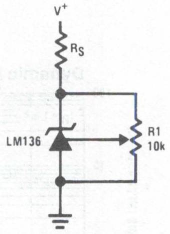
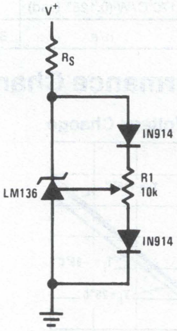


FIGURE 1. LM136 With Pot for Adjustment of Breakdown Voltage (Trim Range = ± 120 mV typical)

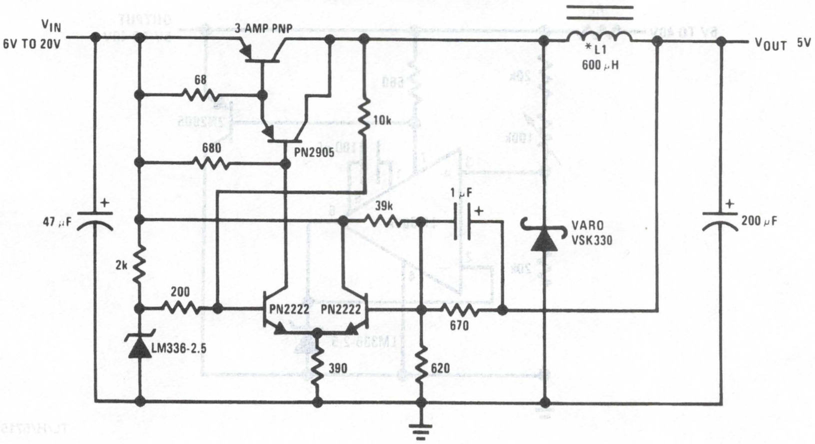


TL/H/5715–4

FIGURE 2. Temperature Coefficient Adjustment (Trim Range = ±70 mV typical)

Typical Applications (Continued)

Low Cost 2 Amp Switching Regulator†

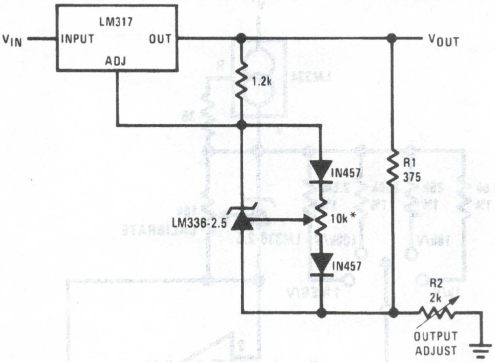

VIN
6V TO 20V
3 AMP PNP
68
680
PN2905
10k
*L1
600 μH
VOUT 5V
47 μF
+
2k
200
LM336-2.5
PN2222
PN2222
390
620
39k
1 μF
+
670
VARO
VSK330
200 μF
+

*L1 60 turns #16 wire on Arnold Core A-254168-2

†Efficiency ≈ 80%

TL/H/5715–5

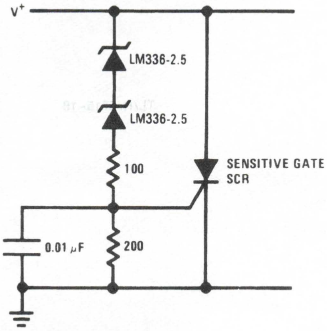
Precision Power Regulator with Low Temperature Coefficient


LM317
VIN
INPUT
OUT
ADJ
VOUT
1.2k
IN457
LM336-2.5
10k*
IN457
R1
375
R2
2k
OUTPUT
ADJUST

*Adjust for 3.75V across R1

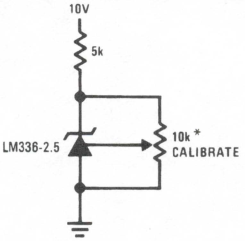
TL/H/5715–13

5V Crowbar


V+
LM336-2.5
LM336-2.5
100
SENSITIVE GATE
SCR
0.01 μF
200

TL/H/5715–14

Trimmed 2.5V Reference with Temperature Coefficient Independent of Breakdown Voltage

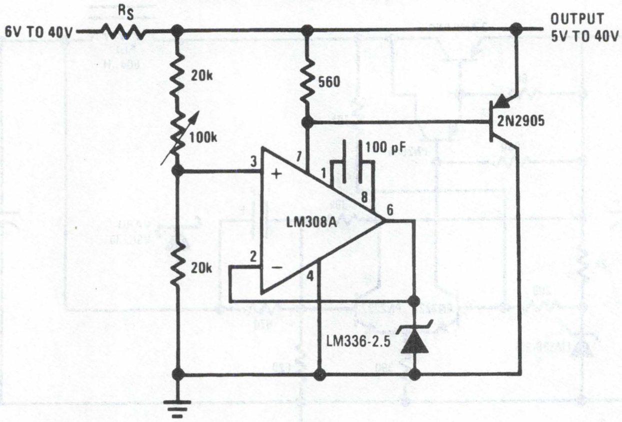

10V
5k
LM336-2.5
10k*
CALIBRATE

*Does not affect temperature coefficient

TL/H/5715–15

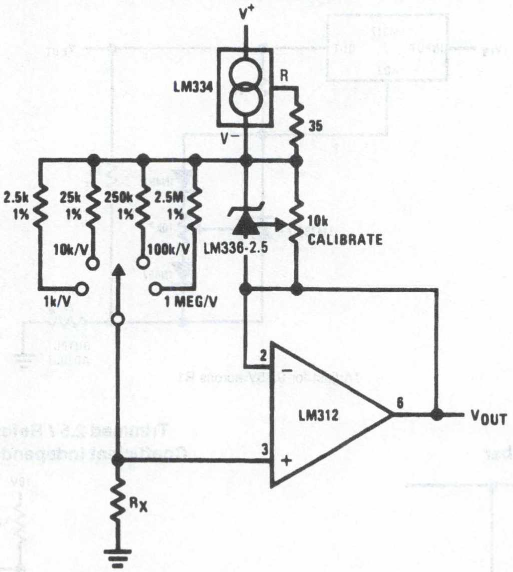
Typical Applications (Continued)

Adjustable Shunt Regulator


R_S
6V TO 40V
OUTPUT
5V TO 40V
20k
100k
20k
560
2N2905
100 pF
LM308A
3
2
7
1
8
6
4
+
−
LM336-2.5

TL/H/5715-6

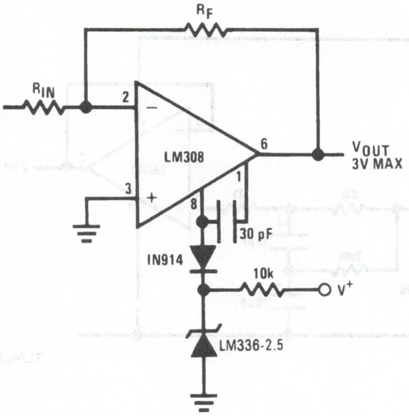
Linear Ohmmeter


V+
LM334
R
V−
35
2.5k
1%
25k
1%
250k
1%
2.5M
1%
10k/V
100k/V
1k/V
1 MEG/V
LM336-2.5
10k
CALIBRATE
LM312
2
3
6
−
+
V_OUT
R_X

TL/H/5715-16

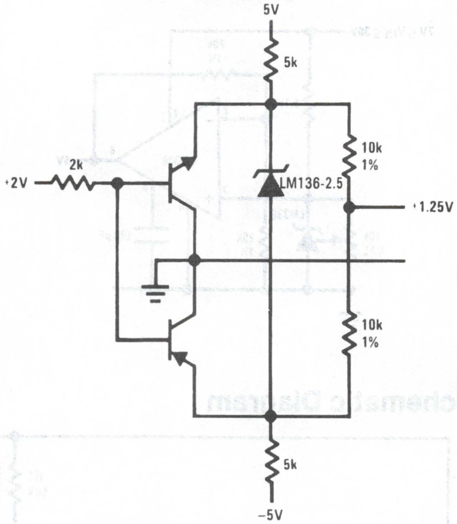
Typical Applications (Continued)

Op Amp with Output Clamped


R$_F$
R$_{IN}$
2
3
6
8
1
LM308
V$_{OUT}$
3V MAX
30 pF
IN914
10k
V$^+$
LM336-2.5

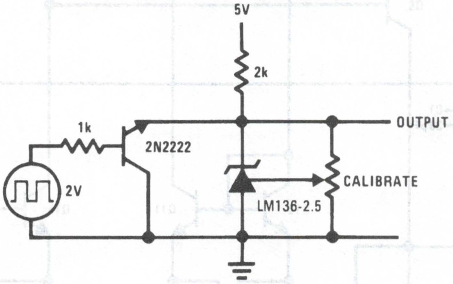
TL/H/5715-17

Bipolar Output Reference


5V
5k
10k
1%
+2V
2k
LM136-2.5
+1.25V
10k
1%
5k
−5V

TL/H/5715-18

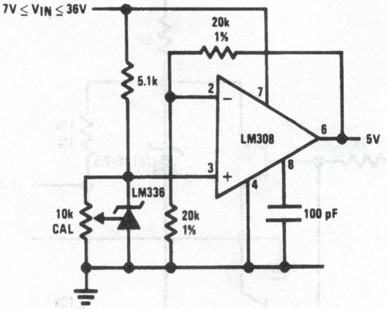
2.5V Square Wave Calibrator


5V
2k
1k
2N2222
OUTPUT
2V
CALIBRATE
LM136-2.5

TL/H/5715-19

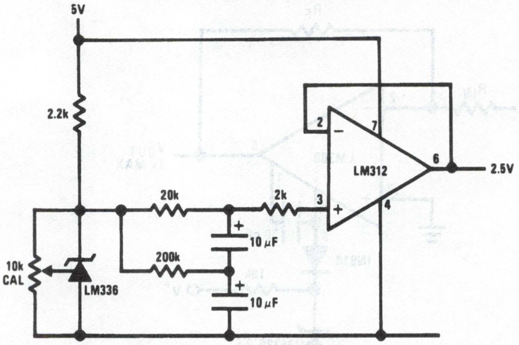
Typical Applications (Continued)

5V Buffered Reference



7V ≤ VIN ≤ 36V
20k
1%
5.1k
2
7
−
LM308
6
5V
3
+
8
4
LM336
10k
CAL
20k
1%
100 pF

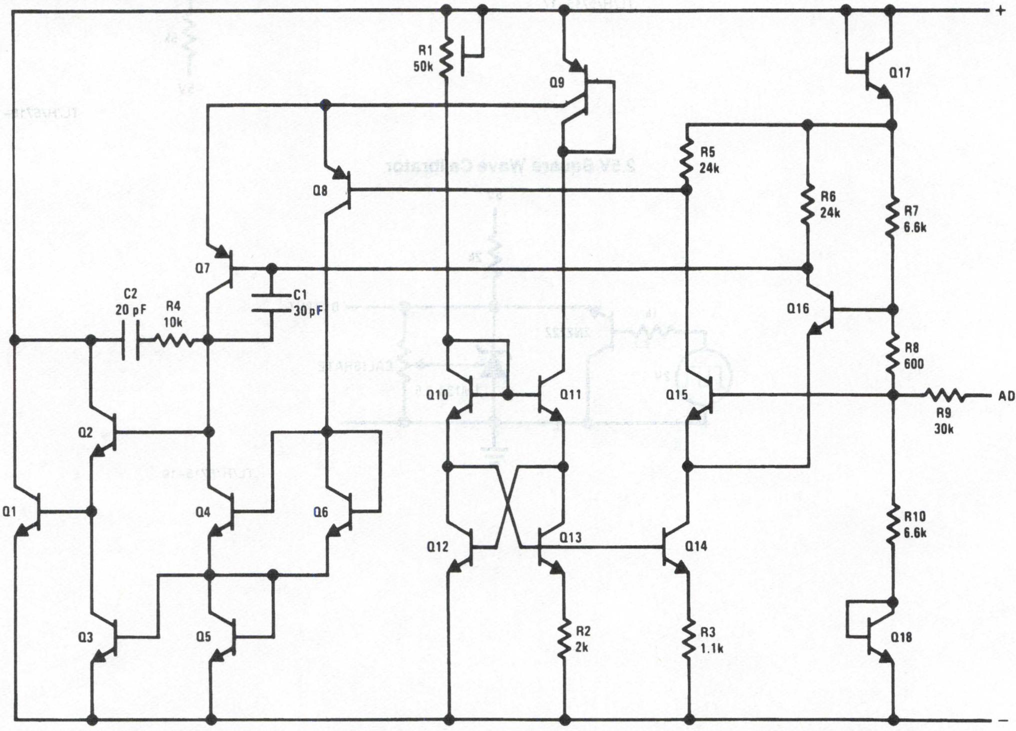
Low Noise Buffered Reference



5V
2.2k
2
−
7
LM312
6
2.5V
20k
2k
3
+
4
10 μF
200k
10k
CAL
LM336
10 μF

TL/H/5715-7

Schematic Diagram



+
R1
50k
Q9
Q17
R5
24k
Q8
R6
24k
R7
6.6k
Q7
C2
20 pF
R4
10k
C1
30 pF
Q16
R8
600
Q10
Q11
Q15
ADJ
R9
30k
Q2
Q1
Q4
Q6
R10
6.6k
Q12
Q13
Q14
Q3
Q5
R2
2k
R3
1.1k
Q18
−

TL/H/5715-1

National Semiconductor Corporation

LM136-5.0/LM236-5.0/LM336-5.0, 5.0V Reference Diode

General Description

The LM136-5.0/LM236-5.0/LM336-5.0 integrated circuits are precision 5.0V shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient 5.0V zener with 0.6Ω dynamic impedance. A third terminal on the LM136-5.0 allows the reference voltage and temperature coefficient to be trimmed easily.

The LM136-5.0 series is useful as a precision 5.0V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 5.0V makes it convenient to obtain a stable reference from low voltage supplies. Further, since the LM136-5.0 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

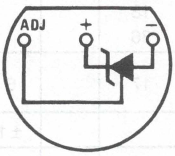
The LM136-5.0 is rated for operation over −55°C to +125°C while the LM236-5.0 is rated over a −25°C to +85°C temperature range. Both are packaged in a TO-46 package. The LM336-5.0 is rated for operation over a 0°C to +70°C temperature range and is available in a TO-92 plastic package. For applications requiring 2.5V see LM136-2.5.

Features

- Adjustable 4V to 6V
- Low temperature coefficient
- Wide operating current of 600 μA to 10 mA
- 0.6Ω dynamic impedance
- ± 1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

Connection Diagrams

TO-92
Plastic Package

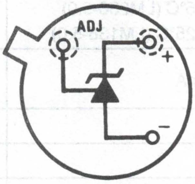


TL/H/5716-4

Bottom View

Order Number LM336Z-5.0 or LM336BZ-5.0
See NS Package Number Z03A

TO-46
Metal Can Package

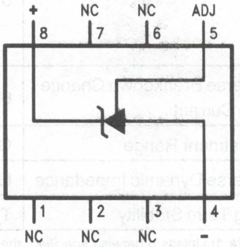


TL/H/5716-5

Bottom View

Order Number LM136H-5.0, LM236H-5.0, LM136AH-5.0 or LM236AH-5.0
See NS Package Number H03H

SO Package

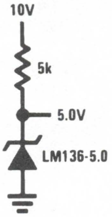


TL/H/5716-7

Order Number LM336M-5.0 or LM236BM-5.0
See NS Package Number H03H

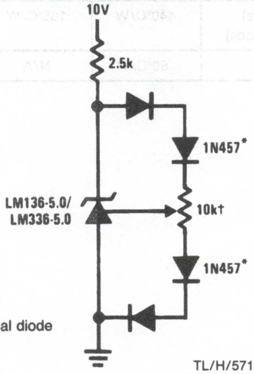
Typical Applications

5.0V Reference



TL/H/5716-1

5.0V Reference with Minimum Temperature Coefficient

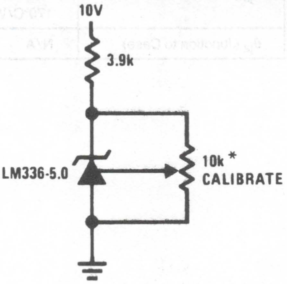


†Adjust to 5.00V

*Any silicon signal diode

TL/H/5716-15

Trimmed 4V to 6V Reference with Temperature Coefficient Independent of Breakdown Voltage



TL/H/5716-3

*Does not affect temperature coefficient

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Reverse Current	15mA
Forward Current	10mA
Storage Temperature	−60°C to +150°C
Operating Temperature Range	
LM136-5.0	−55°C to +150°C
LM236-5.0	−25°C to +85°C
LM336-5.0	0°C to +70°C
Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM136A-5.0/LM236A-5.0 LM136-5.0/LM236-5.0 Min	Typ	Max	LM336B-5.0 LM336-5.0 Min	Typ	Max	Units
Reverse Breakdown Voltage	$T_A=25°C$, $I_R=1$ mA							
	LM136-5.0/LM236-5.0/LM336-5.0	4.9	5.00	5.1	4.8	5.00	5.2	V
	LM136A-5.0/LM236A-5.0, LM336B-5.0	4.95	5.00	5.05	4.90	5.00	5.1	V
Reverse Breakdown Change With Current	$T_A=25°C$, $600\ \mu A \leq I_R \leq 10$ mA		6	12		6	20	mV
Reverse Dynamic Impedance	$T_A=25°C$, $I_R=1$ mA		0.6	1.2		0.6	2	Ω
Temperature Stability	V_R Adjusted 5.00V $I_R=1$ mA, (*Figure 2*)							
	$0°C \leq T_A \leq 70°C$ (LM336-5.0)					4	12	mV
	$-25°C \leq T_A \leq +85°C$ (LM236-5.0)		7	18				mV
	$-55°C \leq T_A \leq +125°C$ (LM136-5.0)		20	36				mV
Reverse Breakdown Change With Current	$600\ \mu A \leq I_R \leq 10$ mA		6	17		6	24	mV
Adjustment Range	Circuit of *Figure 1*		±1			±1		V
Reverse Dynamic Impedance	$I_R = 1$ mA		0.8	1.6		0.8	2.5	Ω
Long Term Stability	$T_A=25°C \pm 0.1°C$, $I_R=1$ mA		20			20		ppm

Note 1: Unless otherwise specified, the LM136-5.0 is specified from $-55°C \leq T_A \leq +125°C$, the LM236-5.0 from $-25°C \leq T_A \leq +85°C$ and the LM336-5.0 from $0°C \leq T_A \leq +70°C$.

Note 2: Temperature stability for the LM336 and LM236 family is guaranteed by design. Design limits are guaranteed (but not 100% percent production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels. Stability is defined as the maximum charge in V_{REF} from 25°C to T_A(min) or T_A(max).

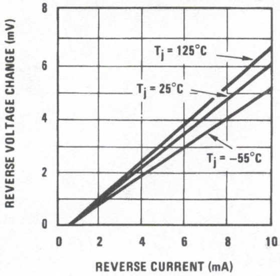
Note 3: For elevated temperature operation, T_j max is:

LM136	150°C
LM236	125°C
LM336	100°C

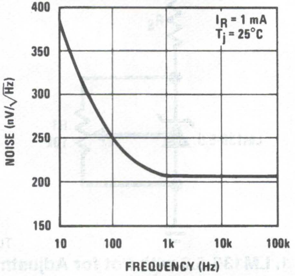
Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4″ Leads) 170°C/W (0.125″ Leads)	440°C/W	165°C/W
θ_{ja} (Junction to Case)	N/A	80°C/W	N/A

Typical Performance Characteristics

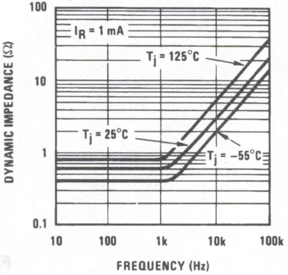
Reverse Voltage Change



Zener Noise Voltage

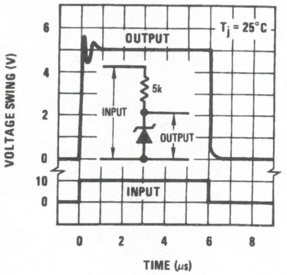


Dynamic Impedance

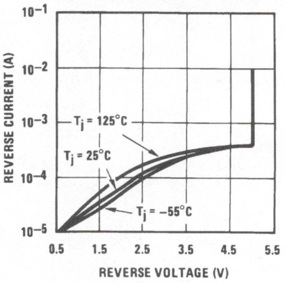


TL/H/5716-2

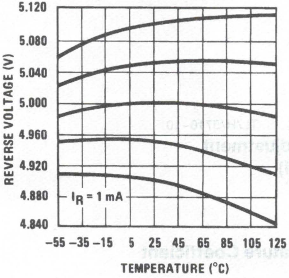
Response Time



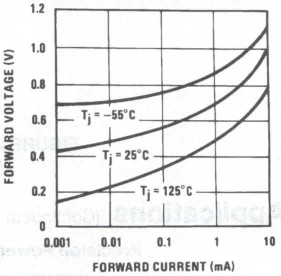
Reverse Characteristics



Temperature Drift



Forward Characteristics



TL/H/5716-8

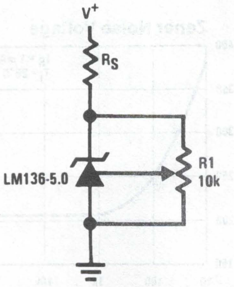
Application Hints

The LM136-5.0 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

Figure 1 shows an LM136-5.0 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device tolerance and inaccuracies in buffer circuitry.

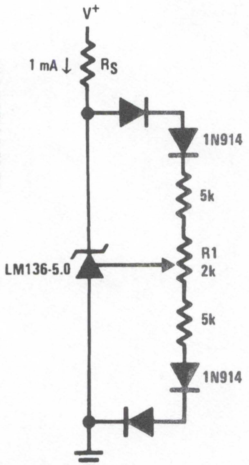
If minimum temperature coefficient is desired, four diodes can be added in series with the adjustment potentiometer as shown in *Figure 2.* When the device is adjusted to 5.00V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136-5.0. It is usually sufficient to mount the diodes near the LM136-5.0 on the printed circuit board. The absolute resistance of the network is not critical and any value from 2k to 20k will work. Because of the wide adjustment range, fixed resistors should be connected in series with the pot to make pot setting less critical.

Application Hints (Continued)


V+
RS
LM136-5.0
R1
10k

TL/H/5716–9

FIGURE 1. LM136-5.0 with Pot for Adjustment of Breakdown Voltage (Trim Range = ±1.0V Typical)

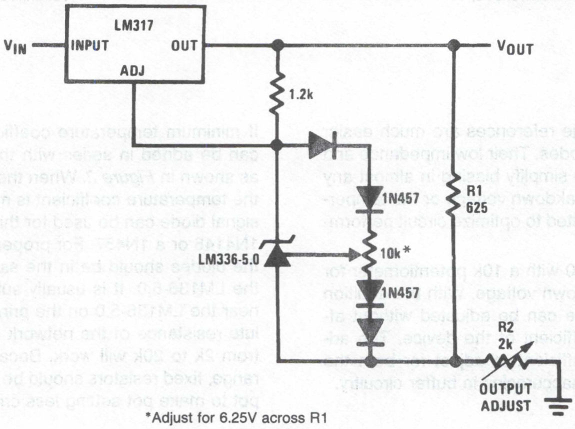

V+
1 mA
RS
1N914
5k
LM136-5.0
R1
2k
5k
1N914

TL/H/5716–10

FIGURE 2. Temperature Coefficient Adjustment (Trim Range = ±0.5V Typical)

Typical Applications (Continued)

Precision Power Regulator with Low Temperature Coefficient

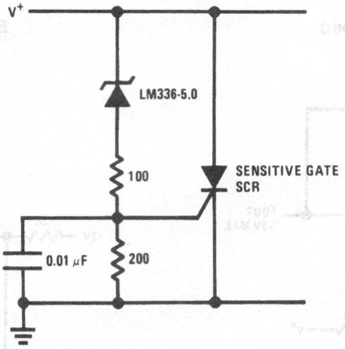

LM317
VIN
INPUT
OUT
ADJ
VOUT
1.2k
1N457
R1
625
LM336-5.0
10k*
1N457
R2
2k
OUTPUT ADJUST

*Adjust for 6.25V across R1

TL/H/5716–11

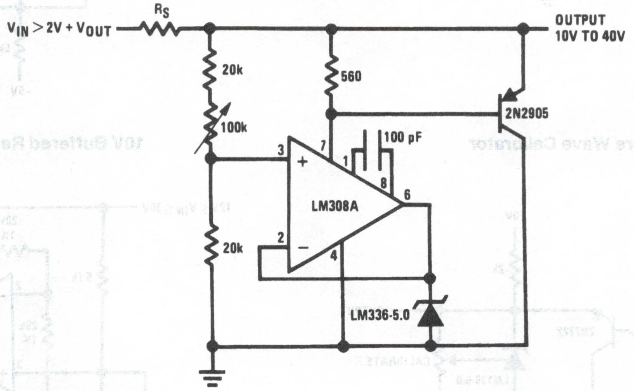
Typical Applications (Continued)

5V Crowbar


V+
LM336-5.0
100
SENSITIVE GATE
SCR
0.01 μF
200

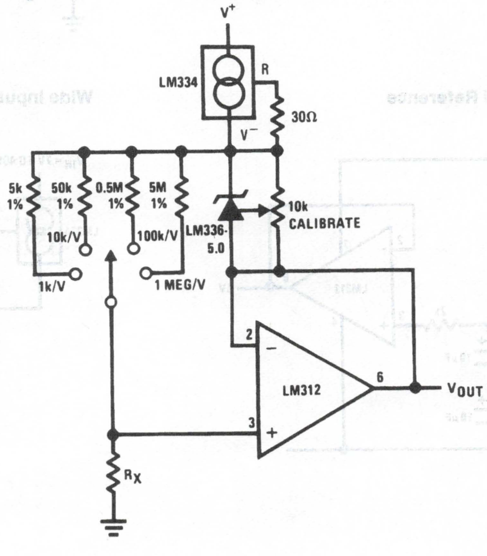
TL/H/5716-12

Adjustable Shunt Regulator


RS
VIN > 2V + VOUT
OUTPUT
10V TO 40V
20k
560
2N2905
100k
100 pF
3
7
1
8
6
LM308A
2
4
20k
LM336-5.0

TL/H/5716-13

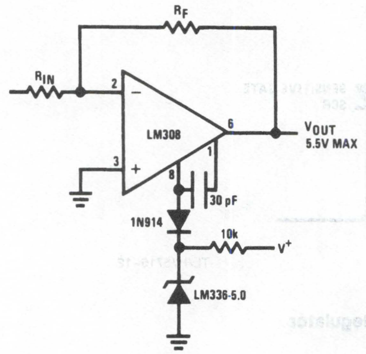
Linear Ohmmeter


V+
LM334
R
30Ω
V−
5k
1%
50k
1%
0.5M
1%
5M
1%
10k/V
100k/V
LM336-
5.0
10k
CALIBRATE
1k/V
1 MEG/V
2
LM312
6
VOUT
3
RX

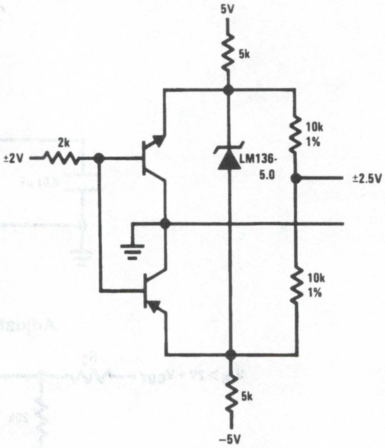
TL/H/5716-14

Typical Applications (Continued)

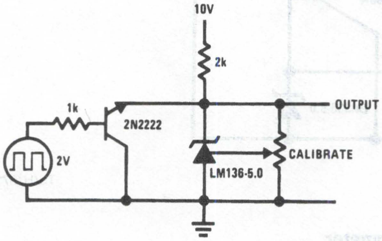
Op Amp with Output Clamped


R_F
R_IN
2
−
LM308
+
3
6
1
8
30 pF
V_OUT
5.5V MAX
1N914
10k
V+
LM336-5.0

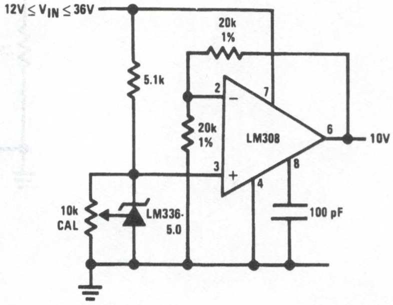
Bipolar Output Reference


5V
5k
10k
1%
LM136-
5.0
±2V
2k
±2.5V
10k
1%
5k
−5V

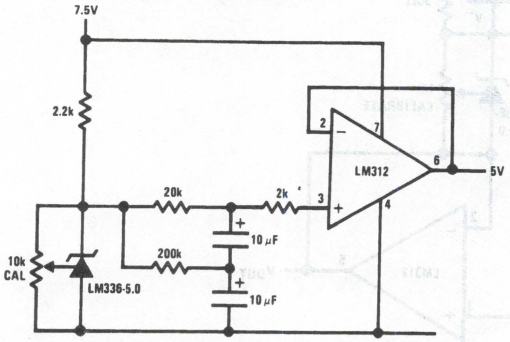
5.0V Square Wave Calibrator


10V
2k
1k
2N2222
OUTPUT
2V
CALIBRATE
LM136-5.0

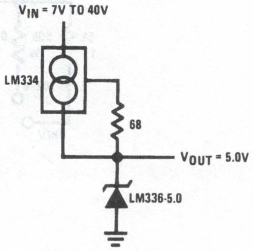
10V Buffered Reference


12V ≤ V_IN ≤ 36V
20k
1%
5.1k
2
−
7
20k
1%
LM308
6
10V
3
+
8
4
10k
CAL
LM336-
5.0
100 pF

Low Noise Buffered Reference

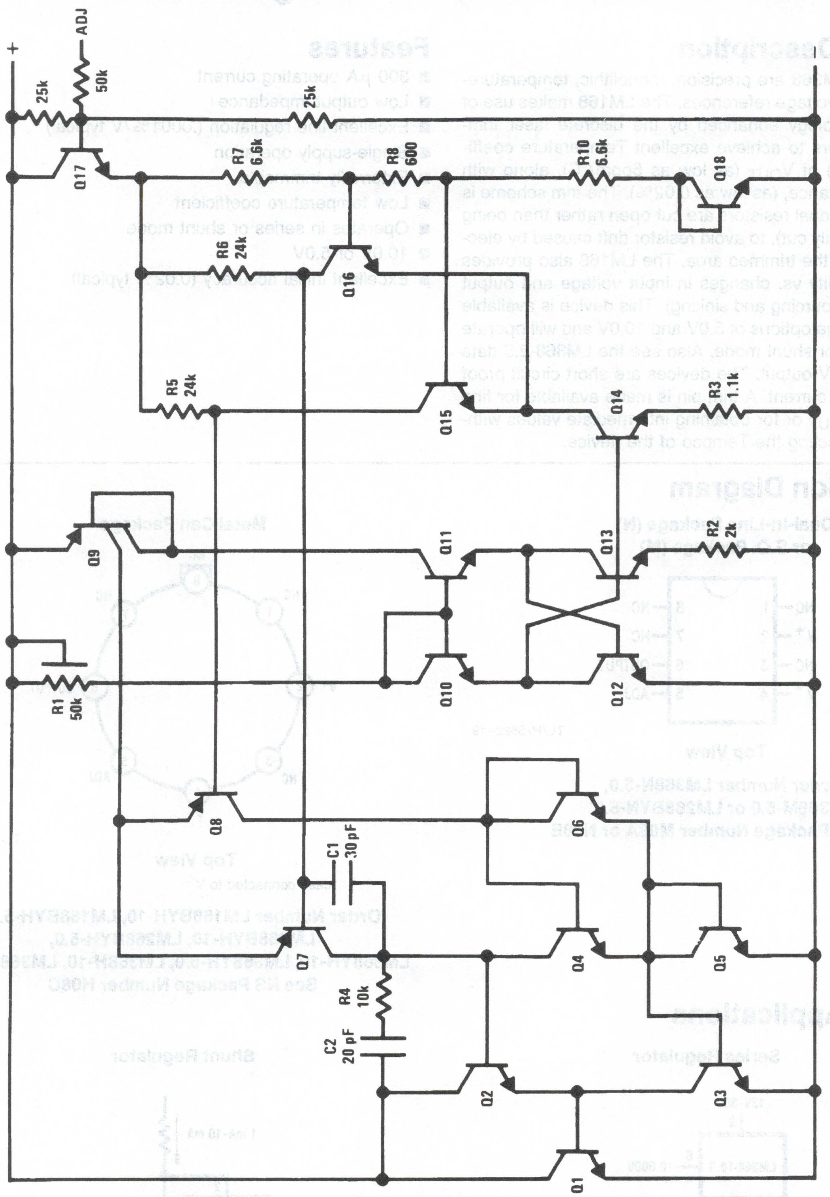

7.5V
2.2k
2
−
7
LM312
6
5V
20k
2k
3
+
4
10 μF
10k
CAL
200k
LM336-5.0
10 μF

Wide Input Range Reference


V_IN = 7V TO 40V
LM334
68
V_OUT = 5.0V
LM336-5.0

TL/H/5716-6

Schematic Diagram


+
ADJ
25k
50k
25k
Q17
R7
6.6k
R8
600
R10
6.6k
Q18
R6
24k
Q16
R5
24k
Q15
Q14
R3
1.1k
Q9
Q11
Q13
R2
2k
R1
50k
Q10
Q12
Q8
Q6
C1
30 pF
Q7
Q4
Q5
R4
10k
C2
20 pF
Q2
Q3
Q1

TL/H/5716-16

National Semiconductor Corporation

PRELIMINARY

LM168/LM268/LM368 Precision Voltage Reference

General Description

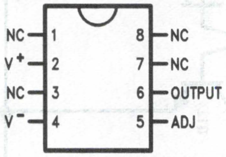
The LM168/LM368 are precision, monolithic, temperature-compensated voltage references. The LM168 makes use of thin-film technology enhanced by the discrete laser trimming of resistors to achieve excellent Temperature coefficient (Tempco) of V_{OUT} (as low as 5ppm/°C), along with tight initial tolerance, (as low as 0.02%). The trim scheme is such that individual resistors are cut open rather than being trimmed (partially cut), to avoid resistor drift caused by electromigration in the trimmed area. The LM168 also provides excellent stability vs. changes in input voltage and output current (both sourcing and sinking). This device is available in output voltage options of 5.0V and 10.0V and will operate in both series or shunt mode. Also see the LM368-2.5 data sheet for a 2.5V output. The devices are short circuit proof when sourcing current. A trim pin is made available for fine trimming of V_{OUT} or for obtaining intermediate values without greatly affecting the Tempco of the device.

Features

- 300 μA operating current
- Low output impedance
- Excellent line regulation (.0001%/V typical)
- Single-supply operation
- Externally trimmable
- Low temperature coefficient
- Operates in series or shunt mode
- 10.0V or 5.0V
- Excellent initial accuracy (0.02% typical)

Connection Diagram

Dual-In-Line Package (N) or S.O. Package (M)

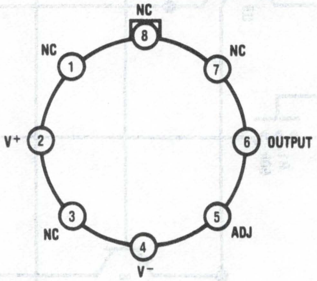


TL/H/5522-19

Top View

Order Number LM368N-5.0, LM368M-5.0 or LM268BYN-5.0
See NS Package Number M08A or N08E

Metal Can Package



TL/H/5522-1

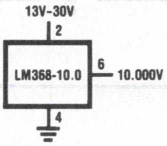
Top View

*case connected to V−

Order Number LM168BYH-10, LM168BYH-5.0, LM268BYH-10, LM268BYH-5.0, LM368YH-10, LM368YH-5.0, LM368H-10, LM368H-5.0
See NS Package Number H08C

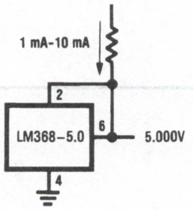
Typical Applications

Series Regulator



TL/H/5522-2

Shunt Regulator



TL/H/5522-3

Absolute Maximum Ratings (Note 8)

Input Voltage (Series Mode)	35V
Reverse Current (Shunt Mode)	50 mA
Power Dissipation	600 mW
Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	
LM168	−55°C to +125°C
LM268	−40°C to +85°C
LM368	0°C to +70°C

Soldering Information	
DIP (N) Package, 10 sec.	+260°C
TO-5 (H) Package, 10 sec.	+300°C
SO (M) Package, Vapor Phase (60 sec.)	+215°C
Infrared (15 sec.)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM168/LM268/LM368			Units (Max. unless noted)
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OUT} Error: LM168B, LM268B		±0.02	±0.05		%
LM368		±0.02	±0.1		%
Line Regulation	$(V_{OUT}+3V) \le V_{IN} \le 30V$	±0.0001	±0.0005		%/V
Load Regulation	$0\ mA \le I_{SOURCE} \le 10\ mA$	±0.0003	±0.001		%/mA
(Note 4)	$-10\ mA \le I_{SINK} \le 0\ mA$	±0.003	±0.008		%/mA
Thermal Regulation	T = 20 mS (Note 5)	±0.005	±0.01		%/100 mW
Quiescent Current		250	350		µA
Change of Quiescent Current vs. V_{IN}	$(V_{OUT}+3V) \le V_{IN} \le 30V$	3	5		µA/V
Temperature Coefficient					
of V_{OUT} (see graph): LM168BY	$-55°C \le T_A \le 125°C$	±5	±10		ppm/°C
(Note 6) LM268BY	$-40°C \le T_A \le 85°C$	±7.5	±15		ppm/°C
LM368Y	$0°C \le T_A \le 70°C$	±11	±20		ppm/°C
LM368	$0°C \le T_A \le 70°C$	±15		±30	ppm/°C
Short Circuit Current	$V_{OUT} = 0$	30	70	100	mA
Noise: 10.0V: 0.1 - 10Hz		30			uVp-p
100Hz - 10 kHz		1100			nV/√Hz
6.2V: 0.1 - 10Hz		20			uVp-p
100Hz - 10 kHz		700			nV/√Hz
5.0V: 0.1 - 10Hz		16			uVp-p
100Hz - 10 kHz		575			nV/√Hz
V_{OUT} Adjust Range: 10.000V	$0V \le V_{PIN5} \le V_{OUT}$	4.5-17.0		6.0-15.5	V min.
5.000V		4.4-7.0		4.5-6.0	V min.

Note 1: Unless otherwise noted, these specifications apply: $T_A = 25°C$, $V_{IN} = 15V$, $I_{LOAD} = 0$, $0 \le C_L \le 200\ pF$, Circuit is operating in Series Mode. Or, circuit is operating in Shunt Mode, $V_{IN} = +15V$ or $V_{IN} = V_{OUT}$, $TA = +25°C$, $I_{LOAD} = -1.0\ mA$, $0 \le C_L \le 200\ pF$.

Note 2: Tested Limits are guaranteed and 100% tested in production.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: The LM168 has a Class B output, and will exhibit transients at the crossover point. This point occurs when the device is asked to sink approximately 120 µA. In some applications it may be advantageous to preload the output to either V_{IN} or Ground, to avoid this crossover point.

Note 5: Thermal Regulation is defined as the change in the output Voltage at a time T after a step change in power dissipation of 100 mW.

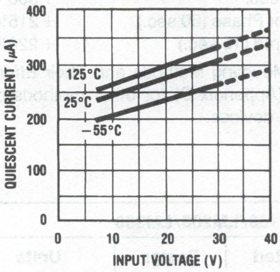
Note 6: Temperature Coefficient of V_{OUT} is defined as the worst case delta-V_{OUT} measured at Specified Temperatures divided by the total span of the Specified Temperature Range (See graphs). There is no guarantee that the Specified Temperatures are exactly at the minimum or maximum deviation.

Note 7: In metal can (H), θ_{J-C} is 75°C/W and θ_{J-A} is 150°C/W. In plastic DIP, θ_{J-A} is 160°C/W. In S0-8, θ_{J-A} is 180°C/W, in TO-92, θ_{J-A} is 160°C/W.

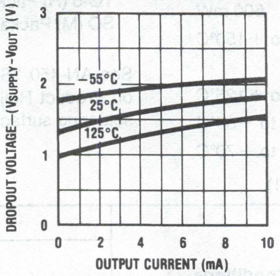
Note 8: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its Rated Operating Conditions (see Note 1 and Conditions).

Typical Performance Characteristics (Note 1)

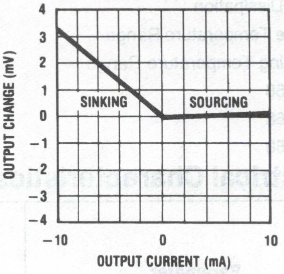
Quiescent Current vs. Input Voltage and Temperature



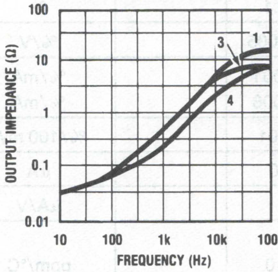
Dropout Voltage vs. Output Current (Series Mode Sourcing Current)



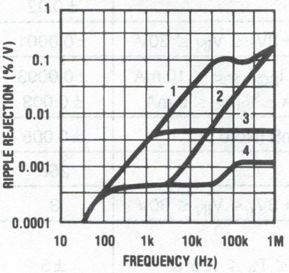
Output Change vs. Output Current



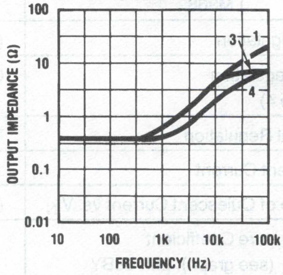
Output Impedance vs. Frequency (Sourcing Current)



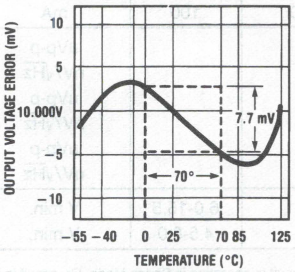
Ripple Rejection vs. Frequency



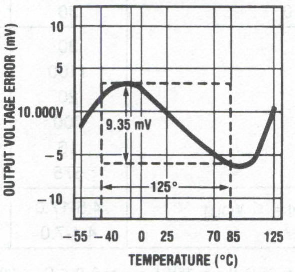
Output Impedance vs. Frequency (Sinking Current)



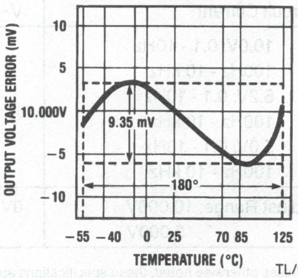
Temperature Coefficient: LM368-10 (Curve A)



Temperature Coefficient: LM268-10 (Curve B)



Temperature Coefficient: LM168-10 (Curve C)



TL/H/5522-4

Typical Temperature Coefficient Calculations:

LM368-10 (see Curve A)

T.C. = 7.7 mV/(70° × 10V)
= 11 × 10E-6 = 11ppm/°C

LM268-10 (see Curve B)

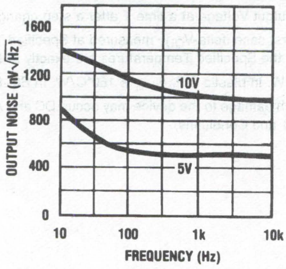
T.C. = 9.35 mV/(125° × 10V)
= 7.5 × 10E-6 = 7.5ppm/°C

LM168-10 (see Curve C)

T.C. = 9.35 mV/(180° × 10V)
= 5.2 × 10E-6 = 5.2ppm/°C

Output Noise vs. Frequency

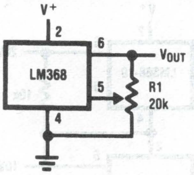
(1) LM368 alone.
(2) with 0.01 μf Mylar, Trim to Gnd.
(3) with 10Ω in series with 10 μf, V_{OUT} to Gnd.
(4) with Both.



TL/H/5522-5

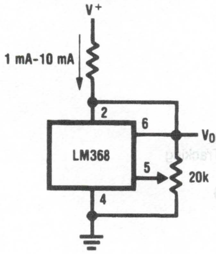
Typical Applications

Wide Range Trimmable Regulator


V+
2
6
VOUT
LM368
5
R1
20k
4

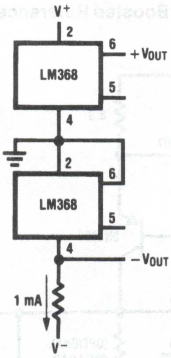
TL/H/5522-7

Adjustable Zener


V+
1 mA-10 mA
2
6
VOUT
LM368
5
20k
4

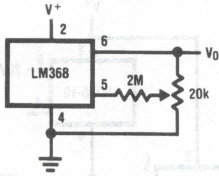
TL/H/5522-9

± Reference


V+
2
6
+VOUT
LM368
5
4
2
6
LM368
5
4
−VOUT
1 mA
V−

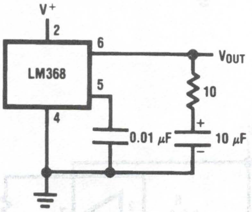
TL/H/5522-11

Narrow Range Trimmable Regulator (±1% min.)


V+
2
6
VOUT
LM368
5
2M
20k
4

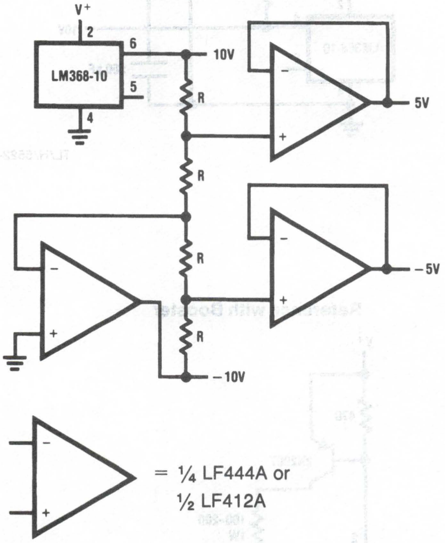
TL/H/5522-8

Improved Noise Performance


V+
2
6
VOUT
LM368
5
10
4
+
0.01 μF
10 μF

TL/H/5522-10

±10V, ±5V References

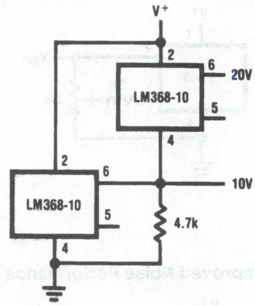

V+
2
6
10V
LM368-10
5
4
R
−
+
5V
R
−
R
−
+
+
−5V
R
−10V
−
+
= ¼ LF444A or
½ LF412A

TL/H/5522-12

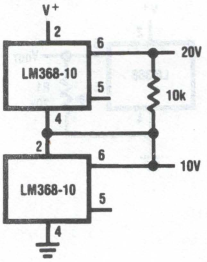
R = Thin Film Resistor Network, ±0.05% Matching and 5ppm Tracking (Beckman 694-3-R-10K-A), (Caddock T-914-10K-100-05) or similar.

Typical Applications (Continued)

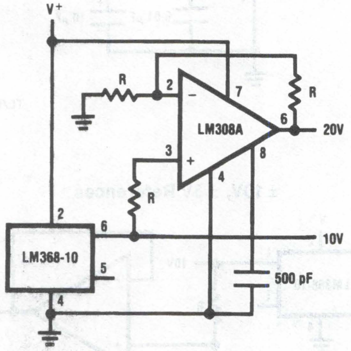
Multiple Output Voltages


V+
2
6
20V
LM368-10
5
4
2
6
10V
LM368-10
5
4.7k
4

TL/H/5522-13


V+
2
6
20V
LM368-10
5
10k
4
2
6
10V
LM368-10
5
4

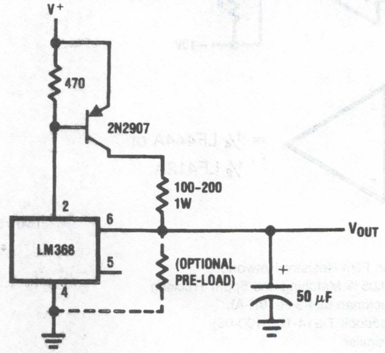
TL/H/5522-14


V+
R
2
−
7
R
LM308A
6
20V
3
+
8
4
R
2
6
10V
LM368-10
5
500 pF
4

R= Thin Film Resistor Network
0.05% Matching and 5ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
or similar.

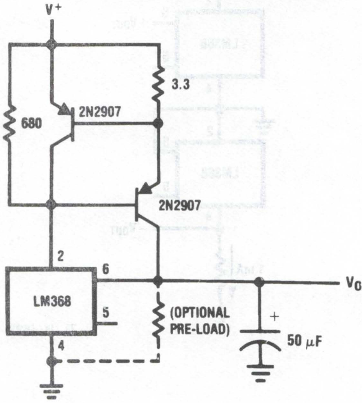
TL/H/5522-15

Reference with Booster


V+
470
2N2907
100-200
1W
2
6
VOUT
LM368
5
(OPTIONAL
PRE-LOAD)
+
50 μF
4

TL/H/5522-16

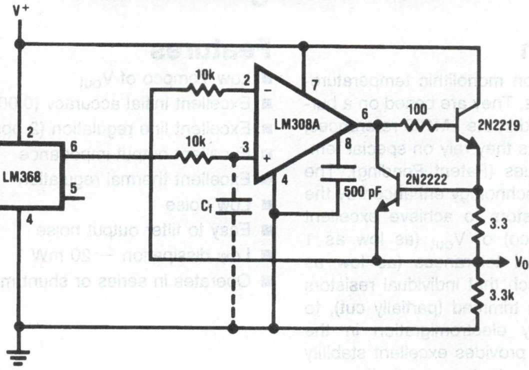
100 mA Boosted Reference


V+
3.3
680
2N2907
2N2907
2
6
VOUT
LM368
5
(OPTIONAL
PRE-LOAD)
+
50 μF
4

TL/H/5522-17

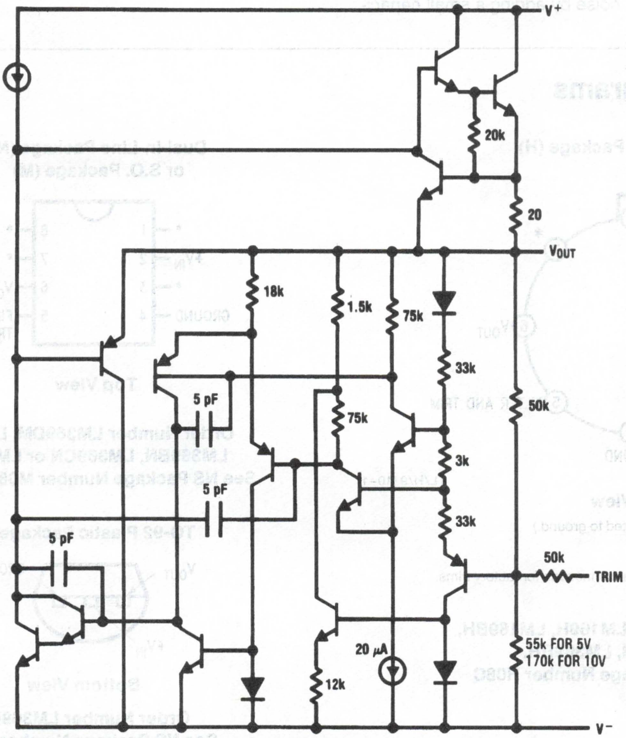
Typical Applications (Continued)

Buffered High-Current Reference with Filter


V+
10k
2
7
LM308A
6
100
2N2219
10k
3
8
LM368
2
6
5
4
4
C_f
500 pF
2N2222
3.3
V_{OUT}
3.3k

TL/H/5522–18

Simplified Schematic Diagram


V+
20k
20
V_{OUT}
18k
1.5k
75k
33k
50k
5 pF
75k
3k
5 pF
33k
5 pF
50k
TRIM
20 µA
12k
55k FOR 5V
170k FOR 10V
V−

TL/H/5522–6

*Reg. U.S. Pat. Off.

National Semiconductor Corporation

PRELIMINARY

LM169/LM369 Precision Voltage Reference

General Description

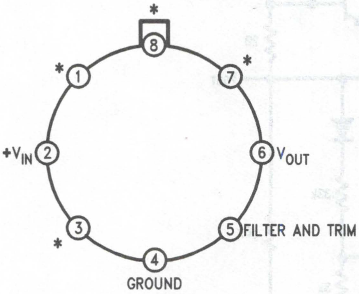
The LM169/LM369 are precision monolithic temperature-compensated voltage references. They are based on a buried zener reference as pioneered in the LM199 references, but do not require any heater, as they rely on special temperature-compensation techniques (Patent Pending). The LM169 makes use of thin-film technology enhanced by the discrete laser trimming of resistors to achieve excellent Temperature coefficient (Tempco) of V_{out} (as low as 1 ppm/°C), along with tight initial tolerances (as low as 0.01%). The trim scheme is such that individual resistors are cut open rather than being trimmed (partially cut), to avoid resistor drift caused by electromigration in the trimmed area. The LM169 also provides excellent stability vs. changes in input voltage and output current (both sourcing and sinking). The devices have a 10.000V output and will operate in either series or shunt mode; the output is short-circuit-proof to ground. A trim pin is available which permits fine-trimming of V_{out}, and also permits filtering to greatly decrease the output noise by adding a small capacitor (0.05 to 0.5 μF).

Features

- Low Tempco of V_{out}
- Excellent initial accuracy (0.003%)
- Excellent line regulation (2 ppm/V)
- Excellent output impedance
- Excellent thermal regulation
- Low noise
- Easy to filter output noise
- Low dissipation — 20 mW
- Operates in series or shunt mode

Connection Diagrams

Metal Can Package (H)



TL/H/9110-1

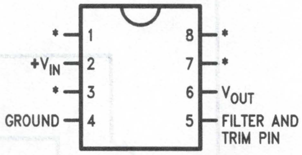
Top View

(Case is connected to ground.)

*Do not connect; internal connection for factory trims.

Order Number LM169H, LM169BH, LM369H, LM369BH,
See NS Package Number H08C

Dual-In-Line Package (N) or S.O. Package (M)

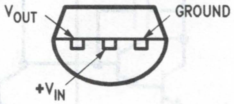


TL/H/9110-5

Top View

Order Number LM369DM, LM369N, LM369BN, LM369CN or LM369DN
See NS Package Number M08A or N08E

TO-92 Plastic Package (Z)



TL/H/9110-28

Bottom View

Order Number LM369DZ
See NS Package Number Z03A

Absolute Maximum Ratings (Note 8)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage (Series Mode)	35V
Reverse Current (Shunt Mode)	50 mA
Power Dissipation (Note 7)	600 mW
Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	(T_j min to T_j max)
LM169	−55°C to +125°C
LM369	0°C to +70°C

Soldering Information	
DIP (N) Package, 10 sec.	+260°C
TO-5 (H) Package, 10 sec.	+300°C
SO (M) Package, Vapor Phase (60 sec.)	+215°C
Infrared (15 sec.)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

ESD Tolerance	
C_{zap} = 100 pF, R_{zap} = 1.5k	800V

Electrical Characteristics, LM169, LM369 (Note 1)

Parameter	Conditions	Typical	Tested Limits (Note 2)	Design Limit (Note 3)	Units (Max Unless Noted)
V_{out} Nominal		+10.000			V
V_{out} Error	(Note 11)	50 0.50	±500 ±5		ppm mV
V_{out} Tempco					
LM169B, LM369B	$T_{min} < T_j < T_{max}$	1.5	**3.0**	—	ppm/°C
LM169, LM369	$T_{min} < T_j < T_{max}$	2.7	**5.0**	—	ppm/°C
LM369C	$T_{min} < T_j < T_{max}$	6	**10**	—	ppm/°C
(Note 6) (Note 11)					
Line Regulation	$13V \leq V_{IN} \leq 30V$	2.0	4.0	**8.0**	ppm/V
Load Regulation					
Sourcing	0 to 10 mA	+3	±8.0	**20.0**	ppm/mA
Sinking (Note 12)	0 to −10 mA	+80	+150		ppm/mA
(Note 4, Note 9)					
Thermal Regulation	(t = 10 msec				
Sourcing	After Load	3.0	±20	—	ppm/100 mW
Sinking (Note 12)	is Applied)	3.0	—	—	ppm/100 mW
(Note 5)					
Supply Current		1.4	1.8	**2.0**	mA
ΔSupply Current	$13V \leq V_{IN} \leq 30V$	0.06	0.12	**0.2**	mA
Short Circuit Current		27	15 50	**11** **65**	mA min mA max
Noise Voltage	10 Hz to 1 kHz	10	30	—	µV rms
	0.1 Hz to 10 Hz	4	—	—	µV p-p
	(10 Hz to 10 kHz, C_{filter} = 0.1 µF)	4	—	—	µV rms
Long-term Stability (Non-Cumulative) (Note 10)	1000 hours, $T_j < T_{max}$ (Measured at +25°C)	6	—	—	ppm
Temperature Hysteresis of V_{out}	ΔT = 25°C	3	—	—	ppm
Output Shift per 1 µA at Pin 5		1500	2600	—	ppm

Electrical Characteristics LM369D (Note 1)

Parameter	Conditions	Typical	Tested Limits (Note 2)	Design Limit (Note 3)	Units (Max Unless Noted)
V_{out} Nominal		+10.000			V
V_{out} Error, LM369D		70 0.7	±1000 ±10.0	— —	ppm mV
V_{out} Tempco (Note 6)	$T_{min} \leq T_j \leq T_{max}$	5		**30**	ppm/°C
Line Regulation	$13V \leq V_{IN} \leq 30V$	2.4	±6.0	**12**	ppm/V
Load Regulation Sourcing Sinking (Note 12) (Note 4, Note 9)	 0 to 10 mA 0 to −10 mA	 +3 +80	 ±12 +160	 **±25**	 ppm/mA ppm/mA
Thermal Regulation Sourcing Sinking (Note 12) (Note 5)	(t = 10 msec After Load is Applied)	 4.0 4.0	 ±25 —	 — —	 ppm/100 mW ppm/100 mW
Supply Current		1.5	2.0	**2.4**	mA
ΔSupply Current	$13V \leq V_{IN} \leq 30V$	0.06	0.16	**0.3**	mA
Short Circuit Current		27	14 50	**10** **65**	mA min mA max
Noise Voltage	10 Hz to 1 kHz 0.1 Hz to 10 Hz (10 Hz to 10 kHz, $C_{filter} = 0.1 \mu F$)	10 4 4	30 — —	— — —	µV rms µV p-p µV rms
Long-Term Stability (Non-Cumulative)	1000 Hours, $T_j < T_{max}$ (Measured at +25°C)	8	—	—	ppm
Temperature Hysteresis of V_{out}	ΔT = 25°C	5	—	—	ppm
Output Shift Per 1 µA at Pin 5		1500	2800	—	ppm

Note 1: Unless otherwise noted, these conditions apply: $T_j = +25°C$, $13V \leq V_{in} \leq 17V$, $0 \leq I_{load} \leq 1.0$ mA, $C_L = \leq 200$ pF. Specifications in **BOLDFACED TYPE** apply over the rated operating temperature range.

Note 2: Tested limits are guaranteed and 100% tested in production.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not to be used to calculate outgoing quality levels.

Note 4: The LM169 has a Class B output, and will exhibit transients at the crossover point. This point occurs when the device is required to sink approximately 1.0 mA. In some applications it may be advantageous to pre-load the output to either V_{in} or to ground, to avoid this crossover point.

Note 5: Thermal regulation is defined as the change in the output voltage at a time T after a step change of power dissipation of 100 mW.

Note 6: Temperature Coefficient of V_{OUT} is defined as the worst-case ΔV_{out} measured at Specified Temperatures divided by the total span of the Specified Temperature Range (see graphs). There is no guarantee that the Specified Temperatures are exactly at the minimum or maximum deviation.

Note 7: In metal can (H), θ_{J-C} is 75°C/W and θ_{J-A} is 150°C/W. In plastic DIP, θ_{J-A} is 160°C/W. In S0-8, θ_{J-A} is 180°C/W, in TO-92, θ_{J-A} is 160°C/W.

Note 8: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not guaranteed beyond the Rated Operating Conditions.

Note 9: Regulation is measured at constant temperature using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for Thermal Regulation and Tempco. Load Regulation is measured at a point on the output pin 1/8″ below the bottom of the package.

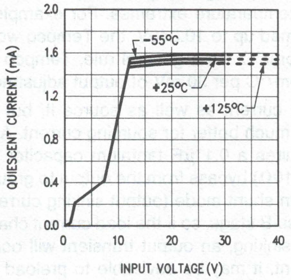
Note 10: Consult factory for availability of devices with Guaranteed Long-term Stability.

Note 11: Consult factory for availability of devices with tighter Accuracy and Tempco Specifications.

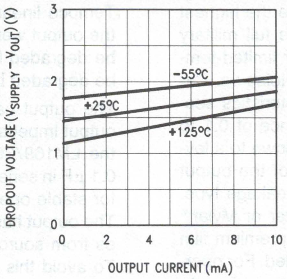
Note 12: In Sinking mode, connect 0.1 µF tantalum capacitor from output to ground.

Typical Performance Characteristics (Note 1)

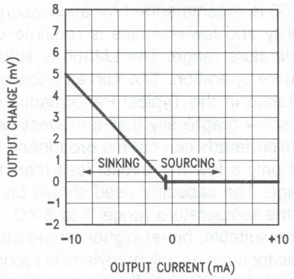
Quiescent Current vs Input Voltage and Temperature



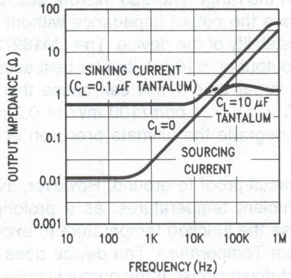
Dropout Voltage vs Output Current (Series Mode Sourcing Current)



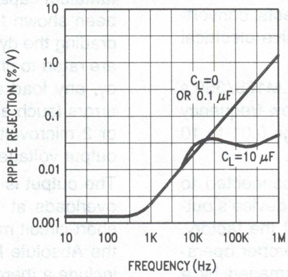
Output Change vs Output Current



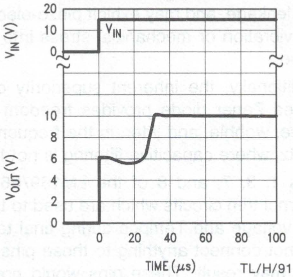
Output Impedance vs Frequency



Ripple Rejection vs Frequency

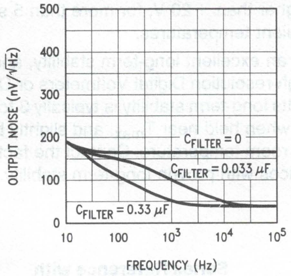


Start-up Response



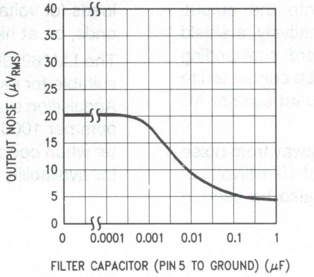
TL/H/9110-6

Output Noise vs Frequency



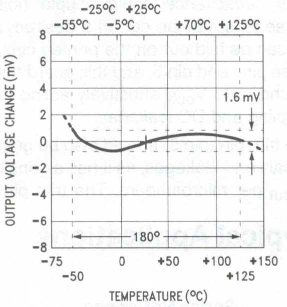
TL/H/9110-24

Output Noise vs Filter Capacitor



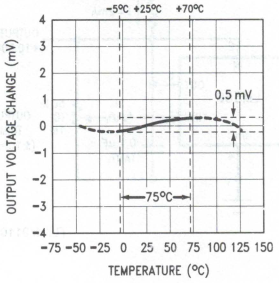
TL/H/9110-25

LM169 Temperature Coefficient



TL/H/9110-26

LM369 Temperature Coefficient



TL/H/9110-27

Typical Temperature Coefficient Calculations:

LM169 (see curve above):
T.C. = 1.6 mV/(180° × 10V)
= 8.9 × 10^{-7} = 0.89 ppm/°C

LM369 (see curve at left):
T.C. = 0.5 mV/(75° × 10V)
= 6.7 × 10^{-7} = 0.67 ppm/°C

Application Hints

The LM169/LM369 can be applied in the same way as any other voltage reference. The adjacent Typical Applications Circuits suggest various uses for the LM169/LM369. The LM169 is recommended for applications where the highest stability and lowest noise is required over the full military temperature range. The LM369 is suitable for limited-temperature operation. The curves showing the Noise vs. Capacitance in the Typical Performance Characteristics section show graphically that a modest capacitance of 0.1 to 0.3 microfarads can cut the broadband noise down to a level of only a few microvolts, less than 1 ppm of the output voltage. The capacitor used should be a low-leakage type. For the temperature range 0 to 50°C, polyester or Mylar® will be suitable, but at higher temperatures, a premium film capacitor such as polypropylene is recommended. For operation at +125°C, a Teflon® capacitor would be required, to ensure sufficiently low leakage. Ceramic capacitors may seem to do the job, but are not recommended for production use, as the high-K ceramics cannot be guaranteed for low leakage, and may exhibit piezo-electric effects, converting vibration or mechanical stress into excessive electrical noise.

Additionally, the inherent superiority of the LM169/369's buried Zener diode provides freedom from low-frequency noise, wobble, and jitter, in the frequency range 0.01 to 10 Hertz, where capacitive filtering is not feasible.

Pins 1, 3, 7, and 8 of the LM169/369 are connected to internal trim circuits which are used to trim the device's output voltage and Tempco during final testing at the factory. Do not connect anything to these pins, or improper operation may result. These pins would not be damaged by a short to ground, or by Electrostatic Discharges; however, keep them away from large transients or AC signals, as stray capacitance could couple noises into the output. These pins may be cut off if desired. Alternatively, a shield foil can be laid out on the printed circuit board, surrounding these pins and pin 5, and this guard foil can be connected to ground or to V_{out}, effectively acting as a guard against AC coupling and DC leakages.

The trim pin (pin 5) should also be guarded away from noise signals and leakages, as it has a sensitivity of 15 millivolts of ΔV_{out} per microampere. The trim pin can also be used in the circuits shown, to provide an output trim range of ±10 millivolts. Trimming to a wider range is possible, but is not recommended as it may degrade the Tempco and the Tempco linearity at temperature extremes. For example, if the output were trimmed up to 10.240V, the Tempco would be degraded by 8 ppm/°C. As a general rule, Tempco will be degraded by 1 ppm/°C per 30 mV of output adjustment.

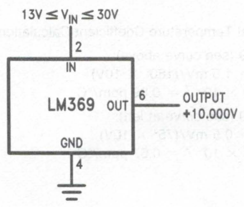
The output can sink current as well as source it, but the output impedance is much better for sourcing current. Also, the LM169/369 requires a 0.1 μF tantalum capacitor (or, 0.1 μF in series with 10Ω) bypass from the output to ground, for stable operation in shunt mode (output sinking current). The output has a class-B stage, so if the load current changes from sourcing to sinking, an output transient will occur. To avoid this transient, it may be advisable to preload the output with a few milliamperes of load to ground. The LM169/369 does have an excellent tolerance of load capacitance, and in cases of load transients, electrolytic or tantalum capacitors in the range 1 to 500 microfarads have been shown to improve the output impedance without degrading the dynamic stability of the device. The LM169/369 are rated to drive an output of ±10 mA, but for best accuracy, any load current larger than 1 mA can cause thermal errors (such as, 1 mA × 5V × 4 ppm/100 mW = 0.2 ppm or 2 microvolts) and degrade the ultimate precision of the output voltage.

The output is short-circuit-proof to ground. However, avoid overloads at high ambient temperatures, as a prolonged short-circuit may cause the junction temperature to exceed the Absolute Maximum Temperature. The device does not include a thermal shut-down circuit. If the output is pulled to a positive voltage such as +15 or +20V, the output current will be limited, but overheating may occur. Avoid such overloads for voltages higher than +20 V, for more than 5 seconds, or, at high ambient temperatures.

The LM169/369 has an excellent long-term stability, and is suitable for use in high-resolution Digital Voltmeters or Data Acquisition systems. Its long-term stability is typically 3 to 10 ppm per 1000 hours when held near T_{max}, and slightly better when operated at room temperature. Contact the factory for availability of devices with proven long-term stability.

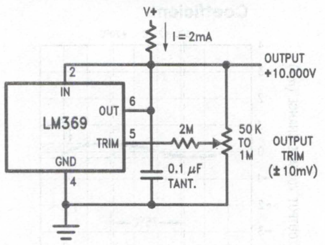
Typical Applications

Series Reference



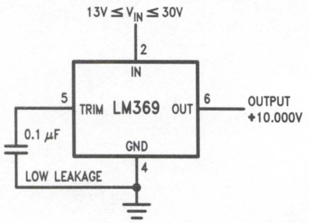
TL/H/9110-2

Shunt Reference with Optional Trim



TL/H/9110-3

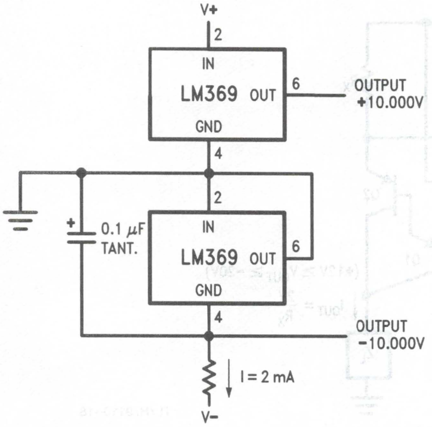
Series Reference with Optional Filter for Reduced Noise



TL/H/9110-4

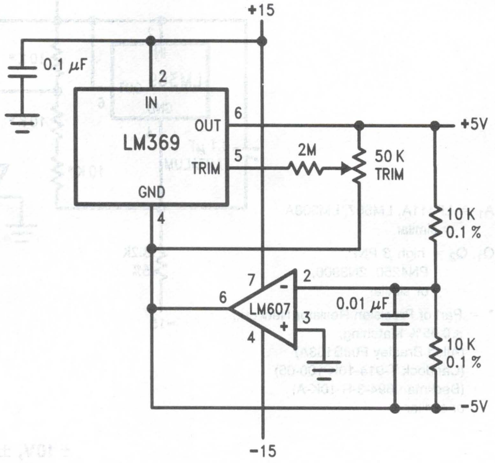
Typical Applications (Continued)

±10V Reference


V+
2
IN
LM369
OUT
6
GND
4
OUTPUT
+10.000V
2
IN
LM369
OUT
6
GND
4
0.1 μF
TANT.
OUTPUT
−10.000V
I = 2 mA
V−

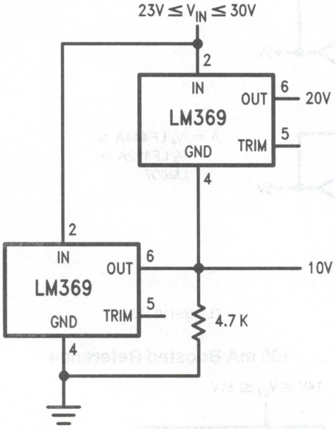
TL/H/9110-7

±5V Reference

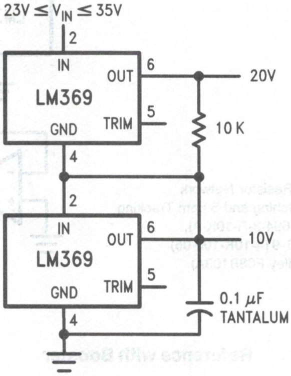

+15
0.1 μF
2
IN
LM369
OUT
6
5
TRIM
GND
4
2M
50 K
TRIM
+5V
10 K
0.1 %
7
2
6
LM607
3
4
0.01 μF
10 K
0.1 %
−5V
−15

TL/H/9110-8

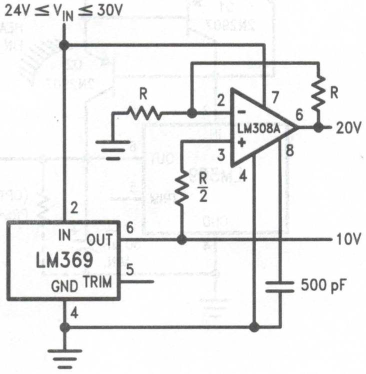
Multiple Output Voltages


23V ≤ V_IN ≤ 30V
2
IN
LM369
OUT
6
20V
GND
TRIM
5
4
2
IN
LM369
OUT
6
10V
GND
TRIM
5
4
4.7 K

TL/H/9110-9


23V ≤ V_IN ≤ 35V
2
IN
LM369
OUT
6
20V
GND
TRIM
5
4
10 K
2
IN
LM369
OUT
6
10V
GND
TRIM
5
4
0.1 μF
TANTALUM

TL/H/9110-10

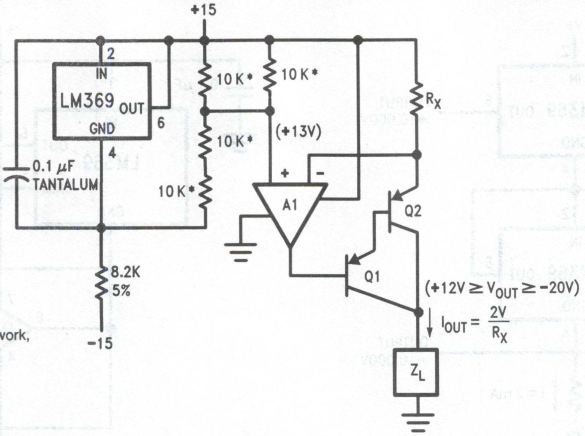

24V ≤ V_IN ≤ 30V
R
2
7
R
6
LM308A
20V
3
8
R
2
4
2
IN
LM369
OUT
6
10V
GND
TRIM
5
4
500 pF

TL/H/9110-11

R = Thin Film Resistor Network
0.05% Matching and 5 ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
(Allen Bradley F08B103A)
or similar.

Typical Applications (Continued)

Precision Wide-Range Current Source


+15
2
IN
LM369
OUT
GND
6
4
10K*
10K*
10K*
10K*
(+13V)
0.1 µF
TANTALUM
8.2K
5%
-15
+
-
A1
Q2
Q1
R_X
(+12V ≥ V_OUT ≥ -20V)
I_OUT = 2V/R_X
Z_L

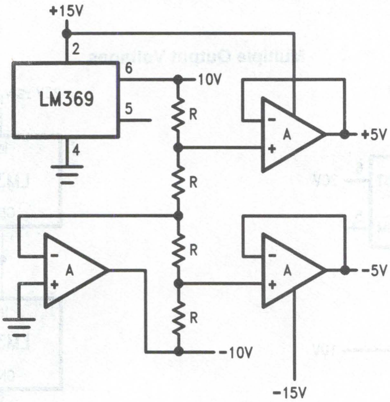
A_1 = LF411A, LM607, LM308A or similar

Q_1, Q_2 = high β PNP, PN4250, 2N3906, or similar

* = Part of Precision Resistor Network, ±0.05% Matching, (Allen Bradley F08B103A) (Caddock T-914-10K-100-05) (Beckman 694-3-R-10K-A) or similar

TL/H/9110–18

±10V, ±5V References

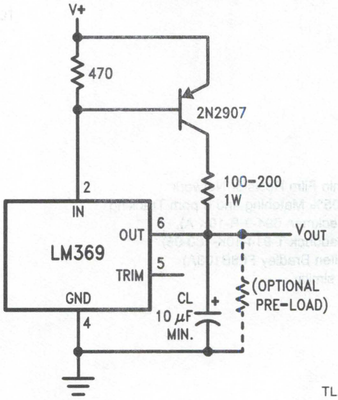

+15V
2
6
LM369
5
4
10V
R
R
R
R
A
A
A
-
+
+5V
-5V
-10V
-15V

A = ¼ LF444A or ½ LF412A or LM607

R = Thin Film Resistor Network 0.05% Matching and 5 ppm Tracking (Beckman 694-3-R-10K-A), (Caddock T-914-10K-100-05) (Allen Bradley F08B103A) or similar.

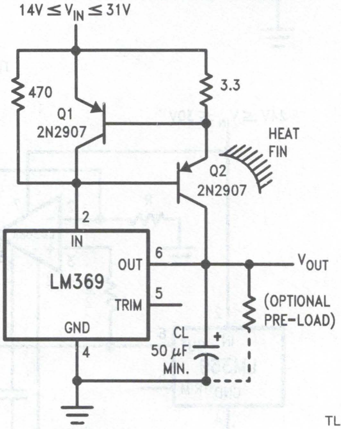
TL/H/9110–12

Reference with Booster


V+
470
2N2907
100–200
1W
2
IN
LM369
OUT
6
TRIM
5
GND
4
V_OUT
CL
10 µF
MIN.
+
(OPTIONAL
PRE-LOAD)

TL/H/9110–13

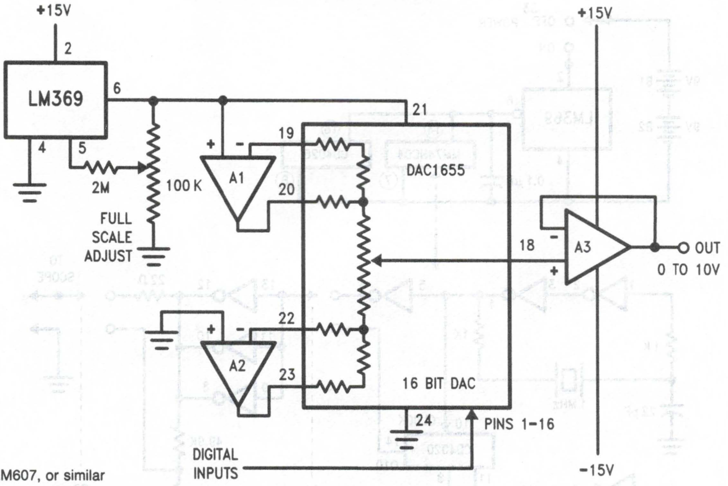
100 mA Boosted Reference


14V ≤ V_IN ≤ 31V
470
3.3
Q1
2N2907
HEAT
FIN
Q2
2N2907
2
IN
LM369
OUT
6
TRIM
5
GND
4
V_OUT
CL
50 µF
MIN.
+
(OPTIONAL
PRE-LOAD)

TL/H/9110–14

Typical Applications (Continued)

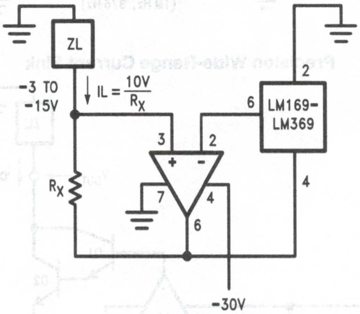
Precision Programmable Supply


+15V
2
LM369
6
4
5
2M
100 K
FULL
SCALE
ADJUST
A1
19
20
21
DAC1655
+15V
A3
18
OUT
0 TO 10V
A2
22
23
16 BIT DAC
24
PINS 1–16
DIGITAL
INPUTS
−15V

A_1, A_2, A_3 = LF411A, LM607, or similar

TL/H/9110–21

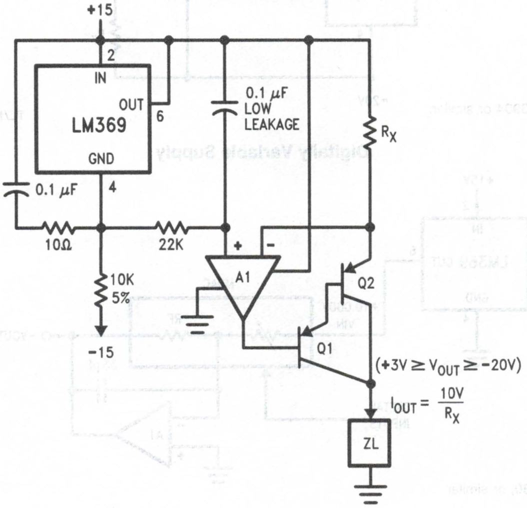
Current Source


ZL
−3 TO
−15V
IL = 10V/RX
6
2
LM169-
LM369
3
2
4
7
4
6
RX
−30V

2k ≤ Rx ≤ 10M

TL/H/9110–16

Precision Current Source


+15
2
IN
OUT
6
LM369
GND
4
0.1 μF
LOW
LEAKAGE
0.1 μF
10Ω
22K
10K
5%
−15
RX
A1
Q2
Q1
(+3V ≥ VOUT ≥ −20V)
IOUT = 10V/RX
ZL

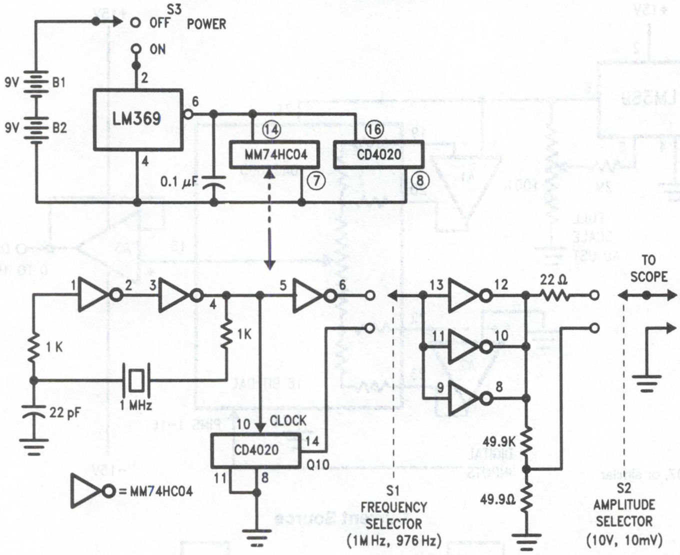
Q_1, Q_2 = high β PNP, PN4250, 2N3906 or similar

A_1 = LM607, LM11, LF411A or similar

TL/H/9110–17

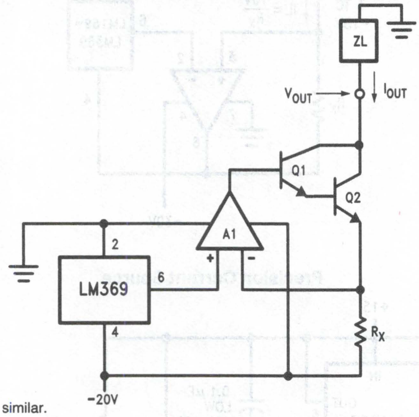
Typical Applications (Continued)

Oscilloscope Calibrator


S3
OFF
POWER
ON
9V
B1
9V
B2
LM369
2
6
4
0.1 µF
⑭
MM74HC04
⑦
⑯
CD4020
⑧
1
2
3
4
5
6
1K
1 K
1 MHz
22 pF
10
CLOCK
CD4020
14
Q10
11
8
= MM74HC04
13
12
11
10
9
8
22 Ω
TO SCOPE
49.9K
49.9Ω
S1
FREQUENCY SELECTOR
(1M Hz, 976 Hz)
S2
AMPLITUDE SELECTOR
(10V, 10mV)

TL/H/9110-22

Precision Wide-Range Current Sink


ZL
VOUT
IOUT
Q1
Q2
A1
+
-
2
LM369
6
4
RX
-20V

$I_{out} = \frac{10V}{Rx}$

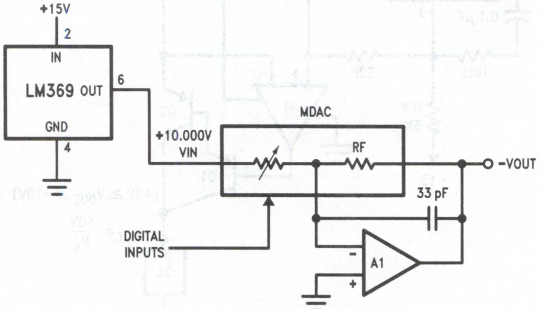
A_1 = LM11, LM607 or similar.

$(V3 + 2V) \le V_{out} \le +20V$.

Q1, Q2 = high Beta NPN, 2N3707, 2N3904 or similar.

TL/H/9110-19

Digitally Variable Supply


+15V
2
IN
LM369 OUT
GND
6
4
+10.000V
VIN
MDAC
RF
-VOUT
33 pF
DIGITAL INPUTS
-
+
A1

$V_{out} = -10V \times$ (Digitally Set Gain).

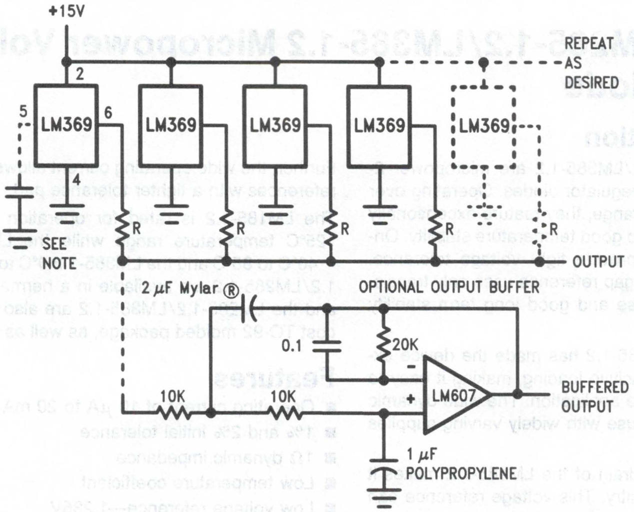
A_1 = LM11A, LM607, or similar.

MDAC = DAC1220, DAC1208, DAC1230, or similar.

TL/H/9110-20

Typical Applications (Continued)

Ultra-Low-Noise Statistical Reference


+15V
2
5
6
4
LM369
LM369
LM369
LM369
LM369
REPEAT AS DESIRED
SEE NOTE
R
R
R
R
R
OUTPUT
2 μF Mylar ®
OPTIONAL OUTPUT BUFFER
0.1
20K
LM607
+
−
BUFFERED OUTPUT
10K
10K
1 μF POLYPROPYLENE

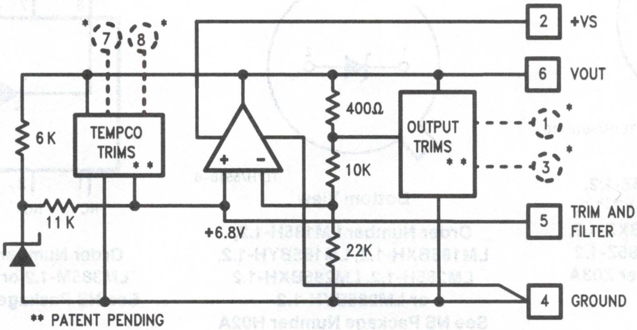
TL/H/9110–23

$200\Omega \le R \le 1k$

When N pieces of LM369 are used, the V_{out} noise is decreased by a factor of $\frac{1}{\sqrt{N}}$

If the output buffer is not used, for lowest noise add 0.1 μF Mylar® from ground to pin 5 of each LM369.

LM169 Block Diagram


7
8
*
*
2
+VS
6
VOUT
6K
TEMPCO TRIMS
**
+
−
400Ω
10K
OUTPUT TRIMS
**
1
3
*
*
11K
+6.8V
22K
5
TRIM AND FILTER
4
GROUND

** PATENT PENDING

TL/H/9110–15

*Do not connect; internal connection for factory trim.

National Semiconductor Corporation

LM185-1.2/LM285-1.2/LM385-1.2 Micropower Voltage Reference Diode

General Description

The LM185-1.2/LM285-1.2/LM385-1.2 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 10 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185-1.2 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

Careful design of the LM185-1.2 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185-1.2 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

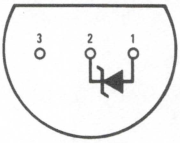
The LM185-1.2 is rated for operation over a −55°C to 125°C temperature range while the LM285-1.2 is rated −40°C to 85°C and the LM385-1.2 0°C to 70°C. The LM185-1.2/LM285-1.2 are available in a hermetic TO-46 package and the LM285-1.2/LM385-1.2 are also available in a low-cost TO-92 molded package, as well as S.O.

Features

- Operating current of 10 μA to 20 mA
- 1% and 2% initial tolerance
- 1Ω dynamic impedance
- Low temperature coefficient
- Low voltage reference—1.235V
- 2.5V device also available—LM385-2.5

Connection Diagrams

TO-92
Plastic Package (Z)

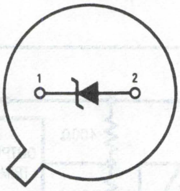


TL/H/5518-10

Bottom View

Order Number LM385Z-1.2, LM385BZ-1.2, LM385BXZ-1.2, LM385BYZ-1.2, LM285BXZ-1.2, LM285BYZ-1.2 or LM285Z-1.2
See NS Package Number Z03A

TO-46
Metal Can Package (H)

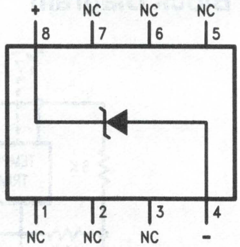


TL/H/5518-6

Bottom View

Order Number LM185H-1.2, LM185BXH-1.2, LM185BYH-1.2, LM285H-1.2, LM285BXH-1.2 or LM285BYH-1.2
See NS Package Number H02A

SO Package

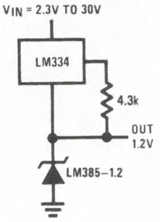


TL/H/5518-9

Order Number LM285M-1.2, LM385M-1.2 or LM385BM-1.2
See NS Package Number M08A

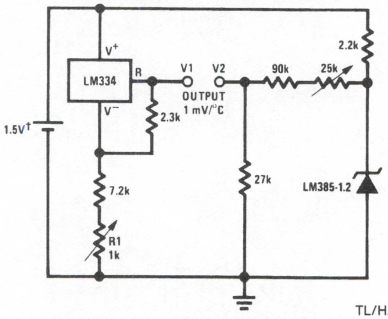
Applications

Wide Input Range Reference



TL/H/5518-8

Centigrade Thermometer



TL/H/5518-1

Calibration

1. Adjust R1 so that V1 = temp at 1 mV/°K
2. Adjust V2 to 273.2 mV

†I_Q for 1.3V to 1.6V battery voltage = 50 μA to 150 μA

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 6)

Reverse Current	30mA
Forward Current	10mA
Operating Temperature Range	
LM185-1.2	−55°C to + 125°C
LM285-1.2	−40°C to + 85°C
LM385-1.2	0°C to 70°C
Storage Temperature	−55°C to + 150°C
Soldering information	
TO-92 package: 10 sec.	260°C
TO-46 package: 10 sec.	300°C
SO package: Vapor phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM185-1.2 LM185BX-1.2 LM185BY-1.2 LM285-1.2 LM285BX-1.2 LM285BY-1.2			LM385-1.2 LM385B-1.2 LM385BX-1.2 LM385BY-1.2			Units Limit
		Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_{MIN} \leq I_R \leq I_{MAX}$ LM185-1.2/LM285-1.2/LM385B-1.2	1.235	1.223		1.235	1.223		V_{MIN}
			1.247			1.247		V_{MAX}
	LM385-1.2				1.235	1.205		V_{MIN}
						1.260		V_{MAX}
Minimum Operating Current		8	10	**20**	8	15	**20**	μA
Reverse Breakdown	$I_{MIN} \leq I_R \leq 1$ mA		1	**1.5**		1	**1.5**	mV
Voltage Change with Current	1 mA $\leq I_R \leq$ 20 mA		10	**20**		20	**25**	mV
Reverse Dynamic Impedance	$I_R = 100$ μA. f = 20 Hz	1			1			Ω
Wideband Noise (rms)	$I_R = 100$ μA 10 Hz ≤ f ≤ 10 kHz	60			60			μV
Long Term Stability	$I_R = 100$ μA, T = 1000 Hr $T_A = 25°C \pm 0.1°C$	20			20			ppm
Average Temperature Coefficient (Note 4)	$I_R = 100$ μA							
	X Series		**30**			**30**		ppm/°C
	Y Series		**50**			**50**		ppm/°C
	Other Versions			**150**			**150**	ppm/°C

Note 1: Parameters identified with **boldface type** apply at temperature extremes and for $I_{MIN} < I_R < 20$ mA, unless otherwise specified. All other numbers apply at $T_A = T_J = 25°C$.

Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature and input current ranges. These limits are not to be used to calculate outgoing quality levels.

Note 4: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures between the operating T_{MAX} and T_{MIN}, divided by $T_{MAX} - T_{MIN}$. The measured temperatures are −55°C, −40°C, 0°C, 25°C, 70°C, 85°C, 125°C.

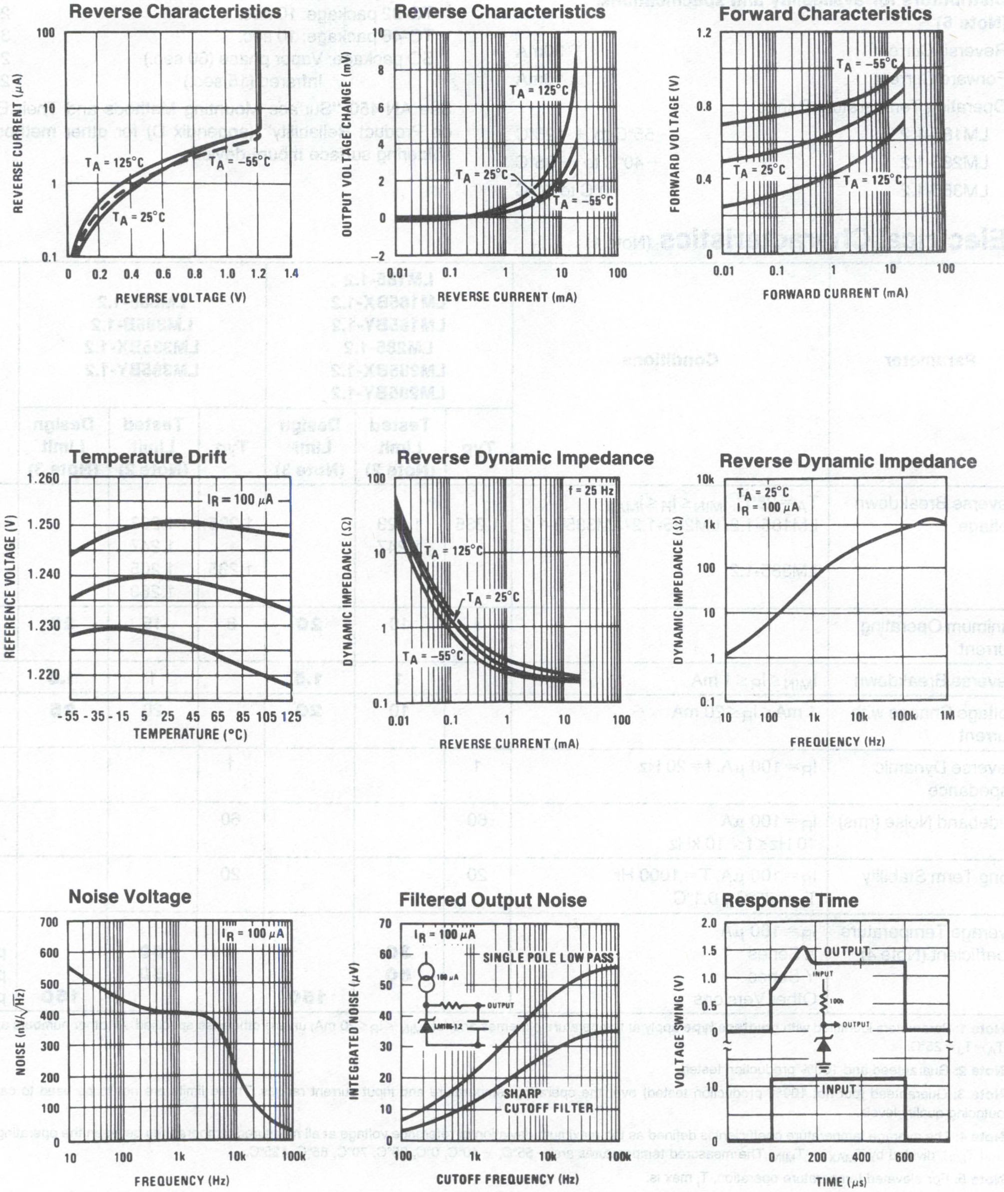
Note 5: For elevated temperature operation, T_j max is:

LM185	150°C
LM285	125°C
LM385	100°C

Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (junction to ambient)	180°C/W (0.4″ leads) 170°C/W (0.125″ leads)	440°C/W	165°C/W
θ_{jc} (junction to case)	n/a	80°C/W	n/a

Note 6: Refer to RETS185H-1.2 for military specifications.

Typical Performance Characteristics


Reverse Characteristics

Reverse Characteristics

Forward Characteristics

Temperature Drift

Reverse Dynamic Impedance

Reverse Dynamic Impedance

Noise Voltage

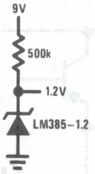
Filtered Output Noise

Response Time

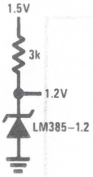
TL/H/5518-3

Applications (Continued)

Micropower Reference from 9V Battery


9V
500k
1.2V
LM385–1.2

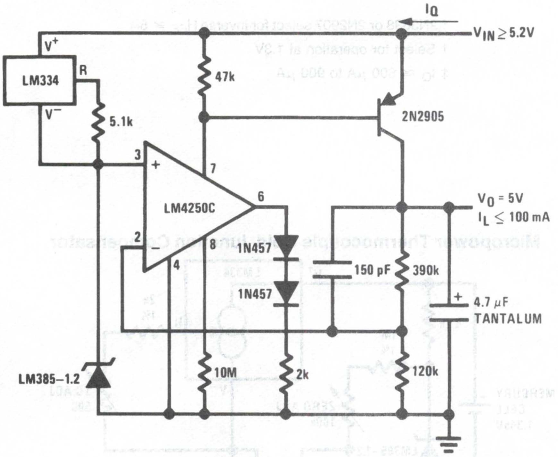
Reference from 1.5V Battery


1.5V
3k
1.2V
LM385–1.2

TL/H/5518–2

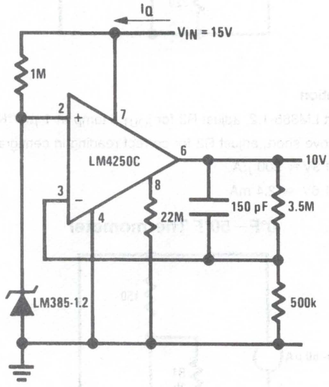
LM385 Applications

Micropower* 5V Regulator


IQ
VIN ≥ 5.2V
V+
LM334
R
V−
5.1k
47k
2N2905
3
+
7
LM4250C
6
2
−
8
4
1N457
1N457
VO = 5V
IL ≤ 100 mA
150 pF
390k
+
4.7 μF
TANTALUM
LM385–1.2
10M
2k
120k

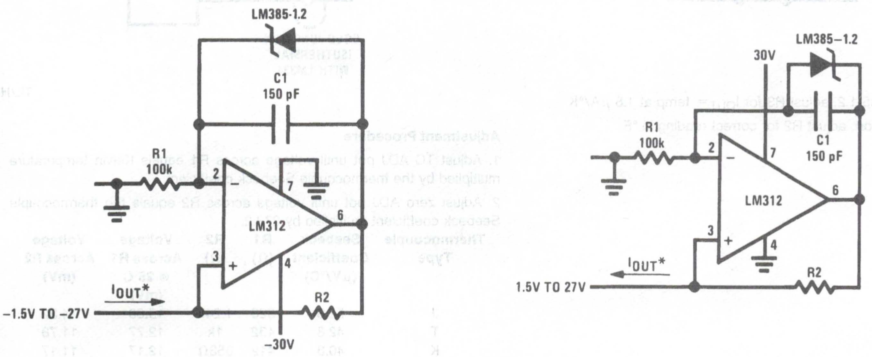
*I_Q ≅ 30 μA

Micropower* 10V Reference


IQ
VIN = 15V
1M
2
+
7
LM4250C
6
10V
3
−
8
4
22M
150 pF
3.5M
LM385-1.2
500k

*I_Q ≅ 20 μA standby current

Precision 1 μA to 1 mA Current Sources


LM385-1.2
C1
150 pF
R1
100k
2
−
7
LM312
6
3
+
4
IOUT*
−1.5V TO −27V
R2
−30V
LM385−1.2
30V
R1
100k
C1
150 pF
2
−
7
LM312
6
3
+
4
IOUT*
1.5V TO 27V
R2

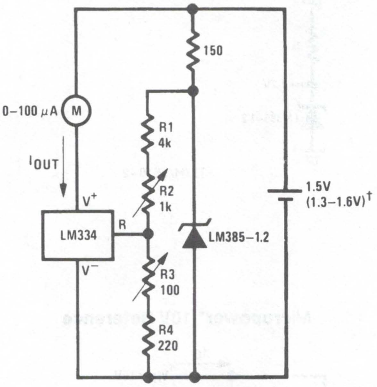
$*I_{OUT} = \frac{1.23V}{R2}$

TL/H/5518–4

LM385 Applications (Continued)

METER THERMOMETERS

0°C – 100°C Thermometer


150
0–100 μA
M
I_{OUT}
R1
4k
R2
1k
V^+
LM334
R
V^-
LM385–1.2
R3
100
R4
220
1.5V
(1.3–1.6V)†

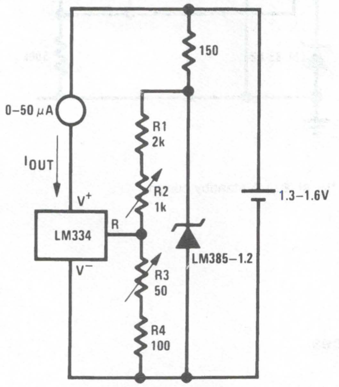
Calibration

1. Short LM385-1.2, adjust R3 for I_{OUT} = temp at 1 μA/°K
2. Remove short, adjust R2 for correct reading in centigrade

†I_Q at 1.3V ≅ 500 μA

I_Q at 1.6V ≅ 2.4 mA

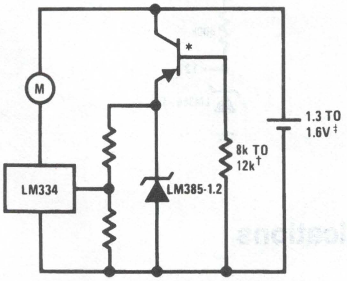
0°F – 50°F Thermometer


150
0–50 μA
I_{OUT}
R1
2k
R2
1k
V^+
LM334
R
V^-
LM385–1.2
R3
50
R4
100
1.3–1.6V

Calibration

1. Short LM385-1.2, adjust R3 for I_{OUT} = temp at 1.8 μA/°K
2. Remove short, adjust R2 for correct reading in °F

Lower Power Thermometer

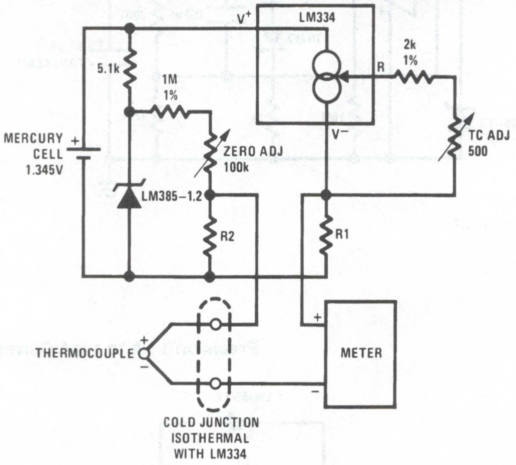

*
M
1.3 TO
1.6V‡
8k TO
12k†
LM334
LM385-1.2

* 2N3638 or 2N2907 select for inverse H_{FE} ≅ 5

† Select for operation at 1.3V

‡ I_Q ≅ 600 μA to 900 μA

Micropower Thermocouple Cold Junction Compensator


V^+
LM334
5.1k
1M
1%
2k
1%
R
MERCURY
CELL
1.345V
+
ZERO ADJ
100k
V^-
TC ADJ
500
LM385–1.2
R2
R1
+
THERMOCOUPLE
+
−
METER
−
COLD JUNCTION
ISOTHERMAL
WITH LM334

TL/H/5518–5

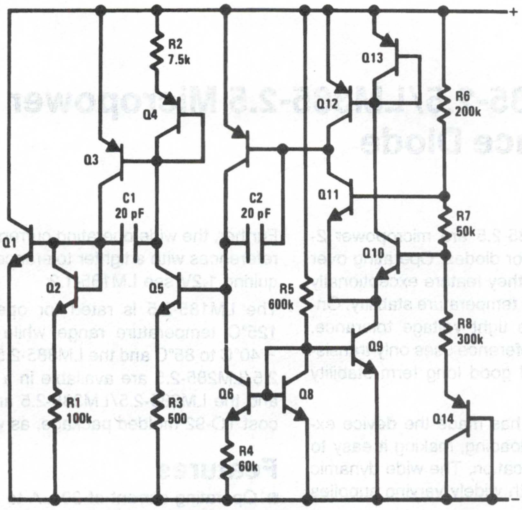
Adjustment Procedure

1. Adjust TC ADJ pot until voltage across R1 equals Kelvin temperature multiplied by the thermocouple Seebeck coefficient.
2. Adjust zero ADJ pot until voltage across R2 equals the thermocouple Seebeck coefficient multiplied by 273.2.

Thermocouple Type	Seebeck Coefficient (μV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @ 25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

Typical supply current 50 μA

Schematic Diagram


+
R2
7.5k
Q4
Q3
C1
20 pF
Q1
Q2
Q5
R1
100k
R3
500
C2
20 pF
R5
600k
Q6
Q8
R4
60k
Q13
Q12
Q11
R6
200k
R7
50k
Q10
R8
300k
Q9
Q14
–

TL/H/5518–7

National
Semiconductor
Corporation

LM185-2.5/LM285-2.5/LM385-2.5 Micropower Voltage Reference Diode

General Description

The LM185-2.5/LM285-2.5/LM385-2.5 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 20 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM-185-2.5 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

Careful design of the LM185-2.5 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185-2.5 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life.

Further, the wide operating current allows it to replace older references with a tighter tolerance part. For applications requiring 1.2V see LM185-1.2.

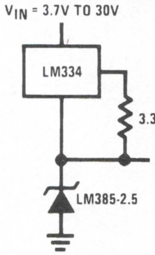
The LM185-2.5 is rated for operation over a −55°C to 125°C temperature range while the LM285-2.5 is rated −40°C to 85°C and the LM385-2.5 0°C to 70°C. The LM185-2.5/LM285-2.5 are available in a hermetic TO-46 package and the LM285-2.5/LM385-2.5 are also available in a low-cost TO-92 molded package, as well as S.O.

Features

- Operating current of 20 μA to 20 mA
- 1.5% and 3% initial tolerance
- 1Ω dynamic impedance
- Low temperature coefficient
- Low voltage reference—2.5V

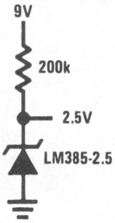
Applications

Wide Input Range Reference



TL/H/5519-12

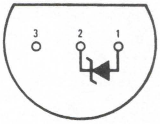
Micropower Reference from 9V Battery



TL/H/5519-2

Connection Diagrams

TO-92
Plastic Package

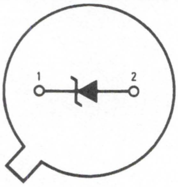


TL/H/5519-8

Bottom View

Order Number LM285BXZ-2.5, LM285BYZ-2.5, LM285Z-2.5, LM385Z-2.5, LM385BZ-2.5, LM385BXZ-2.5 or LM385BYZ-2.5
See NS Package Number Z03A

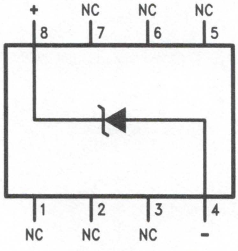
TO-46
Metal Can Package



TL/H/5519-13

Bottom View
Order Number LM185H-2.5, LM185BXH-2.5, LM185BYH-2.5, LM285H-2.5, LM285BXH-2.5 or LM285BYH-2.5
See NS Package Number H02A

SO Package



TL/H/5519-11

Order Number LM285M-2.5, LM385M-2.5 or LM385BM-2.5
See NS Package Number M08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 6)

Reverse Current	30 mA
Forward Current	10 mA
Operating Temperature Range	
LM185-2.5	−55°C to + 125°C
LM285-2.5	−40°C to + 85°C
LM385-2.5	0°C to 70°C
Storage Temperature	−55°C to + 150°C
Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-48 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM185-2.5 LM185BX-2.5 LM185BY-2.5 LM285-2.5 LM285BX-2.5 LM285BY-2.5 Typ	Tested Limit (Note 2)	Design Limit (Note 3)	LM385-2.5 LM385B-2.5 LM385BX-2.5 LM385BY-2.5 Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units Limit
Reverse Breakdown Voltage	$T_A=25°C$, $I_{MIN} \leq I_R \leq I_{MAX}$							
	LM185-2.5/LM285-2.5/LM385B-2.5	2.5	2.462 2.538		2.5	2.462 2.538		V_{MIN} V_{MAX}
	LM385-2.5				2.5	2.425 2.575		V_{MIN} V_{MAX}
Minimum Operating Current		13	20	**30**	13	20	**30**	μA
Reverse Breakdown Voltage Change with Current	20 μA $\leq I_R \leq$ 1 mA 1 mA $\leq I_R \leq$ 20 mA		1 10	**1.5** **20**		2.0 20	**2.5** **25**	mV mV
Reverse Dynamic Impedance	$I_R=100$ μA, f = 20 Hz	1			1			Ω
Wideband Noise (rms)	$I_R=100$ μA 10 Hz ≤ f ≤ 10 kHz	120			120			μV
Long Term Stability	$I_R=100$ μA, T = 1000 Hr $T_A=25°C \pm 0.1°C$	20			20			ppm
Average Temperature Coefficient (Note 4)	$I_R=100$ μA							
	X Series		**30**			**30**		ppm/°C
	Y Series		**50**			**50**		ppm/°C
	Other Versions			**150**			**150**	ppm/°C

Note 1: Parameters identified with **boldface type** apply at temperature extremes and for $I_{MIN} < I_R < 20$ mA, unless otherwise specified. All other numbers apply at $T_A = T_J = 25°C$.

Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature and input current ranges. These limits are not to be used to calculate outgoing quality levels.

Note 4: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures between the operating T_{MAX} and T_{MIN}, divided by $T_{MAX}-T_{MIN}$. The measured temperatures are −55°C, −40°C, 0°C, 25°C, 70°C, 85°C, 125°C.

Note 5: For elevated temperature operation, T_J max is:

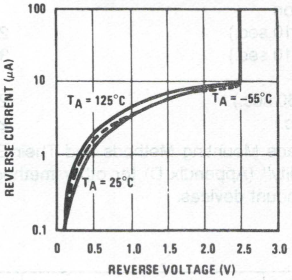
LM185	150°C
LM285	125°C
LM385	100°C

Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4″ leads) 170°C/W (0.125″ leads)	440°C/W	165°C/W
θ_{ja} (Junction to Case)	n/a	80°C/W	n/a

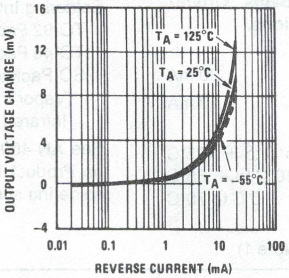
Note 6: Refer to RETS185H-2.5 for military specifications.

Typical Performance Characteristics

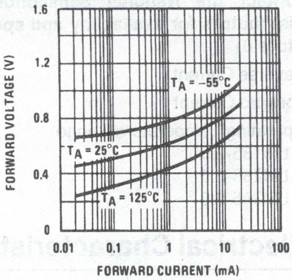
Reverse Characteristics



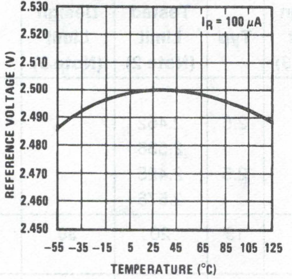
Reverse Characteristics



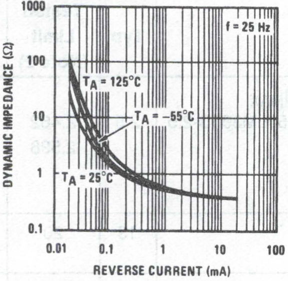
Forward Characteristics



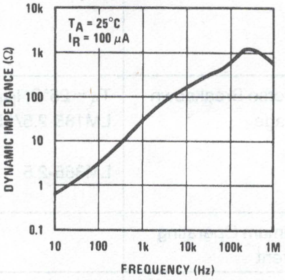
Temperature Drift



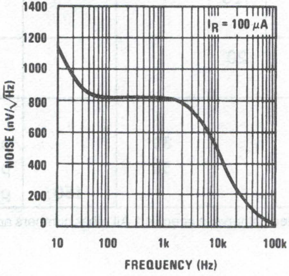
Reverse Dynamic Impedance



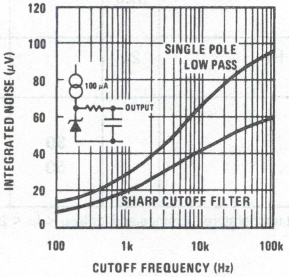
Reverse Dynamic Impedance



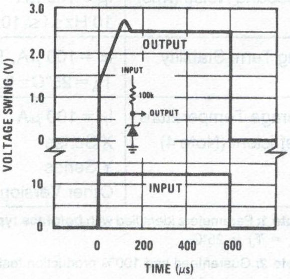
Noise Voltage



Filtered Output Noise



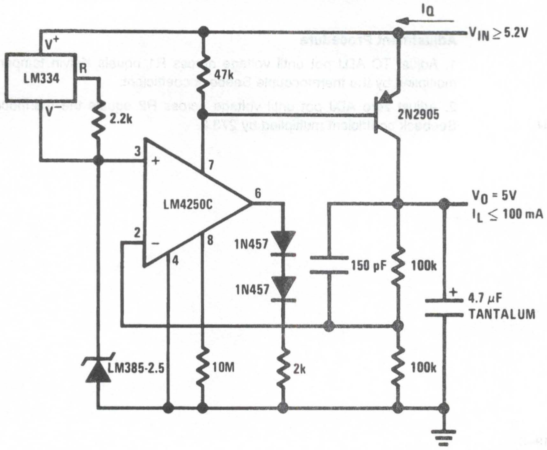
Response Time



TL/H/5519-3

LM385-2.5 Applications

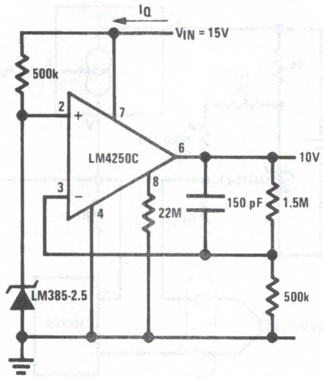
Micropower* 5V Regulator


I_Q
V_IN ≥ 5.2V
V+
LM334
R
V−
47k
2.2k
2N2905
3
+
7
LM4250C
6
2
−
8
4
1N457
1N457
150 pF
100k
V_O = 5V
I_L ≤ 100 mA
4.7 μF TANTALUM
LM385-2.5
10M
2k
100k

*$I_Q \cong 40\ \mu A$

TL/H/5519-9

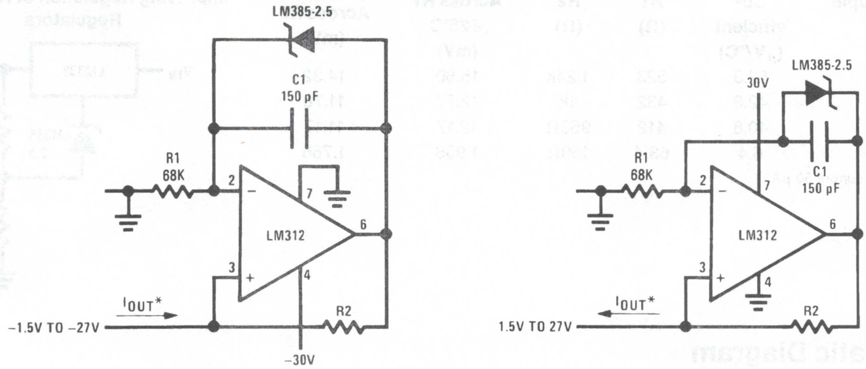
Micropower* 10V Reference


I_Q
V_IN = 15V
500k
2
+
7
LM4250C
6
10V
3
−
8
4
22M
150 pF
1.5M
LM385-2.5
500k

TL/H/5519-10

*$I_Q \cong 30\ \mu A$ standby current

Precision 1 μA to 1 mA Current Sources

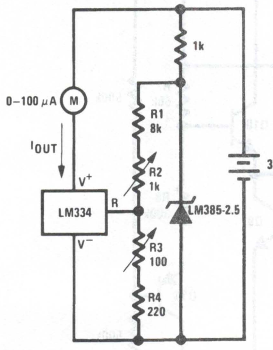

LM385-2.5
C1
150 pF
R1
68K
2
−
7
LM312
6
3
+
4
I_OUT*
−1.5V TO −27V
R2
−30V
LM385-2.5
30V
R1
68K
2
−
7
C1
150 pF
LM312
6
3
+
4
I_OUT*
1.5V TO 27V
R2

TL/H/5519-4

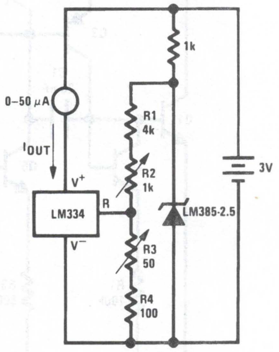
$$^{*}I_{OUT} = \frac{2.5V}{R2}$$

METER THERMOMETERS

0°C–100°C Thermometer


1k
0–100 μA
M
I_OUT
R1
8k
V+
R2
1k
3V
LM334
R
LM385-2.5
V−
R3
100
R4
220

0°F–50°F Thermometer


1k
0–50 μA
R1
4k
I_OUT
V+
R2
1k
3V
LM334
R
LM385-2.5
V−
R3
50
R4
100

TL/H/5519-5

Calibration

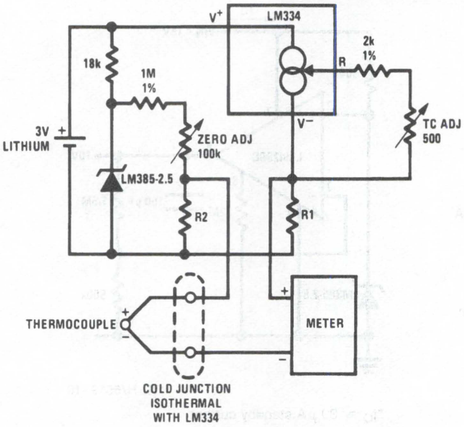
1. Short LM385-2.5, adjust R3 for I_{OUT} = temp at 1μA/°K
2. Remove short, adjust R2 for correct reading in centigrade

Calibration

1. Short LM385-2.5, adjust R3 for I_{OUT} = temp at 1.8 μA/°K
2. Remove short, adjust R2 for correct reading in °F

LM385-2.5 Applications (Continued)

Micropower Thermocouple Cold Junction Compensator


V+
LM334
2k
1%
R
18k
1M
1%
3V
LITHIUM
V−
ZERO ADJ
100k
TC ADJ
500
LM385-2.5
R2
R1
THERMOCOUPLE
+
−
METER
COLD JUNCTION
ISOTHERMAL
WITH LM334

Adjustment Procedure

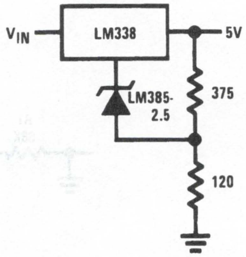
1. Adjust TC ADJ pot until voltage across R1 equals Kelvin temperature multiplied by the thermocouple Seebeck coefficient.
2. Adjust zero ADJ pot until voltage across R2 equals the thermocouple Seebeck coefficient multiplied by 273.2.

TL/H/5519–6

Thermocouple Type	Seebeck Co-efficient (µV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

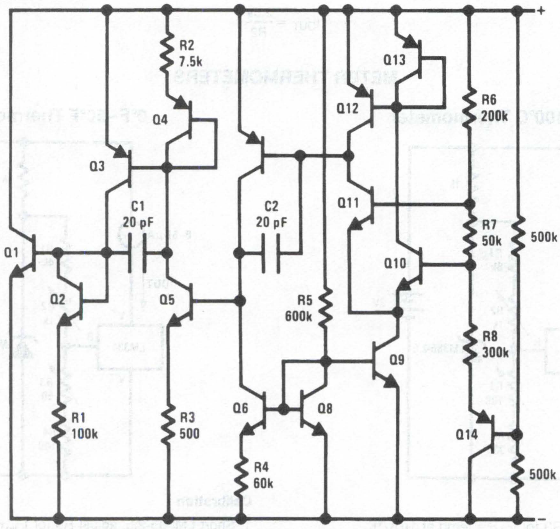
Typical supply current 50 µA

Improving Regulation of Adjustable Regulators


V_IN
LM338
5V
LM385-
2.5
375
120

TL/H/5519–7

Schematic Diagram


+
−
R2
7.5k
Q4
Q3
Q13
Q12
R6
200k
Q11
C1
20 pF
C2
20 pF
R7
50k
500k
Q1
Q10
Q2
Q5
R5
600k
R8
300k
Q9
Q6
Q8
Q14
R1
100k
R3
500
R4
60k
500k

TL/H/5519–1

National Semiconductor Corporation

LM185/285/385 Adjustable Micropower Voltage Reference

General Description

The LM185/LM285/LM385 are micropower 3-terminal adjustable band-gap voltage reference diodes. Operating from 1.24 to 5.3V and over a 10 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185 band-gap reference uses only transistors and resistors, low noise and good long-term stability result.

Careful design of the LM185 has made the device tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

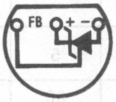
The LM185 is rated for operation over a −55°C to 125°C temperature range, while the LM285 is rated −40°C to 85°C and the LM385 0°C to 70°C. The LM185 is available in a hermetic TO-46 package and the LM285/LM385 are available in a low-cost TO-92 molded package, as well as S.O.

Features

- Adjustable from 1.24V to 5.30V
- Operating current of 10 μA to 20 mA
- 1% and 2% initial tolerance
- 1 Ω dynamic impedance
- Low temperature coefficient

Connection Diagrams

TO-92
Plastic Package

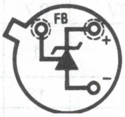


TL/H/5250-9

Bottom View

Order Number LM285BXZ, LM285BYZ, LM285Z, LM385BXZ, LM385BYZ or LM385Z
See NS Package Number Z03A

TO-46
Metal Can Package

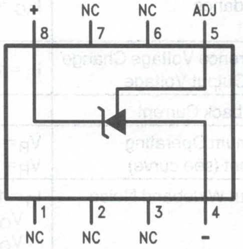


TL/H/5250-1

Bottom View

Order Number LM185BH, LM185BXH or LM185BYH
See NS Package Number H03A

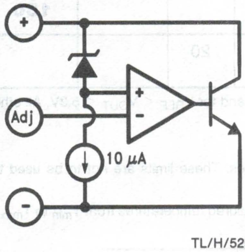
SO Package



TL/H/5250-10

Order Number LM285M or LM385M
See NS Package Number M08A

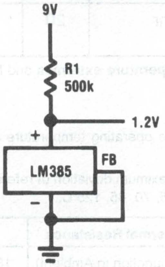
Block Diagram



TL/H/5250-13

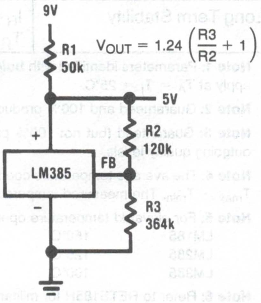
Typical Applications

1.2V Reference



TL/H/5250-14

5.0V Reference



TL/H/5250-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 6)

Reverse Current	30 mA
Forward Current	10 mA
Operating Temperature Range	
LM185 Series	−55°C to 125°C
LM285 Series	−40°C to 85°C
LM385 Series	0°C to 70°C
Storage Temperature	−55°C to 150°C

Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See An-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM185BX, LM185BY, LM185B, LM285BX, LM285BY, LM285			LM385BX, LM385BY, LM385			Unit Limit
		Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
Reference Voltage	$I_R = 100\ \mu A$ B-Series	1.240	1.252 **1.255** 1.228 **1.215**		1.240	1.252 1.228	**1.255** **1.215**	V_{max} V_{min}
	LM285 and LM385	1.240	1.265 1.215	**1.270** **1.205**		1.265 1.215	**1.270** **1.205**	V_{max} V_{min}
Reference Voltage Change with Current	$I_{min} < I_R < 1$ mA 1 mA $< I_R < 20$ mA	0.2 4	1 10	**1.5** **20**	0.2 5	1 15	**1.5** **25**	mV max mV max
Dynamic Output Impedance	$I_R = 100\ \mu A$, $f = 100$ Hz $I_{AC} = 0.1\ I_R$ $V_R = V_{REF}$ $V_R = 5.3V$	0.3 0.7			0.4 1			ohm ohm
Reference Voltage Change with Output Voltage	$I_R = 100\ \mu A$	1	3	**6**	2	5	**10**	mV max
Feedback Current		13	20	**25**	16	30	**35**	nA max
Minimum Operating Current (see curve)	$V_R = V_{REF}$ $V_R = 5.3V$	6 30	9 45	**10** **50**	7 35	11 55	**13** **60**	µA min µA min
Output Wideband Noise	$I_R = 100\ \mu A$, 10 Hz $< f <$ 10 kHz $V_{OUT} = V_{REF}$ $V_{OUT} = 5.3V$	50 170			50 170			µV rms µV rms
Average Temperature Coefficient (Note 4)	$I_R = 100\ \mu A$ X-Series		**30**			**30**		ppm/°C max
	Y-Series		**50**			**50**		ppm/°C max
	LM185B, LM285 and LM385			**150**			**150**	ppm/°C max
Long Term Stability	$I_R = 100\ \mu A$, T = 1000 hr $T_R = 25°C \pm 0.1°C$	20			20			ppm

Note 1: Parameters identified with **boldface type apply at temperature extremes** and for $I_{min} < I_R < 20$ mA and for $V_{REF} < V_{OUT} < 5.3V$. All other numbers apply at $T_A = T_j = 25°C$.

Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature and input current ranges. These limits are not to be used to calculate outgoing quality levels.

Note 4: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures from T_{min} to T_{max}, divided by $T_{max} - T_{min}$. The measured temperatures are −55, −40, 0, 25, 70, 85, 125°C.

Note 5: For elevated temperature operation, T_j max is:

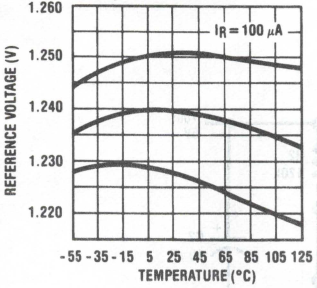
LM185	150°C
LM285	125°C
LM385	100°C

Note 6: Refer to RETS185H for military specifications.

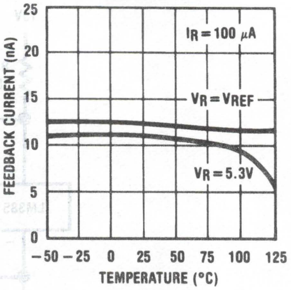
Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4″ leads) 170°C/W (0.125″ leads)	440°C/W	165°C/W
θ_{jc} (Junction to Case)	n/a	80°C/W	n/a

Typical Performance Characteristics

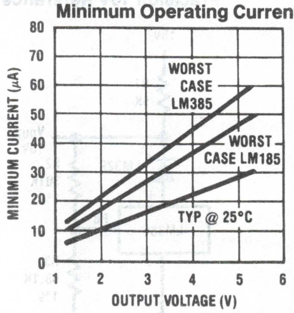
Temperature Drift



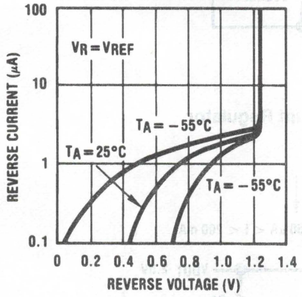
Feedback Current



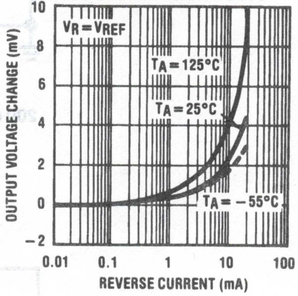
Minimum Operating Current



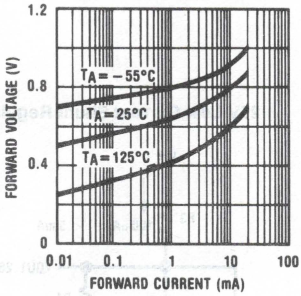
Reverse Characteristics



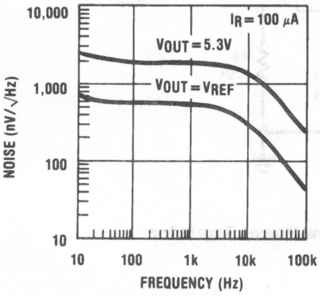
Reverse Characteristics



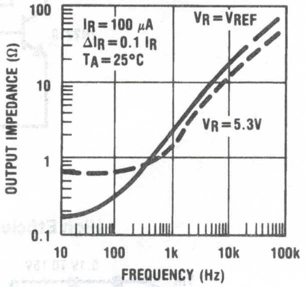
Forward Characteristics



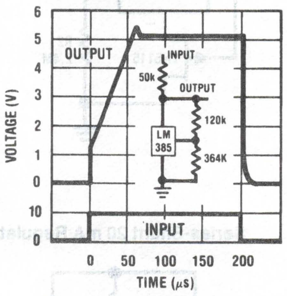
Output Noise Voltage



Dynamic Output Impedance



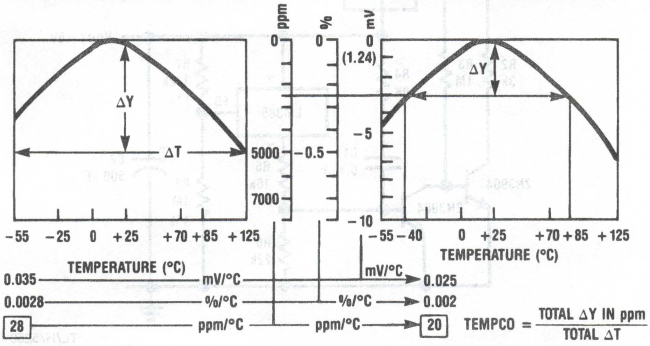
Response Time



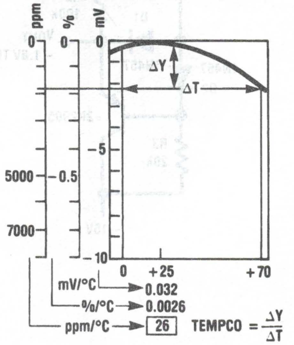
TL/H/5250-3

LM185 Temperature Coefficient Typical

LM285 Temperature Coefficient Typical



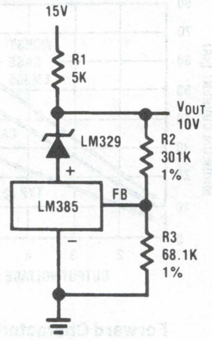
LM385 Temperature Coefficient Typical



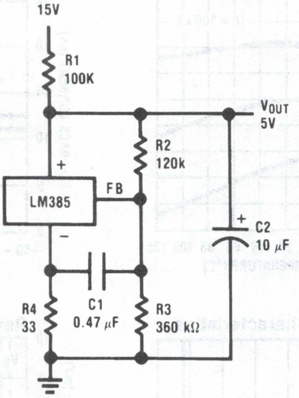
TL/H/5250-4

Typical Applications (Continued)

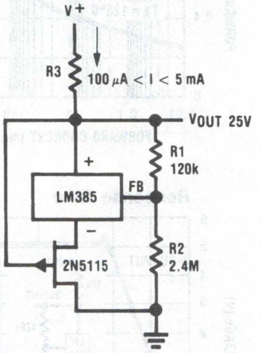
Precision 10V Reference


15V
R1
5K
VOUT
10V
LM329
+
R2
301K
1%
LM385
FB
R3
68.1K
1%

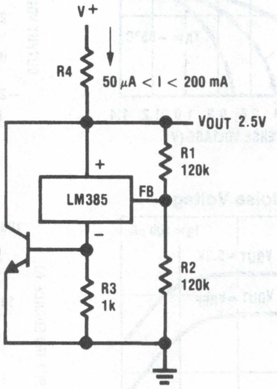
Low AC Noise Reference


15V
R1
100K
VOUT
5V
R2
120k
+
LM385
FB
–
+
C2
10 μF
R4
33
C1
0.47 μF
R3
360 kΩ

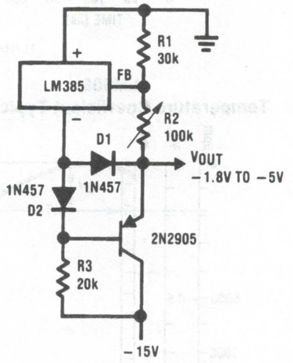
25V Low Current Shunt Regulator


V+
R3
100 μA < I < 5 mA
VOUT 25V
R1
120k
+
LM385
FB
–
R2
2.4M
2N5115

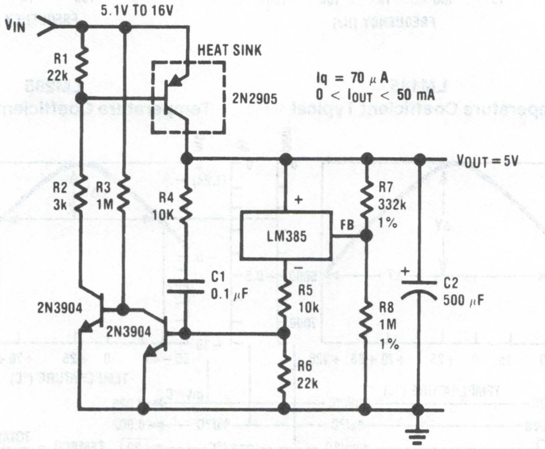
200 mA Shunt Regulator


V+
R4
50 μA < I < 200 mA
VOUT 2.5V
R1
120k
+
LM385
FB
–
2N2219
R3
1k
R2
120k

Series-Shunt 20 mA Regulator


+
LM385
FB
R1
30k
–
R2
100k
D1
VOUT
–1.8V TO –5V
1N457
1N457
D2
2N2905
R3
20k
–15V

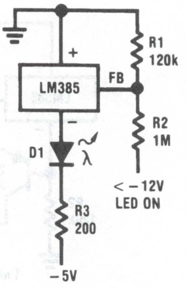
High Efficiency Low Power Regulator


5.1V TO 16V
VIN
R1
22k
HEAT SINK
2N2905
Iq = 70 μA
0 < IOUT < 50 mA
VOUT = 5V
R2
3k
R3
1M
R4
10K
+
LM385
FB
–
R7
332k
1%
C1
0.1 μF
R5
10k
+
C2
500 μF
R8
1M
1%
2N3904
2N3904
R6
22k

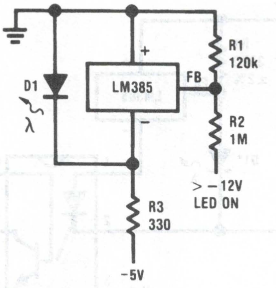
TL/H/5250-5

Typical Applications (Continued)

Voltage Level Detector

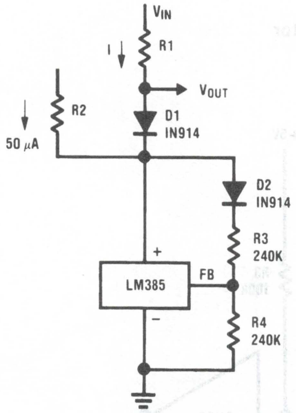

LM385
+
FB
−
R1
120k
R2
1M
D1
λ
R3
200
< −12V
LED ON
−5V

Voltage Level Detector


D1
λ
LM385
+
FB
−
R1
120k
R2
1M
R3
330
> −12V
LED ON
−5V

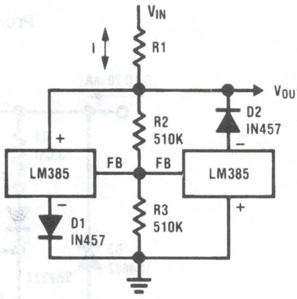
Fast Positive Clamp

2.4V + ΔV$_{D1}$


V$_{IN}$
I
R1
V$_{OUT}$
R2
50 μA
D1
IN914
D2
IN914
R3
240K
R4
240K
LM385
+
FB
−

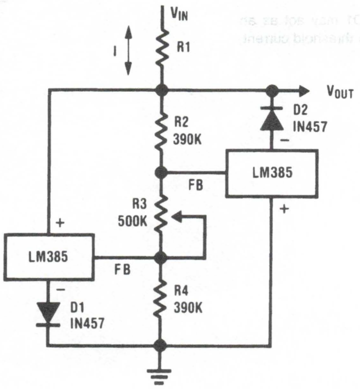
Bidirectional Clamp

±2.4V


V$_{IN}$
I
R1
V$_{OUT}$
D2
IN457
R2
510K
LM385
+
FB
−
D1
IN457
R3
510K
FB
LM385
−
+

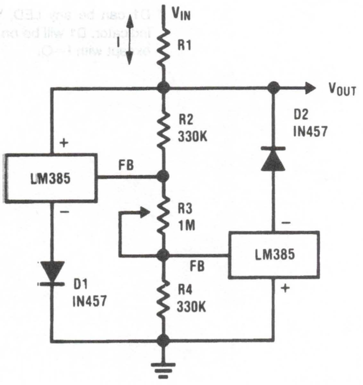
Bidirectional Adjustable Clamp

±1.8V to ±2.4V


V$_{IN}$
I
R1
V$_{OUT}$
D2
IN457
R2
390K
LM385
−
FB
+
R3
500K
LM385
+
FB
−
D1
IN457
R4
390K

Bidirectional Adjustable Clamp

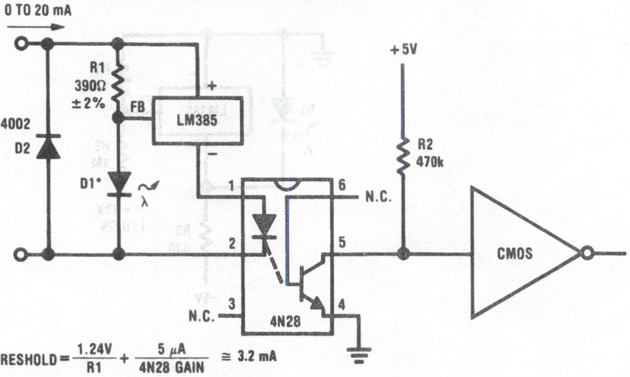
±2.4V to ±6V


V$_{IN}$
I
R1
V$_{OUT}$
R2
330K
D2
IN457
LM385
+
FB
−
R3
1M
D1
IN457
FB
LM385
−
+
R4
330K

TL/H/5250–6

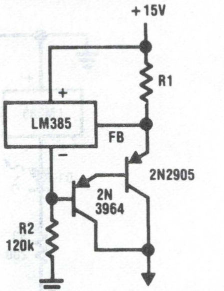
Typical Applications (Continued)

Simple Floating Current Detector


0 TO 20 mA
R1
390Ω
±2%
FB
LM385
+
−
1N4002
D2
D1*
λ
+5V
R2
470k
1
2
3
6
5
4
N.C.
N.C.
4N28
CMOS

$$I_{THRESHOLD} = \frac{1.24V}{R1} + \frac{5\ \mu A}{4N28\ GAIN} \cong 3.2\ mA$$

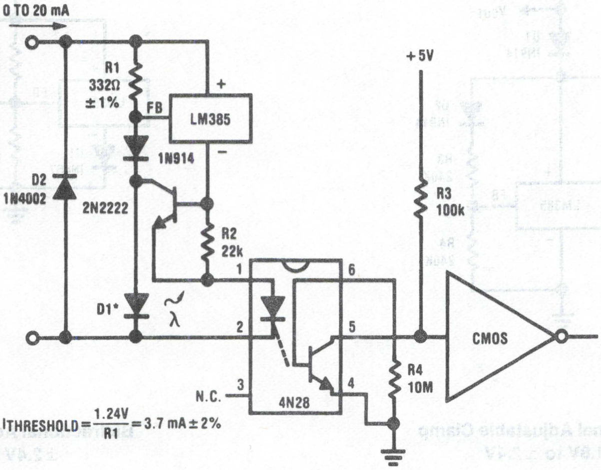
Current Source


+15V
R1
+
LM385
FB
−
2N2905
2N
3964
R2
120k

$1\ \mu A < I_{OUT} < 100\ mA$

$$I_{OUT} = \frac{1.24V}{R1}$$

Precision Floating Current Detector


0 TO 20 mA
R1
332Ω
±1%
FB
LM385
+
−
1N914
D2
1N4002
2N2222
R2
22k
D1*
λ
+5V
R3
100k
1
2
3
6
5
4
N.C.
4N28
R4
10M
CMOS

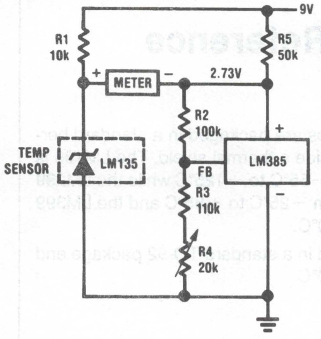
$$I_{THRESHOLD} = \frac{1.24V}{R1} = 3.7\ mA \pm 2\%$$

TL/H/5250-7

* D1 can be any LED, $V_F = 1.5V$ to $2.2V$ at 3 mA. D1 may act as an indicator. D1 will be on if $I_{THRESHOLD}$ falls below the threshold current, except with $I = O$.

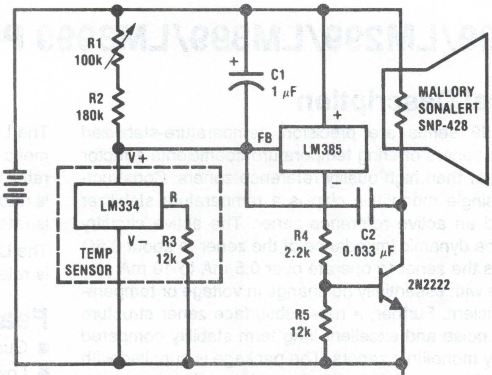
Typical Applications (Continued)

Centigrade Thermometer, 10 mV/°C


9V
R1
10k
R5
50k
+
METER
−
2.73V
R2
100k
+
TEMP
SENSOR
LM135
LM385
FB
−
R3
110k
R4
20k

TL/H/5250–11

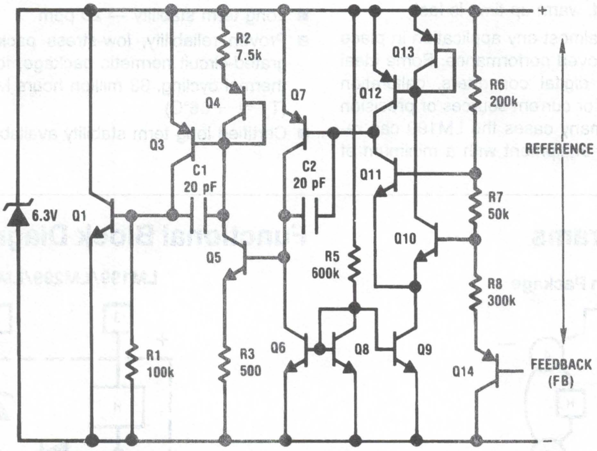
Freezer Alarm


R1
100k
+
C1
1 μF
MALLORY
SONALERT
SNP-428
R2
180k
+
FB
LM385
V+
4.5V
LM334
R
C2
0.033 μF
TEMP
SENSOR
V−
R3
12k
R4
2.2k
2N2222
R5
12k

BEEPS AT TEMPERATURES ABOVE THAT SET BY R1 (RANGE IS −30°F to +120°F)

TL/H/5250–12

Schematic Diagram


+
R2
7.5k
Q13
Q7
Q4
Q12
R6
200k
Q3
REFERENCE
C1
20 pF
C2
20 pF
Q11
R7
50k
6.3V
Q1
Q10
Q5
R5
600k
R8
300k
R1
100k
R3
500
Q6
Q8
Q9
Q14
FEEDBACK
(FB)
−

TL/H/5250–8

National
Semiconductor
Corporation

LM199/LM299/LM399/LM3999 Precision Reference

General Description

The LM199 series are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199 series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

The LM199 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199 can replace references in existing equipment with a minimum of wiring changes.

The LM199 series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299 is rated for operation from −25°C to +85°C and the LM399 is rated from 0°C to +70°C.

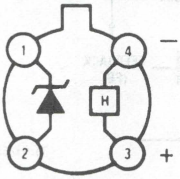
The LM3999 is packaged in a standard TO-92 package and is rated from 0°C to +70°C

Features

- Guaranteed 0.0001%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400 μA
- Wide operating current — 500 μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300 mW at 25°C
- Long term stability — 20 ppm
- Proven reliability, low-stress packaging in TO-46 integrated-circuit hermetic package, for low hysteresis after thermal cycling. 33 million hours MTBF at T_A = +25°C (T_J = +86°C)
- Certified long term stability available

Connection Diagrams

Metal Can Package

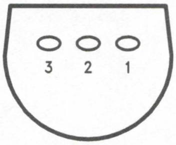


TL/H/5717–14

Top View

LM199/LM299/LM399 (See Table on fourth page)
NS Package Number H04D

Plastic Package TO-92



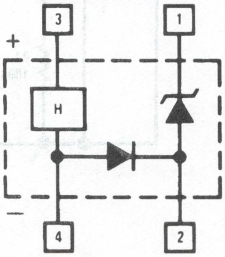
TL/H/5717–10

Bottom View

LM3999 (See Table on fourth page)
NS Package Number Z03A

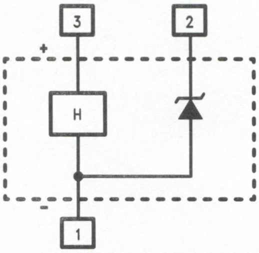
Functional Block Diagrams

LM199/LM299/LM399



TL/H/5717–15

LM3999



TL/H/5717–11

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the following Reliability Electrical Test Specifications documents: RETS199X for LM199, RETS199AX for LM199A.

Temperature Stabilizer Voltage	
LM199/LM299/LM399	40V
LM3999	36V
Reverse Breakdown Current	20 mA
Forward Current	
LM199/LM299/LM399	1 mA
LM3999	−0.1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	40V −0.1V
Operating Temperature Range	
LM199	−55°C to +125°C
LM299	−25°C to +85°C
LM399/LM3999	−0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
TO-92 package (10 sec.)	+260°C
TO-46 package (10 sec.)	+300°C

Electrical Characteristics (Note 2)

Parameter	Conditions		LM199/LM299			LM399			Units
			Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	0.5 mA ≤ I_R ≤ 10 mA		6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change with Current	0.5 mA ≤ I_R ≤ 10 mA			6	9		6	12	mV
Reverse Dynamic Impedance	I_R = 1 mA			0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	−55°C≤T_A≤+85°C	LM199		0.00003	0.0001				%/°C
	+85°C≤T_A≤+125°C	LM199		0.0005	0.0015				%/°C
	−25°C≤T_A≤85°C	LM299		0.00003	0.0001				%/°C
	0°C≤T_A≤+70°C	LM399					0.00003	0.0002	%/°C
RMS Noise	10 Hz ≤ f ≤ 10 kHz			7	20		7	50	μV
Long Term Stability	Stabilized, 22°C≤T_A≤28°C, 1000 Hours, I_R=1 mA±0.1%			20			20		ppm
Temperature Stabilizer Supply Current	T_A=25°C, Still Air, V_S=30V T_A = − 55°C			8.5 22	14 28		8.5	15	mA
Temperature Stabilizer Supply Voltage			9		40	9		40	V
Warm-Up Time to 0.05%	V_S = 30V, T_A = 25°C			3			3		sec.
Initial Turn-on Current	9≤V_S≤40, T_A=+25°C, (Note 3)			140	200		140	200	mA

Electrical Characteristics (Note 2)

Parameter	Conditions	LM3999			Units
		Min	Typ	Max	
Reverse Breakdown Voltage	0.6 mA ≤ I_R ≤ 10 mA	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change with Current	0.6 mA ≤ I_R ≤ 10 mA		6	20	mV
Reverse Dynamic Impedance	I_R = 1 mA		0.6	2.2	Ω
Reverse Breakdown Temperature Coefficient	0°C ≤ T_A ≤ 70°C		0.0002	0.0005	%/°C
RMS Noise	10 Hz ≤ f ≤ 10 kHz		7		μV
Long Term Stability	Stabilized, 22°C ≤ T_A ≤ 28°C, 1000 Hours, I_R = 1 mA ±0.1%		20		ppm
Temperature Stabilizer	T_A = 25°C, Still Air, V_S = 30V		12	18	mA
Temperature Stabilizer Supply Voltage				36	V
Warm-Up Time to 0.05%	V_S = 30V, T_A = 25°C		5		sec.
Initial Turn-On Current	9 ≤ V_S ≤ 40, T_A = 25°C		140	200	mA

Electrical Characteristics (Note 2)

Parameter	Conditions	LM199A, LM299A Min	LM199A, LM299A Typ	LM199A, LM299A Max	LM399A Min	LM399A Typ	LM399A Max	Units
Reverse Breakdown Voltage	$0.5\text{ mA} \le I_R \le 10\text{ mA}$	6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change with Current	$0.5\text{ mA} \le I_R \le 10\text{ mA}$		6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\text{ mA}$		0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \le T_A \le +85°C$ LM199A		0.00002	0.00005				%/°C
	$+85°C \le T_A \le +125°C$ LM199A		0.0005	0.0010				%/°C
	$-25°C \le T_A \le 85°C$ LM299A		0.00002	0.00005				%/°C
	$0°C \le T_A \le +70°C$ LM399A					0.00003	0.0001	%/°C
RMS Noise	$10\text{ Hz} \le f \le 10\text{ kHz}$		7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\text{ mA} \pm 0.1\%$		20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$		8.5	14		8.5	15	mA
	$T_A = -55°C$		22	28				
Temperature Stabilizer Supply Voltage		9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		3			3		sec.
Initial Turn-on Current	$9 \le V_S \le 40$, $T_A = +25°C$, (Note 3)		140	200		140	200	mA

Electrical Characteristics (Note 2)

Parameter	Conditions	LM199AH-20, LM299AH-20 Min	LM199AH-20, LM299AH-20 Typ	LM199AH-20, LM299AH-20 Max	LM399AH-50 Min	LM399AH-50 Typ	LM399AH-50 Max	Units
Reverse Breakdown Voltage	$0.5\text{ mA} \le I_R \le 10\text{ mA}$	6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5\text{ mA} \le I_R \le 10\text{ mA}$		6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\text{ mA}$		0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \le T_A \le 85°$ LM199A		0.00002	0.00005				%/°C
	$85°C \le T_A \le 125°C$ LM199A		0.0005	0.0010				%/°C
	$-25°C \le T_A \le 85°C$ LM299A		0.00002	0.00005				%/°C
	$0°C \le T_A \le 70°C$ LM399A					0.00003	0.0001	%/°C
RMS Noise	$10\text{ Hz} \le f \le 10\text{ kHz}$		7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\text{ mA} \pm 0.1\%$		8	20		9	50	ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$		8.5	14		8.5	15	mA
	$T_A = 55°C$		22	28				
Temperature Stabilizer Supply Voltage		9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		3			3		s
Initial Turn-on Current	$9 \le V_S \le 40$, $T_A = 25°C$, (Note 3)		140	200		140	200	mA

Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \le T_A \le +125°C$ for the LM199; $-25°C \le T_A \le +85°C$ for the LM299 and $0°C \le T_A \le +70°C$ for the LM399 and LM3999.

Note 3: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

Note 4: Do not wash the LM199 with its polysulfone thermal shield in TCE.

Ordering Information

Initial Tolerance	0°C to +70°C	−25°C to +85°C	−55°C to +125°C	NS Package
2%		LM299AH	LM199AH	H04D
5%	LM399H LM399AH	LM299H	LM199H	H04D
5%	LM3999Z			Z03A
Guaranteed Long Term Stability	LM399AH-50	LM299AH-20	LM199AH-20	H04D

Certified Long Term Drift

The National Semiconductor LM199AH-20, LM299AH-20, and LM399AH-50 are ultra-stable Zener references specially selected from the production runs of LM199AH, LM299AH, LM399AH and tested to confirm a long-term stability of 20, 20, or 50 ppm per 1000 hours, respectively. The devices are measured every 168 hours and the voltage of each device is logged and compared in such a way as to show the deviation from its initial value. Each measurement is taken with a probable-worst-case deviation of ±2 ppm, compared to the Reference Voltage, which is derived from several groups of NBS-traceable references such as LM199AH-20's, 1N827's, and saturated standard cells, so that the deviation of any one group will not cause false indications. Indeed, this comparison process has recently been automated using a specially prepared computer program which is custom-designed to reject noisy data (and require a repeat reading) and to record the average of the best 5 of 7 readings, just as a sagacious standards engineer will reject unbelievable readings.

The typical characteristic for the LM199AH-20 is shown below. This computerized print-out form of each reference's stability is shipped with the unit.

Typical Characteristics

National Semiconductor
Certified Long Term Drift

Hrs	Drift
168	−20
336	−24
504	−36
672	−34
840	−40
1008	−36

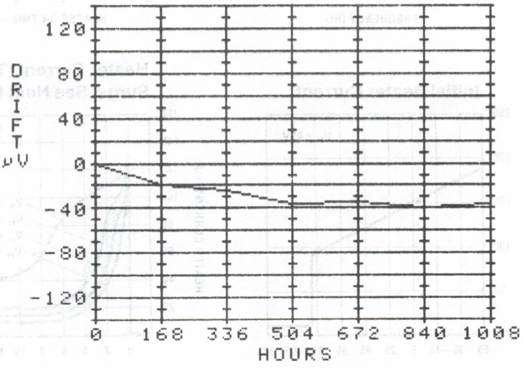
LM199AH-20
Part #6849

Limits

LM199AH-20	140 μV
LM299AH-20	140 μV
LM399AH-20	350 μV

Testing Conditions

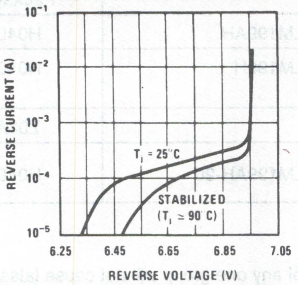
Heater Voltage	30V
Zener Current	1 mA
Ambient Temp.	25°C



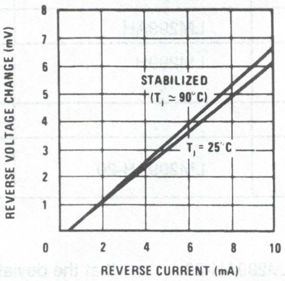
TL/H/5717-12

Typical Performance Characteristics

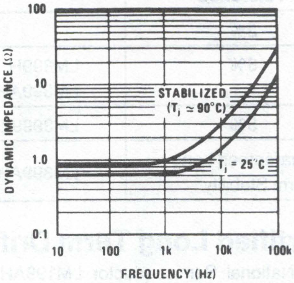
Reverse Characteristics



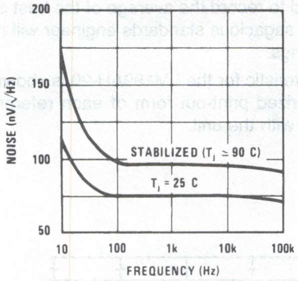
Reverse Voltage Change



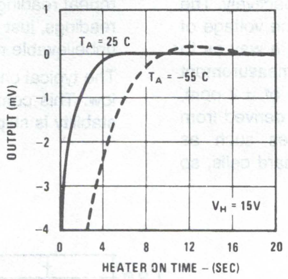
Dynamic Impedance



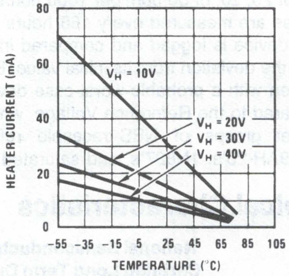
Zener Noise Voltage



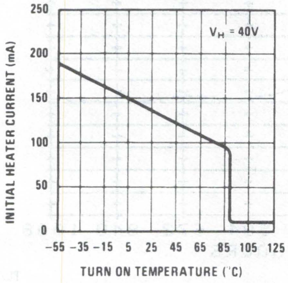
Stabilization Time



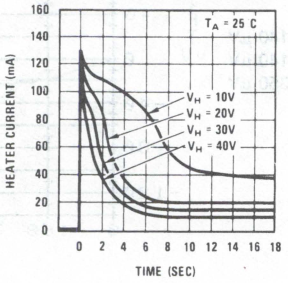
Heater Current



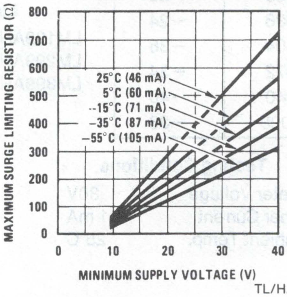
Initial Heater Current



Heater Current (To Limit This Surge, See Next Graph)



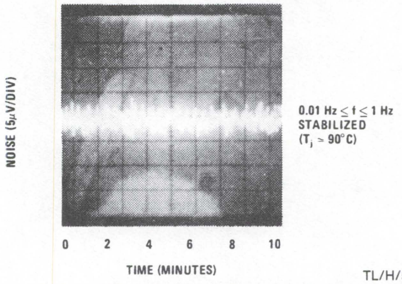
Heater Surge Limit Resistor vs Minimum Supply Voltage at Various Minimum Temperatures



TL/H/5717–2

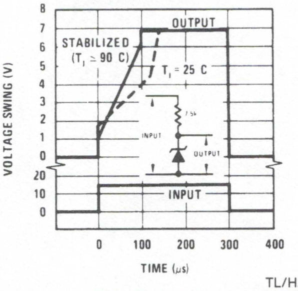
*Heater must be bypassed with a 2 μF or larger tantalum capacitor if resistors are used.

Low Frequency Noise Voltage



TL/H/5717–3

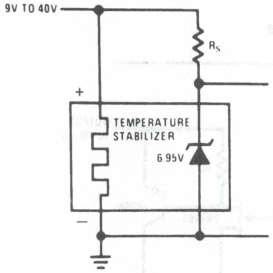
Response Time



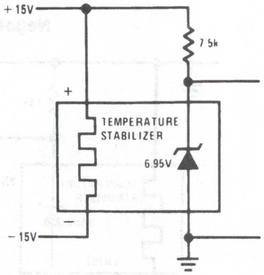
TL/H/5717–7

Typical Applications

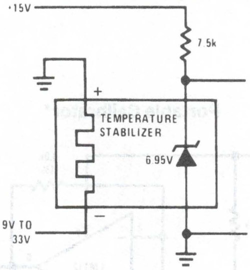
Single Supply Operation


9V TO 40V
R_S
+
TEMPERATURE
STABILIZER
6.95V
−

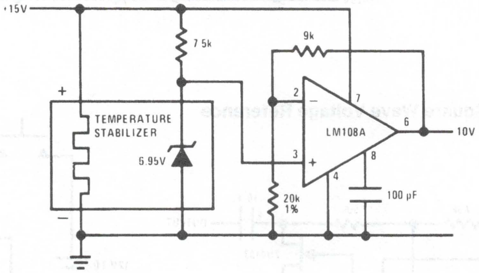
Split Supply Operation


+15V
7.5k
+
TEMPERATURE
STABILIZER
6.95V
−
−15V

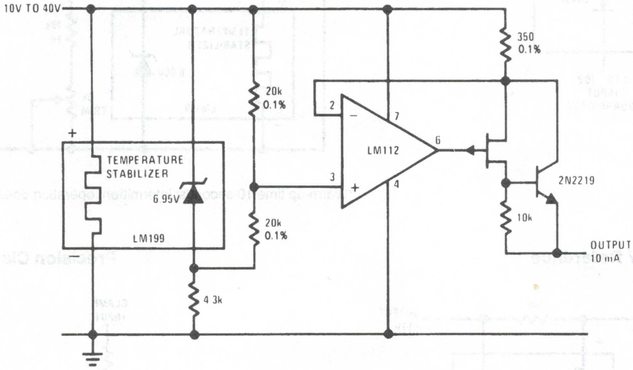
Negative Heater Supply with Positive Reference


+15V
7.5k
+
TEMPERATURE
STABILIZER
6.95V
−
9V TO
33V

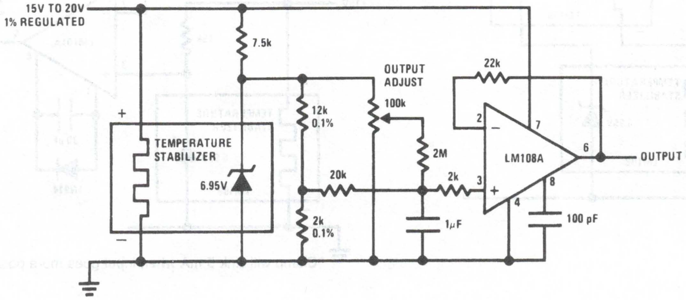
Buffered Reference With Single Supply


+15V
7.5k
9k
+
TEMPERATURE
STABILIZER
6.95V
−
2
3
7
6
8
4
LM108A
10V
20k
1%
100 pF

Positive Current Source


10V TO 40V
350
0.1%
20k
0.1%
+
TEMPERATURE
STABILIZER
6.95V
LM199
−
2
3
7
6
4
LM112
2N2219
20k
0.1%
10k
4.3k
OUTPUT
10 mA

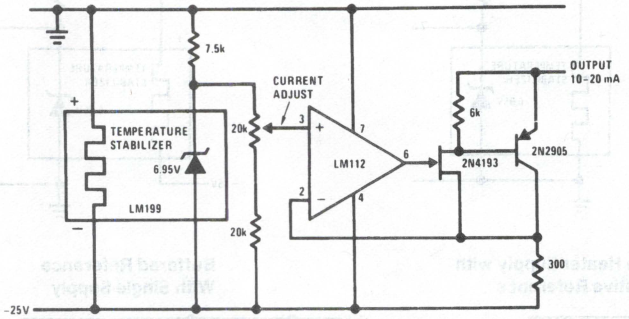
Standard Cell Replacement


15V TO 20V
1% REGULATED
7.5k
OUTPUT
ADJUST
100k
22k
12k
0.1%
+
TEMPERATURE
STABILIZER
6.95V
−
20k
2M
2k
2
3
7
6
8
4
LM108A
OUTPUT
2k
0.1%
1 μF
100 pF

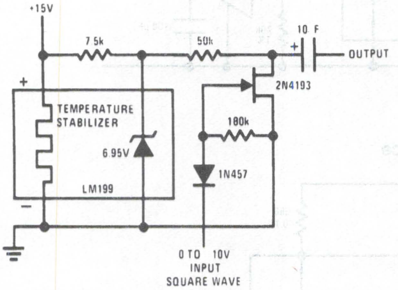
TL/H/5717-4

Typical Applications (Continued)

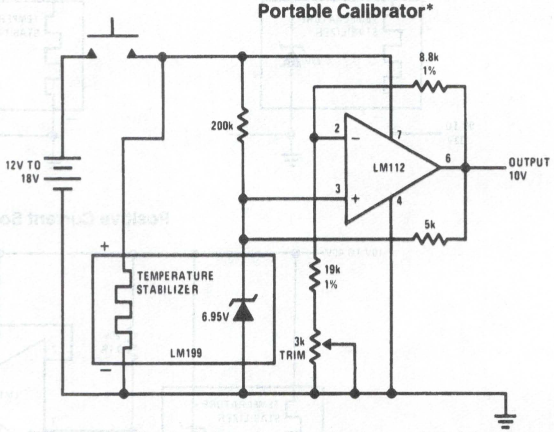
Negative Current Source


7.5k
CURRENT
ADJUST
20k
20k
TEMPERATURE
STABILIZER
6.95V
LM199
+
−
3
2
7
4
6
LM112
2N4193
2N2905
6k
OUTPUT
10–20 mA
300
−25V

Square Wave Voltage Reference

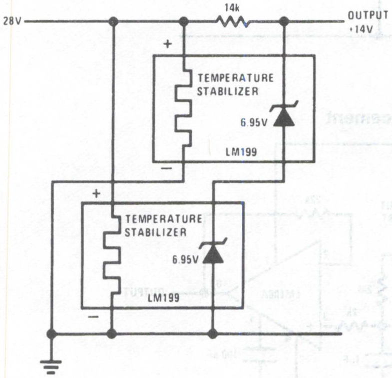

+15V
7.5k
50k
10 F
OUTPUT
2N4193
180k
1N457
TEMPERATURE
STABILIZER
6.95V
LM199
+
−
0 TO 10V
INPUT
SQUARE WAVE

Portable Calibrator*

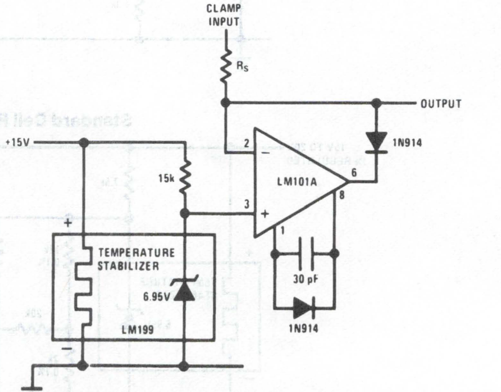

12V TO
18V
200k
8.8k
1%
2
3
7
4
6
LM112
OUTPUT
10V
5k
19k
1%
3k
TRIM
TEMPERATURE
STABILIZER
6.95V
LM199
+
−

*Warm-up time 10 seconds; intermittent operation does not degrade long term stability.

14V Reference


28V
14k
OUTPUT
+14V
TEMPERATURE
STABILIZER
6.95V
LM199
+
−
TEMPERATURE
STABILIZER
6.95V
LM199
+
−

Precision Clamp*

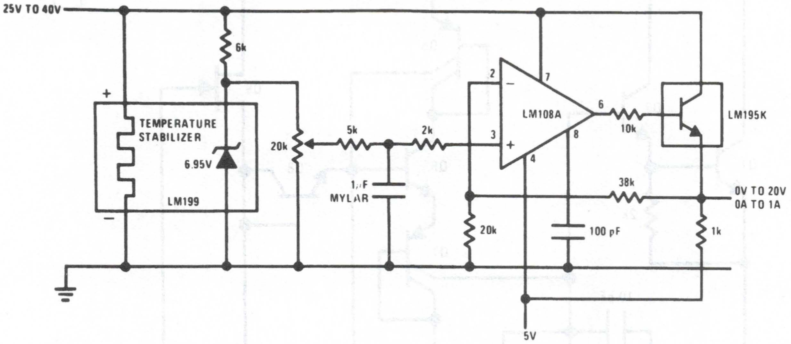

CLAMP
INPUT
R_S
OUTPUT
1N914
+15V
15k
2
3
6
8
1
LM101A
30 pF
1N914
TEMPERATURE
STABILIZER
6.95V
LM199
+
−

*Clamp will sink 5 mA when input goes more positive than reference

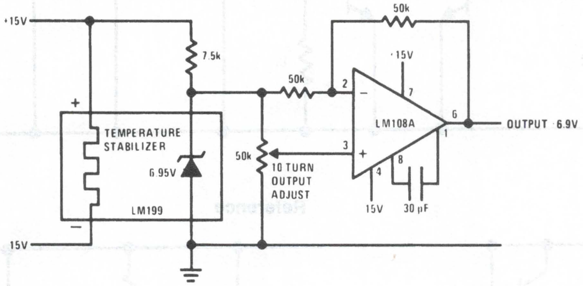
TL/H/5717-5

Typical Applications (Continued)

0V to 20V Power Reference

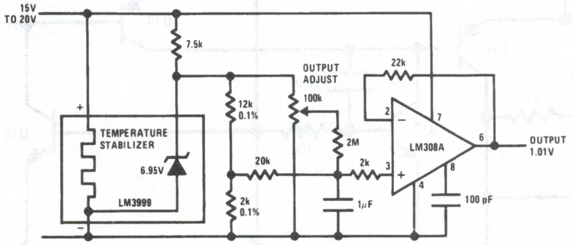

25V TO 40V
6k
+
TEMPERATURE STABILIZER
6.95V
LM199
−
20k
5k
2k
1μF MYLAR
2
7
LM108A
6
10k
LM195K
3
8
4
38k
0V TO 20V 0A TO 1A
20k
100 pF
1k
5V

Bipolar Output Reference


+15V
7.5k
+
TEMPERATURE STABILIZER
6.95V
LM199
−
15V
50k
+15V
50k
2
7
LM108A
6
OUTPUT 6.9V
1
3
8
4
50k
10 TURN OUTPUT ADJUST
15V
30 pF

TL/H/5717-6

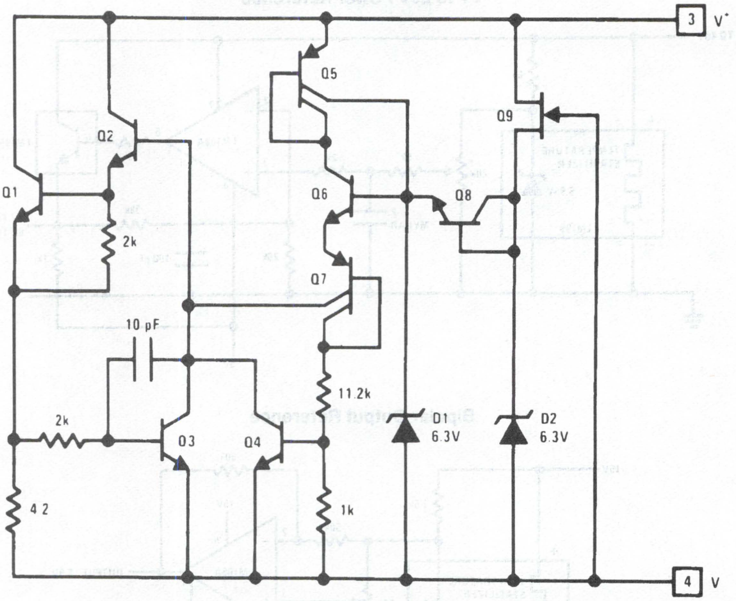
Voltage Reference


15V TO 20V
7.5k
+
TEMPERATURE STABILIZER
6.95V
LM3999
−
12k 0.1%
OUTPUT ADJUST
100k
22k
2
7
LM308A
6
OUTPUT 1.01V
2M
20k
2k
3
8
4
1μF
100 pF
2k 0.1%

TL/H/5717-9

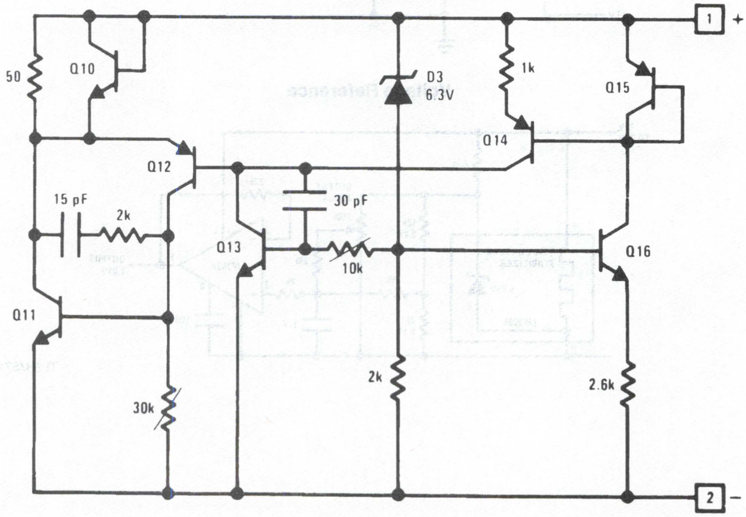
Schematic Diagrams

Temperature Stabilizer


3
V+
Q5
Q9
Q2
Q1
2k
Q6
Q8
Q7
10 pF
11.2k
2k
Q3
Q4
D1
6.3V
D2
6.3V
4 2
1k
4
V

TL/H/5717-01

Reference


1
+
50
Q10
D3
6.3V
1k
Q15
Q14
Q12
30 pF
15 pF
2k
Q13
10k
Q16
Q11
2k
2.6k
30k
2
−

TL/H/5717-13

National Semiconductor Corporation

PRELIMINARY

LM368-2.5 Precision Voltage Reference

General Description

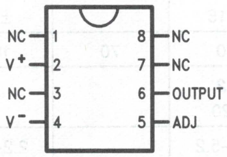
The LM368-2.5 is a precision, monolithic, temperature-compensated voltage reference. The LM368-2.5 makes use of thin-film technology enhanced by the discrete laser trimming of resistors to achieve excellent Temperature coefficient (Tempco) of V_{OUT} (as low as 11 ppm/°C), along with tight initial tolerance, (as low as 0.02%). The trim scheme is such that individual resistors are cut open rather than being trimmed (partially cut), to avoid resistor drift caused by electromigration in the trimmed area. The LM368-2.5 also provides excellent stability vs. changes in input voltage and output current. The output is short circuit proof. A trim pin is made available for fine trimming of V_{OUT} or for obtaining intermediate values without greatly affecting the Tempco of the device.

Features

- 400 µA operating current
- Low output impedance
- Excellent line regulation (.0001%/V typical)
- Single-supply operation
- Externally trimmable
- Low temperature coefficient
- Excellent initial accuracy (0.02% typical)
- Best reference available for low-voltage operation ($V_S = 5V$, $V_{REF} = 2.500V$)

Connection Diagrams

Dual-In-Line Package (N) or S.O. Package (M)

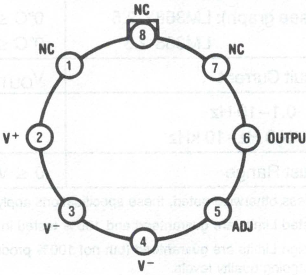


TL/H/8446-15

Top View

Order Number LM368M-2.5 or LM368N-2.5
See NS Package Number M08A or N08E

Metal Can Package



TL/H/8446-1

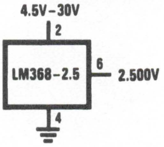
Top View

*case connected to V−

Order Number LM368H-2.5 LM368YH-2.5
See NS Package Number H08C

Typical Applications

Low Voltage Reference



TL/H/8446-2

Absolute Maximum Ratings (Note 7)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage	35V
Power Dissipation	600 mW
Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	0°C to +70°C

Soldering Information

DIP (N) Package (10 sec.)	+260°C
TO-5 (H) Package (10 sec.)	+300°C
SO (M) Package, Vapor Phase (60 sec.)	+215°C
Infrared (15 sec.)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM368-2.5			Units (Max. unless noted)
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OUT} Error: LM368		±0.02	±0.2		%
Line Regulation	$5.0V \leq V_{IN} \leq 30V$	±0.0001	±0.0005		%/V
Load Regulation (Note 8)	$0\ mA \leq I_{SOURCE} \leq 10\ mA$	±0.0003	±0.0025		%/mA
Thermal Regulation	T = 20 mS (Note 4)	±0.005	±0.02		%/100 mW
Quiescent Current		350	550		μA
Change of Quiescent Current vs. V_{IN}	$5.0V \leq V_{IN} \leq 30V$	3	5		μA/V
Temperature Coefficient of V_{OUT} (see graph): LM368Y-2.5	$0°C \leq T_A \leq 70°C$	±11	±20		ppm/°C
(Note 5) LM368-2.5	$0°C \leq T_A \leq 70°C$	±15		±30	ppm/°C
Short Circuit Current	$V_{OUT} = 0$	30	70	100	mA
Noise: 0.1–10 Hz		12			uVp-p
100 Hz–10 kHz		420			$nV/\sqrt{Hz}$
V_{OUT} Adjust Range	$0 \leq V_{PIN5} \leq V_{OUT}$	1.9–5.2		2.2–5.0	V min.

Note 1: Unless otherwise noted, these specifications apply: $T_A = 25°C$, $4.9V \leq V_{IN} \leq 10.5V$, $0 \leq I_{LOAD} \leq 0.5\ mA$, $0 \leq C_L \leq 200\ pF$.

Note 2: Tested Limits are guaranteed and 100% tested in production.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: Thermal Regulation is defined as the change in the output Voltage at a time T after a step change in power dissipation of 100 mW.

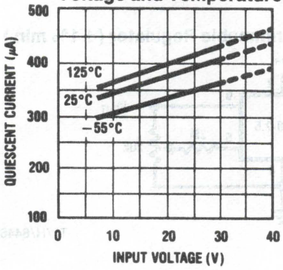
Note 5: Temperature Coefficient of V_{OUT} is defined as the worst case delta-V_{OUT} measured at Specified Temperatures divided by the total span of the Specified Temperature Range (See graphs). There is no guarantee that the Specified Temperatures are exactly at the minimum or maximum deviation.

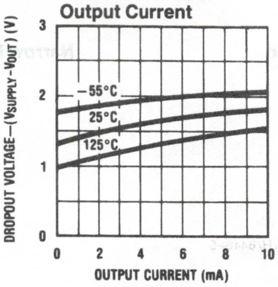
Note 6: In metal can (H), θ_{J-C} is 75°C/W and θ_{J-A} is 150°C/W. In plastic DIP, θ_{J-A} is 160°C/W. In SO-8, θ_{J-A} is 180°C/W, in TO-92, θ_{J-A} is 160°C/W.

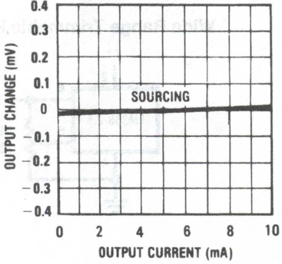
Note 7: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its Rated Operating Conditions (see Note 1 and Conditions).

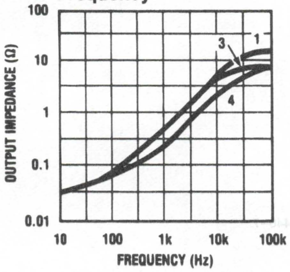
Note 8: Load regulation is measured on the output pin at a point ⅛″ below the base of the package. Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

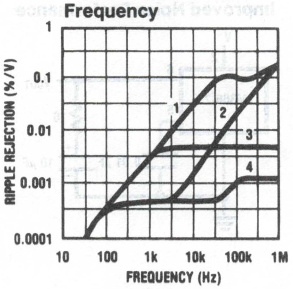
Typical Performance Characteristics (Note 1)


Quiescent Current vs. Input Voltage and Temperature


Dropout Voltage vs. Output Current


Output Change vs. Output Current


Output Impedance vs. Frequency

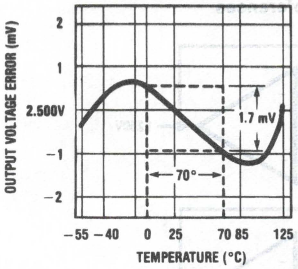

Ripple Rejection vs. Frequency

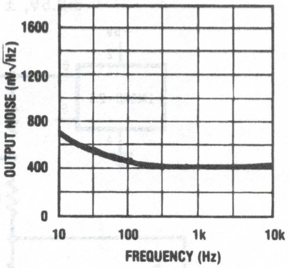
(1) LM368 as is.

(2) with 0.01 μf Mylar, Trim to Gnd.

(3) with 10Ω in series with 10 μf, V_{OUT} to Gnd.

(4) with Both.


Temperature Coefficient: LM368-2.5 (Curve A)

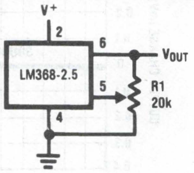

Output Noise vs. Frequency

TL/H/8446-3

Typical Temperature Coefficient Calculations:
LM368-2.5 (see Curve A)
T.C. = 1.7 mV/(70° × 2.5V)
= 9.7 ppm/°C

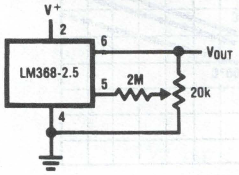
Typical Applications

Wide Range Trimmable Regulator


V+
2
6
VOUT
LM368-2.5
5
R1
20k
4

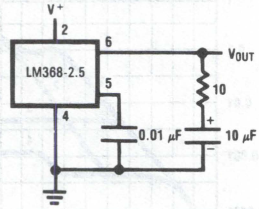
TL/H/8446-5

Narrow Range Trimmable Regulator (±1% min.)


V+
2
6
VOUT
LM368-2.5
5
2M
20k
4

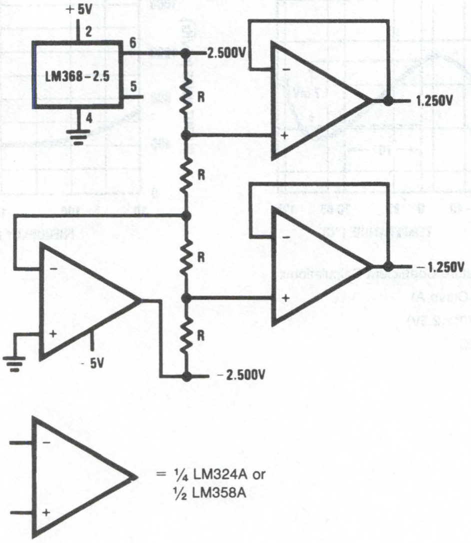
TL/H/8446-6

Improved Noise Performance


V+
2
6
VOUT
LM368-2.5
5
10
4
0.01 μF
+
10 μF

TL/H/8446-7

±2.5V, ±1.25V References

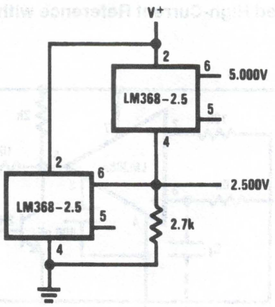

+5V
2
6
2.500V
LM368-2.5
5
4
R
1.250V
R
−1.250V
R
R
−5V
−2.500V
= ¼ LM324A or
½ LM358A

TL/H/8446-8

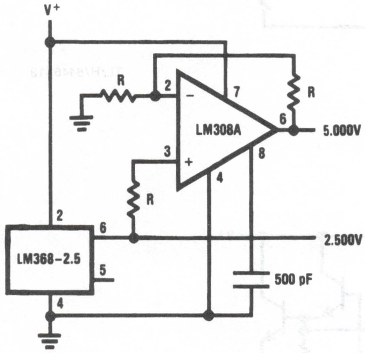
R= Thin Film Resistor Network,
±0.05% Matching and 5 ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
or similar.

Typical Applications (Continued)

Multiple Output Voltages


V+
2
6
5.000V
LM368-2.5
5
4
2
6
2.500V
LM368-2.5
5
2.7k
4

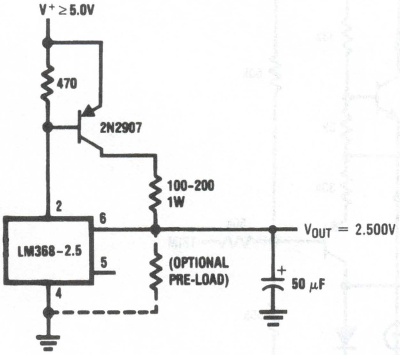
TL/H/8446-9


V+
R
2
−
7
R
LM308A
6
5.000V
3
+
8
4
R
2
6
2.500V
LM368-2.5
5
500 pF
4

R = Thin Film Resistor Network
0.05% Matching and 5 ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
or similar.

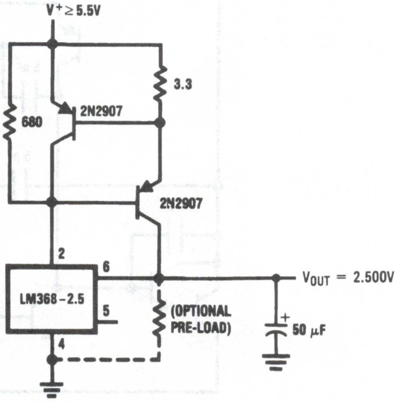
TL/H/8446-10

Reference with Booster


V+ ≥ 5.0V
470
2N2907
100-200
1W
2
6
VOUT = 2.500V
LM368-2.5
5
(OPTIONAL
PRE-LOAD)
+
50 μF
4

TL/H/8446-11

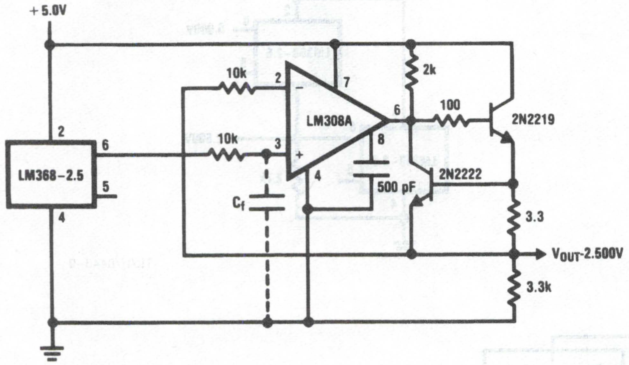
100 mA Boosted Reference


V+ ≥ 5.5V
3.3
2N2907
680
2N2907
2
6
VOUT = 2.500V
LM368-2.5
5
(OPTIONAL
PRE-LOAD)
+
50 μF
4

TL/H/8446-12

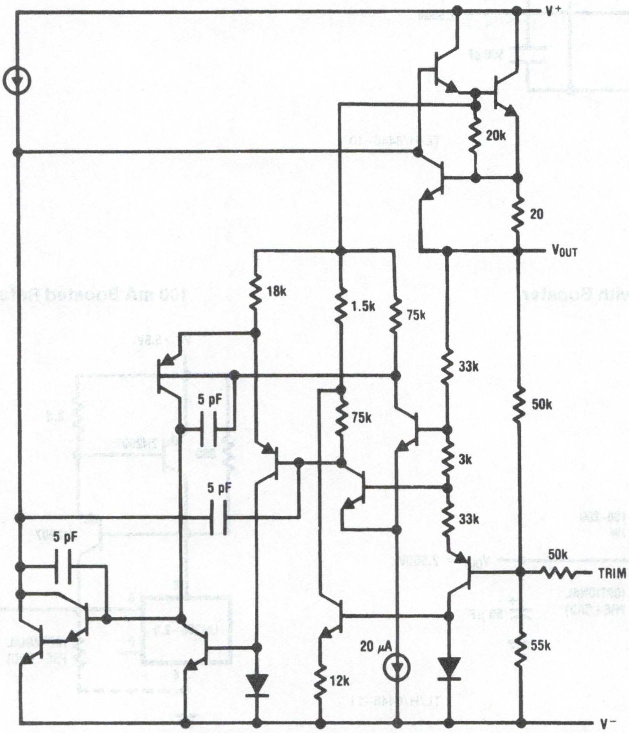
Typical Applications (Continued)

Buffered High-Current Reference with Filter


+5.0V
2
6
5
4
LM368-2.5
10k
2
10k
3
7
−
+
LM308A
6
8
4
500 pF
C$_f$
2k
100
2N2219
2N2222
3.3
V$_{OUT}$-2.500V
3.3k

TL/H/8446-13

Simplified Schematic Diagram


V+
20k
20
V$_{OUT}$
18k
1.5k
75k
33k
5 pF
75k
50k
3k
5 pF
33k
5 pF
50k
TRIM
20 µA
12k
55k
V−

TL/H/8446-14

*Reg. U.S. Pat. Off.

National Semiconductor Corporation

ADVANCED INFORMATION

LM581 Precision 10-Volt Voltage Reference

General Description

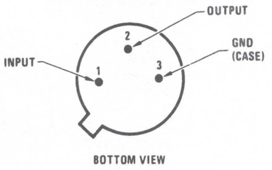
The LM581 Series are precision monolithic temperature-compensated voltage references. They are based on a buried zener reference as pioneered in the LM199 references, but do not require any heater, as they rely on special temperature-compensation techniques (Patent Pending). The LM581 makes use of thin-film technology enhanced by the discrete laser trimming of resistors to achieve excellent Temperature coefficient (Tempco) of V_{out} (as low as 1 ppm/°C), along with tight initial tolerances (as low as 0.01%). The trim scheme is such that individual resistors are cut open rather than being trimmed (partially cut), to avoid resistor drift caused by electromigration in the trimmed area. The LM581 also provides excellent stability vs. changes in input voltage and output current (both sourcing and sinking). The devices have a 10.000V output and will operate in either series or shunt mode; the output is short-circuit-proof to ground.

Features

- Low Tempco of V_{out}
- Excellent initial accuracy (0.008%)
- Excellent line regulation (2 ppm/V)
- Excellent output impedance
- Excellent thermal regulation
- Low noise
- Low dissipation — 20 mW
- Operates in series or shunt mode
- Direct replacement for AD581

Connection Diagram

Metal Can Package



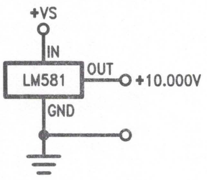
TL/H/9217-1

(Case is connected to ground.)

Order Number LM581JH, LM581KH, LM581LH, LM581SH, LM581TH or LM581UH
See NS Package Number H03B

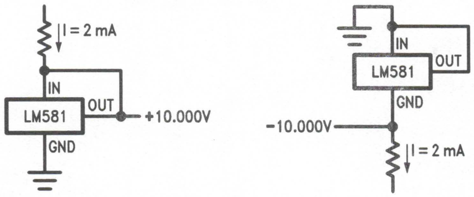
Typical Applications

Series Regulator



TL/H/9217-2

Shunt Regulators



TL/H/9217-4

TL/H/9217-3

Section 8

Surface Mount

Section 8 Contents

Surface Mount 8-3

National Semiconductor Corporation

Surface Mount

Cost pressures today are forcing many electronics manufacturers to automate their production lines. Surface mount technology plays a key role in this cost-savings trend because:

1. The mounting of devices on the PC board surface eliminates the expense of drilling holes;
2. The use of pick-and-place machines to assemble the PC boards greatly reduces labor costs;
3. The lighter and more compact assembled products resulting from the smaller dimensions of surface mount packages mean lower material costs.

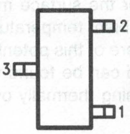
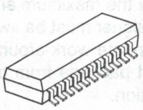
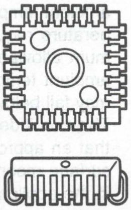
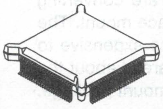
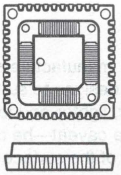
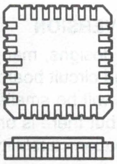
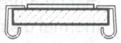
Production processes now permit both surface mount and insertion mount components to be assembled on the same PC board.

SURFACE MOUNT PACKAGING AT NATIONAL

To help our customers take advantage of this new technology, National has developed a line of surface mount packages. Ranging in lead counts from 3 to 360, the package offerings are summarized in Table I.

Lead center spacing keeps shrinking with each new generation of surface mount package. Traditional packages (e.g., DIPs) have a 100 mil lead center spacing. Surface mount packages currently in production (e.g., SOT, SOIC, PCC, LCC, LDCC) have a 50 mil lead center spacing. Surface mount packages in production release (e.g., PQFP) have a 25 mil lead center spacing. Surface mount packages in development (e.g., TAPEPAK™) will have a lead center spacing of only 12–20 mils.

TABLE I. Surface Mount Packages from National

Package Type	Small Outline Transistor (SOT)	Small Outline IC (SOIC)	Plastic Chip Carrier (PCC)	Plastic Quad Flat Pack (PQFP)	TAPEPAK™ (TP)	Leadless Chip Carrier (LCC)	Leaded Chip Carrier (LDCC)
							
Package Material	Plastic	Plastic	Plastic	Plastic	Plastic	Ceramic	Ceramic
Lead Bend	Gull Wing	Gull Wing	J-Bend	Gull Wing	Gull Wing	—	Gull Wing
Lead Center Spacing	50 Mils	50 Mils	50 Mils	25 Mils	20, 15, 12 Mils	50 Mils	50 Mils
Tape & Reel Option	Yes	Yes	Yes	tbd	tbd	No	No
Lead Counts	SOT-23 High Profile SOT-23 Low Profile	SO-8(*) SO-14(*) SO-14 Wide(*) SO-16(*) SO-16 Wide(*) SO-20(*) SO-24(*)	PCC-20(*) PCC-28(*) PCC-44(*) PCC-68 PCC-84 PCC-124	PQFP-84 PQFP-100 PQFP-132 PQFP-196(*) PQFP-244	TP-40 (*) TP-68 TP-84 TP-132 TP-172 TP-220 TP-284 TP-360	LCC-18 LCC-20(*) LCC-28 LCC-32 LCC-44 (*) LCC-48 LCC-52 LCC-68 LCC-84 LCC-124	LDCC-44 LDCC-68 LDCC-84 LDCC-124

*In production (or planned) for linear products.

LINEAR PRODUCTS IN SURFACE MOUNT

Linear functions available in surface mount include:

- Op amps
- Comparators
- Regulators
- References
- Data conversion
- Industrial
- Consumer
- Automotive

A complete list of linear part numbers in surface mount is presented in Table III. Refer to the datasheet in the appropriate chapter of this databook for a complete description of the device. In addition, National is continually expanding the list of devices offered in surface mount. If the functions you need do not appear in Table III, contact the sales office or distributor branch nearest you for additional information.

Automated manufacturers can improve their cost savings by using Tape-and-Reel for surface mount devices. Simplified handling results because hundreds-to-thousands of semiconductors are carried on a single Tape-and-Reel pack (see ordering and shipping information—printed later in this section—for a comparison of devices/reel vs. devices/rail for those surface mount package types being used for linear products). With this higher device count per reel (when compared with less than a 100 devices per rail), pick-and-place machines have to be re-loaded less frequently and lower labor costs result.

With Tape-and-Reel, manufacturers save twice—once from using surface mount technology for automated PC board assembly and again from less device handling during shipment and machine set-up.

BOARD CONVERSION

Besides new designs, many manufacturers are converting existing printed circuit board designs to surface mount. The resulting PCB will be smaller, lighter and less expensive to manufacture; but there is one caveat—be careful about the thermal dissipation capability of the surface mount package.

Because the surface mount package is smaller than the traditional dual-in-line package, the surface mount package is not capable of conducting as much heat away as the DIP (i.e., the surface mount package has a higher thermal resistance—see Table II).

The silicon for most National devices can operate up to a 150°C junction temperature (check the datasheet for the rare exception). Like the DIP, the surface mount package can actually withstand an ambient temperature of up to 125°C (although a commercial temperature range device will only be specified for a max ambient temperature of 70°C and an industrial temperature range device will only be specified for a max ambient temperature of 85°C). See AN-336, "Understanding Integrated Circuit Package Power Capabilities", (reprinted in the appendix of each linear databook volume) for more information.

TABLE II: Surface Mount Package Thermal Resistance Range*

Package	Thermal Resistance** (θ_{jA}, °C/W)
SO-8	120–175
SO-14	100–140
SO-14 Wide	70–110
SO-16	90–130
SO-16 Wide	70–100
SO-20	60–90
SO-24	55–85
PCC-20	70–100
PCC-28	60–90
PCC-44	40–60

*Actual thermal resistance for a particular device depends on die size. Refer to the datasheet for the actual θ_{jA} value.

**Test conditions: PCB mount (FR4 material), still air (room temperature), copper traces (150 × 20 × 10 mils).

Given a max junction temperature of 150°C and a maximum allowed ambient temperature, the surface mount device will be able to dissipate less power than the DIP device. This factor must be taken into account for new designs.

For board conversion, the DIP and surface mount devices would have to dissipate the same power. This means the surface mount circuit would have a lower maximum allowable ambient temperature than the DIP circuit. For DIP circuits where the maximum ambient temperature required is substantially lower than the maximum ambient temperature allowed, there may be enough margin for safe operation of the surface mount circuit with its lower maximum allowable ambient temperature. But where the maximum ambient temperature required of the DIP current is close to the maximum allowable ambient temperature, the lower maximum ambient temperature allowed for the surface mount circuit may fall below the maximum ambient temperature required. The circuit designer must be aware of this potential pitfall so that an appropriate work-around can be found to keep the surface mount package from being thermally overstressed in the application.

SURFACE MOUNT LITERATURE

National has published extensive literature on the subject of surface mount packaging. Engineers from packaging, quality, reliability, and surface mount applications have pooled their experience to provide you with practical hands-on knowledge about the construction and use of surface mount packages.

The applications note AN-450 "Surface Mounting Methods and their Effect on Product Reliability" is referenced on each SMD datasheet. In addition, "Wave Soldering of Surface Mount Components" is reprinted in this section for your information.

TABLE III. Linear Surface Mount Current Device Listing

Amplifiers and Comparators

Part Number
LF347WM
LF351M
LF451CM
LF353M
LF355M
LF356M
LF357M
LF444CWM
LM10CWM
LM10CLWM
LM308M
LM308AM
LM310M
LM311M
LM318M
LM319M
LM324M
LM339M
LM346M
LM348M
LM358M
LM359M
LM392M
LM393M
LM741CM
LM1458M
LM2901M
LM2902M
LM2903M
LM2904M
LM2924M
LM3403M
LM4250M
LM324M
LM339M
LM365WM
LM607CM
LMC669BCWM
LMC669CCWM
LF441CM

Regulators and References

Part Number
LM317LM
LF3334M
LM336M-2.5
LF336BM-2.5
LM336M-5.0
LM336BM-5.0
LM337LM
LM385M
LM385M-1.2
LM385BM-1.2
LM385M-2.5
LM385BM-2.5
LM723CM
LM2931CM
LM2931M-5.0
LM3524M
LM78L05ACM
LM78L12ACM
LM78L15ACM
LM79L05ACM
LM79L12ACM
LM79L15ACM
LP2951ACM
LP2951CM

Data Acquisition Circuits

Part Number
ADC0802LCV
ADC0802LCWM
ADC0804LCV
ADC0804LCWM
ADC0808CCV
ADC0809CCV
ADC0811BCV
ADC0811CCV
ADC0819BCV
ADC0819CCV
ADC0820BCV
ADC0820CCV
ADC0838BCV
ADC0838CCV
ADC0841BCV
ADC0841CCV
ADC0848BCV
ADC0848CCV
ADC1005BCV
ADC1005CCV
ADC1025BCV
ADC1025CCV
DAC0800LCM
DAC0801LCM
DAC0802LCM
DAC0806LCM
DAC0807LCM
DAC0808LCM
DAC0830LCWM
DAC0830LCV
DAC0832LCWM
DAC0832LCV

Industrial Functions

Part Number
AH5012CM
LF13331M
LF13509M
LF13333M
LM555CM
LM556CM
LM567CM
LM1496M
LM2917M
LM3046M
LM3086M
LM3146M
LM13600M
LM13700M
LMC555CM
LM567CM
MF4CWM-50
MF4CWM-100
MF6CWM-50
MF10CCWM
MF6CWM-100
MF5CWM

Commercial and Automotive

Part Number
LM386M-1
LM592M
LM831M
LM832M
LM833M
LM837M
LM838M
LM1131CM
LM1837M
LM1851M
LM1863M
LM1865M
LM1870M
LM1894M
LM1964V
LM2893M
LM3361AM
LM1881M

Hybrids

Part Number	Part Number
LH0002E LH4002E	LH0032E LH0033E

A FINAL WORD

National is a world leader in the design and manufacture of surface mount components.

Because of design innovations such as perforated copper leadframes, our small outline package is as reliable as our DIP—the laws of physics would have meant that a straight "junior copy" of the DIP would have resulted in an "S.O." package of lower reliability. You benefit from this equivalence of reliability. In addition, our ongoing vigilance at each step of the production process assures that the reliability we designed in stays in so that only devices of the highest quality and reliability are shipped to your factory.

Our surface mount applications lab at our headquarters site in Santa Clara, California continues to research (and publish) methods to make it even easier for you to use surface mount technology. Your problems are our problems.

When you think "Surface Mount"—think "National"!

Ordering and Shipping Information

When you order a surface mount semiconductor, it will be in one of the several available surface mount package types. Specifying the Tape-and-Reel method of shipment means that you will receive your devices in the following quantities per Tape-and-Reel pack: SMD devices can also be supplied in conventional conductive rails.

Package	Package Designator	Max/Rail	Per Reel*
SO-8	M	100	2500
SO-14	M	50	2500
SO-14 Wide	WM	50	1000
SO-16	M	50	2500
SO-16 Wide	WM	50	1000
SO-20	M	40	1000
SO-24	M	30	1000
PCL-20	V	50	1000
PCL-28	V	40	1000
PCL-44	V	25	500
PQFP-196	VF	TBD	—
TP-40	TP	100	TBD
LCC-20	E	50	—
LCC-44	E	25	—

*Incremental ordering quantities. (National Semiconductor reserves the right to provide a smaller quantity of devices per Tape-and-Reel pack to preserve lot or date code integrity. See example below.)

Example: You order 5,000 LM324M ICs shipped in Tape-and-Reel.

- Case 1: All 5,000 devices have the same date code
  - You receive 2 SO-14 (Narrow) Tape-and-Reel packs, each having 2500 LM324M ICs
- Case 2: 3,000 devices have date code A and 2,000 devices have date code B
  - You receive 3 SO-14 (Narrow) Tape-and-Reel packs as follows:

    Pack #1 has 2,500 LM324M ICs with date code A

    Pack #2 has 500 LM324M ICs with date code A

    Pack #3 has 2,000 LM324M ICs with date code B

Short-Form Procurement Specification

TAPE FORMAT

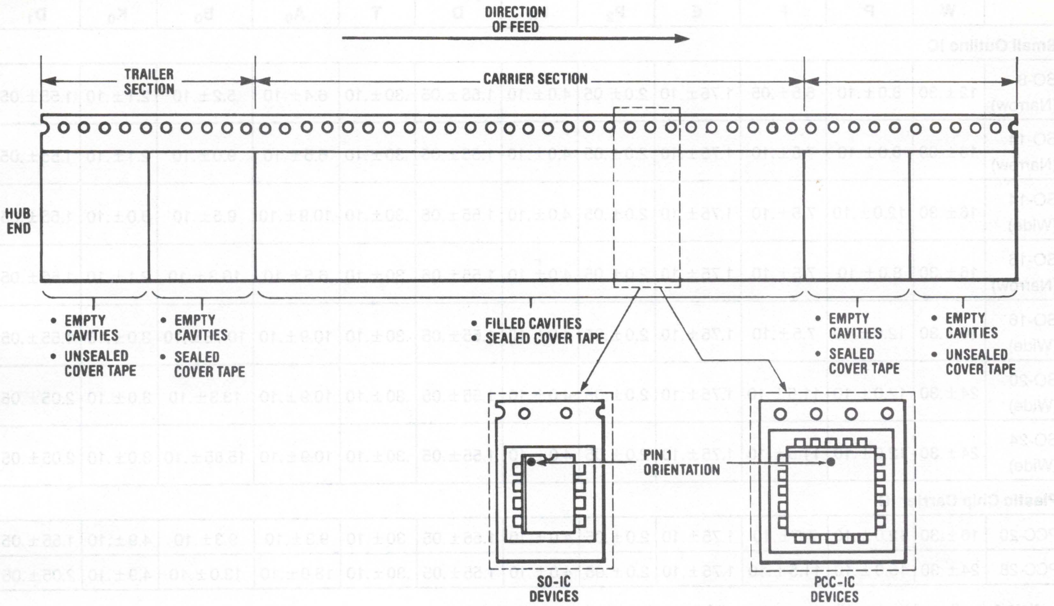
→ Direction of Feed

	Trailer (Hub End)*		Carrier*	Leader (Start End)*	
	Empty Cavities, min (Unsealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Filled Cavities (Sealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Empty Cavities, min (Unsealed Cover Tape)
Small Outline IC					
SO-8 (Narrow)	2	2	2500	5	5
SO-14 (Narrow)	2	2	2500	5	5
SO-14 (Wide)	2	2	1000	5	5
SO-16 (Narrow)	2	2	2500	5	5
SO-16 (Wide)	2	2	1000	5	5
SO-20 (Wide)	2	2	1000	5	5
SO-24 (Wide)	2	2	1000	5	5
Plastic Chip Carrier IC					
PCC-20	2	2	1000	5	5
PCC-28	2	2	750	5	5
PCC-44	2	2	500	5	5

***The following diagram identifies these sections of the tape and Pin #1 device orientation.**

Short-Form Procurement Specification (Continued)

DEVICE ORIENTATION


DIRECTION OF FEED
TRAILER SECTION
CARRIER SECTION
HUB END
• EMPTY CAVITIES
• UNSEALED COVER TAPE
• EMPTY CAVITIES
• SEALED COVER TAPE
• FILLED CAVITIES SEALED COVER TAPE
• EMPTY CAVITIES
• SEALED COVER TAPE
• EMPTY CAVITIES
• UNSEALED COVER TAPE
PIN 1 ORIENTATION
SO-IC DEVICES
PCC-IC DEVICES

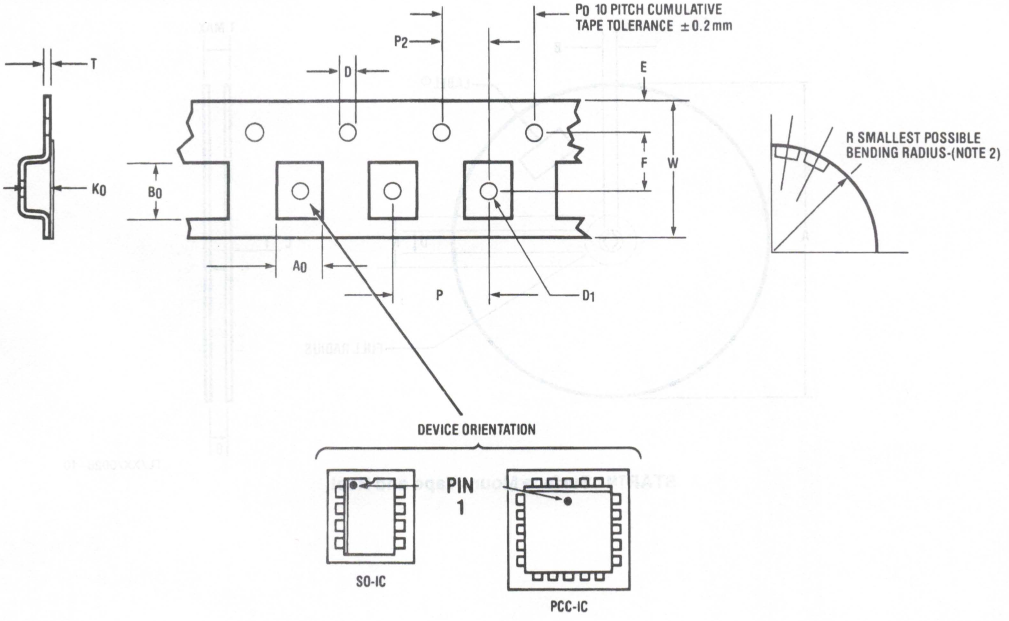
TL/XX/0026-8

MATERIALS

- Cavity Tape: Conductive PVC (less than 10^5 Ohms/Sq)
- Cover Tape: Polyester
  (1) Conductive cover available

- Reel:
  (1) Solid 80 pt fibreboard (standard)
  (2) Conductive fibreboard available
  (3) Conductive plastic (PVC) available

TAPE DIMENSIONS (24 Millimeter Tape or Less)


T
K0
B0
D
P2
P0 10 PITCH CUMULATIVE TAPE TOLERANCE ±0.2 mm
E
F
W
A0
P
D1
R SMALLEST POSSIBLE BENDING RADIUS-(NOTE 2)
DEVICE ORIENTATION
PIN 1
SO-IC
PCC-IC

TL/XX/0026-9

Short-Form Procurement Specification (Continued)

	W	P	F	E	P_2	P_0	D	T	A_0	B_0	K_0	D_1	R
Small Outline IC													
SO-8 (Narrow)	12±.30	8.0±.10	5.5±.05	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.4±.10	5.2±.10	2.1±.10	1.55±.05	30
SO-14 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	9.0±.10	2.1±.10	1.55±.05	40
SO-14 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	9.5±.10	3.0±.10	1.55±.05	40
SO-16 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	10.3±.10	2.1±.10	1.55±.05	40
SO-16 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	10.76±.10	3.0±.10	1.55±.05	40
SO-20 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	13.3±.10	3.0±.10	2.05±.05	50
SO-24 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	15.85±.10	3.0±.10	2.05±.05	50
Plastic Chip Carrier IC													
PCC-20	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	9.3±.10	9.3±.10	4.9±.10	1.55±.05	40
PCC-28	24±.30	16.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	13.0±.10	13.0±.10	4.9±.10	2.05±.05	50

Note 1: A_0, B_0 and K_0 dimensions are measured 0.3 mm above the inside wall of the cavity bottom.

Note 2: Tape with components shall pass around a mandril radius R without damage.

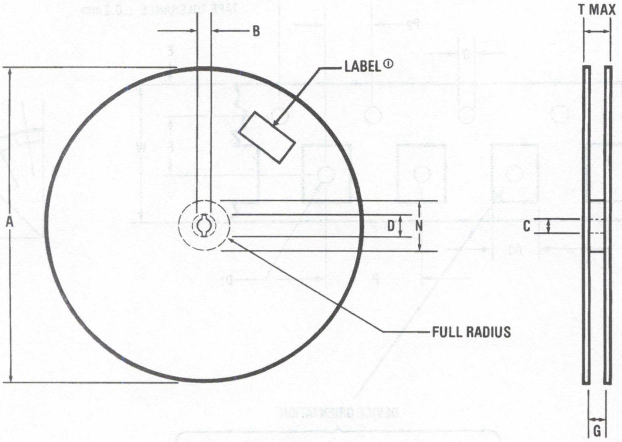
Note 3: Cavity tape material shall be PVC conductive (less than 10^5 Ohms/Sq).

Note 4: Cover tape material shall be polyester (30–65 grams peel-back force).

Note 5: D_1 Dimension is centered within cavity.

Note 6: All dimensions are in millimeters.

REEL DIMENSIONS



TL/XX/0026-10

STAR™* Surface Mount Tape and Reel

Short-Form Procurement Specifications (Continued)

		A (Max)	B (Min)	C	D (Min)	N (Min)	G	T (Max)
12 mm Tape	SO-8 (Narrow)	(13.00) (330)	.059 1.5	.512 ± .002 13 ± 0.05	.795 20.2	1.969 50	$0.488^{+.078}_{-.000}$ 12.4^{+2}_{-0}	.724 18.4
16 mm Tape	SO-14 (Narrow) SO-14 (Wide) SO-16 (Narrow) SO-16 (Wide) PCC-20	(13.00) (330)	.059 1.5	.512 ± .002 13 ± 0.05	.795 20.2	1.969 50	$0.646^{+.078}_{-.000}$ 16.4^{+2}_{-0}	.882 22.4
24 mm Tape	SO-20 (Wide) SO-24 (Wide) PCC-28	(13.00) (330)	.059 1.5	.512 ± .002 13 ± 0.05	.795 20.2	1.969 50	$0.960^{+.078}_{-.000}$ 24.4^{+2}_{-0}	1.197 30.4
32 mm Tape	PCC-44	(13.00) (330)	.059 1.5	.512 ± .002 13 ± 0.05	.795 20.2	1.969 50	$1.276^{+.078}_{-.000}$ 32.4^{+2}_{-0}	1.512 38.4

Units: $\frac{\textbf{Inches}}{\textbf{Millimeters}}$

Material: Paperboard (Non-Flaking)

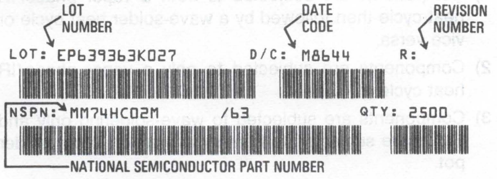
LABEL

Human and Machine Readable Label is provided on reel. A variable (C.P.I) density code 39 is available. NSC STD label (7.6 C.P.I.)

FIELD

Lot Number
Date Code
Revision Level
National Part No. I.D.
Qty.

EXAMPLE



LOT: EP639363K027 D/C: M8644 R:

NSPN: MM74HC02M /63 QTY: 2500

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Fields are separated by at least one blank space.

Future Tape-and-Reel packs will also include a smaller-size bar code label (high-density code 39) at the beginning of the tape. (This tape label is not available on current production.) National Semiconductor will also offer additional labels containing information per your specific specification.

Wave Soldering of Surface Mount Components

ABSTRACT

In facing the upcoming surge of "surface mount technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this new process. However, as the availability of surface mount components is still limited, may have taken to mixing the lead-inserted standard dual-in-line packages (DIPs) with the surface mounted devices (SMDs). Furthermore, to take advantage of using both sides of the board, surface-mounted components are generally adhered to the bottom side of the board while the top side is reserved for the conventional lead-inserted packages. If processed through a wave solder machine, the semiconductor components are now subjected to extra thermal stresses (now that the components are totally immersed into the molten solder).

A discussion of the effect of wave soldering on the reliability of plastic semiconductor packages follows. This is intended to highlight the limitations which should be understood in the use of wave soldering of surface mounted components.

ROLE OF WAVE-SOLDERING IN APPLICATION OF SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave-soldering machine.

Wave Soldering of Surface Mount Components (Continued)

The reasons being:

1) Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.
2) Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.
3) Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

PW BOARD ASSEMBLY PROCEDURES

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

a) Whether to mount ICs on one or both sides of the board.

b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or combination of two or more methods.

The various processes that may be employed are:

A) Wave Solder before Vapor/IR reflow solder.
   1. Components on the same side of PW Board.
      Lead insert standard DIPS onto PW Board Wave solder (conventional)
      Wash and lead trim
      Dispense solder paste on SMD pads
      Pick and place SMDs onto PW Board
      Bake
      Vapor phase/IR reflow
      Clean
   2. Components on opposite side of PW Board.
      Lead insert standard DIPs onto PW Board
      Wave Solder (conventional)
      Clean and lead trim
      Invert PW Board
      Dispense solder paste on SMD pads
      Dispense drop of adhesive on SMD sites (optional for smaller components)
      Pick and place SMDs onto board
      Bake/Cure
      Invert board to rest on raised fixture
      Vapor/IR reflow soldering
      Clean

B) Vapor/IR reflow solder then Wave Solder.
   1. Components on the same side of PW Board.
      Solder paste screened on SMD side of Printed Wire Board
      Pick and place SMDs
      Bake
      Vapor/IR reflow
      Lead insert on same side as SMDs
      Wave solder
      Clean and trim underside of PCB

C) Vapor/IR reflow only.
   1. Components on the same side of PW Board.
      Trim and form standard DIPs in "gull wing" configuration
      Solder paste screened on PW Board
      Pick and place SMDs and DIPs
      Bake
      Vapor/IR reflow
      Clean
   2. Components on opposite sides of PW Board.
      Solder paste screened on SMD-side of Printed Wire Board
      Adhesive dispensed at central location of each component
      Pick and place SMDs
      Bake
      Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads
      Lead insert DIPs
      Vapor/IR reflow
      Clean and lead trim

D) Wave Soldering Only
   1. Components on opposite sides of PW Board.
      Adhesive dispense on SMD side of PW Board
      Pick and place SMDs
      Cure adhesive
      Lead insert top side with DIPs
      Wave solder with SMDs down and into solder bath
      Clean and lead trim

All of the above assembly procedures can be divided into three categories for I.C. Reliability considerations:

1) Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
2) Components are subjected to only a vapor phase/IR heat cycle.
3) Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a 'pallet' where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

Wave Soldering of Surface Mount Components (Continued)

THERMAL CHARACTERISTICS OF MOLDED INTEGRATED CIRCUITS

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1*. Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on lead frames, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of lead frame material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal lead frame in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the expoxy-metal interface. Howerver, if the package is subjected to temprature above its glass-transition temperature, the epoxy will begin to expand much faster than the metal and the probability of separation is greatly increased.

CONVENTIONAL WAVE-SOLDERING

Most wave-soldering operations occur at temperatures between 240–260°C. Conventional epoxies for encapsulation have glass-transition temperature between 140–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

1) The PW board has a certain amount of heat-sink effect and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.

2) In conventional soldering, only the tip of each lead in a DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

EFFECT ON PACKAGE PERFORMANCE BY EPOXY-METAL SEPARATION

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metallization over time and premature failure of the device in the field.

VAPOR PHASE/IR REFLOW SOLDERING

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Operating temperatures are 215°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec–60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-lead frame interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

BIAS MOISTURE TEST

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a stream chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to fail.

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and

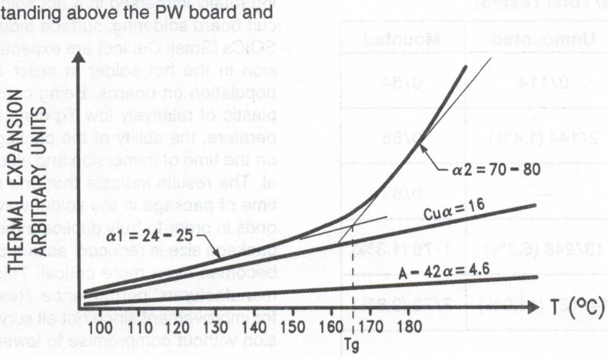

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FIGURE 1. Thermal Expansion and Glass Transition Temperature

Wave Soldering of Surface Mount Components (Continued)

85% relative humidity. Once cycle of approximately 100 hours has been shown to be equivalent to 2000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

TEST RESULTS

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave-soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

TABLE IV. Vapor Phase vs. Wave Solder

1. Vapor phase (60 sec. exposure @ 215°C)
   = 9 failures/1723 samples
   = 0.5% (average over 32 sample lots)
2. Wave solder (2 sec total immersion @ 260°C)
   = 16 failures/1201 samples
   = 1.3% (average over 27 sample lots)

Package: SO-14 lead
Test: Bias moisture test 85% R.H., 85°C for 2000 hours
Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4000 hours 85/85 test. Results were compared for packages by itself against packages which were surface-mounted onto a FR-4 printed wire board.

TABLE V. Summary of Wave Solder Results (85% R.H./85°C Bias Moisture Test, 2000 hours) (# Failures/Total Tested)

	Unmounted	Mounted
Control/Vapor Phase 15 sec @ 215°C	0/114	0/84
Solder Dip 2 sec @ 260°C	2/144 (1.4%)	0/85
Solder Dip 4 sec @ 260°C	—	0/83
Solder Dip 6 sec @ 260°C	13/248 (5.2%)	1/76 (1.3%)
Solder Dip 10 sec @ 260°C	14/127 (11.0%)	3/79 (3.8%)

Package: SO-14 lead
Device: LM324M

Since the package is of very small mass and experiences a rather sharp thermal shock followed by stresses created by the mismatch in expansion, the results show the package being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6000 hours in a 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

TABLE VI. U.S. Manufacturers Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Tested)

Package SO-8	Vapor Phase 30 sec	Wave Solder 2 sec	Wave Solder 4 sec	Wave Solder 6 sec	Wave Solder 10 sec
Manuf A	8/30*	1/30*	0.30	12/30*	16/30*
Manuf B	2/30*	8/30*	2/30*	22/30*	20/30*
Manuf C	0/30	0/29	0/29	0/30	0/30
Manuf D	1/30*	0/30	12/30*	14/30*	2/30*
Manuf E	1/30**	0/30	0/30	0/30	0/30
Manuf F	0/30	0/30	0/30	0/30	0/30
Manuf G	0/30	0/30	0/30	0/30	0/30

*Corrosion-failures

**No Visual Defects—Non-corrosion failures

Test: Accelerated Bias Moisture Test; 85% R.H./85°C, 6000 equivalent hours.

SUMMARY

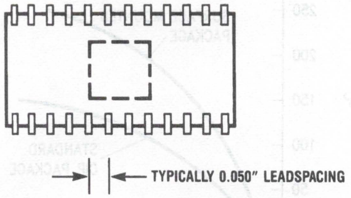
Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in a hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low Tg compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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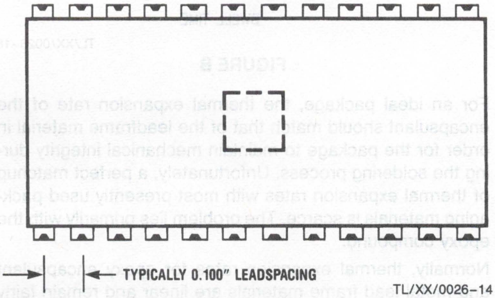
Standard DIP Package



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Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

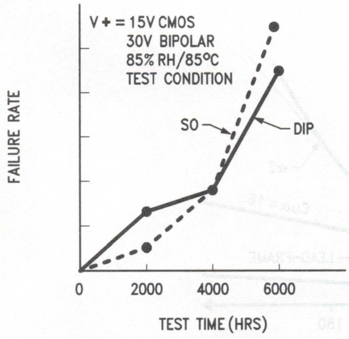

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FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

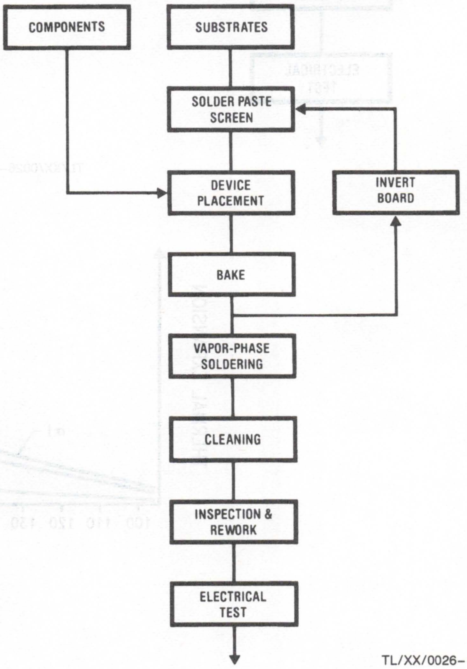
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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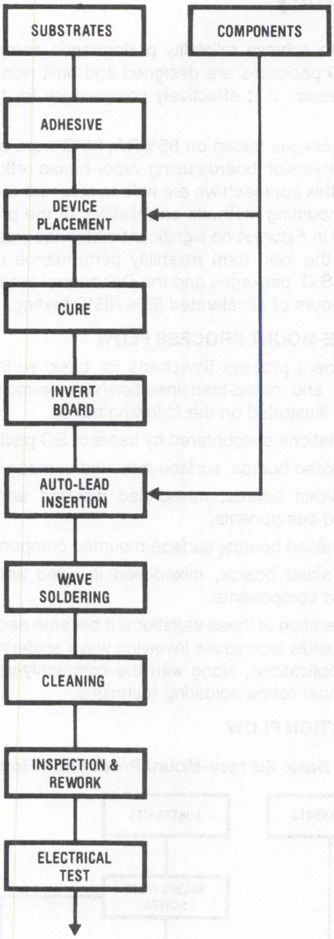
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



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Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

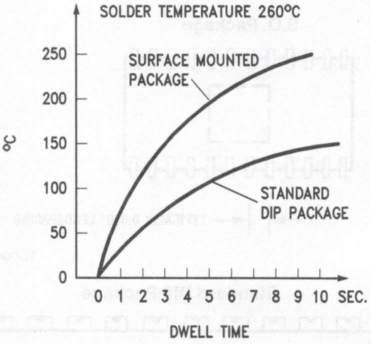

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FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

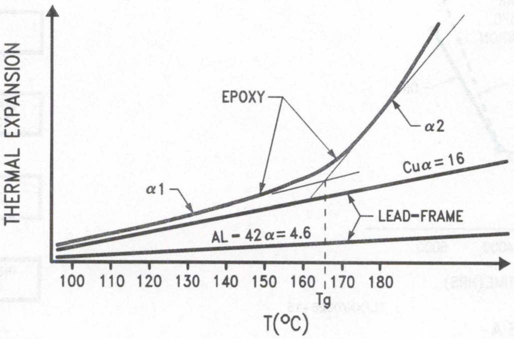

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FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

Group 3-6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds

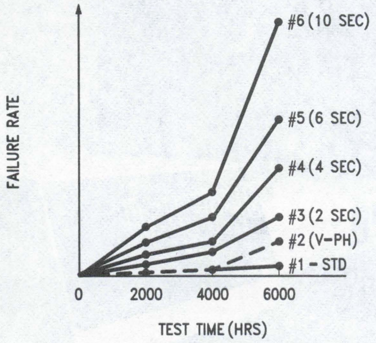

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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement
  - Fixed placement stations
  - Boards indexed under head and respective components placed

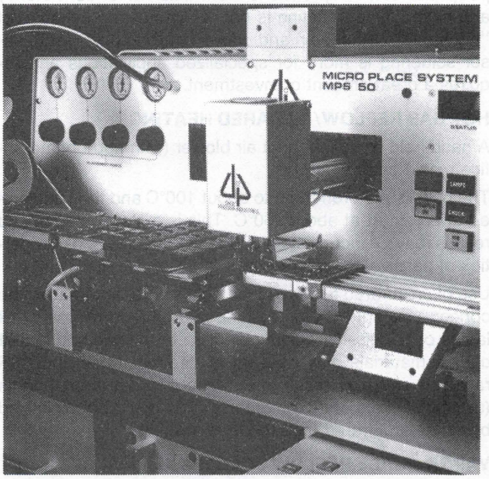
(b) Sequential placement
  - Either a X-Y moving table system or a θ, X-Y moving pickup system used
  - Individual components picked and placed onto boards

(c) Simultaneous placement
  - Multiple pickup heads
  - Whole array of components placed onto the PCB at the same time

(d) Sequential/simultaneous placement
  - X-Y moving table, multiple pickup heads system
  - Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

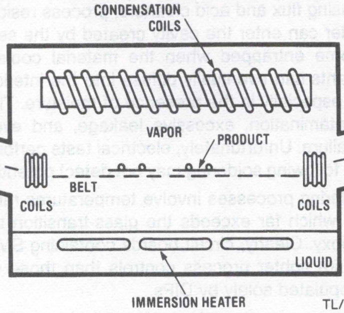
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

In-Line Conveyorized Vapor-Phase Soldering



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The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

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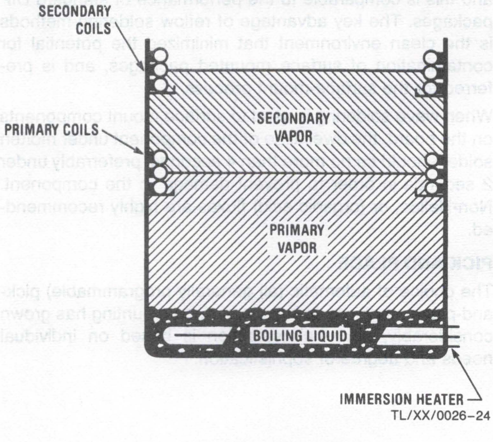
Batch-Fed Production Vapor-Phase Soldering Unit



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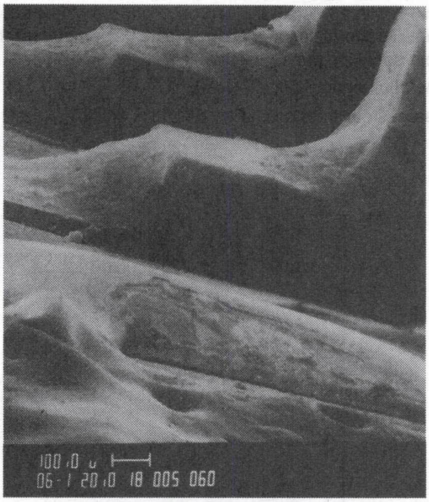
Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

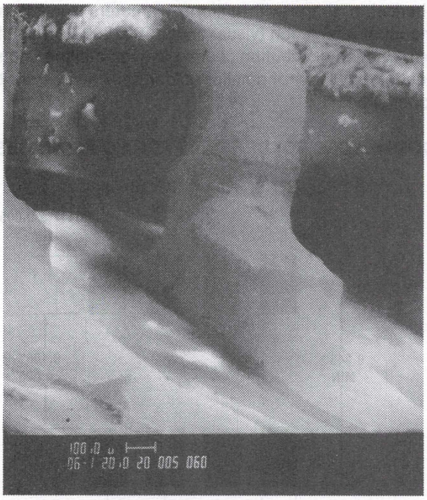
  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

Solder Joints on a SO-14 Package on PCB



TL/XX/0026-26

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050″ lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005″ usually used to achieve a solder paste thickness (wet) of about 0.008″ typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed ⅛″, to avoid damage to screens and minimize distortion.

SOLDER PASTE

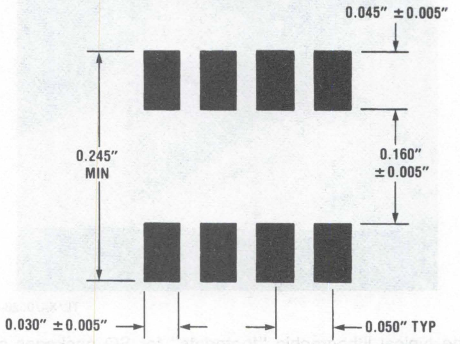
Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.

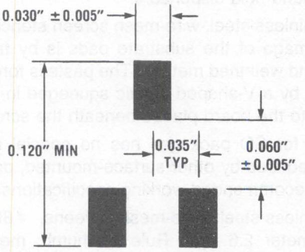
RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16


0.045″ ±0.005″
0.245″ MIN
0.160″ ±0.005″
0.030″ ±0.005″
0.050″ TYP

TL/XX/0026-27

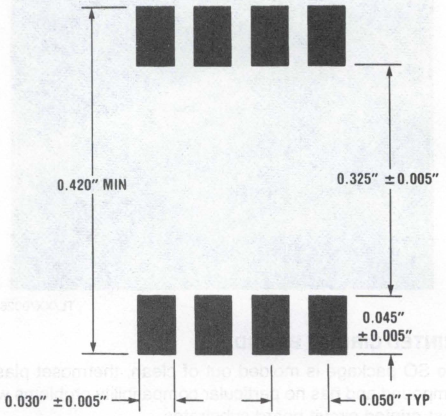
SOT-23


0.030″ ±0.005″
0.120″ MIN
0.035″ TYP
0.060″ ±0.005″

TL/XX/0026-29

- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

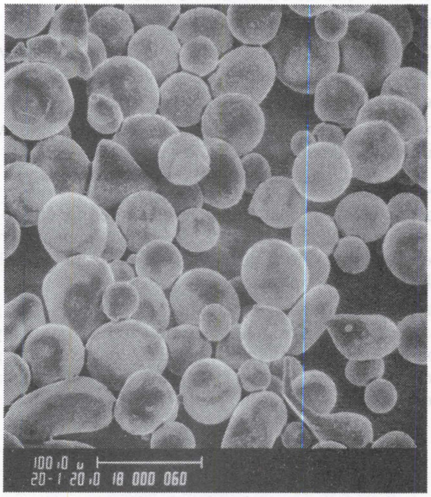
SO-16L, SO-20


0.420″ MIN
0.325″ ±0.005″
0.045″ ±0.005″
0.030″ ±0.005″
0.050″ TYP

TL/XX/0026-28

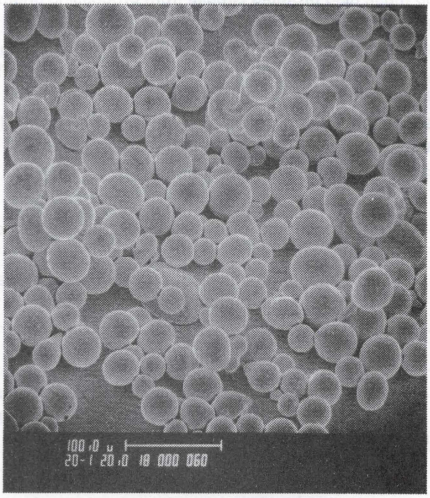
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)


100.0 u
20-1 20.0 18 000 060

TL/XX/0026-30

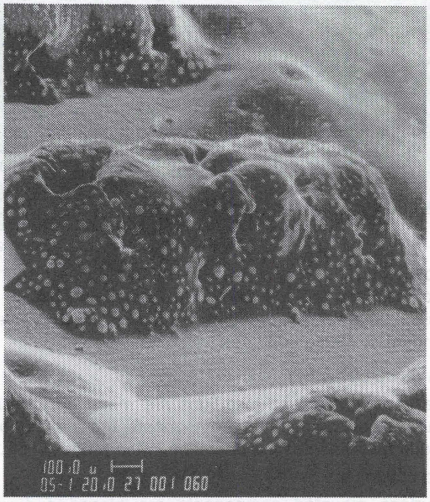
200 × Kester (63/37)


100.0 u
20-1 20.0 18 000 060

TL/XX/0026-31

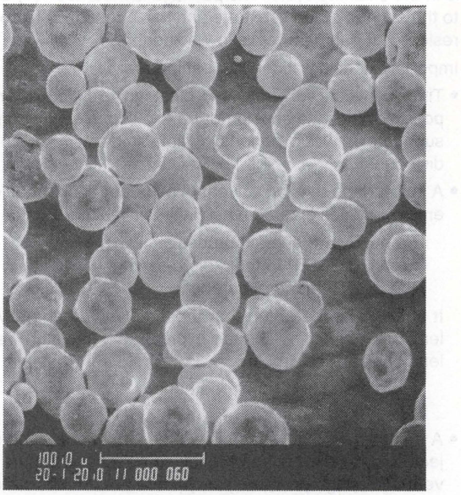
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads


100.0 u
05-1 20.0 27 001 060

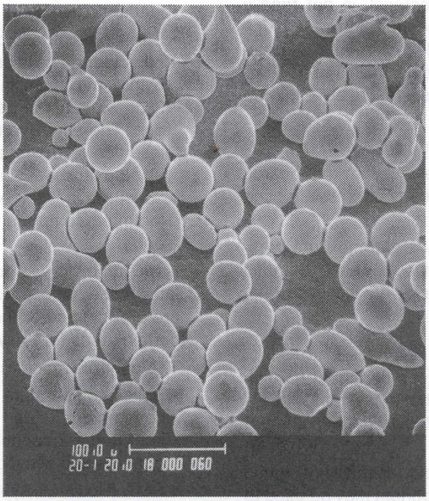
TL/XX/0026–32

200 × Fry Metal (63/37)


100.0 u
20-1 20.0 11 000 060

TL/XX/0026–33

200 ESL (63/37)


100.0 u
20-1 20.0 18 000 060

TL/XX/0026–34

CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

    Freon TMS (general purpose)
    Freon TE35/TP35 (cold-dip cleaning)
    Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

    Prelete or 1,1,1-Trichloroethane
    Kester 5120/5121

- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

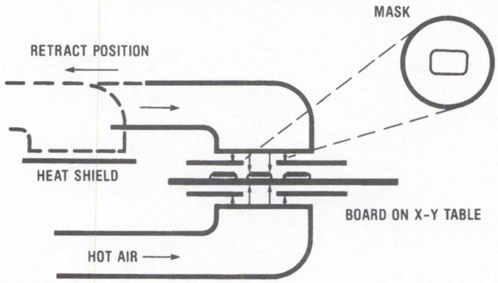
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

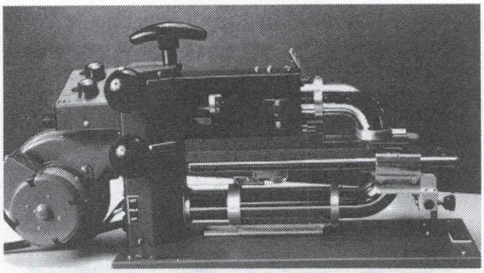
When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



TL/XX/0026-35

Hot-Air Rework Machine



TL/XX/0026-36

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

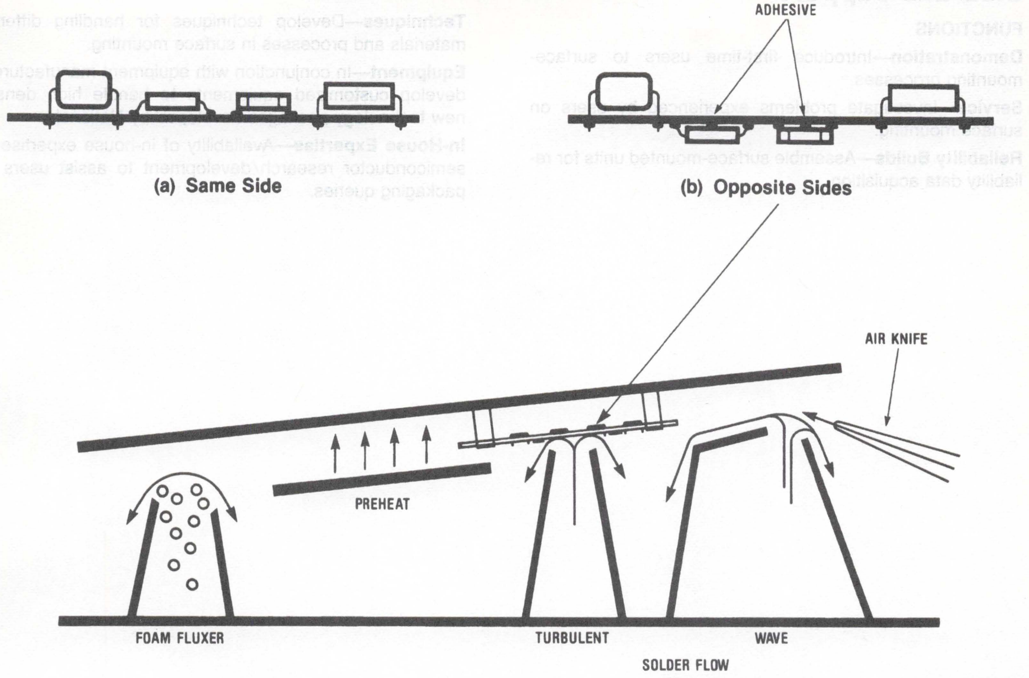
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



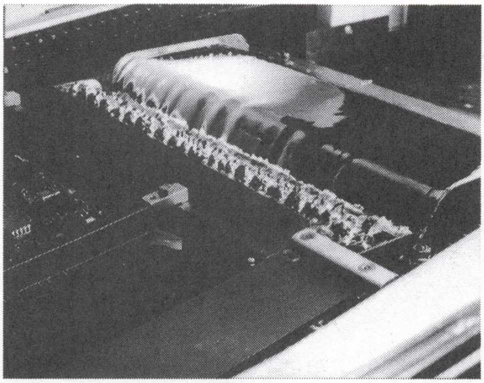
TL/XX/0026-37

A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



TL/XX/0026-38

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

Section 9

Appendices/
Physical Dimensions

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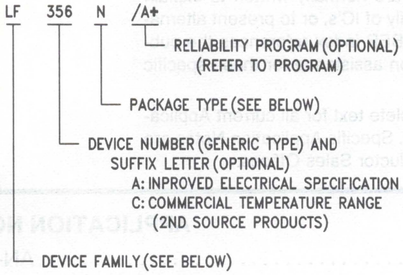
Distributors

National
Semiconductor
Corporation

Appendix A
General Product Marking & Code Explanation


LF
356
N
/A+
RELIABILITY PROGRAM (OPTIONAL)
(REFER TO PROGRAM)
PACKAGE TYPE (SEE BELOW)
DEVICE NUMBER (GENERIC TYPE) AND
SUFFIX LETTER (OPTIONAL)
A: IMPROVED ELECTRICAL SPECIFICATION
C: COMMERCIAL TEMPERATURE RANGE
(2ND SOURCE PRODUCTS)
DEVICE FAMILY (SEE BELOW)

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Device Family

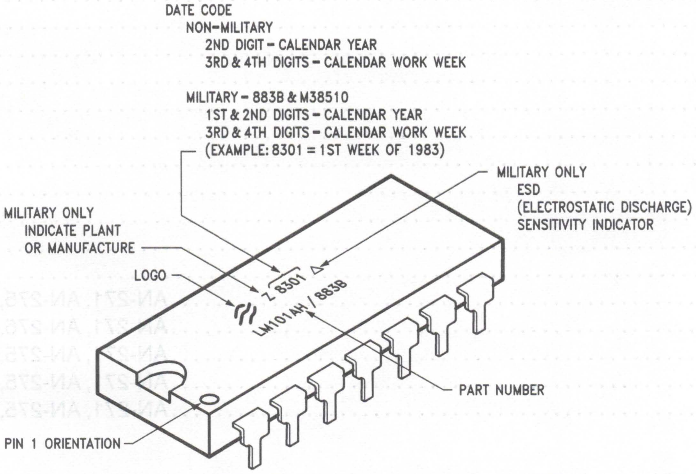
Integrated Circuits (IC's)

ADC	Data Conversion
AF	Active Filter
AH	Analog Switch (Hybrid)
AM	Analog Switch (Monolithic)
DAC	Data Conversion
DM	Digital (Monolithic)
HS	Hybrid
LF	Linear (Bifet)
LH	Linear (Hybrid)
LM	Linear (Monolithic)
LMC	Linear CMOS
LP	Linear (Low Power)
MF	Linear (Monolithic Filter)
SL	Special Linear
LMF	Linear Monolithic Filter

Package Type*

IC's Only

D	Glass/Metal DIP
E	Ceramic Leadless Chip Carrier (LCC)
F	Glass/Metal Flat Pak (¼″ x ¼″)
G	12 Lead TO-8 M/C
H	Multi-Lead M/C
H-05	4 Lead M/C (TO-5) } Shipped with Thermal Shield
H-46	4 Lead M/C (TO-46)
J	Lo-Temp Ceramic DIP (Sometimes referred to as the "Fit-Seal" Package).
J-8	8 Lead Ceramic DIP ("MiniDIP")
J-14	14 Lead Ceramic DIP (-14 used only when product is also available in -8 pkg).
K	TO-3 M/C in Steel, except LM309K which is shipped in Aluminum
KC	TO-3 M/C (Aluminum)
K Steel	TO-3 M/C (Steel)
M	Small Outline Package
N	Molded DIP (EPOXY B)
N-01	Molded DIP (Epoxy B) with Staggered Leads
N-8	8 Lead Molded DIP (Epoxy B) ("Mini-DIP")
N-14	14 Lead Molded DIP (Epoxy B) (-14 used only when product is also available in -8 pkg).
P	3 Lead TO-202 PWR Pkg
Q	Cerdip with UV Window
T	3,5,11,15 & 23 Lead TO-220 PWR Pkg (Epoxy B)
V	Multi-lead Plastic Chip Carrier (PCC)
W	Lo-Temp Ceramic Flat Pak
WM	Wide Body Small Outline Package


DATE CODE
NON-MILITARY
2ND DIGIT – CALENDAR YEAR
3RD & 4TH DIGITS – CALENDAR WORK WEEK
MILITARY – 883B & M38510
1ST & 2ND DIGITS – CALENDAR YEAR
3RD & 4TH DIGITS – CALENDAR WORK WEEK
(EXAMPLE: 8301 = 1ST WEEK OF 1983)
MILITARY ONLY
ESD
(ELECTROSTATIC DISCHARGE)
SENSITIVITY INDICATOR
MILITARY ONLY
INDICATE PLANT
OR MANUFACTURE
LOGO
Z 8301 △
LM101AH / 883B
PART NUMBER
PIN 1 ORIENTATION

TL/XX/0027–2

National
Semiconductor
Corporation

Appendix B

APPLICATION NOTE REFERENCED BY PART NUMBER

National Semiconductor Linear Application notes are normally written to explain the operation and use of a particular device or family of IC's, or to present alternative technical solutions. The following PART NUMBER index references the published application notes that would offer application assistance for those specific IC's.

The 1986 Linear Applications Handbook is a complete text for all current Application Notes for both Monolithic and Hybrid products. Specific Application Notes are available upon request through National Semiconductor Sales Offices.

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ADCXXXX	AN-156
ADC80	AN-360
ADC0801	AN-233, AN-271, AN-274, AN-280, AN-281, AN-294, LB-53
ADC0802	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0803	AN-233, AN–274, AN-280, AN-281, LB-53
ADC0804	AN-233, AN-274, AN-276, AN-280, AN-281, LB-53
ADC0805	AN-233, AN-274, AN-280, AN-281, LB-53
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ADC0809	AN-247, AN-280
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ADC1005	AN-280
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DAC1022	AN-269
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DAC1209	AN-271, AN-284
DAC1210	AN-271, AN-284
DAC1218	AN-293
DAC1220	AN-253, AN-269
DAC1221	AN-269
DAC1222	AN-269
DAC1230	AN-284
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DS8608	AN-382
DT1058	AN-287
DT1060	AN-287
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DTSW250GI	AN-287
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LF155	AN-263, AN-447
LF198	AN-245, AN-294
LF311	AN-301
LF347	AN-256, AN-262, AN-263, AN-265, AN-266, AN-301, AN-344, AN-447
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LF351B	Appendix D
LF353	AN-256, AN-258, AN-263, AN-264, AN-271, AN-285, AN-293, AN-447, LB-44, Appendix D
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LF13509	AN-289, AN-295, AN-447
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LH0033	AN-48, AN-115, AN-227, AN-253
LH0042	AN-63

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LH0052	AN-63
LH0053	AN-245
LH0062	AN-75
LH0063	AN-227
LH0070	AN-301
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LH0082	AN-244, AN-266
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LH0094	AN-301
LH0101	AN-261
LH1605	AN-343
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LM109A	LB-15
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LM126	AN-82
LM129	AN-173,AN-178, AN-262, AN-266
LM131	AN-210, Appendix D
LM131A	AN-210
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LM135	AN-225, AN-262, AN-292, AN-298
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LM137HV	LB-46
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LM199A	AN-161
LM211	LB-39
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LM231A	AN-225
LM235	AN-225
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LM309	AN-178, AN-182
LM311	AN-41, AN-103, AN-260, AN-263, AN-288, AN-294, AN-295, AN-307, LB-12, LB-16, LB-18, LB-39
LM313	AN-263
LM316	AN-258
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LM319	AN-115, AN-271, AN-293
LM320	AN-288
LM321	LB-24
LM324	AN-88, AN-258, AN-274, AN-284, AN-301, LB-44, AB-25, Appendix C
LM329	AN-256, AN-263, AN-284, AN-295, AN-301
LM329B	AN-225
LM330	AN-301
LM331	AN-210, AN-240, AN-265, AN-278, AN-285, AN-311, LB-45, Appendix, C Appendix D
LM331A	AN-210, Appendix C
LM334	AN-242, AN-256, AN-284
LM335	AN-225, AN-263, AN-295
LM336	AN-202, AN-247, AN-258
LM337	LB-46
LM338	LB-49, LB-51
LM339	AN-74, AN-245, AN-274
LM340	AN-103, AN-182
LM340L	AN-256
LM342	AN-288
LM346	AN-202, LB-54
LM347	LB-44
LM348	AN-202, LB-42
LM349	LB-42
LM358	AN-116, AN-247, AN-271, AN-274, AN-284, AN-298, Appendix C
LM358A	Appendix D

DEVICE NUMBER	APPLICATION NOTE
LM359	AN-278, AB-24
LM360	AN-87
LM361	AN-87, AN-294
LM363	AN-271
LM380	AN-69, AN-146
LM381	AN-64, AN-104
LM382	AN-147
LM385	AN-242, AN-256, AN-301, AN-344
LM386	LB-54
LM389	AN-256, AN-263, AN-264, AN-274
LM391	AN-272
LM392	AN-274, AN-286
LM393	AN-271, AN-274, AN-293
LM394	AN-262, AN-263, AN-264, AN-271, AN-293, AN-299, AN-311, LB-52
LM395	AN-178, AN-181, AN-262, AN-263, AN-266, AN-301, LB-28
LM399	AN-184
LM555	AB-7
LM556	AB-7
LM565	AN-46, AN-146
LM566	AN-146
LM567	AN-46
LM709	AN-24, AN-30
LM710	AN-41, LB-12
LM725	LB-22
LM741	AN-75, AN-79, LB-19, LB-22
LM832	AN-386, AN-390
LM833	AN-346
LM1036	AN-390
LM1310	AN-81
LM1524	AN-272, AN-288, AN-292, AN-293
LM1800	AN-81, AN-147
LM1812	AB-20
LM1818	AN-407
LM1820	LB-29
LM1823	AN-391
LM1828	Appendix B
LM1830	AB-10
LM1837	AN-407
LM1845	Appendix B
LM1863	AN-381, AN-382
LM1865	AN-382, AN-390
LM1870	AN-382
LM1886	AN-402
LM1889	AN-402
LM1894	AN-384, AN-386, AN-390
LM1897	AN-407
LM2878	AN-147
LM2889	AN-391, AN-402
LM2907	AN-162
LM2917	AN-162
LM2931	AB-12
LM2931CT	AB-11

DEVICE NUMBER	APPLICATION NOTE
LM3045	AN-286
LM3046	AN-146, AN-299
LM3089	AN-147
LM3524	AN-272, AN-288, AN-292, AN-293
LM3820	AN-147, LB-29
LM3900	AN-72, AN-263, AN-274, AN-278, LB-20, AB-24
LM3909	AN-154
LM3911	LB-27
LM3914	LB-48, AB-25
LM3915	AN-386
LM3999	AN161
LM4250	AN-88, LB-34
LM7800	AN-178
LM78L12	AN-146
LMC835	AN-435
LP324	AN-284
MF10	AN-307
MM1458	AN-116
MM1558	AN-116
MM1558C	AN-116
MM2716	LB-54
MM54104	AN-252, AN-287, LB-54
MM57110	AN-382
MM74C00	AN-88
MM74C02	AN-88
MM74C04	AN-88
MM74C948	AN-193
MM74LS138	LB-54
2N4339	AN-32
LH4101	AN-480
LM34/35	AN-460
LM32900	AN-478
LM3578	AB-30
LPXXXX	AN-462
LM34	AN-462
LM35	AN-462
LM385	AN-462
LMC13334	AN-462
LP2950	AN-462
LP2951	AN-462
LP311	AN-462
LP324	AN-462
LP339	AN-462
LP365	AN-462

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Appendix C
Summary of Commercial Reliability Programs

General

National Semiconductor Commercial Reliability Programs provide a broad range of off-the-shelf enhanced semiconductor products that supply an extra measure of quality and reliability needed in high-stress or difficult to service applications.

National's A+ and B+ programs allow each individual customer to:

- Minimize the need for incoming electrical inspection
- Eliminate the need and associated costs of using independent testing laboratories
- Reduction in infant mortality rate
- Reduction in reworked board costs
- Reduction in warranty and service costs

A+ Product Enhancement

The A+ Product Enhancement incorporates the benefits of the Multiple-Pass and Elevated Temperature along with "BURN-IN."

The A+ Program provides:

- 100% Temperature Cycling
- 100% Electrical Testing at Room and High Temperature
- 100% Burn-In Testing Combining Increased Temperature with Applied Voltage
- Acceptable Quality Levels Greater than Industry Norm

Typical A+ Flow is:

- SEM
- Assembly and Seal
- Four Hour 150°C Bake
- Five Temperature Cycles (0°C to +100°C)
- High Temperature Electrical Test
- Electrical Test
- Burn-In (160 hours at a minimum junction temperature of 125°C)
- DC Parametric and Function Tests
- Tightened Quality Control Inspection Plans

Note: Certain products may follow slightly different process flows dictated by specific capabilities and device characteristics, consult NSC.

P+ Product Enhancement

The P+ product enhancement program applies to regulator devices and offers an added advantage. P+ involves a dynamic self-heating burn-in that tests the thermal shutdown of the regulator. P+ is proven more effective than the standard 125°C burn-in as an early screen for infant mortality defects. It sharply reduces the cost of testing incoming components. Reliability Report L-140 further explains the P+ process. The following chart lists regulators which receive P+ prior to shipment and at no additional cost.

Device	Package Types				
	TO-3 K STEEL	TO-39 H	TO-220 T	TO-202 P	TO-92 Z
LM109/309	X	X			
LM117/317	X	X	X	X	
LM117HV/317HV	X	X			
LM120/320	X	X	X	X	
LM123/323	X				
LM137/337	X	X	X	X	
LM137HV/337HV	X	X			
LM138/338	X				
LM140/340	X	X	X	X	
LM145/345	X				
LM150/250/350	X				
LM196/396	X				
LM2930/2935/2940/2984			X		
LM2931			X		X
LM78XX			X		

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Appendix D
Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our *1987 Reliability Handbook.*

MIL-M-38510

The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government-certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

There are two processing levels specified within MIL-M-38510: Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table III.

Tables I and II explain the JAN device marking system.

Copies of MIL-M-38510, the QPL, and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

DESC Specifications

DESC specifications are issued to provide standardized versions of devices which are not yet available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's DESC specification offerings can be obtained from our franchised distributors, sales offices, or DESC. DESC is located in Dayton, Ohio.

MIL-STD-883

Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision C of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

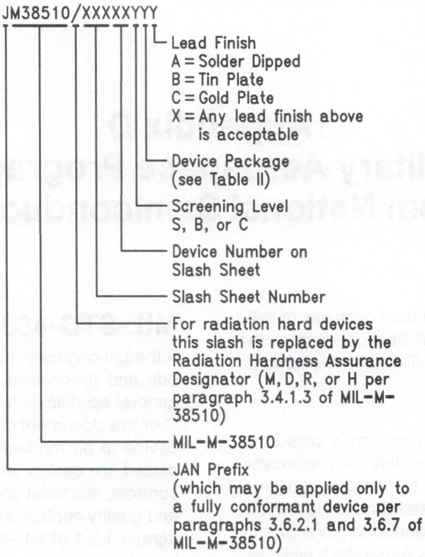
As with DESC specifications, a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits, and test temperatures must be clearly documented. At National Semiconductor, this information is available via our RETS (Reliability Electrical Test Specification Program). The RETS document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

Military Screening Program (MSP)

National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

TABLE I. The MIL-M-38510 Part Marking



JM38510/XXXXXYYY

Lead Finish
A = Solder Dipped
B = Tin Plate
C = Gold Plate
X = Any lead finish above is acceptable

Device Package (see Table II)

Screening Level S, B, or C

Device Number on Slash Sheet

Slash Sheet Number

For radiation hard devices this slash is replaced by the Radiation Hardness Assurance Designator (M, D, R, or H per paragraph 3.4.1.3 of MIL-M-38510)

MIL-M-38510

JAN Prefix (which may be applied only to a fully conformant device per paragraphs 3.6.2.1 and 3.6.7 of MIL-M-38510)

CI24-1

TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-Pin 1/4″ X 1/4″ (metal) flat pack
B	14-Pin 3/16″ X 1/4″ flat pack
C	14-Pin 1/4″ X 3/4″ dual-in-line
D	14-Pin 1/4″ X 3/8″ (ceramic) flat pack
E	16-Pin 1/4″ X 3/8″ dual-in-line
F	16-Pin 1/4″ X 3/8″ (metal or ceramic) flat pack
G	8-pin TO-99 can or header
H	10-pin 1/4″ x 1/4″ (metal) flat pack
I	10-pin TO-100 can or header
J	24-pin 1/2″ x 1-1/4″ dual-in-line
K	24-pin 3/8″ x 5/8″ flat pack
L	24-pin 1/4″ x 1-1/4″ dual-in-line
M	12-pin TO-101 can or header
N	(Note 1)
P	8-pin 1/4″ x 3/8″ dual-in-line
Q	40-pin 3/16″ x 2-1/16″ dual-in-line
R	20-pin 1/4″ x 1-1/16″ dual-in-line
S	20-pin 1/4″ x 1/2″ flat pack
T	(Note 1)
U	(Note 1)
V	18-pin 3/8″ x 15/16″ dual-in-line
W	22-pin 3/8″ x 1-1/8″ dual-in-line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-terminal 0.350″ x 0.350″ chip carrier
3	28-terminal 0.450″ x 0.450″ chip carrier

Note 1: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

Screen	Class S		Class B	
	Method	**Reqmt**	**Method**	**Reqmt**
1. Wafer Lot Acceptance	5007	All Lots		—
2. Nondestructive Bond Pull	2023	100%		—
3. Internal Visual (Note 1)	2010, Condition A	100%	2010, Condition B	100%
4. Stabilization Bake	1008, Condition C, 24 hrs. Min.	100%	1008, Condition C, 24 hrs. Min.	100%
5. Temp. Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6. Constant Acceleration	2001, Condition E (Min.) Y_1 Orientation Only	100%	2001, Condition E, (Min.), Y_1 Orientation Only	100%
7. Visual Inspection (Note 3)		100%		100%
8. Particle Impact Noise Detection (PIND)	2020, Condition A (Note 4)	100%		—
9. Serialization	(Note 5)	100%		—
10. Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	—
11. Burn-In Test	1015 240 Hrs. @ 125°C Min. (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min.	100%
12. Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%		
13. Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min. (Cond. F Not Allowed)	100%		—
15. PDA Calculation	5% Parametric (Note 14), 3% Functional −25°C	All Lots	5% Parametric (Note 14)	All Lots
16. Final Electrical Test	Per Applicable Device Specification		Per Applicable Device Specification	
a) Static Tests				
1) 25°C (Subgroup 1, Table I, 5005)		100%		100%
2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005)		100%		100%
b) Dynamic Tests & Switching Tests, 25°C (Subgroups 4, 9, Table I, 5005)		100%		100%
c) Functional Test, 25°C (Subgroup 7, Table I, 5005)		100%		100%

TABLE III. 100% Screening Requirements (Continued)

Screen		Class S		Class B	
		Method	**Reqmt**	**Method**	**Reqmt**
17.	Seal Fine, Gross	1014	100%, (Note 8)	1014	100%, (Note 9)
18.	Radiographic (Note 10)	2012 Two Views	100%		—
19.	Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20.	External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g. bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock method 1011, test condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-M-38510, paragraph 4.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separate or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g. flatpacks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 19.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and Record when past burn-in delta measurements are specified.

Note 14: PDA shall apply to all static, dynamic, functional, and switching measurements at either 25°C or maximum rated operating temperature.

Military Analog Products Available From National Semiconductor

Listed below are the military class B Analog devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

Device Type	Mil * Class B	883 Class B	Desc	JAN
AH0014D	x			
AH0015D	x			
AH0019D	x			
LF111H	x			
LF11201D		x		
LF11202D		x		
LF11331D		x		
LF11332D		x		
LF11333D		x		
LF11508D	x			
LF11509D	x			
LF147D		x		
LF155AH		x		
LF155H		x		x
LF155J-8				x
LF155W				x
LF156AH		x		
LF156H		x		x
LF156J-8				x
LF156W				x
LF157AH		x		
LF157H		x		
LF198H		x		
LF411MH		x		x
LF411W				x
LF412MH		x		x
LF441MH	x			
LF442MH		x		
LF444MD		x		
LH0002H		x	x	
LH0003H	x			
LH0004H	x			
LH0020G	x			
LH0021K	x			
LH0022D	x			
LH0022H	x			
LH0023G	x			
LH0024H	x			

Device Type	Mil * Class B	883 Class B	Desc	JAN
LH0032G	x		x	
LH0033AG	x			
LH0033G	x		x	
LH0036G	x			
LH0038D	x			
LH0041G	x			
LH0042D	x			
LH0042H	x			
LH0043G	x			
LH0044AH	x			
LH0044H	x			
LH0052H	x			
LH0053G	x			
LH0061K	x			
LH0062D	x			
LH0062H	x			
LH0063K	x			
LH0070-0H	x			
LH0070-1H	x			
LH0070-2H	x			
LH0071-0H	x			
LH0071-1H	x			
LH0071-2H	x			
LH0075G	x			
LH0076G	x			
LH0082D	x			
LH0084D	x			
LH0086D	x			
LH0091D	x			
LH0094D	x			
LH00101AK	x			
LH0101K	x			
LH2101AD		x		
LH2108AD		x		
LH2108D		x		
LH2110D		x		
LH2111D		x		
LH2111F	x			

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

Military Analog Products Available From National Semiconductor

Listed below are the military class B Analog devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

Device Type	Mil * Class B	883 Class B	Desc	JAN
LH24250F	x			
LM10H		x		
LM101AH		x		x
LM101AJ-14		x		x
LM101AJ		x		
LM101AW				x
LM102H		x		
LM103H-3.0		x	x	
LM103H-3.3		x	x	
LM103H-3.6		x	x	
LM103H-3.9		x	x	
LM104H		x		
LM105H		x		
LM106H		x		
LM107H		x		
LM107J-14		x		
LM107J		x		
LM108AH		x		x
LM108AJ-8		x		x
LM108AJ		x		
LM108AW				x
LM108H		x		
LM108J-8		x		
LM108J		x		
LM109H		x		
LM109KSTEEL		x		
LM11H		x		
LM110H		x		
LM110J-8		x		
LM110J		x		
LM111H		x		x
LM111J		x		x
LM111W				x
LM112H		x		
LM113-1H		x	x	
LM113-2H		x	x	
LM113H		x	x	
LM117H		x	x	x

Device Type	Mil * Class B	883 Class B	Desc	JAN
LM117HVH		x	x	
LM117HVKSTL		x	x	
LM117KSTEEL		x	x	x
LM118H		x		x
LM118J-8		x		x
LM118J		x		
LM118W				x
LM119H		x	x	
LM119J		x	x	
LM120H-12		x		
LM120H-15		x		
LM120H-5.0		x		
LM120K-12		x		
LM120K-15		x		
LM120K-5.0		x		
LM121AH		x		
LM121H		x		
LM122H		x		
LM123KSTEEL		x		
LM124AJ		x		
LM124J		x		x
LM125H		x		
LM126H		x		
LM129AH		x		
LM129BH		x		
LM131AH		x		
LM131H		x		
LM135H		x		
LM136AH-2.5		x	x	
LM136H-2.5		x		
LM136H-5.0		x		
LM137H		x	x	
LM137HVH		x	x	
LM137HVKSTEEL		x	x	
LM137KSTEEL		x	x	
LM138KSTEEL		x		
LM139AJ		x		
LM139J		x		x

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

Military Analog Products Available From National Semiconductor

Listed below are the military class B Analog devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

Device Type	Mil * Class B	883 Class B	Desc	JAN
LM139W				x
LM140AK-12		x		
LM140AK-15		x		
LM140AK-5.0		x		
LM140K-12		x		
LM140K-15		x		
LM140K-5.0		x		
LM140LAH-12		x		
LM140LAH-15		x		
LM140LAH-5.0		x		
LM143H		x	x	
LM144H		x	x	
LM145K-5.0		x		
LM145K-5.2		x		
LM146J		x		
LM148J		x		x
LM149J		x		
LM150KSTEEL	x			
LM1536H		x	x	
LM1558H		x		
LM1558J		x		
LM158AH		x		
LM158AJ		x		
LM158H		x		
LM158J		x		
LM1596H		x		
LM160H		x		
LM160J-14		x		
LM160J		x		
LM161F	x			
LM161H		x		
LM161J		x		
LM185BXH-1.2		x		
LM185BYH-1.2		x		

Device Type	Mil * Class B	883 Class B	Desc	JAN
LM185H-1.2		x		
LM193AH		x		
LM193H		x		x
LM193J-8				x
LM193W				x
LM194H		x		
LM195H		x		
LM195K		x		
LM199AH-20		x		
LM199AH		x		
LM199H		x		
LM4250H	x			
LM4250J	x			
LM555H		x		
LM555J		x		
LM556J	x			
LM567H		x		
LM709AH		x		
LM709H		x		
LM710H		x		
LM723H		x		
LM723J				x
LM725H		x		
LM733H	x			
LM741AJ-14		x		
LM741AJ		x		
LM741H		x		x
LM7415-14		x		
LM741J		x		x
LM741W		x		x
LM747H		x		x
LM747J		x		
LM748H		x		
LM748J		x		

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

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Appendix E
Understanding Integrated Circuit Package Power Capabilities

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

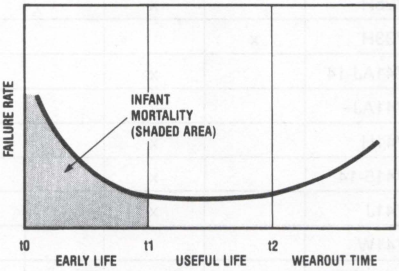

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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

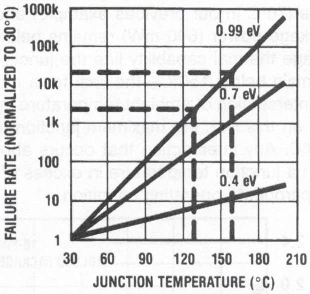

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D(\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using IC components.

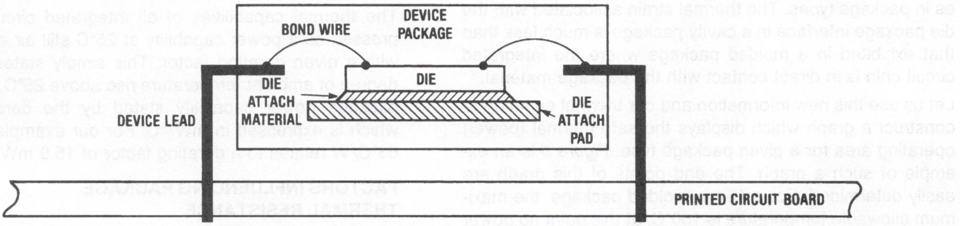

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

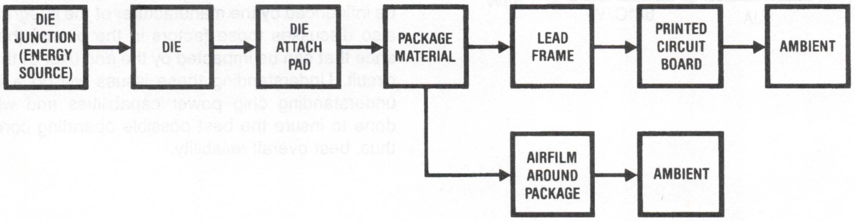

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, $T_A(\text{max})$, the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°\text{C} + (63°\text{C/W}) \times (0.6\text{W}) = 108°\text{C}$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°\text{C} = \frac{T_J(\text{max}) - T_A}{\theta_{JA}} = \frac{150°\text{C} - 25°\text{C}}{63°\text{C/W}} = 1.98\text{W}$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

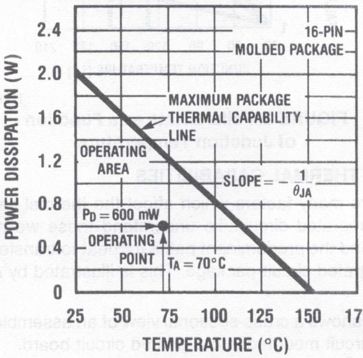

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all integrated circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

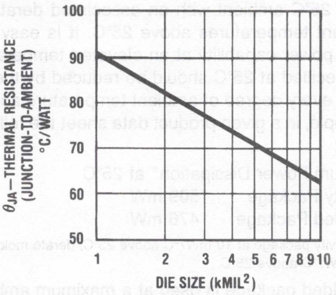

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

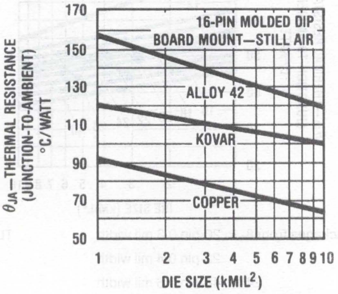

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

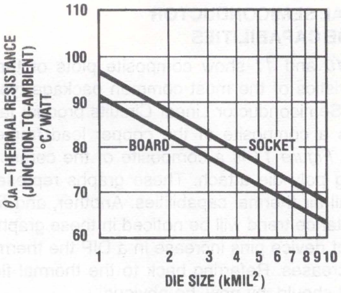

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

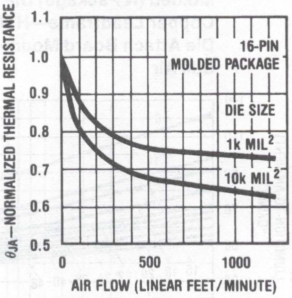

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Linear Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Linear Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the linear data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

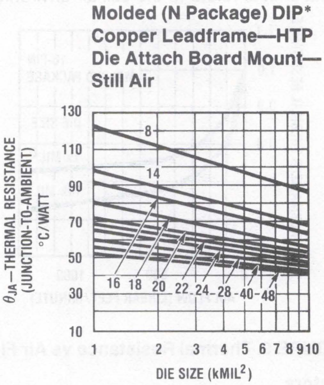
The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D \text{ @ } 70°C = 1476\text{ mW} - (11.8\text{ mW/°C}) \times (70°C - 25°C)$$
$$= 945\text{ mW}$$



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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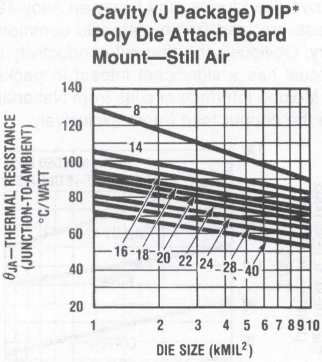
FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

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FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

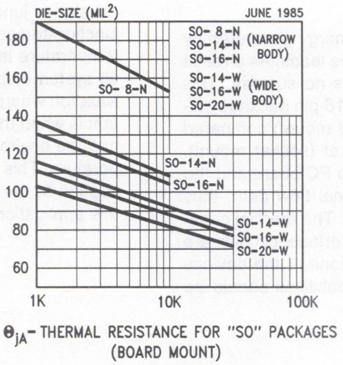

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FIGURE 12

National
Semiconductor
Corporation

APPENDIX F

How to Get the Right Information From a Data Sheet

Not All Data Sheets Are Created Alike, and False Assumptions Could Cost an Engineer Time and Money

By Robert A. Pease

When a new product arrives in the marketplace, it hopefully will have a good, clear data sheet with it.

The data sheet can show the prospective user how to apply the device, what performance specifications are guaranteed and various typical applications and characteristics. If the data-sheet writer has done a good job, the user can decide if the product will be valuable to him, exactly how well it will be of use to him and what precautions to take to avoid problems.

SPECIFICATIONS

The most important area of a data sheet specifies the characteristics that are guaranteed—and the test conditions that apply when the tests are done. Ideally, all specifications that the users will need will be spelled out clearly. If the product is similar to existing products, one can expect the data sheet to have a format similar to other devices.

But, if there are significant changes and improvements that nobody has seen before, then the writer must clarify what is meant by each specification. Definitions of new phrases or characteristics may even have to be added as an appendix.

For example, when fast-settling operational amplifiers were first introduced, some manufacturers defined settling time as the time after slewing before the output finally enters and stays within the error-band; but other manufacturers included the slewing time in their definition. Because both groups made their definitions clear, the user was unlikely to be confused or misled.

However, the reader ought to be on the alert. In a few cases, the data-sheet writer is playing a specsmanship game, and is trying to show an inferior (to some users) aspect of a product in a light that makes it look superior (which it may be, to a couple of users).

GUARANTEES

When a data sheet specifies a guaranteed minimum value, what does it mean? An assumption might be made that the manufacturer has actually tested that specification and has great confidence that no part could fail that test and still be shipped. Yet that is not always the case.

For instance, in the early days of op amps (20 years ago), the differential-input impedance might have been guaranteed at 1 MΩ—but the manufacturer obviously did not measure the impedance. When a customer insisted, "I have to know how you measure this impedance," it had to be explained that the impedance was not measured, but that the base current was. The correlation between I_b and Z_{in} permitted the substitution of this simple dc test for a rather messy, noisy, hard-to-interpret test.

Every year, for the last 20 years, manufacturers have been trying to explain, with varying success, why they do not measure the Z_{in} *per se,* even though they do guarantee it.

In other cases, the manufacturer may specify a test that can be made only on the die as it is probed on the wafer, but cannot be tested after the die is packaged because that signal is not accessible any longer. To avoid frustrating and confusing the customer, some manufacturers are establishing two classes of guaranteed specifications:

- The tested limit represents a test that cannot be doubted, one that is actually performed directly on 100 percent of the devices, 100 percent of the time.
- The design limit covers other tests that may be indirect, implicit or simply guaranteed by the inherent design of the device, and is unlikely to cause a failure rate (on that test), even as high as one part per thousand.

Why was this distinction made? Not just because customers wanted to know which specifications were guaranteed by testing, but because the quality-assurance group insisted that it was essential to separate the tested guarantees from the design limits so that the AQL (assurance-quality level) could be improved from 0.1 percent to down below 100 ppm.

Some data sheets guarantee characteristics that are quite expensive and difficult to test (even harder than noise) such as long-term drift (20 ppm or 50 ppm over 1,000 hours). The data sheet may not tell the reader if it is measured, tested or estimated. One manufacturer may perform a 100-percent test, while another states, "Guaranteed by sample testing." This is not a very comforting assurance that a part is good, especially in a critical case where only a long-term test can prove if the device did meet the manufacturer's specification. If in doubt, question the manufacturer.

TYPICALS

Next to a guaranteed specification, there is likely to be another in a column labeled "typical".

It might mean that the manufacturer once actually saw one part as good as that. It could indicate that half the parts are better than that specification, and half will be worse. But it is equally likely to mean that, five years ago, half the parts were better and half worse. It could easily signify that a few parts might be slightly better, and a few parts a lot worse; after all, if the noise of an amplifier is extremely close to the theoretical limit, one cannot expect to find anything much better than that, but there will always be a few noisy ones.

If the specification of interest happens to be the bias current (I_b) of an op amp, a user can expect broad variations. For example, if the specification is 200 nA maximum, there might be many parts where I_b is 40 nA on one batch (where the beta is high), and a month later, many parts where the I_b is 140 nA when the beta is low.

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Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temperature,	
TO-46 Package	−76°F to +356°F
TO-92 Package	−76°F to +300°F
* Lead Temp. (Soldering, 4 seconds)	
TO-46 Package	+300°C
TO-92 Package	+260°C
Specified Operating Temp. Range (Note 2)	
	T_{MIN} to T_{MAX}
LM34, LM34A	−50°F to +300°F
LM34C, LM34CA	−40°F to +230°F
LM34D	+32°F to +212°F

DC Electrical Characteristics (Note 1, Note 6)

Parameter	Conditions	LM34A Typical	LM34A Tested Limit (Note 4)	LM34A Design Limit (Note 5)	LM34CA Typical	LM34CA Tested Limit (Note 4)	LM34CA Design Limit (Note 5)	Units (Max)
Accuracy (Note 7)	$T_A = +77°F$	±0.4	±1.0		±0.4	±1.0		°F
	$T_A = 0°F$	±0.6			±0.6		±2.0	°F
	$T_A = T_{MAX}$	±0.8	±2.0		±0.8	±2.0		°F
	$T_A = T_{MIN}$	±0.8	±2.0		±0.8		±3.0	°F
Nonlinearity (Note 8)	$T_{MIN} \leq T_A \leq T_{MAX}$	±**0.35**		±**0.7**	±**0.30**		±**0.6**	°F
Sensor Gain (Average Slope)	$T_{MIN} \leq T_A \leq T_{MAX}$	+**10.0**	+**9.9**,		+**10.0**		+**9.9**,	mV/°F, min
			+**10.1**				+**10.1**	mV/°F, max
Load Regulation (Note 3)	$T_A = +77°F$	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \leq T_A \leq T_{MAX}$ $0 \leq I_L \leq 1$ mA	±**0.5**		±**3.0**	±**0.5**		±**3.0**	mV/mA
Line Regulation (Note 3)	$T_A = +77°F$	±0.01	±0.05		±0.01	±0.05		mV/V
	$5V \leq V_S \leq 30V$	±**0.02**		±**0.1**	±**0.02**		±**0.1**	mV/V
Quiescent Current (Note 9)	$V_S = +5V, +77°F$	75	90		75	90		μA
	$V_S = +5V$	**131**		**160**	**116**		**139**	μA
	$V_S = +30V, +77°F$	76	92		76	92		μA
	$V_S = +30V$	**132**		**163**	**117**		**142**	μA
Change of Quiescent Current (Note 3)	$4V \leq V_S \leq 30V, +77°F$	+0.5	2.0		0.5	2.0		μA
	$5V \leq V_S \leq 30V$	+**1.0**		**3.0**	**1.0**		**3.0**	μA
Temperature Coefficient of Quiescent Current		+**0.30**		+**0.5**	+**0.30**		+**0.5**	μA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, $I_L = 0$	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	$T_j = T_{MAX}$ for 1000 hours	±0.16			±0.16			°F

Note 1: Unless otherwise noted, these specifications apply: $-50°F \leq T_j \leq +300°F$ for the LM34 and LM34A; $-40°F \leq T_j \leq +230°F$ for the LM34C and LM34CA; and $+32°F \leq T_j \leq +212°F$ for the LM34D. $V_S = +5$ Vdc and $I_{LOAD} = 50$ μA in the circuit of *Figure 2;* +6 Vdc for LM34 and LM34A for $230°F \leq T_j \leq 300°F$. These specifications also apply from +5°F to T_{MAX} in the circuit of *Figure 1*.

Note 2: Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

Note 10: Contact factory for availability of LM34CAZ.

** **Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

A Point-By-Point Look

Let's look a little more closely at the data sheet of the National Semiconductor LM34, which happens to be a temperature sensor.

Note 1 lists the nominal test conditions and test circuits in which all the characteristics are defined. Some additional test conditions are listed in the column "Conditions", but Note 1 helps minimize the clutter.

Note 2 gives the thermal impedance, (which may also be shown in a chart or table).

Note 3 warns that an output impedance test, if done with a long pulse, could cause significant self-heating and thus, error.

Note 6 is intended to show which specs apply at all rated temperatures.

Note 7 is the definition of the "Accuracy" spec, and Note 8 the definition for non-linearity. Note 9 states in what test circuit the quiescent current is defined. Note 10 indicates that one model of the family may not be available at the time of printing (but happens to be available now), and Note 11 is the definition of Absolute Max Ratings.

* Note—the "4 seconds" soldering time is a new standard for plastic packages.

** Note—the wording of Note 11 has been revised—this is the best wording we can devise, and we will use it on all future datasheets.

APPLICATIONS

Another important part of the data sheet is the applications section. It indicates the novel and conventional ways to use a device. Sometimes these applications are just little ideas to tweak a reader's mind. After looking at a couple of applications, one can invent other ideas that are useful. Some applications may be of no real interest or use.

In other cases, an application circuit may be the complete definition of the system's performance; it can be the test circuit in which the specification limits are defined, tested and guaranteed. But, in all other instances, the performance of a typical application circuit is not guaranteed, it is only typical. In many circumstances, the performance may depend on external components and their precision and matching. Some manufacturers have added a phrase to their data sheets:

"Applications for any circuits contained in this document are for illustration purposes only and the manufacturer makes no representation or warranty that such applications will be suitable for the use indicated without further testing or modification."

In the future, manufacturers may find it necessary to add disclaimers of this kind to avoid disappointing users with circuits that work well, much of the time, but cannot be easily guaranteed.

The applications section is also a good place to look for advice on quirks—potential drawbacks or little details that may not be so little when a user wants to know if a device will actually deliver the expected performance.

For example, if a buffer can drive heavy loads and can handle fast signals cleanly (at no load), the maker isn't doing anybody any favors if there is no mention that the distortion goes sky-high if the rated load is applied.

Another example is the application hint for the LF156 family: "Exceeding the negative common-mode limit on either input will cause a reversal of the phase to output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and, thus the amplifier, in a normal operating mode."

That's the kind of information a manufacturer should really give to a data-sheet reader because no one could ever guess it.

Sometimes, a writer slips a quirk into a characteristic curve, but it's wiser to draw attention to it with a line of text. This is because it's better to make the user sad before one gets started, rather than when one goes into production. Conversely, if a user is going to spend more than 10 minutes using a new product, one ought to spend a full five minutes reading the entire data sheet.

FINE PRINT

What other fine print can be found on a data sheet? Sometimes the front page may be marked "advance" or "preliminary." Then on the back page, the fine print may say something such as:

"This data sheet contains preliminary limits and design specifications. Supplemental information will be published at a later date. The manufacturer reserves the right to make changes in the products contained in this document in order to improve design or performance and to supply the best possible products. We also assume no responsibility for the use of any circuits described herein, convey no license under any patent or other right and make no representation that the circuits are free from patent infringement."

In fact, after a device is released to the marketplace in a preliminary status, the engineers love to make small improvements and upgrades in specifications and characteristics, and hate to degrade a specification from its first published value—but occasionally that is necessary.

Another item in the fine print is the manufacturer's telephone number. Usually it is best to refer questions to the local sales representative or field-applications engineer, because they may know the answer or they may be best able to put a questioner in touch with the right person at the factory.

Occasionally, the factory's applications engineers have all the information. Other times, they have to bring in product engineers, test engineers or marketing people. And sometimes the answer can't be generated quickly—data have to be gathered, opinions solidified or policies formulated before the manufacturer can answer the question. Still, the telephone number is the key to getting the factory to help.

ORIGINS OF DATA SHEETS

Of course, historically, most data sheets for a class of products have been closely modeled on the data sheet of the forerunner of that class. The first data sheet was copied to make new versions.

That's the way it happened with the UA709 (the first monolithic op amp) and all its copies, as well as many other similar families of circuits.

Even today, an attempt is made to build on the good things learned from the past and add a few improvements when necessary. But, it's important to have real improvements, not just change for the sake of change.

So, while it's not easy to get the format and everything in it exactly right to please everybody, new data sheets are continually surfacing with new features, applications ideas, specifications and aids for the user. And, if the users complain loudly enough about misleading or inadequate data sheets, they can help lead the way to change data sheets. That's how many of today's improvements came about—through customer demand.

Who writes data sheets? In some cases, a marketing person does the actual writing and engineers do the checking. In other companies, the engineer writes, while marketing people and other engineers check. Sometimes, a committee seems to be doing the writing. None of these ways is necessarily wrong.

For example, one approach might be: The original designer of the product writes the data sheet (inside his head) at the same time the product is designed. The concept here is, if one can't find the proper ingredients for a data sheet—good applications, convenient features for the user and nicely tested specifications as the part is being designed—then maybe it's not a very good product until all those ingredients are completed. Thus, the collection of raw materials for a good data sheet is an integral part of the design of a product. The actual assembly of these materials is an art which can take place later.

WHEN TO WRITE DATA SHEETS

A new product becomes available. The applications engineers start evaluating their application circuits and the test engineers examine their production test equipment.

But how can the users evaluate the new device? They have to have a data sheet—which is still in the process of being written. Every week, as the data sheet writer tries to polish and refine the incipient data sheet, other engineers are reporting, "These spec limits and conditions have to be revised," and, "Those application circuits don't work like we thought they would; we'll have one running in a couple of days." The marketing people insist that the data sheet must be finalized and frozen right away so that they can start printing copies to go out with evaluation samples.

These trying conditions may explain why data sheets always seem to have been thrown together under panic conditions and why they have so many rough spots. Users should be aware of the conflicting requirements: Getting a data sheet "as completely as possible" and "as accurately as possible" is compromised if one wants to get the data sheet "as quickly as possible."

The reader should always question the manufacturer. What are the alternatives? By not asking the right question, a misunderstanding could arise; getting angry with the manufacturer is not to anyone's advantage.

Robert Pease has been staff scientist at National Semiconductor Corp., Santa Clara, Calif., for eleven years. He has designed numerous op amps, data converters, voltage regulators and analog-circuit functions.

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Appendix G
Obsolete Product Replacement Guide

Some device types, individual temperature grades and package options have been discontinued. This guide is provided to help design engineers select and specify an appropriate alternative.

NSC Part Number	Replacement	Note
ADB1200	ADC3711	2
DAC1200/1201	DAC1265	2
LF352	LM3631	2
LF13300	ADC3711	2
LH0001	LM4250	2
LH0005/LH0005A	LH0003	2
LH0037	LH0036	3
LH0132	LH0032	2
LH2011	LM11	2
LH2108	LM108	2
LH2201A	LM201A	2
LH2208	LM208	2
LH2208A	LM208A	2
LH2308	LM308	2
LH24250	LM11	2
LM170/270/370	LM13600N	2
LM171/271/371	no replacement	
LM172/272/372	no replacement	
LM173/273/373	no replacement	
LM174/274/374	no replacement	
LM175/275/375	no replacement	
LM216/316	LM11	2
LM388N-2/N-3	LM388N-1	2
LM377N	LM2877P	3
LM378N	LM2878P	3
LM379	LM2879T	3
LM1014	no replacement	
LM1017	no replacement	
LM1019	no replacement	
LM1821S	LM1823	2
LM1822	LM1823	3
LM1828	no replacement	
LM1848	no replacement	
LM1877N-1/N-2/N-3	LM1877N-9	2
LM2003	no replacement	
LM2808	no replacement	
LM2831	LM1851	2
LM3011	no replacement	
LM3064	no replacement	
LM3075	no replacement	
TBA120V	no replacement	
TBA440C	LM1823	2
TBA510	no replacement	
TBA530	no replacement	
TBA540	no replacement	
TBA560C	no replacement	
TBA920	no replacement	
TBA950-2	no replacement	
TBA970	no replacement	
TBA990	no replacement	
TDA440	no replacement	
TDA2522/23	no replacement	
TDA2530	no replacement	
TDA2530/31	no replacement	
TDA2540/41	no replacement	
TDA2560	no replacement	
TDA2590	no replacement	
TDA3500	no replacement	

Note 1: IMPROVED REPLACEMENT: Pin for Pin replacement with superior electrical specifications.

Note 2: FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

Note 3: SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

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Appendix H
Products Not Recommended for New Designs

The popular National Semiconductor Corporation monolithic IC's may have been designed into your systems. We believe that there are more cost-effective circuits manufactured by National Semiconductor Corporation that should be considered in your new designs. These recommendations are listed in this section. To eliminate the necessity to redesign proven equipment, we are continuing to make these products for use in existing designs for which they were uniquely suitable.

NSC Part Number	Recommended Replacement	Note
LH2301A	LM301A	2
LM103	LM185	3
LM113	LM1851-2	1
LM313	LM3851-2	1
LM377N	LM1877N-9	2
LM377N	LM2877P	3
LM378N	LM2878P	3
LM391N-60	LM391N-100	1
LM391N-80	LM391N-100	1
LM709	LF441	3
LM710	LM106	2
LM725	LM607	3
LM748	LF441	3

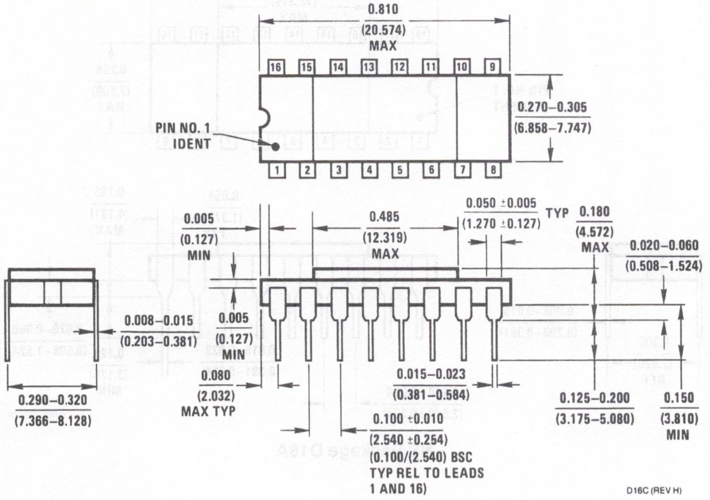
Notes:

Note 1: IMPROVED REPLACEMENT: Pin for Pin replacement with superior electrical specifications.

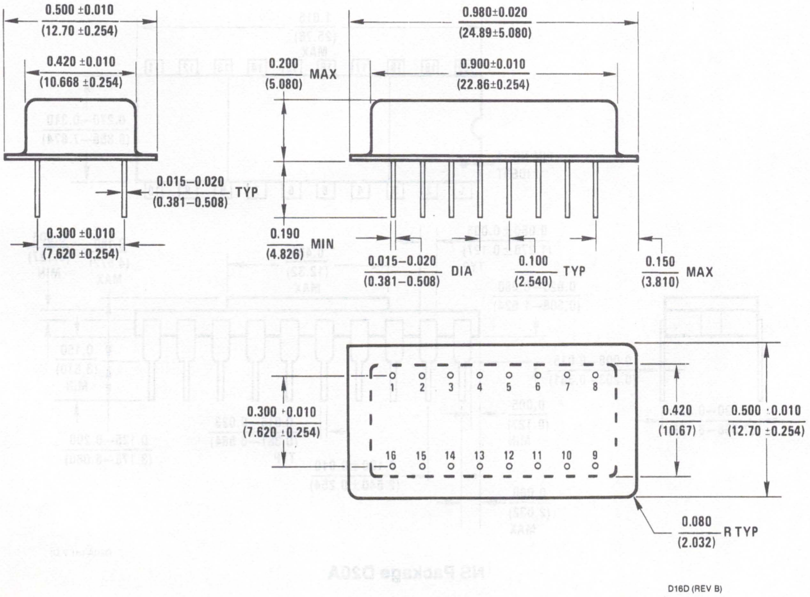
Note 2: FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

Note 3: SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

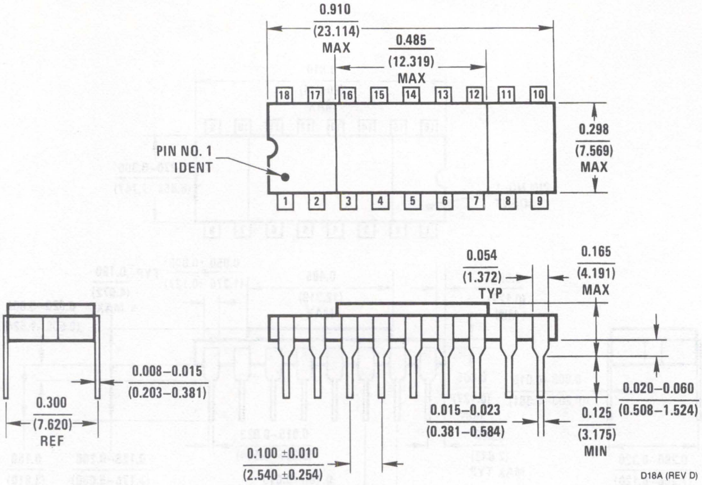
All dimensions are in inches (millimeters)


0.810
(20.574)
MAX
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
PIN NO. 1
IDENT
0.270–0.305
(6.858–7.747)
0.005
(0.127)
MIN
0.485
(12.319)
MAX
0.050 ±0.005
(1.270 ±0.127)
TYP
0.180
(4.572)
MAX
0.020–0.060
(0.508–1.524)
0.008–0.015
(0.203–0.381)
0.005
(0.127)
MIN
0.080
(2.032)
MAX TYP
0.015–0.023
(0.381–0.584)
0.290–0.320
(7.366–8.128)
0.100 ±0.010
(2.540 ±0.254)
(0.100/(2.540) BSC
TYP REL TO LEADS
1 AND 16)
0.125–0.200
(3.175–5.080)
0.150
(3.810)
MIN
D16C (REV H)

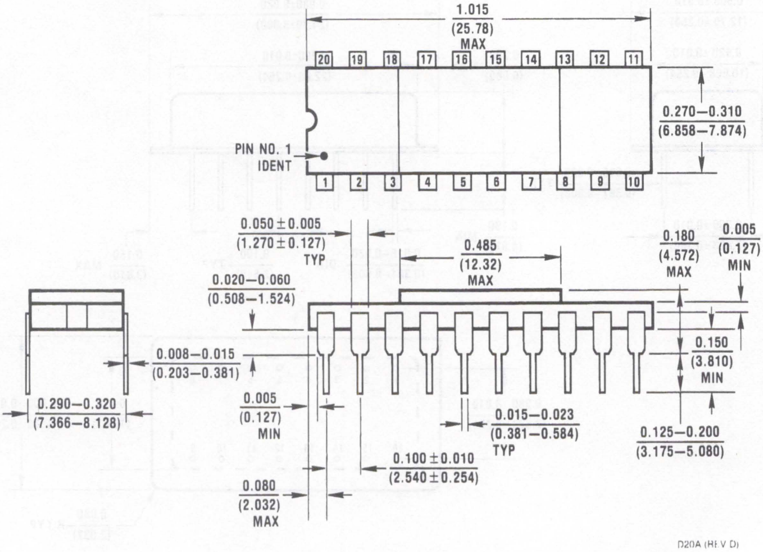
NS Package D16C


0.500 ±0.010
(12.70 ±0.254)
0.420 ±0.010
(10.668 ±0.254)
0.200
(5.080)
MAX
0.980±0.020
(24.89±5.080)
0.900±0.010
(22.86±0.254)
0.015–0.020
(0.381–0.508)
TYP
0.300 ±0.010
(7.620 ±0.254)
0.190
(4.826)
MIN
0.015–0.020
(0.381–0.508)
DIA
0.100
(2.540)
TYP
0.150
(3.810)
MAX
1 2 3 4 5 6 7 8
16 15 14 13 12 11 10 9
0.300 ±0.010
(7.620 ±0.254)
0.420
(10.67)
0.500 ±0.010
(12.70 ±0.254)
0.080
(2.032)
R TYP
D16D (REV B)

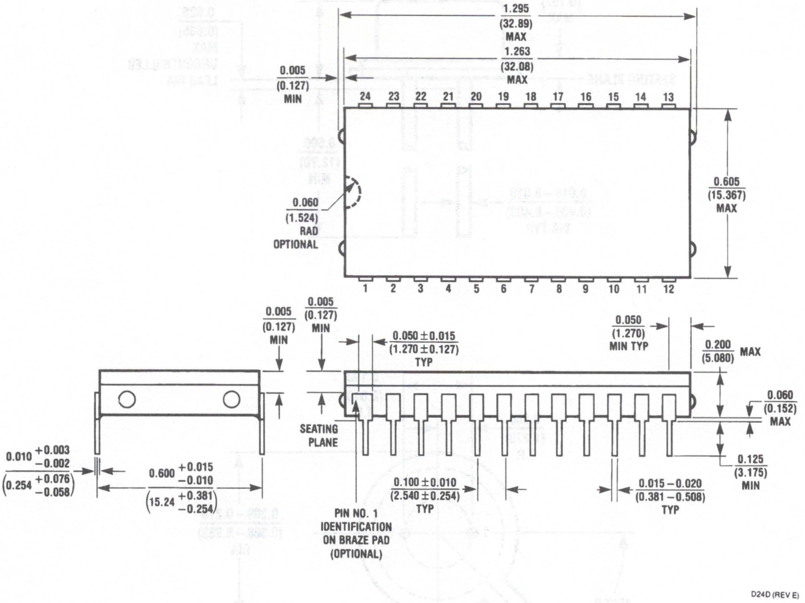
NS Package D16D


0.910
(23.114)
MAX
0.485
(12.319)
MAX
18
17
16
15
14
13
12
11
10
PIN NO. 1
IDENT
0.298
(7.569)
MAX
1
2
3
4
5
6
7
8
9
0.054
(1.372)
TYP
0.165
(4.191)
MAX
0.008–0.015
(0.203–0.381)
0.300
(7.620)
REF
0.020–0.060
(0.508–1.524)
0.015–0.023
(0.381–0.584)
0.125
(3.175)
MIN
0.100 ±0.010
(2.540 ±0.254)
D18A (REV D)

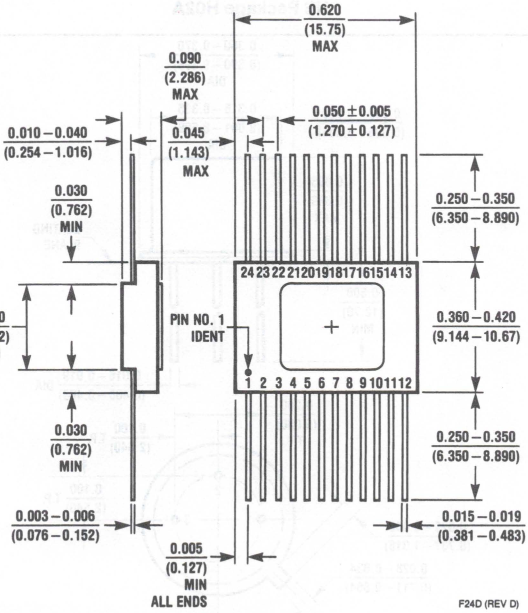
NS Package D18A


1.015
(25.78)
MAX
20
19
18
17
16
15
14
13
12
11
0.270–0.310
(6.858–7.874)
PIN NO. 1
IDENT
1
2
3
4
5
6
7
8
9
10
0.050 ± 0.005
(1.270 ± 0.127)
TYP
0.485
(12.32)
MAX
0.180
(4.572)
MAX
0.005
(0.127)
MIN
0.020–0.060
(0.508–1.524)
0.008–0.015
(0.203–0.381)
0.150
(3.810)
MIN
0.290–0.320
(7.366–8.128)
0.005
(0.127)
MIN
0.015–0.023
(0.381–0.584)
TYP
0.125–0.200
(3.175–5.080)
0.100 ± 0.010
(2.540 ± 0.254)
0.080
(2.032)
MAX
D20A (REV D)

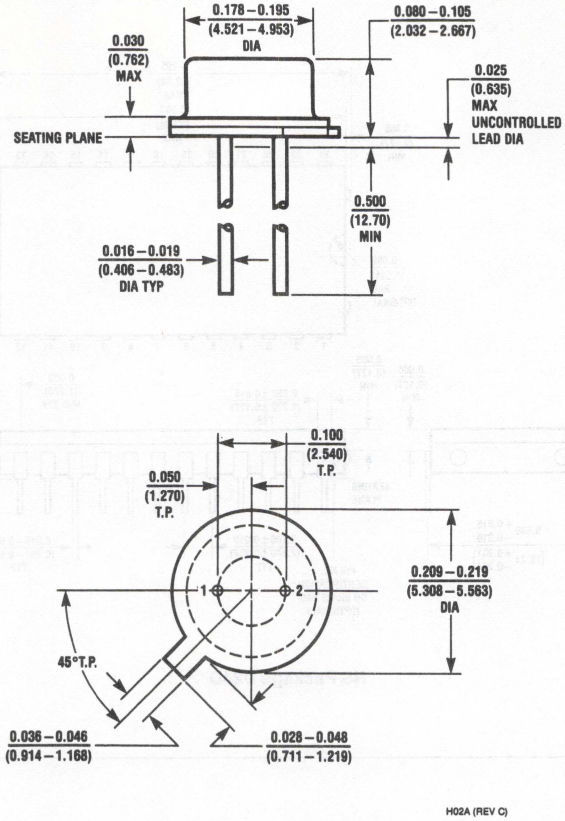
NS Package D20A


1.295
(32.89)
MAX
1.263
(32.08)
MAX
0.005
(0.127)
MIN
24 23 22 21 20 19 18 17 16 15 14 13
0.605
(15.367)
MAX
0.060
(1.524)
RAD
OPTIONAL
1 2 3 4 5 6 7 8 9 10 11 12
0.005
(0.127)
MIN
0.005
(0.127)
MIN
0.050 ± 0.015
(1.270 ± 0.127)
TYP
0.050
(1.270)
MIN TYP
0.200
(5.080) MAX
0.060
(0.152)
MAX
SEATING
PLANE
0.125
(3.175)
MIN
0.010 +0.003 −0.002
(0.254 +0.076 −0.058)
0.600 +0.015 −0.010
(15.24 +0.381 −0.254)
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.015 − 0.020
(0.381 − 0.508)
TYP
PIN NO. 1
IDENTIFICATION
ON BRAZE PAD
(OPTIONAL)
D24D (REV E)

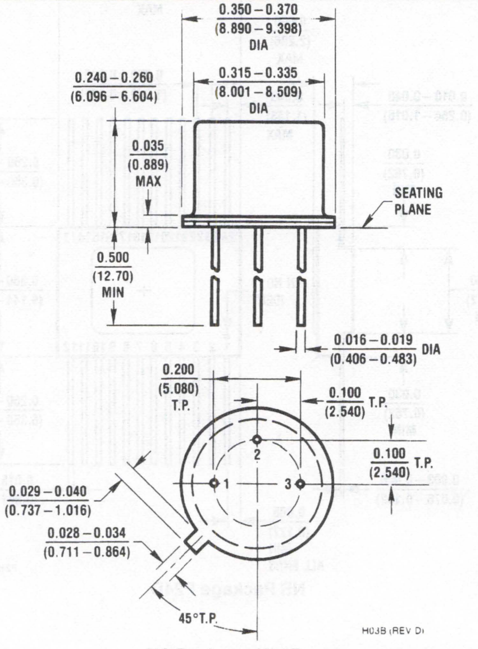
NS Package D24D


0.620
(15.75)
MAX
0.090
(2.286)
MAX
0.050 ± 0.005
(1.270 ± 0.127)
0.010 − 0.040
(0.254 − 1.016)
0.045
(1.143)
MAX
0.030
(0.762)
MIN
0.250 − 0.350
(6.350 − 8.890)
24 23 22 21 20 19 18 17 16 15 14 13
0.180
(4.572)
MIN
PIN NO. 1
IDENT
0.360 − 0.420
(9.144 − 10.67)
1 2 3 4 5 6 7 8 9 10 11 12
0.030
(0.762)
MIN
0.250 − 0.350
(6.350 − 8.890)
0.003 − 0.006
(0.076 − 0.152)
0.015 − 0.019
(0.381 − 0.483)
0.005
(0.127)
MIN
ALL ENDS
F24D (REV D)

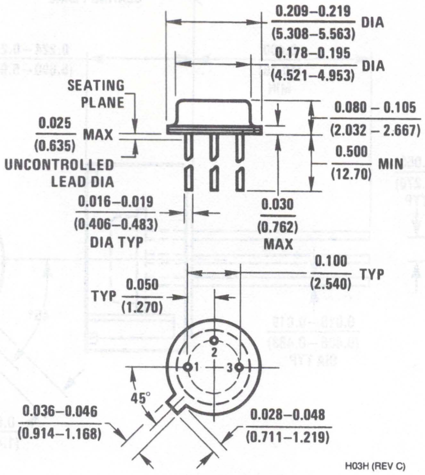
NS Package F24D


0.178 – 0.195
(4.521 – 4.953)
DIA
0.080 – 0.105
(2.032 – 2.667)
0.030
(0.762)
MAX
0.025
(0.635)
MAX
UNCONTROLLED
LEAD DIA
SEATING PLANE
0.500
(12.70)
MIN
0.016 – 0.019
(0.406 – 0.483)
DIA TYP
0.100
(2.540)
T.P.
0.050
(1.270)
T.P.
1
2
0.209 – 0.219
(5.308 – 5.563)
DIA
45°T.P.
0.036 – 0.046
(0.914 – 1.168)
0.028 – 0.048
(0.711 – 1.219)
H02A (REV C)

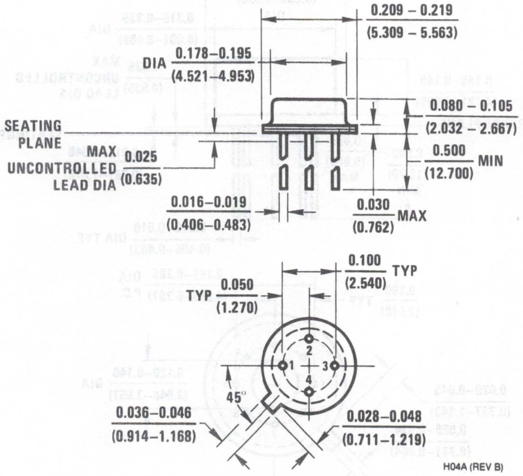
NS Package H02A


0.350 – 0.370
(8.890 – 9.398)
DIA
0.315 – 0.335
(8.001 – 8.509)
DIA
0.240 – 0.260
(6.096 – 6.604)
0.035
(0.889)
MAX
SEATING
PLANE
0.500
(12.70)
MIN
0.016 – 0.019
(0.406 – 0.483)
DIA
0.200
(5.080)
T.P.
0.100
(2.540)
T.P.
2
1
3
0.100
(2.540)
T.P.
0.029 – 0.040
(0.737 – 1.016)
0.028 – 0.034
(0.711 – 0.864)
45°T.P.
H03B (REV D)

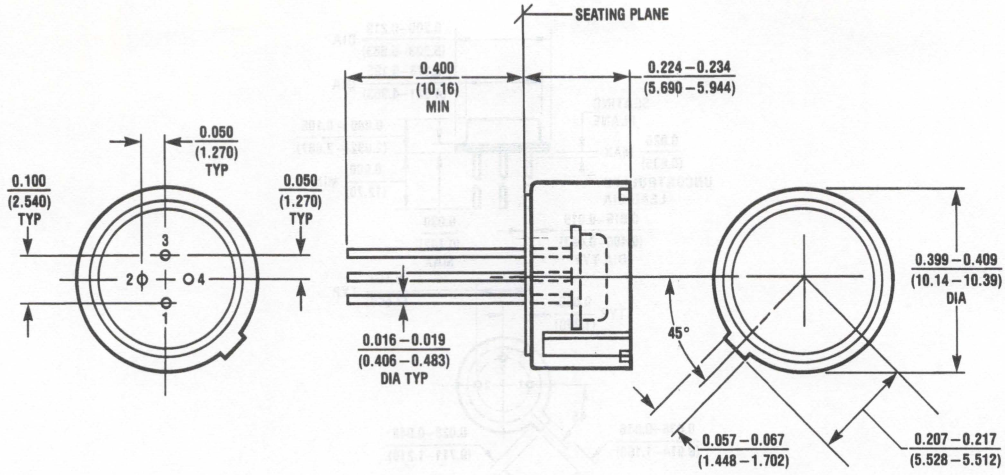
NS Package H03B


0.209–0.219 (5.308–5.563) DIA
0.178–0.195 (4.521–4.953) DIA
SEATING PLANE
0.025 (0.635) MAX
UNCONTROLLED LEAD DIA
0.080 – 0.105 (2.032 – 2.667)
0.500 (12.70) MIN
0.016–0.019 (0.406–0.483) DIA TYP
0.030 (0.762) MAX
0.100 (2.540) TYP
TYP 0.050 (1.270)
2
1
3
45°
0.036–0.046 (0.914–1.168)
0.028–0.048 (0.711–1.219)
H03H (REV C)

NS Package H03H

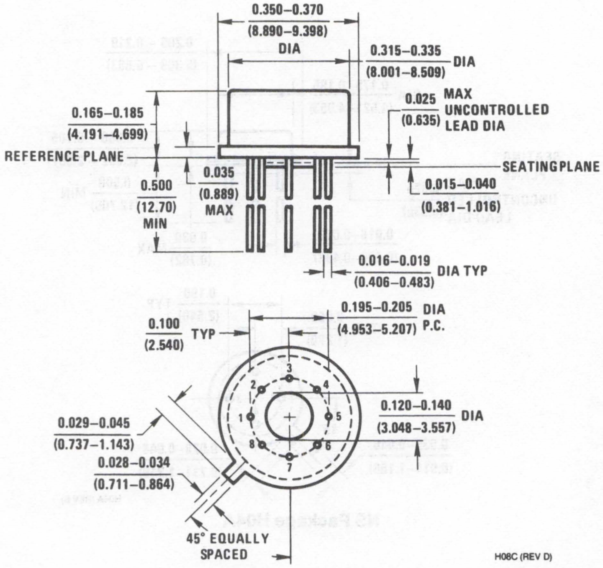

0.209 – 0.219 (5.309 – 5.563)
DIA 0.178–0.195 (4.521–4.953)
SEATING PLANE
MAX 0.025 (0.635)
UNCONTROLLED LEAD DIA
0.080 – 0.105 (2.032 – 2.667)
0.500 (12.700) MIN
0.016–0.019 (0.406–0.483)
0.030 (0.762) MAX
0.100 (2.540) TYP
TYP 0.050 (1.270)
2
1
3
4
45°
0.036–0.046 (0.914–1.168)
0.028–0.048 (0.711–1.219)
H04A (REV B)

NS Package H04A


SEATING PLANE
0.400
(10.16)
MIN
0.224 – 0.234
(5.690 – 5.944)
0.050
(1.270)
TYP
0.100
(2.540)
TYP
0.050
(1.270)
TYP
3
2
4
1
0.016 – 0.019
(0.406 – 0.483)
DIA TYP
0.399 – 0.409
(10.14 – 10.39)
DIA
45°
0.057 – 0.067
(1.448 – 1.702)
0.207 – 0.217
(5.528 – 5.512)

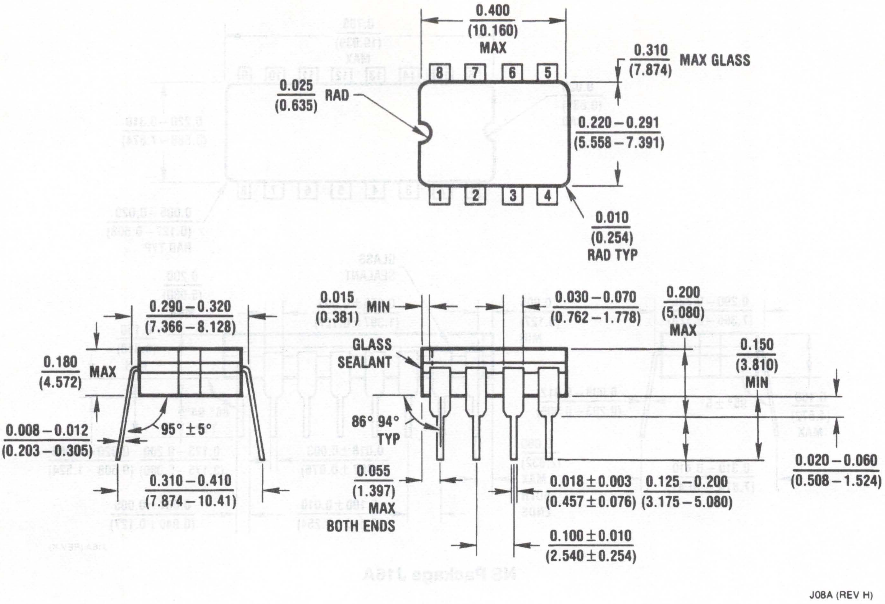
H04D (REV D)

NS Package H04D

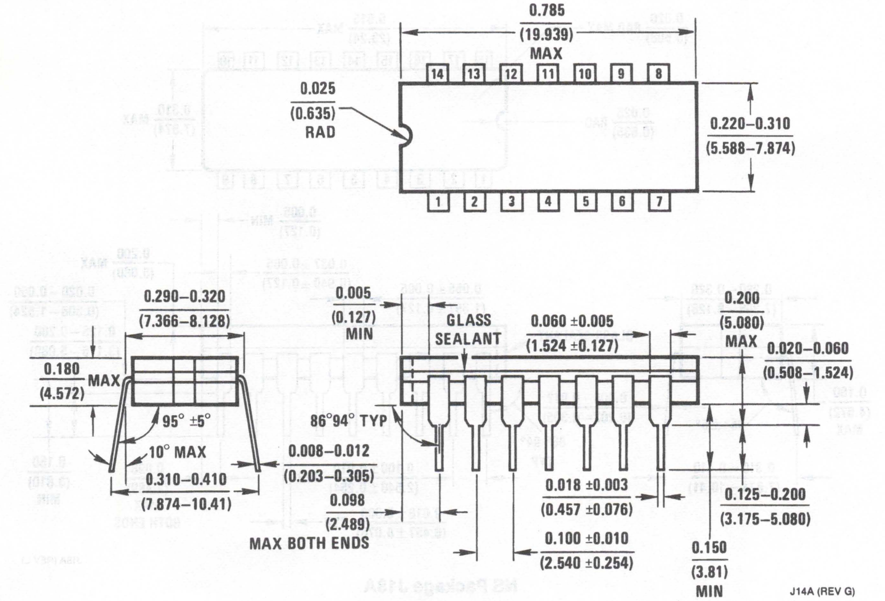

0.350–0.370
(8.890–9.398)
DIA
0.315–0.335
(8.001–8.509)
DIA
0.025
(0.635)
MAX
UNCONTROLLED
LEAD DIA
0.165–0.185
(4.191–4.699)
REFERENCE PLANE
SEATING PLANE
0.035
(0.889)
MAX
0.500
(12.70)
MIN
0.015–0.040
(0.381–1.016)
0.016–0.019
(0.406–0.483)
DIA TYP
0.195–0.205
(4.953–5.207)
DIA
P.C.
0.100
(2.540)
TYP
1
2
3
4
5
6
7
8
0.120–0.140
(3.048–3.557)
DIA
0.029–0.045
(0.737–1.143)
0.028–0.034
(0.711–0.864)
45° EQUALLY
SPACED

H08C (REV D)

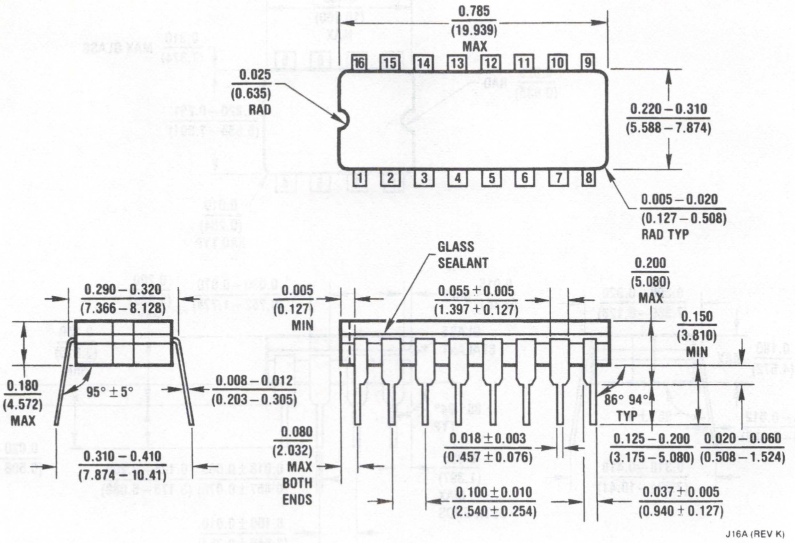
NS Package H08C


0.400
(10.160)
MAX
0.310
(7.874)
MAX GLASS
0.025
(0.635)
RAD
8
7
6
5
0.220 – 0.291
(5.558 – 7.391)
1
2
3
4
0.010
(0.254)
RAD TYP
0.290 – 0.320
(7.366 – 8.128)
0.015
(0.381)
MIN
0.030 – 0.070
(0.762 – 1.778)
0.200
(5.080)
MAX
0.180
(4.572)
MAX
GLASS
SEALANT
0.150
(3.810)
MIN
95° ± 5°
86° 94°
TYP
0.008 – 0.012
(0.203 – 0.305)
0.020 – 0.060
(0.508 – 1.524)
0.310 – 0.410
(7.874 – 10.41)
0.055
(1.397)
MAX
BOTH ENDS
0.018 ± 0.003
(0.457 ± 0.076)
0.125 – 0.200
(3.175 – 5.080)
0.100 ± 0.010
(2.540 ± 0.254)
J08A (REV H)

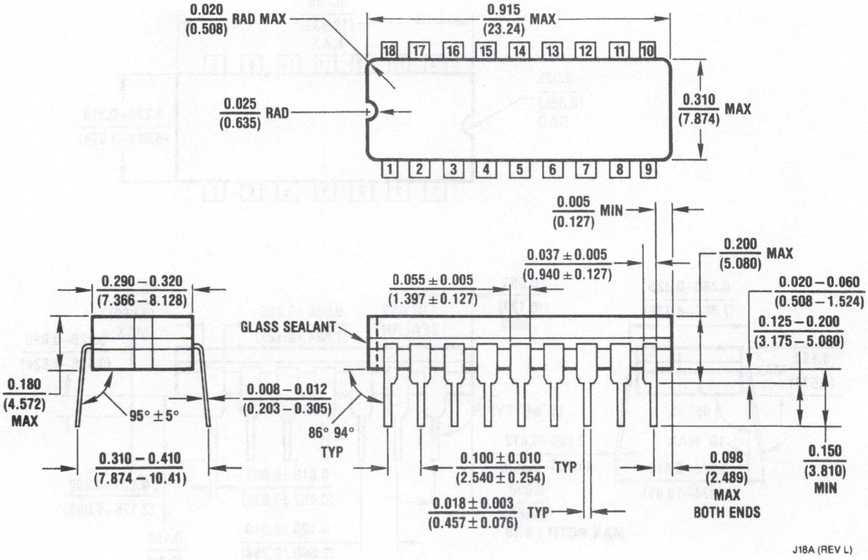
NS Package J08A


0.785
(19.939)
MAX
14
13
12
11
10
9
8
0.025
(0.635)
RAD
0.220–0.310
(5.588–7.874)
1
2
3
4
5
6
7
0.290–0.320
(7.366–8.128)
0.005
(0.127)
MIN
GLASS
SEALANT
0.060 ±0.005
(1.524 ±0.127)
0.200
(5.080)
MAX
0.020–0.060
(0.508–1.524)
0.180
(4.572)
MAX
95° ±5°
86°94° TYP
10° MAX
0.008–0.012
(0.203–0.305)
0.310–0.410
(7.874–10.41)
0.098
(2.489)
MAX BOTH ENDS
0.018 ±0.003
(0.457 ±0.076)
0.125–0.200
(3.175–5.080)
0.100 ±0.010
(2.540 ±0.254)
0.150
(3.81)
MIN
J14A (REV G)

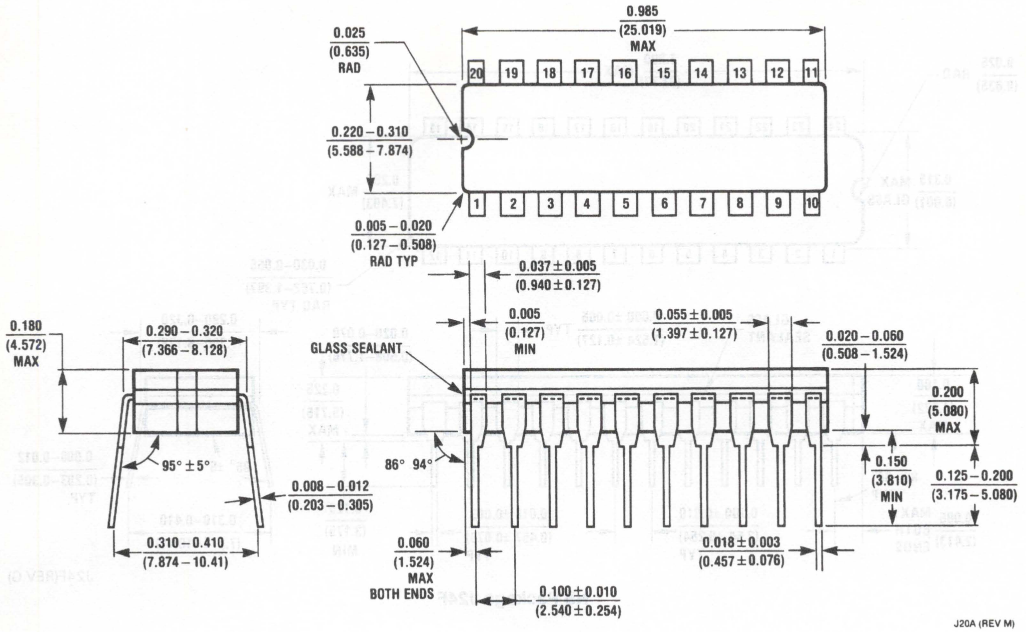
NS Package J14A


0.785
(19.939)
MAX
16 15 14 13 12 11 10 9
0.025
(0.635)
RAD
0.220 – 0.310
(5.588 – 7.874)
1 2 3 4 5 6 7 8
0.005 – 0.020
(0.127 – 0.508)
RAD TYP
GLASS
SEALANT
0.200
(5.080)
MAX
0.290 – 0.320
(7.366 – 8.128)
0.005
(0.127)
MIN
0.055 ± 0.005
(1.397 ± 0.127)
0.150
(3.810)
MIN
0.180
(4.572)
MAX
95° ± 5°
0.008 – 0.012
(0.203 – 0.305)
86° 94°
TYP
0.080
(2.032)
MAX
BOTH
ENDS
0.018 ± 0.003
(0.457 ± 0.076)
0.125 – 0.200
(3.175 – 5.080)
0.020 – 0.060
(0.508 – 1.524)
0.310 – 0.410
(7.874 – 10.41)
0.100 ± 0.010
(2.540 ± 0.254)
0.037 ± 0.005
(0.940 ± 0.127)
J16A (REV K)

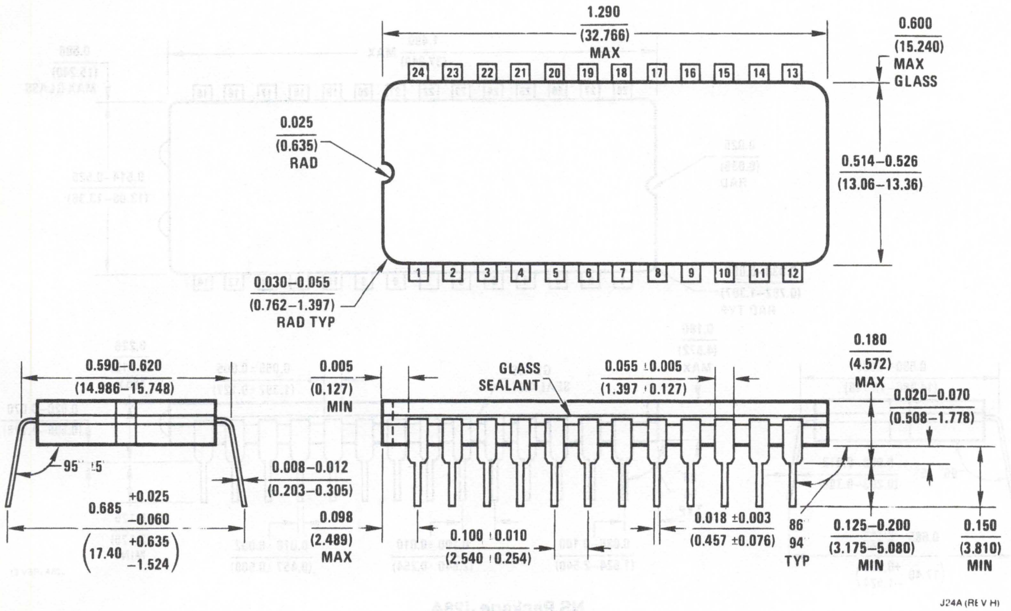
NS Package J16A


0.020
(0.508)
RAD MAX
0.915
(23.24)
MAX
18 17 16 15 14 13 12 11 10
0.025
(0.635)
RAD
0.310
(7.874)
MAX
1 2 3 4 5 6 7 8 9
0.005
(0.127)
MIN
0.037 ± 0.005
(0.940 ± 0.127)
0.200
(5.080)
MAX
0.290 – 0.320
(7.366 – 8.128)
0.055 ± 0.005
(1.397 ± 0.127)
0.020 – 0.060
(0.508 – 1.524)
GLASS SEALANT
0.125 – 0.200
(3.175 – 5.080)
0.180
(4.572)
MAX
95° ± 5°
0.008 – 0.012
(0.203 – 0.305)
86° 94°
TYP
0.310 – 0.410
(7.874 – 10.41)
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.098
(2.489)
MAX
BOTH ENDS
0.150
(3.810)
MIN
0.018 ± 0.003
(0.457 ± 0.076)
TYP
J18A (REV L)

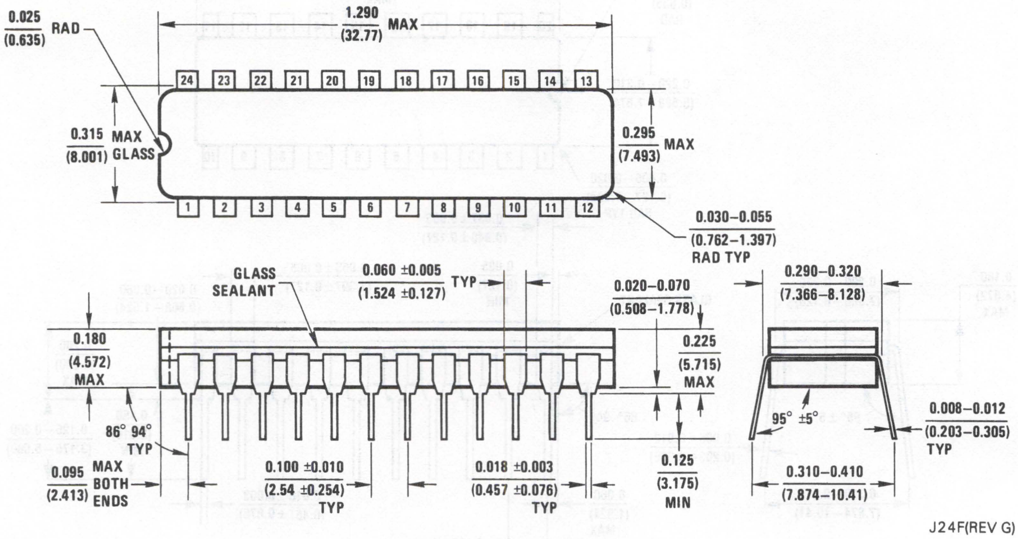
NS Package J18A


0.985
(25.019)
MAX
0.025
(0.635)
RAD
20
19
18
17
16
15
14
13
12
11
0.220 – 0.310
(5.588 – 7.874)
1
2
3
4
5
6
7
8
9
10
0.005 – 0.020
(0.127 – 0.508)
RAD TYP
0.037 ± 0.005
(0.940 ± 0.127)
0.180
(4.572)
MAX
0.290 – 0.320
(7.366 – 8.128)
GLASS SEALANT
0.005
(0.127)
MIN
0.055 ± 0.005
(1.397 ± 0.127)
0.020 – 0.060
(0.508 – 1.524)
0.200
(5.080)
MAX
95° ± 5°
86° 94°
0.008 – 0.012
(0.203 – 0.305)
0.150
(3.810)
MIN
0.125 – 0.200
(3.175 – 5.080)
0.310 – 0.410
(7.874 – 10.41)
0.060
(1.524)
MAX
BOTH ENDS
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
J20A (REV M)

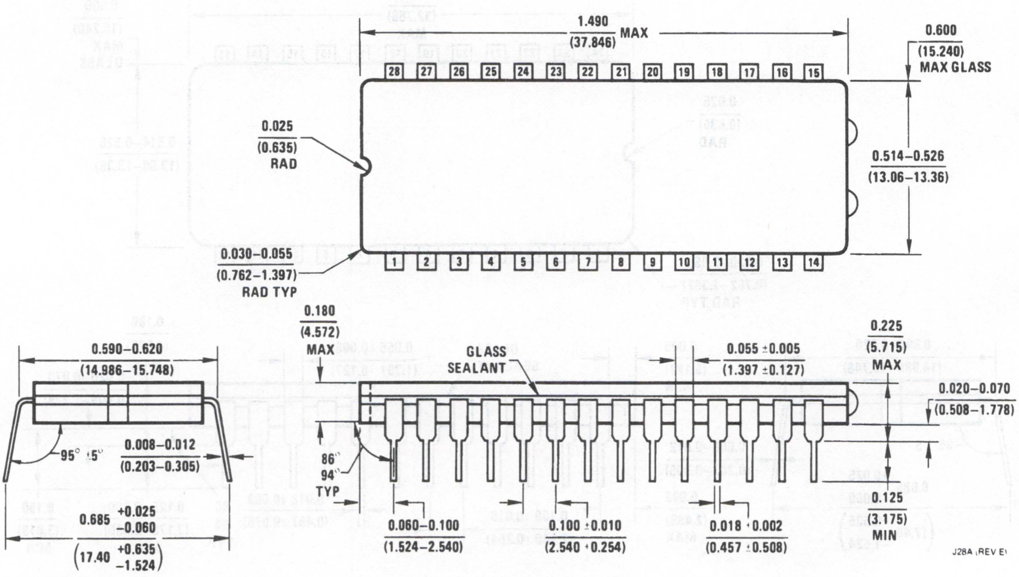
NS Package J20A


1.290
(32.766)
MAX
0.600
(15.240)
MAX
GLASS
24
23
22
21
20
19
18
17
16
15
14
13
0.025
(0.635)
RAD
0.514–0.526
(13.06–13.36)
1
2
3
4
5
6
7
8
9
10
11
12
0.030–0.055
(0.762–1.397)
RAD TYP
0.590–0.620
(14.986–15.748)
0.005
(0.127)
MIN
GLASS
SEALANT
0.055 ±0.005
(1.397 ±0.127)
0.180
(4.572)
MAX
0.020–0.070
(0.508–1.778)
95° ±5°
0.008–0.012
(0.203–0.305)
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.098
(2.489)
MAX
0.100 ±0.010
(2.540 ±0.254)
0.018 ±0.003
(0.457 ±0.076)
86°
94°
TYP
0.125–0.200
(3.175–5.080)
MIN
0.150
(3.810)
MIN
J24A (REV H)

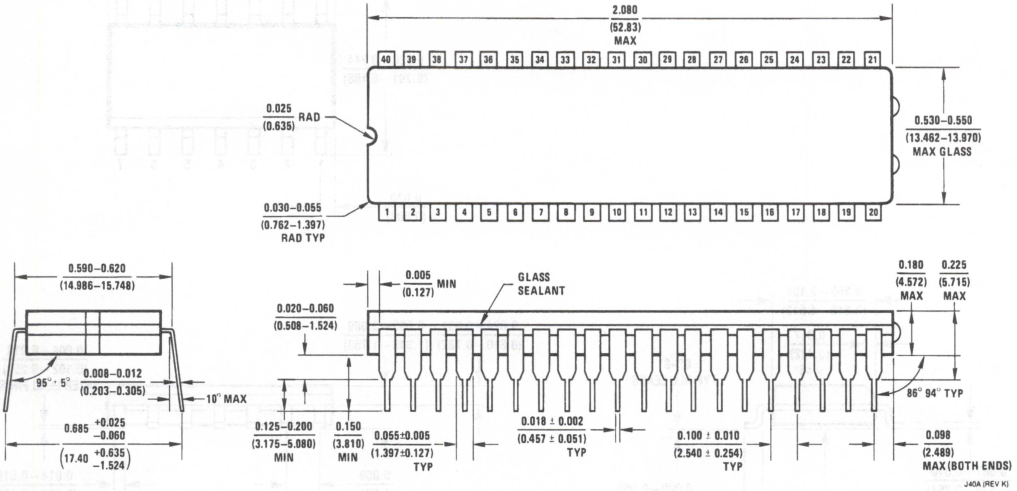
NS Package J24A


0.025
(0.635)
RAD
1.290
(32.77)
MAX
24
23
22
21
20
19
18
17
16
15
14
13
0.315
(8.001)
MAX
GLASS
0.295
(7.493)
MAX
1
2
3
4
5
6
7
8
9
10
11
12
0.030–0.055
(0.762–1.397)
RAD TYP
GLASS
SEALANT
0.060 ±0.005
(1.524 ±0.127)
TYP
0.020–0.070
(0.508–1.778)
0.290–0.320
(7.366–8.128)
0.180
(4.572)
MAX
0.225
(5.715)
MAX
86° 94°
TYP
95° ±5°
0.008–0.012
(0.203–0.305)
TYP
0.095
(2.413)
MAX
BOTH
ENDS
0.100 ±0.010
(2.54 ±0.254)
TYP
0.018 ±0.003
(0.457 ±0.076)
TYP
0.125
(3.175)
MIN
0.310–0.410
(7.874–10.41)
J24F(REV G)

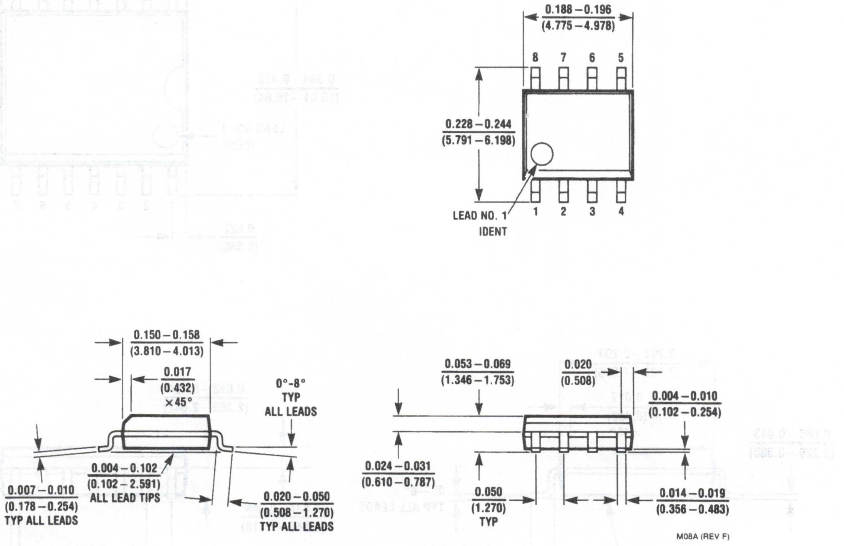
NS Package J24F


1.490
(37.846)
MAX
0.600
(15.240)
MAX GLASS
28
27
26
25
24
23
22
21
20
19
18
17
16
15
0.025
(0.635)
RAD
0.514–0.526
(13.06–13.36)
0.030–0.055
(0.762–1.397)
RAD TYP
1
2
3
4
5
6
7
8
9
10
11
12
13
14
0.180
(4.572)
MAX
0.590–0.620
(14.986–15.748)
GLASS
SEALANT
0.055 ±0.005
(1.397 ±0.127)
0.225
(5.715)
MAX
0.020–0.070
(0.508–1.778)
95° ±5°
0.008–0.012
(0.203–0.305)
86°
94°
TYP
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.060–0.100
(1.524–2.540)
0.100 ±0.010
(2.540 ±0.254)
0.018 ±0.002
(0.457 ±0.508)
0.125
(3.175)
MIN
J28A (REV E)

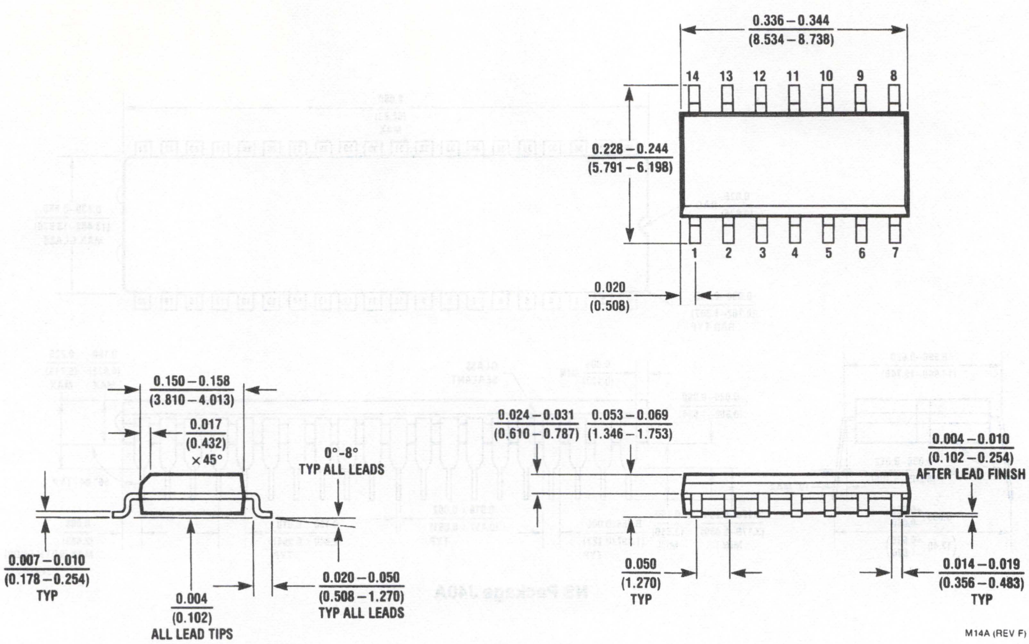
NS Package J28A


2.080
(52.83)
MAX
40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21
0.025
(0.635)
RAD
0.530–0.550
(13.462–13.970)
MAX GLASS
0.030–0.055
(0.762–1.397)
RAD TYP
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
0.590–0.620
(14.986–15.748)
0.005
(0.127)
MIN
GLASS
SEALANT
0.020–0.060
(0.508–1.524)
0.180
(4.572)
MAX
0.225
(5.715)
MAX
95° ± 5°
0.008–0.012
(0.203–0.305)
10° MAX
86° 94° TYP
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.125–0.200
(3.175–5.080)
MIN
0.150
(3.810)
MIN
0.055±0.005
(1.397±0.127)
TYP
0.018 ± 0.002
(0.457 ± 0.051)
TYP
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.098
(2.489)
MAX (BOTH ENDS)
J40A (REV K)

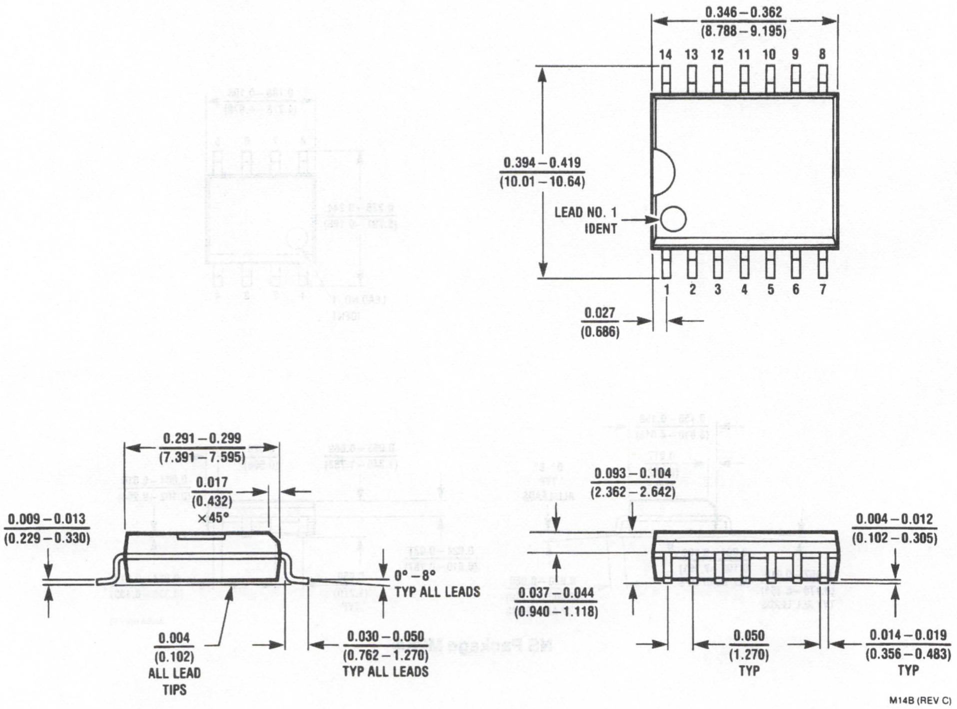
NS Package J40A


0.188 – 0.196
(4.775 – 4.978)
8 7 6 5
0.228 – 0.244
(5.791 – 6.198)
LEAD NO. 1
IDENT
1 2 3 4
0.150 – 0.158
(3.810 – 4.013)
0.017
(0.432)
× 45°
0°–8°
TYP
ALL LEADS
0.004 – 0.102
(0.102 – 2.591)
ALL LEAD TIPS
0.007 – 0.010
(0.178 – 0.254)
TYP ALL LEADS
0.020 – 0.050
(0.508 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.020
(0.508)
0.004 – 0.010
(0.102 – 0.254)
0.024 – 0.031
(0.610 – 0.787)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
M08A (REV F)

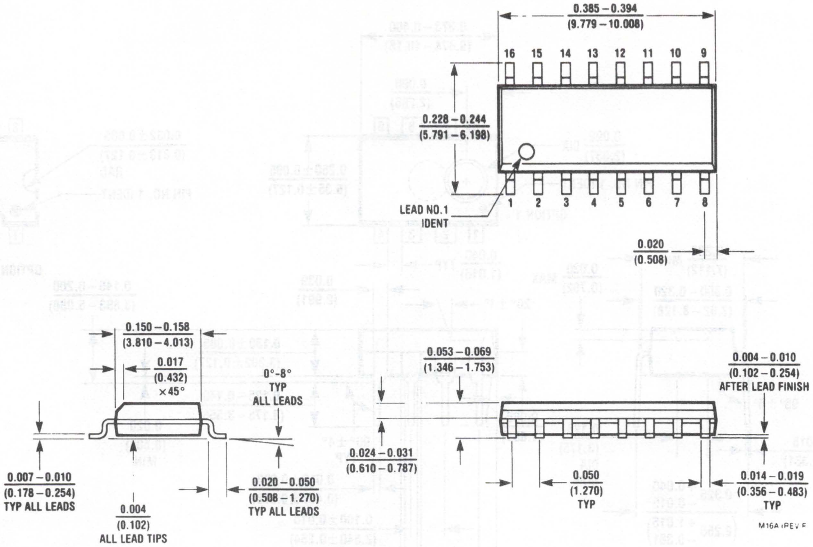
NS Package M08A


0.336 – 0.344
(8.534 – 8.738)
14
13
12
11
10
9
8
0.228 – 0.244
(5.791 – 6.198)
1
2
3
4
5
6
7
0.020
(0.508)
0.150 – 0.158
(3.810 – 4.013)
0.017
(0.432)
× 45°
0°-8°
TYP ALL LEADS
0.024 – 0.031
(0.610 – 0.787)
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
AFTER LEAD FINISH
0.007 – 0.010
(0.178 – 0.254)
TYP
0.004
(0.102)
ALL LEAD TIPS
0.020 – 0.050
(0.508 – 1.270)
TYP ALL LEADS
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M14A (REV F)

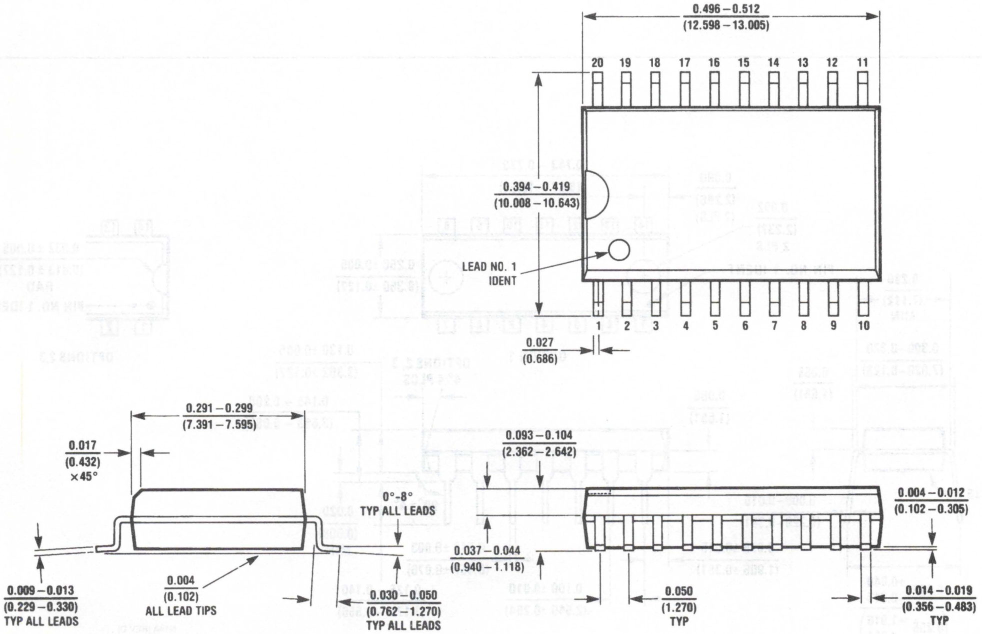
NS Package M14A


0.346 – 0.362
(8.788 – 9.195)
14
13
12
11
10
9
8
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1
IDENT
1
2
3
4
5
6
7
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432)
× 45°
0.009 – 0.013
(0.229 – 0.330)
0° – 8°
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
0.037 – 0.044
(0.940 – 1.118)
0.004
(0.102)
ALL LEAD
TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M14B (REV C)

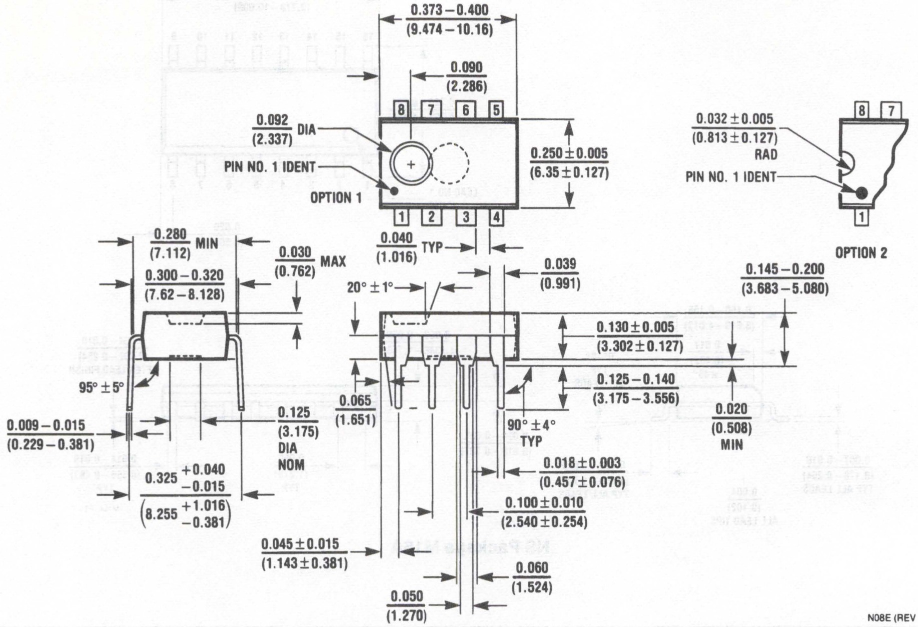
NS Package M14B


0.385 – 0.394
(9.779 – 10.008)
16 15 14 13 12 11 10 9
0.228 – 0.244
(5.791 – 6.198)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7 8
0.020
(0.508)
0.150 – 0.158
(3.810 – 4.013)
0.017
(0.432)
×45°
0°-8°
TYP
ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
AFTER LEAD FINISH
0.024 – 0.031
(0.610 – 0.787)
0.007 – 0.010
(0.178 – 0.254)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.020 – 0.050
(0.508 – 1.270)
TYP ALL LEADS
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M16A (REV F

NS Package M16A

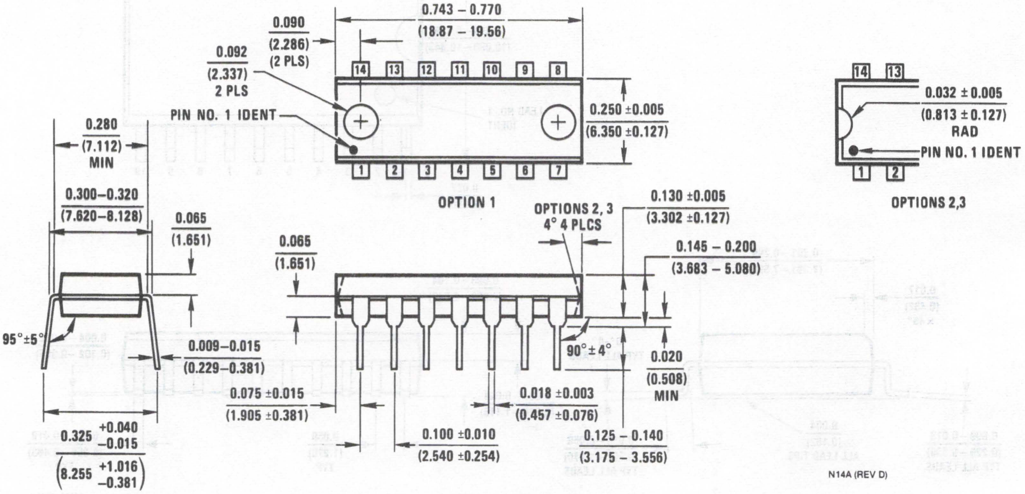

0.496 – 0.512
(12.598 – 13.005)
20 19 18 17 16 15 14 13 12 11
0.394 – 0.419
(10.008 – 10.643)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7 8 9 10
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432)
×45°
0.093 – 0.104
(2.362 – 2.642)
0°-8°
TYP ALL LEADS
0.004 – 0.012
(0.102 – 0.305)
0.037 – 0.044
(0.940 – 1.118)
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M20B (REV D)

NS Package M20B


0.373 – 0.400
(9.474 – 10.16)
0.090
(2.286)
0.092
(2.337)
DIA
PIN NO. 1 IDENT
OPTION 1
8
7
6
5
1
2
3
4
0.250 ± 0.005
(6.35 ± 0.127)
0.032 ± 0.005
(0.813 ± 0.127)
RAD
PIN NO. 1 IDENT
OPTION 2
0.280
(7.112)
MIN
0.300 – 0.320
(7.62 – 8.128)
0.030
(0.762)
MAX
0.040
(1.016)
TYP
0.039
(0.991)
20° ± 1°
0.145 – 0.200
(3.683 – 5.080)
0.130 ± 0.005
(3.302 ± 0.127)
0.125 – 0.140
(3.175 – 3.556)
0.020
(0.508)
MIN
95° ± 5°
0.065
(1.651)
0.125
(3.175)
DIA
NOM
90° ± 4°
TYP
0.009 – 0.015
(0.229 – 0.381)
0.018 ± 0.003
(0.457 ± 0.076)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.100 ± 0.010
(2.540 ± 0.254)
0.045 ± 0.015
(1.143 ± 0.381)
0.060
(1.524)
0.050
(1.270)

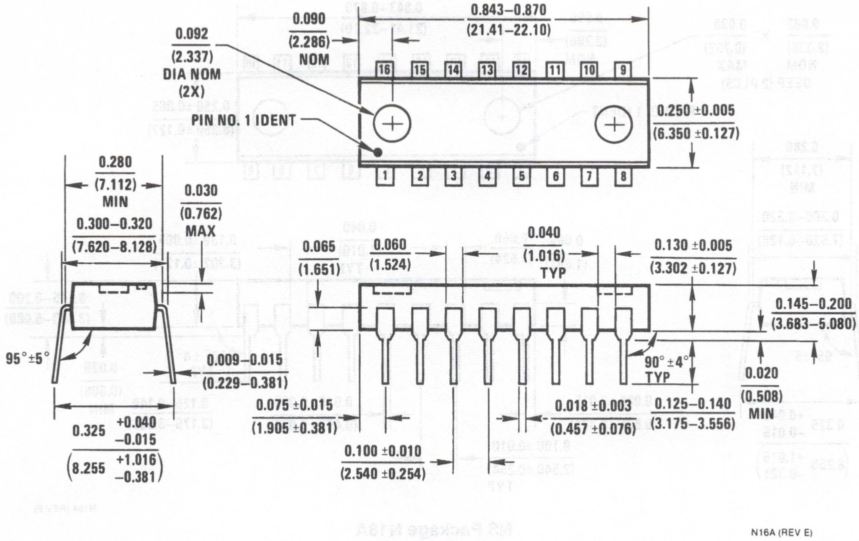
N08E (REV F)

NS Package N08E

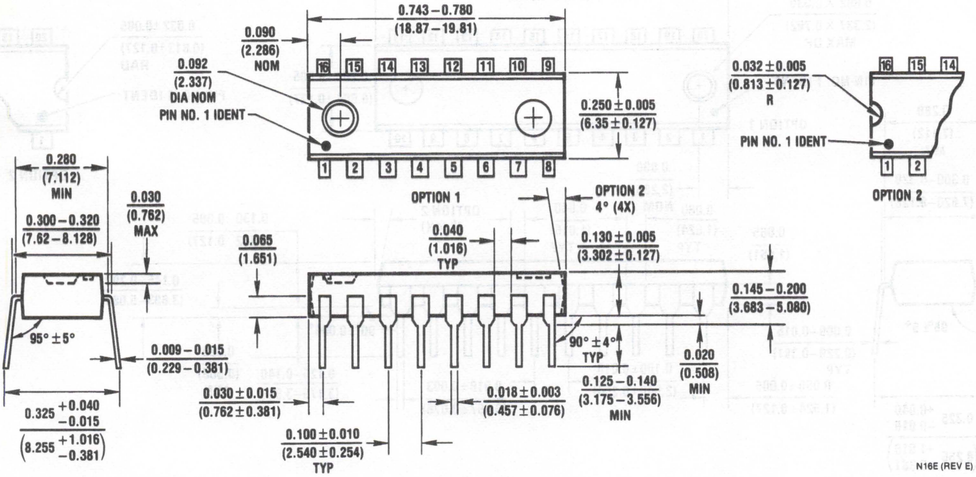

0.743 – 0.770
(18.87 – 19.56)
0.090
(2.286)
(2 PLS)
0.092
(2.337)
2 PLS
PIN NO. 1 IDENT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
0.250 ±0.005
(6.350 ±0.127)
OPTION 1
0.032 ± 0.005
(0.813 ± 0.127)
RAD
PIN NO. 1 IDENT
OPTIONS 2,3
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
0.065
(1.651)
0.065
(1.651)
OPTIONS 2, 3
4° 4 PLCS
0.130 ±0.005
(3.302 ±0.127)
0.145 – 0.200
(3.683 – 5.080)
95°±5°
0.009–0.015
(0.229–0.381)
90° ± 4°
0.020
(0.508)
MIN
0.075 ±0.015
(1.905 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.100 ±0.010
(2.540 ±0.254)
0.125 – 0.140
(3.175 – 3.556)

N14A (REV D)

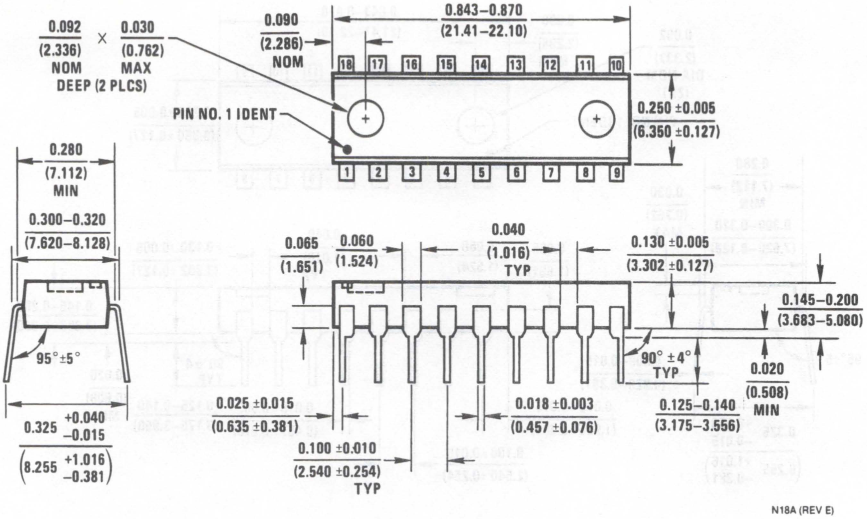
NS Package N14A


0.843–0.870
(21.41–22.10)
0.090
(2.286)
NOM
0.092
(2.337)
DIA NOM
(2X)
PIN NO. 1 IDENT
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
0.250 ±0.005
(6.350 ±0.127)
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
0.030
(0.762)
MAX
95° ±5°
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.009–0.015
(0.229–0.381)
0.065
(1.651)
0.060
(1.524)
0.040
(1.016)
TYP
0.130 ±0.005
(3.302 ±0.127)
0.145–0.200
(3.683–5.080)
90° ±4°
TYP
0.020
(0.508)
MIN
0.075 ±0.015
(1.905 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
0.100 ±0.010
(2.540 ±0.254)
N16A (REV E)

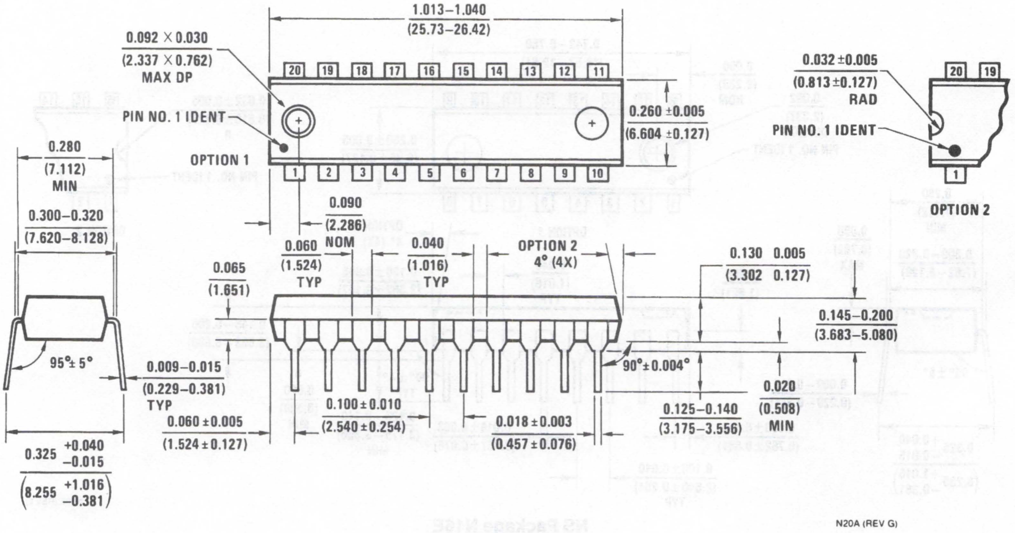
NS Package N16A


0.743 – 0.780
(18.87 – 19.81)
0.090
(2.286)
NOM
0.092
(2.337)
DIA NOM
PIN NO. 1 IDENT
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
0.250 ± 0.005
(6.35 ± 0.127)
0.032 ± 0.005
(0.813 ± 0.127)
R
PIN NO. 1 IDENT
16
15
14
1
2
OPTION 1
OPTION 2
OPTION 2
4° (4X)
0.280
(7.112)
MIN
0.300 – 0.320
(7.62 – 8.128)
0.030
(0.762)
MAX
0.065
(1.651)
0.040
(1.016)
TYP
0.130 ± 0.005
(3.302 ± 0.127)
0.145 – 0.200
(3.683 – 5.080)
95° ± 5°
0.009 – 0.015
(0.229 – 0.381)
90° ± 4°
TYP
0.020
(0.508)
MIN
0.125 – 0.140
(3.175 – 3.556)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.030 ± 0.015
(0.762 ± 0.381)
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
TYP
N16E (REV E)

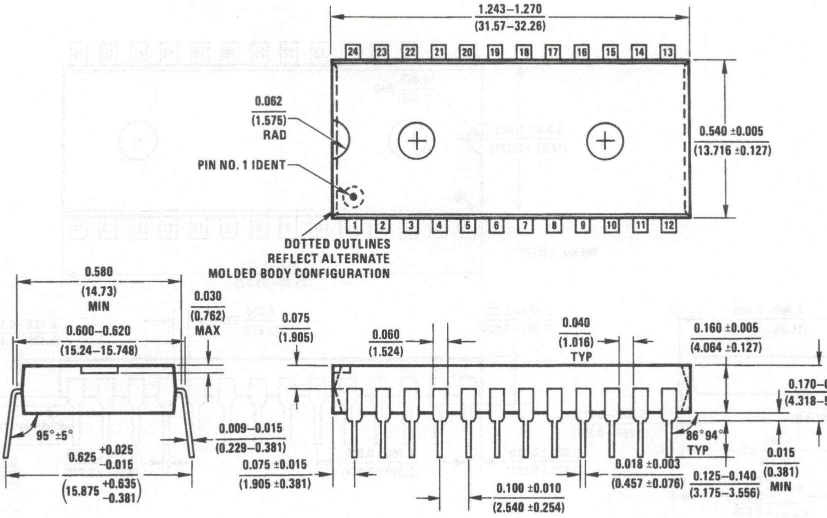
NS Package N16E


0.092 (2.336) NOM × 0.030 (0.762) MAX DEEP (2 PLCS)
0.090 (2.286) NOM
0.843–0.870 (21.41–22.10)
18 17 16 15 14 13 12 11 10
1 2 3 4 5 6 7 8 9
PIN NO. 1 IDENT
0.250 ±0.005 (6.350 ±0.127)
0.280 (7.112) MIN
0.300–0.320 (7.620–8.128)
95° ±5°
0.065 (1.651)
0.060 (1.524)
0.040 (1.016) TYP
0.130 ±0.005 (3.302 ±0.127)
0.145–0.200 (3.683–5.080)
90° ±4° TYP
0.020 (0.508) MIN
0.125–0.140 (3.175–3.556)
0.325 +0.040 −0.015 (8.255 +1.016 −0.381)
0.025 ±0.015 (0.635 ±0.381)
0.018 ±0.003 (0.457 ±0.076)
0.100 ±0.010 (2.540 ±0.254) TYP
N18A (REV E)

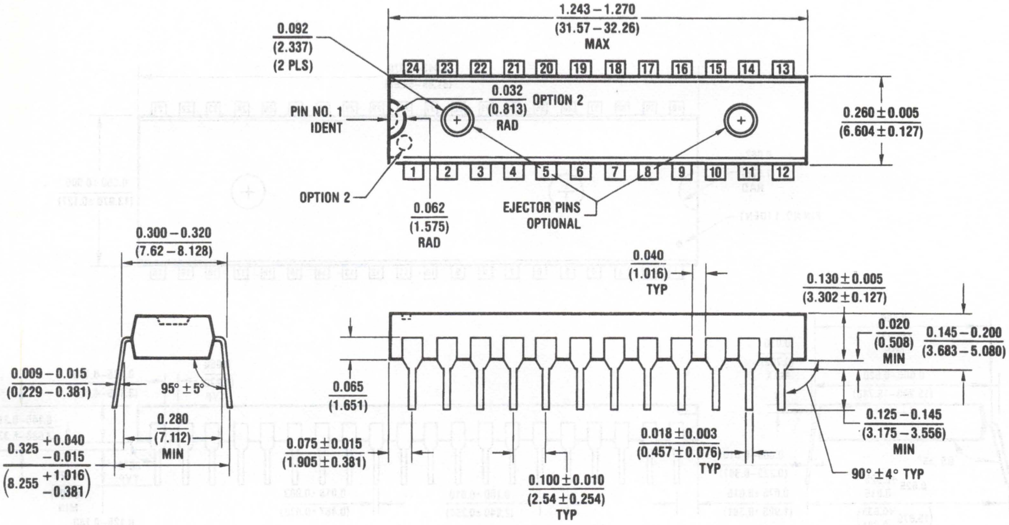
NS Package N18A


1.013–1.040 (25.73–26.42)
0.092 × 0.030 (2.337 × 0.762) MAX DP
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
PIN NO. 1 IDENT
OPTION 1
0.260 ±0.005 (6.604 ±0.127)
0.032 ±0.005 (0.813 ±0.127) RAD
PIN NO. 1 IDENT
OPTION 2
0.280 (7.112) MIN
0.300–0.320 (7.620–8.128)
0.090 (2.286) NOM
0.065 (1.651)
0.060 (1.524) TYP
0.040 (1.016) TYP
OPTION 2 4° (4X)
0.130 0.005 (3.302 0.127)
0.145–0.200 (3.683–5.080)
95° ± 5°
0.009–0.015 (0.229–0.381) TYP
90° ± 0.004°
0.020 (0.508) MIN
0.125–0.140 (3.175–3.556)
0.100 ± 0.010 (2.540 ± 0.254)
0.018 ± 0.003 (0.457 ± 0.076)
0.060 ± 0.005 (1.524 ± 0.127)
0.325 +0.040 −0.015 (8.255 +1.016 −0.381)
N20A (REV G)

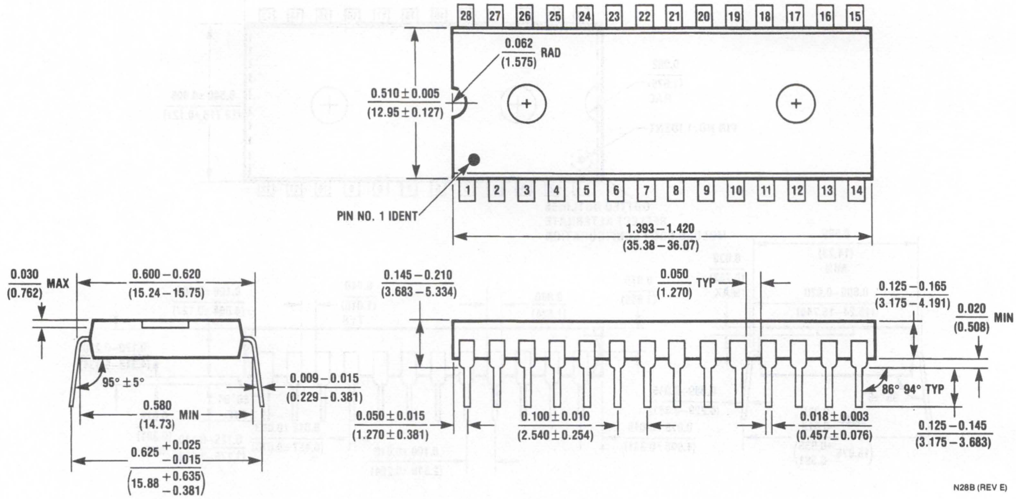
NS Package N20A


1.243–1.270
(31.57–32.26)
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
0.062
(1.575)
RAD
PIN NO. 1 IDENT
0.540 ±0.005
(13.716 ±0.127)
DOTTED OUTLINES
REFLECT ALTERNATE
MOLDED BODY CONFIGURATION
0.580
(14.73)
MIN
0.030
(0.762)
MAX
0.600–0.620
(15.24–15.748)
0.075
(1.905)
0.060
(1.524)
0.040
(1.016)
TYP
0.160 ±0.005
(4.064 ±0.127)
0.170–0.210
(4.318–5.334)
95° ±5°
0.009–0.015
(0.229–0.381)
0.625 +0.025 −0.015
(15.875 +0.635 −0.381)
0.075 ±0.015
(1.905 ±0.381)
86°94°
TYP
0.015
(0.381)
MIN
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
0.100 ±0.010
(2.540 ±0.254)
N24A (REV E)

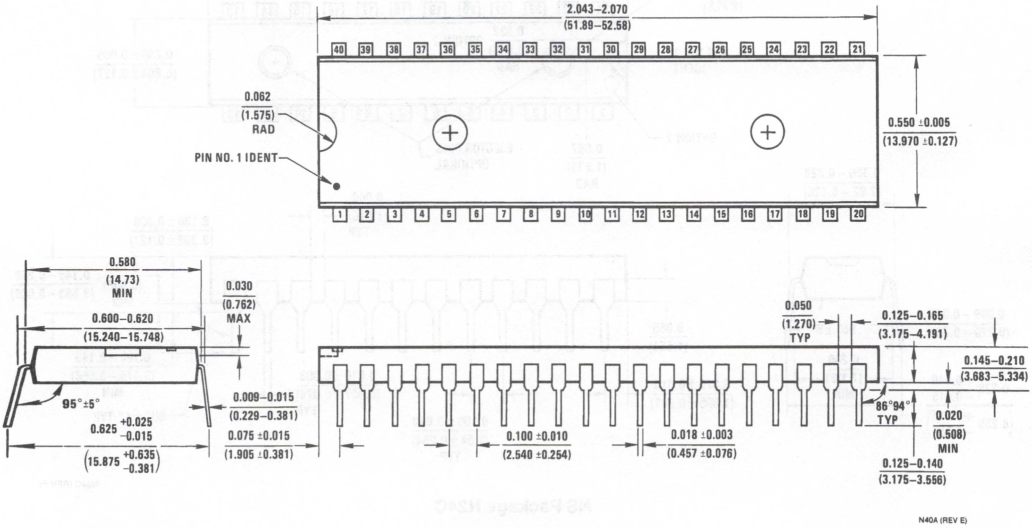
NS Package N24A


1.243 – 1.270
(31.57 – 32.26)
MAX
0.092
(2.337)
(2 PLS)
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
0.032
(0.813)
RAD
OPTION 2
PIN NO. 1
IDENT
0.260 ± 0.005
(6.604 ± 0.127)
OPTION 2
0.062
(1.575)
RAD
EJECTOR PINS
OPTIONAL
0.300 – 0.320
(7.62 – 8.128)
0.040
(1.016)
TYP
0.130 ± 0.005
(3.302 ± 0.127)
0.020
(0.508)
MIN
0.145 – 0.200
(3.683 – 5.080)
0.009 – 0.015
(0.229 – 0.381)
95° ± 5°
0.065
(1.651)
0.280
(7.112)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.075 ± 0.015
(1.905 ± 0.381)
0.018 ± 0.003
(0.457 ± 0.076)
TYP
0.125 – 0.145
(3.175 – 3.556)
MIN
90° ± 4° TYP
0.100 ± 0.010
(2.54 ± 0.254)
TYP
N24C (REV F)

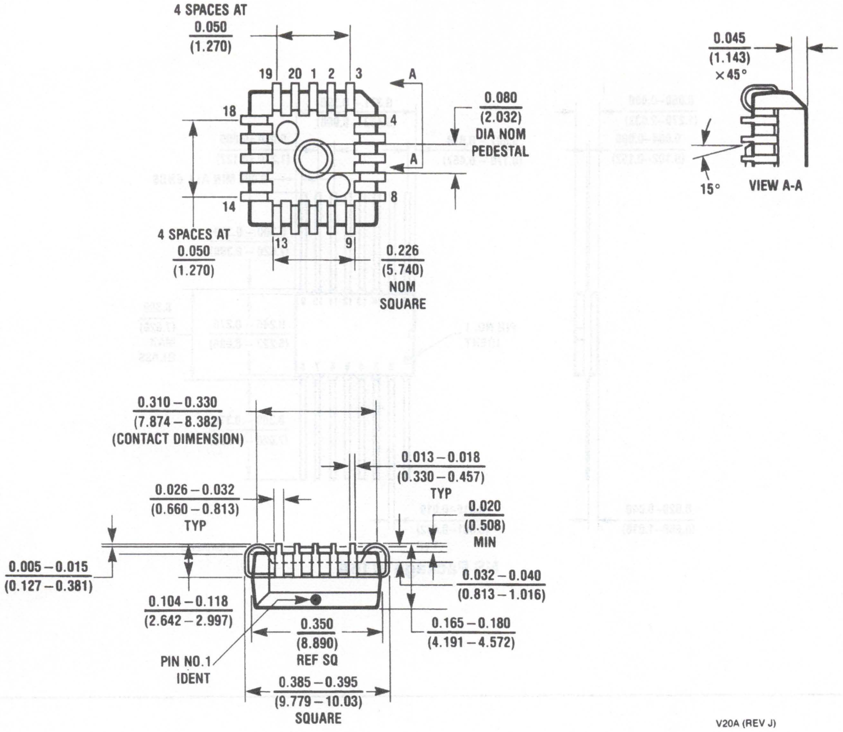
NS Package N24C


28
27
26
25
24
23
22
21
20
19
18
17
16
15
0.062 (1.575) RAD
0.510 ± 0.005 (12.95 ± 0.127)
PIN NO. 1 IDENT
1
2
3
4
5
6
7
8
9
10
11
12
13
14
1.393 – 1.420 (35.38 – 36.07)
0.030 (0.762) MAX
0.600 – 0.620 (15.24 – 15.75)
95° ± 5°
0.009 – 0.015 (0.229 – 0.381)
0.580 (14.73) MIN
0.625 +0.025 −0.015 (15.88 +0.635 −0.381)
0.145 – 0.210 (3.683 – 5.334)
0.050 (1.270) TYP
0.125 – 0.165 (3.175 – 4.191)
0.020 (0.508) MIN
86° 94° TYP
0.050 ± 0.015 (1.270 ± 0.381)
0.100 ± 0.010 (2.540 ± 0.254)
0.018 ± 0.003 (0.457 ± 0.076)
0.125 – 0.145 (3.175 – 3.683)
N28B (REV E)

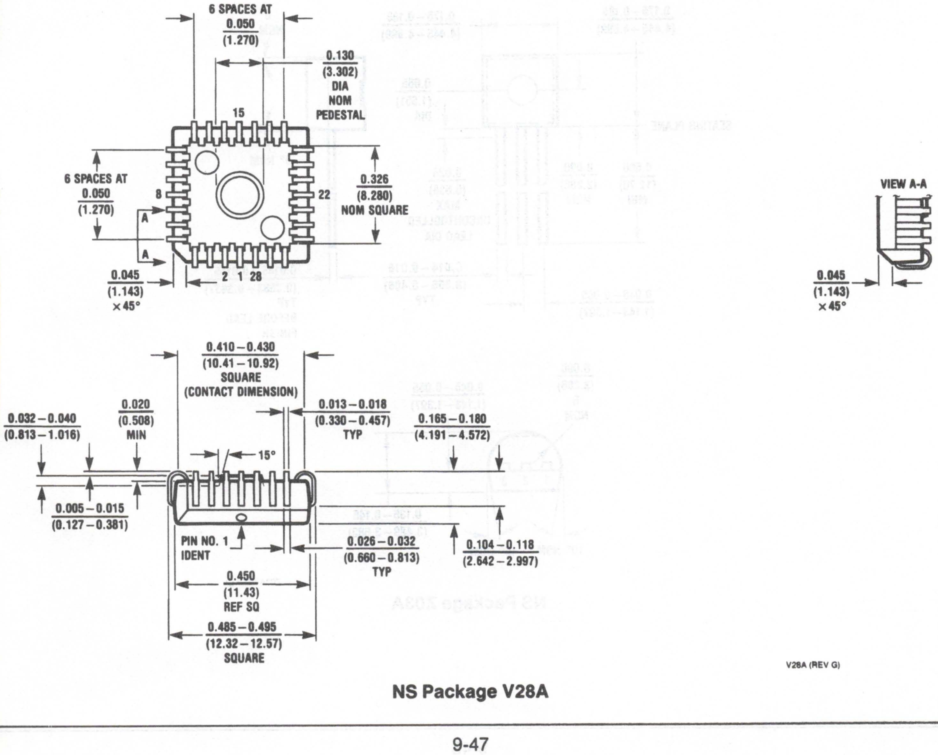
NS Package N28B


2.043–2.070 (51.89–52.58)
40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
24
23
22
21
0.062 (1.575) RAD
PIN NO. 1 IDENT
0.550 ±0.005 (13.970 ±0.127)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
0.580 (14.73) MIN
0.030 (0.762) MAX
0.600–0.620 (15.240–15.748)
95°±5°
0.625 +0.025 −0.015 (15.875 +0.635 −0.381)
0.009–0.015 (0.229–0.381)
0.075 ±0.015 (1.905 ±0.381)
0.050 (1.270) TYP
0.125–0.165 (3.175–4.191)
0.145–0.210 (3.683–5.334)
86°94° TYP
0.020 (0.508) MIN
0.100 ±0.010 (2.540 ±0.254)
0.018 ±0.003 (0.457 ±0.076)
0.125–0.140 (3.175–3.556)
N40A (REV E)

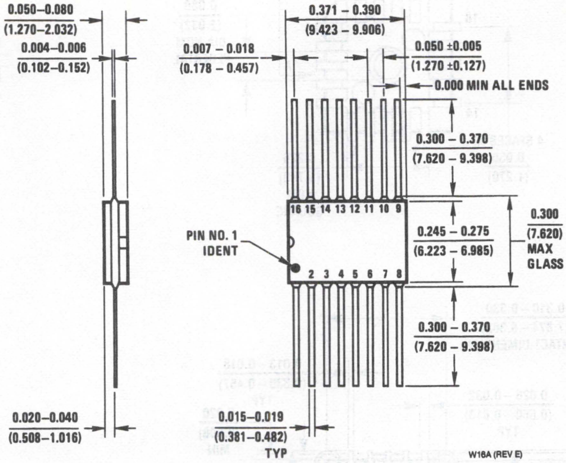
NS Package N40A


4 SPACES AT
0.050
(1.270)
19
20
1
2
3
18
4
8
14
13
9
A
A
0.080
(2.032)
DIA NOM
PEDESTAL
4 SPACES AT
0.050
(1.270)
0.226
(5.740)
NOM
SQUARE
0.045
(1.143)
×45°
15°
VIEW A-A
0.310 – 0.330
(7.874 – 8.382)
(CONTACT DIMENSION)
0.013 – 0.018
(0.330 – 0.457)
TYP
0.026 – 0.032
(0.660 – 0.813)
TYP
0.020
(0.508)
MIN
0.005 – 0.015
(0.127 – 0.381)
0.032 – 0.040
(0.813 – 1.016)
0.104 – 0.118
(2.642 – 2.997)
0.350
(8.890)
REF SQ
0.165 – 0.180
(4.191 – 4.572)
PIN NO.1
IDENT
0.385 – 0.395
(9.779 – 10.03)
SQUARE
V20A (REV J)

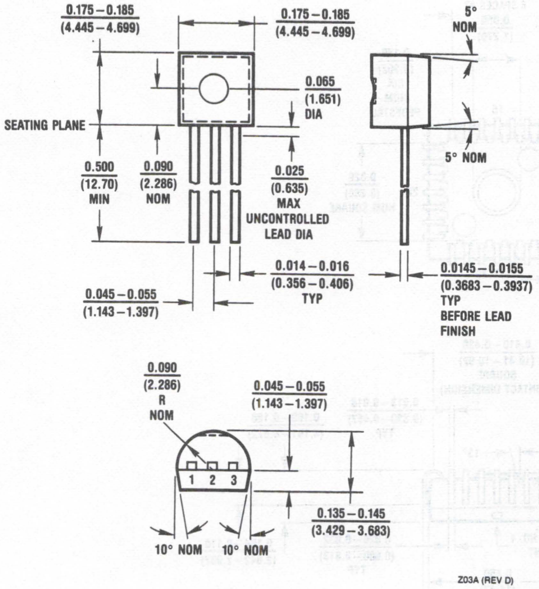
NS Package V20A


6 SPACES AT
0.050
(1.270)
0.130
(3.302)
DIA
NOM
PEDESTAL
15
6 SPACES AT
0.050
(1.270)
8
22
A
A
0.326
(8.280)
NOM SQUARE
0.045
(1.143)
×45°
2
1
28
VIEW A-A
0.045
(1.143)
×45°
0.410 – 0.430
(10.41 – 10.92)
SQUARE
(CONTACT DIMENSION)
0.032 – 0.040
(0.813 – 1.016)
0.020
(0.508)
MIN
0.013 – 0.018
(0.330 – 0.457)
TYP
0.165 – 0.180
(4.191 – 4.572)
15°
0.005 – 0.015
(0.127 – 0.381)
PIN NO. 1
IDENT
0.026 – 0.032
(0.660 – 0.813)
TYP
0.104 – 0.118
(2.642 – 2.997)
0.450
(11.43)
REF SQ
0.485 – 0.495
(12.32 – 12.57)
SQUARE
V28A (REV G)

NS Package V28A


0.050–0.080
(1.270–2.032)
0.004–0.006
(0.102–0.152)
0.007 – 0.018
(0.178 – 0.457)
0.371 – 0.390
(9.423 – 9.906)
0.050 ±0.005
(1.270 ±0.127)
0.000 MIN ALL ENDS
0.300 – 0.370
(7.620 – 9.398)
16 15 14 13 12 11 10 9
PIN NO. 1
IDENT
1 2 3 4 5 6 7 8
0.245 – 0.275
(6.223 – 6.985)
0.300
(7.620)
MAX
GLASS
0.300 – 0.370
(7.620 – 9.398)
0.020–0.040
(0.508–1.016)
0.015–0.019
(0.381–0.482)
TYP
W16A (REV E)

NS Package W16A


0.175 – 0.185
(4.445 – 4.699)
0.175 – 0.185
(4.445 – 4.699)
5°
NOM
0.065
(1.651)
DIA
SEATING PLANE
5° NOM
0.500
(12.70)
MIN
0.090
(2.286)
NOM
0.025
(0.635)
MAX
UNCONTROLLED
LEAD DIA
0.014 – 0.016
(0.356 – 0.406)
TYP
0.0145 – 0.0155
(0.3683 – 0.3937)
TYP
BEFORE LEAD
FINISH
0.045 – 0.055
(1.143 – 1.397)
0.090
(2.286)
R
NOM
0.045 – 0.055
(1.143 – 1.397)
1 2 3
0.135 – 0.145
(3.429 – 3.683)
10° NOM
10° NOM
Z03A (REV D)

NS Package Z03A

NOTES

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